REALTEK

RTL8812BRH-VN-CG

Single-Chip 802.11ac/a/n 2T2R WLAN
With PCI Express Interface

DATASHEET
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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information. Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface.
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
0.1	2017/07/21	Preliminary release.

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1. General Description

The Realtek RTL8812BRH-VN-CG is a highly integrated single-chip that support 2-stream 802.11ac solutions with Wireless LAN (WLAN) PCI Express network interface. It combines a WLAN MAC, a 2T2R capable WLAN baseband, and RF in a single chip.

The RTL8812BRH-VN-CG baseband implements Orthogonal Frequency Division Multiplexing (OFDM) with two transmit and two receive paths (2T2R). Features include two spatial stream transmissions, short Guard Interval (GI) of 400ns, spatial spreading, and support for variant channel bandwidth. Moreover, RTL8812BRH-VN-CG provides one spatial stream space-time block code (STBC), Transmit Beamforming (TxBF) and Low Density Parity Check (LDPC) to extend the range of transmission. At the receiver, extended range and good minimum sensitivity is achieved by having receiver diversity up to 2 antennas. As the recipient, the RTL8812BRH-VN-CG also supports explicit sounding packet feedback that helps senders with beamforming capability.

For legacy compatibility, OFDM baseband processing is included to support all IEEE 802.11a, 802.11n and 802.11ac data rates. The high speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation of the individual subcarriers, and rate compatible coding rate of 1/2, 2/3, 3/4, and 5/6, provide up to 866.7Mbps for IEEE 802.11ac MIMO OFDM.

The RTL8812BRH-VN-CG builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams. For better detection quality, receive diversity with Maximal-Ratio-Combine (MRC) applying up to two receive paths, and Maximum-Likelihood Detection (MLD) are implemented.

Receive vector diversity for multi-stream application is implemented for efficient utilization of the MIMO channel. Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end.

The RTL8812BRH-VN-CG supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control functions to obtain better performance in the analog portions of the transceiver.

The RTL8812BRH-VN-CG MAC supports 802.11e for multimedia applications, 802.11i and WAPI (Wireless Authentication Privacy Infrastructure) for security, and 802.11n/802.11ac for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, U-APSD, and MIMO power saving reduce the power wasted during idle time, and compensate for the extra power required to transmit MIMO OFDM. The RTL8812BRH-VN-CG provides simple legacy, 20MHz/40MHz/80MHz co-existence mechanisms to ensure backward and network compatibility.

2. Features

General

- 88-pin QFN

- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11a/n/ac compatible WLAN

- Complete 802.11n MIMO solution for 5GHz band

- Maximum PHY data rate up to 173.3 Mbps using 20MHz bandwidth, 400Mbps using 40MHz bandwidth, and 866.7Mbps using 80MHz bandwidth.

- Backward compatible with 802.11a devices while operating at 802.11n data rates

- Backward compatible with 802.11a/n devices while operating at 802.11ac data rates.

Host Interface

- Complies with PCI Express Base Specification Revision 1.1

- PCIe LTR/L1.Off state supported

Standards Supported

- IEEE 802.11a/n/ac compatible WLAN

- IEEE 802.11e QoS Enhancement (WMM)

- IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services

- IEEE 802.11h DFS, TPC, Spectrum Measurement

- IEEE 802.11k Radio Resource Measurement

- WAPI (Wireless Authentication Privacy Infrastructure) certified.

- Cisco Compatible Extensions (CCX) for WLAN devices

MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)

- Low latency immediate Block Acknowledgement (BA)

- Long NAV for media reservation with CF-End for NAV release

- PHY-level spoofing to enhance legacy compatibility

- Channel management and co-existence

- Multiple BSSID feature allows the RTL8812BRH to assume multiple MAC identities when used as a wireless bridge

- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth

- WiFi Direct supports wireless peer to peer applications.

Other Features

- Supports Wake-On-WLAN via Magic Packet and Wake-up frame

- Transmit Beamforming

Peripheral Interfaces

- Up to 15 General Purpose Input/Output pins

- Three configurable LED pins (mux with GPIO pins)

PHY Features

- IEEE 802.11ac MIMO OFDM

- IEEE 802.11n MIMO OFDM

- Two Transmit and Two Receive paths

- 5MHz / 10MHz / 20MHz / 40MHz / 80MHz bandwidth transmission

- Support 5GHz band channels

- Short Guard Interval (400ns)

- Sounding packet.

- OFDM with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6

- Maximum data rate 300Mbps in 802.11n and 866.7bps in 802.11ac.

- CCA on secondary through RTS/CTS handshake.

- Support TCP/UDP/IP checksum offload

- Generates 40MHz clock for peripheral chip.

- Single external power source 3.3V only

- OFDM receive diversity with MRC using up to 2 receive paths. Switch diversity used for DSSS/CCK

- Support STBC

- Support LDPC

- Hardware antenna diversity

- Maximum-Likelihood Detection (MLD)

- Fast receiver Automatic Gain Control (AGC)

- On-chip ADC and DAC

- Build-in both 5GHz PA

- Build-in both 5GHz LNA

Peripheral Interfaces

- General Purpose Input/Output (8 pins)

- 4-wire EEPROM control interface (93C46)

- Three configurable LED pins

- Flexible crystal frequency selection(52, 48, 40, 38.4, 27, 26, 25, 24, 20, 19.2, 17.664, 16, 14.318, 13 and 12MHz)

- Support crystal or external clock input

3. Application Diagrams

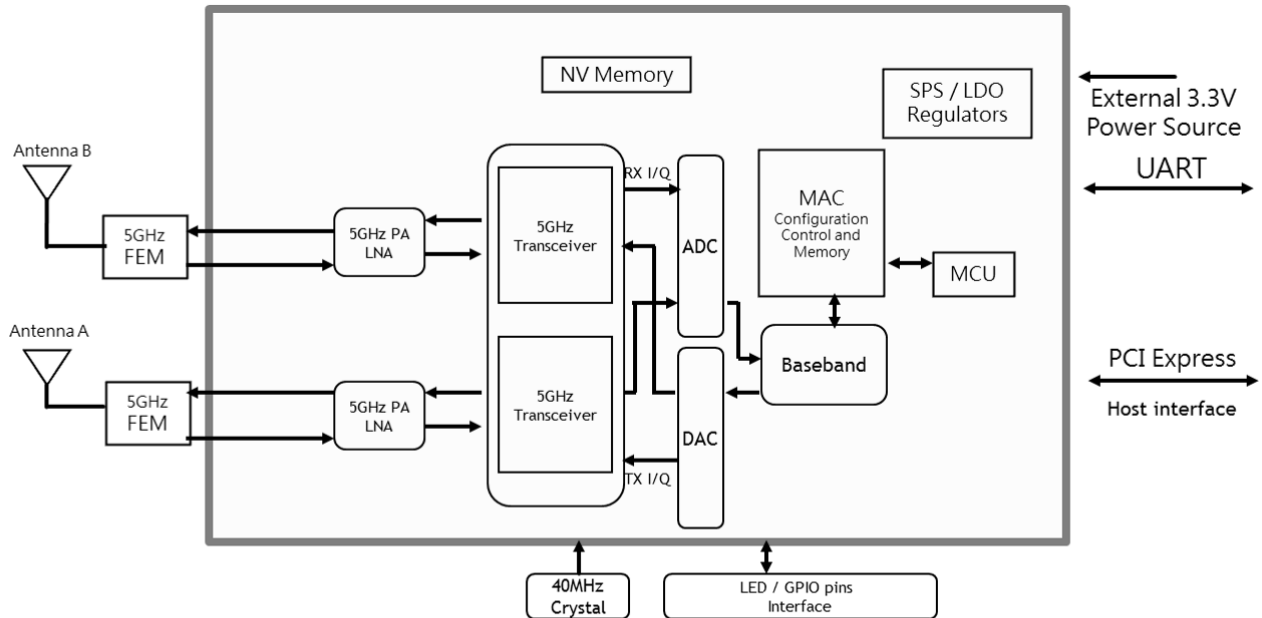## 3.1. 5GHz-Band 2x2 RF Application

Figure 1. 5GHz-Band 2x2 Solution(11ac 2x2 MAC/BB/RF + PA) Solution --- RTL8812BRH-VN-CG

4. Pin Assignments
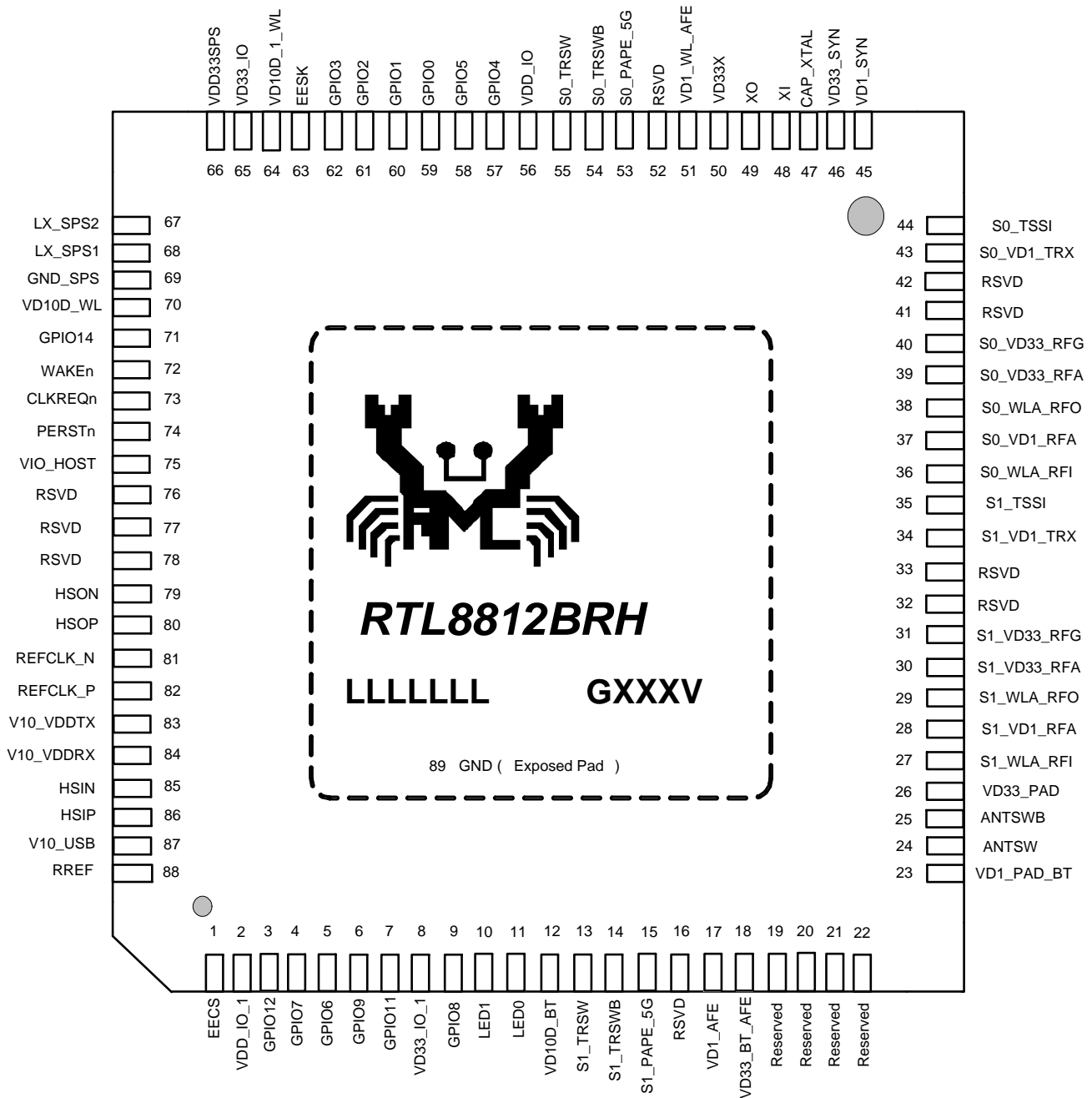
Figure 2. Pin Assignments

4.1. Package Identification & Mark Information

Green package is indicated by a 'G' in the location marked 'G' in Figure 2.

The version is shown in the location marked 'V' in Figure 2.

Body (mm^2)	LOGO FONT		Mark Example						備註 Remark		
	LOGO SIZE	3.11 x 2.53 mm^2									
10x10			RTL8812BRH LLLLLLL GXXXN						1. LOGO 靠左對齊 LOGO aligns to left 2. Pin1 位置在正印的左下 Pin1 mark orientation：bottom left		

Line	Item	FONT	a (mm)	b (mm)	c (mm)	d (mm)	e (mm)	對齊 Alignment
1	Part no.	Realtek standard	1.0	0.40	0.13	0.50	-	Left
2	Lot no.	Realtek standard	1.0	0.40	0.13	0.50	-	Left
	Date Code (BDC/ADC)	Realtek standard	1.0	0.40	0.13	0.50	-	Left 並與 Lot no.間距 1 個字元 Left and space 1 character width with Lot no.

5. Pin Descriptions

The following signal type codes are used in the tables:

I: Input   O: Output

T/S: Tri-State bi-directional input/output pin   S/T/S: Sustained Tri-State

O/D: Open Drain   P: Power pin

N/A: No Bonding pin

5.1. Power On Trap Pin

Table 1.   Power-On Trap Pins

Symbol	Type	Pin No	Description
TEST_MODE_SEL	I	57	Shared with GPIO4 0: Normal operation mode 1: Test/debug mode
SPS_LDO_SEL	I	58	Shared with GPIO5 0: Internal switching regulator select 1: Internal LDO select

Symbol	Type	Pin No	Description
EEPROM_SEL	I	63	Shared with EESK pin 0: Internal NV memory select 1: External EEPROM select

5.2. PCI Express Transceiver Interface

Table 2.   PCI Express Transceiver Interface

Symbol	Type	Pin No	Description
HSIN/HSIP	I	85,86	PCI Express Receive Differential Pair
HSON/HSOP	O	79,80	PCI Express Transmit Differential Pair
REFCLK_N/REFCLK_P	I	81,82	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm
CLKREQ#	I/O/D	73	Reference Clock Request Signal. Also used by L1 PM substates. This signal is used by the RTL8812BRH-VN-CG to request for the PCI Express reference clock.
WAKE#	O/D	72	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks.
PERST#	I	74	PCI Express Reset Signal: active low. When the PERST# is asserted at power-on state, the RTL8812BRH-VN-CG returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERST#.

5.3. EEPROM Interface

Table 3.   EEPROM Interface

Symbol	Type	Pin No	Description
EECS	O	1	External EEPROM Chip Select
EESK	O	63	External EEPROM Clock

5.4. RF Interface

Table 4.   RF Interface

Symbol	Type	Pin No	Description
S1_WLA_RFO	I/O	29	WLAN 5G RF I/O (w/o external FEM) and OUTPUT (w/i external FEM)
S1_WLA_RFI	I	27	WLAN 5G RF INPUT (w/i external FEM)
S0_WLA_RFO	I/O	38	WLAN 5G RF I/O (w/o external FEM) and OUTPUT (w/i external FEM)
S0_WLA_RFI	I	36	WLAN 5G RF INPUT (w/i external FEM)
S1_TSSI	I	35	External PA TSSI INPUT
S0_TSSI	I	44	External PA TSSI INPUT
ANTSW	O	24	External ANTSW CONTROL

Symbol	Type	Pin No	Description
ANTSWB	O	25	External ANTSW CONTROL
S1_PAPE_5G	O	15	External 5G PAPE CONTROL
S1_TRSW	O	13	External TRSW CONTROL
S1_TRSWB	O	14	External TRSW CONTROL
S0_PAPE_5G	O	53	External 5G PAPE CONTROL
S0_TRSW	O	55	External TRSW CONTROL
S0_TRSWB	O	54	External TRSW CONTROL
RSVD		16,32,33, 41,42,52	Reserved.

5.5. LED Interface

Table 5. LED Interface

Symbol	Type	Pin No	Description
LED0	O	11	LED Pin (Active Low)
LED1	O	10	LED Pin (Active Low)
LED2	O	9	LED Pin (Active Low), shared with GPIO8

5.6. Power Management Handshake Interface

Table 6. Power Management Handshake Interface

Symbol	Type	Pin No	Description
WL_DIS#	I	6	This pin can be defined as the WLAN Radio-off function with host interface remaining connected. When this pin is pulled low, WLAN function will be Radio-off. When this function is not required, external pull high is required. Shared with GPIO9.

5.7. Clock and Other Pins

Table 7. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	48	40MHz OSC Input 40MHz Crystal reference clock input
XO	O	49	40MHz Crystal reference clock output
SUS_CLK	I	1	Shared with EECS. External 32K or RTC clock input.
GPIO0	IO	59	General Purpose Input/Output Pin
GPIO1	IO	60	General Purpose Input/Output Pin
GPIO2	IO	61	General Purpose Input/Output Pin
GPIO3	IO	62	General Purpose Input/Output Pin
GPIO4	IO	57	General Purpose Input/Output Pin
GPIO5	IO	58	General Purpose Input/Output Pin

Symbol	Type	Pin No	Description
GPIO6	IO	5	General Purpose Input/Output Pin
GPIO7	IO	4	General Purpose Input/Output Pin
GPIO8	IO	9	General Purpose Input/Output Pin
GPIO9	IO	6	General Purpose Input/Output Pin
GPIO11	IO	7	General Purpose Input/Output Pin
GPIO12	IO	3	General Purpose Input/Output Pin
GPIO14	IO	71	General Purpose Input/Output Pin
RSVD	IO	76,77,78	Reserved

5.8. Power Pins

Table 8.   Power Pins

Symbol	Type	Pin No	Description
LX_SPS	P	67,68	Switching Regulator Output
VD33_SPS	P	66	Switching Regulator Input Or Linear Regulator input from 3.3V to 1.5V
VD33_IO	P	65	VDD3.3V for digital IO
VD33_IO_1	P	8	VDD3.3V for digital IO
VDD_IO	P	56	VDD for GPIO0 to GPIO5 and EESK
VDD_IO_1	P	2	VDD for GPIO6,GPIO7,GPIO9,GPIO11,GPIO12 and EECS.
VIO_HOST	P	75	VIO_HOST
VD10D_WL	P	70	1.05V for WLAN digital power
VD10D_1_WL	P	64	1.05V for WLAN digital power
VD10D_BT	P	12	1.05V for BT/WLAN power
GND_SPS	P	69	Switching Regulator Ground
RREF	P	88	Precision Resistor for Bandgap
V10_VDDTX/ V10_VDDRX	P/I	83,84	1.05V for analog circuits in interface
V10_USB	P	87	1.05V for USB
VD1_PAD_BT	P	23	VDD 1.05V for BT/WLAN RF
VD33_BT_AFE	P	18	VDD 3.3V for BT/WLAN AFE
VD1_ AFE	P	17	VDD 1.05V for WLAN AFE
VD33_PAD	P	26	VDD 3.3V for PAD
S1_VD1_RFA	P	28	VDD 1.05V for WLAN S1 5G RX
S1_VD33_RFA	P	30	VDD3.3V for WLAN S1 5G TX IPA
S1_VD33_RFG	P	31	VDD3.3V for WLAN S1 TX
S1_VD1_TRX	P	34	VDD 1.05V for WLAN S1
S0_VD1_RFA	P	37	VDD 1.05V for WLAN S0 5G RX
S0_VD33_RFA	P	39	VDD3.3V for WLAN S0 5G TX IPA
S0_VD33_RFG	P	40	VDD3.3V for WLAN S0 TX
S0_VD1_TRX	P	43	VDD 1.05V for WLS0
VD1_WL_SYN	P	45	VDD 1.05V for WLAN synthesizer
VD33_WL_SYN	P	46	VDD 3.3V for WLAN synthesizer
VD1_WL_AFE	P	51	VDD 1.05V for WLAN AFE

Symbol	Type	Pin No	Description
VD33X	P	50	VDD 3.3V for Crystal
CAP_XTAL	P	47	LDO output . External CAP 1uF is needed.
Reserved		19,20,21,22	Reserved

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 9. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. DC Characteristics

6.2.1. Power Supply Characteristics

Table 10. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VD33	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
VD10	1.05V Core Supply Voltage	1.04	1.09	1.14	V

6.2.2. Digital IO Pin DC Characteristics

Table 11. 3.3V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	--	0	0.9	V
V_{OH}	Output high voltage	2.97	--	3.3	V
V_{OL}	Output low voltage	0	--	0.33	V

PS. 3.3V and 1.05V ripple < 100mV

7. Interface Timing Specification

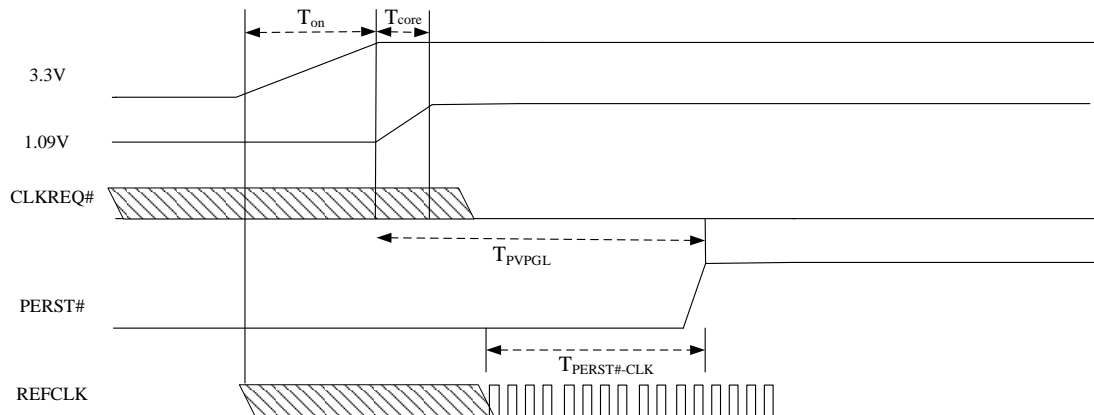## 7.1. PCIe Bus during Power On Sequence

Figure 3. RTL8812BRH-VN-CG PCIe Bus Power On Sequence
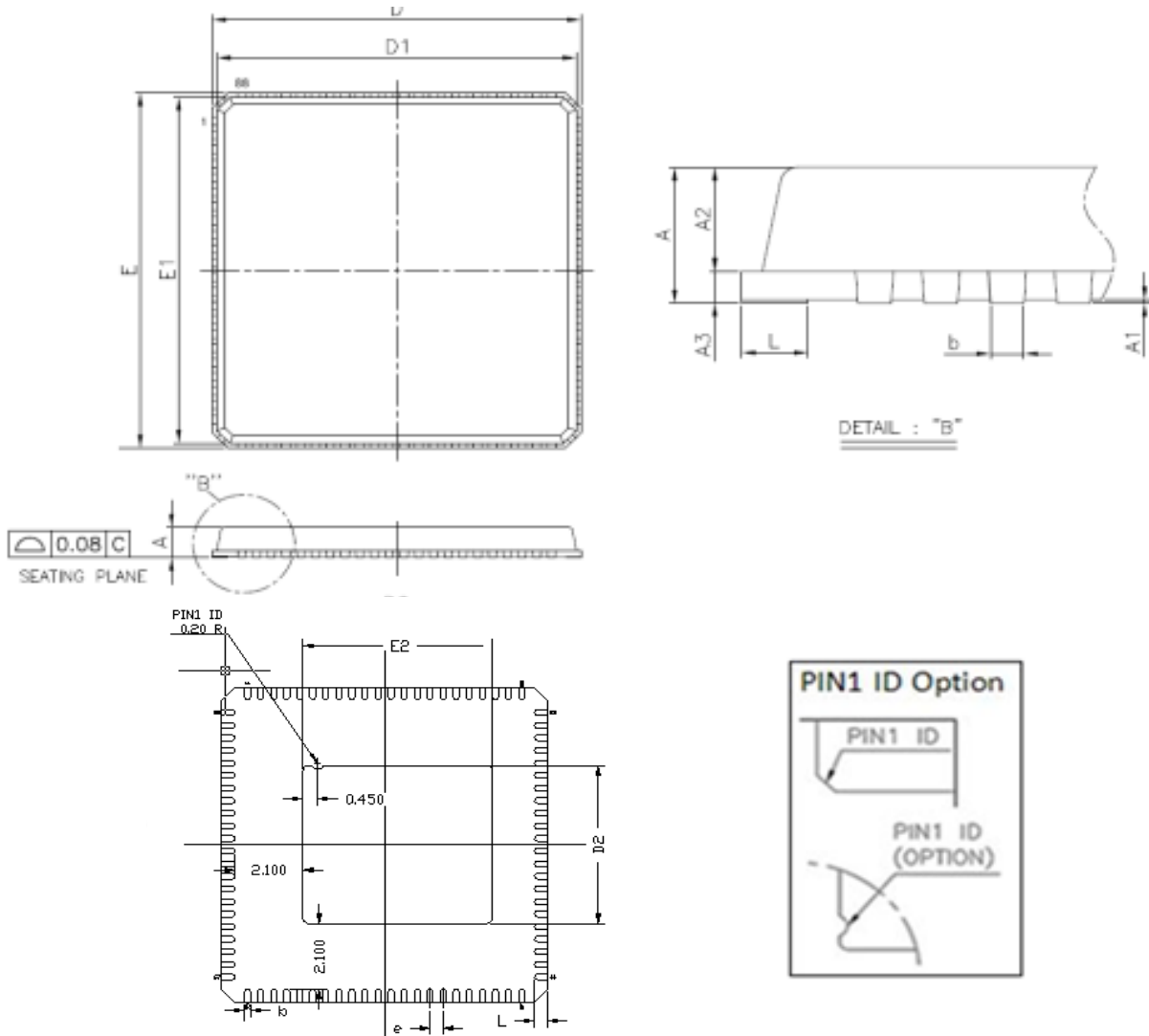
T_{on}: The main power ramp up duration

T_{PVPGL}: Power valid to PERST# input inactive

$T_{PERST\#-CLK}$: Reference clock stable before PERST# inactive

Table 12. The typical timing range

Symbol	Unit	Min	Typical	Max
T_{on}	ms	0.5	1.5	5
T_{core}	ms	0.9	1	1.1
T_{PVPGL}	ms	Implementation specific;recommended 50ms		--
$T_{PERST\#-CLK}$	us	100		--
T_{attach}	ms	2	7	15
$T_{k\text{-}state}$	ms	50	250	--

8. Mechanical Dimensions

8.1. Mechanical Dimensions Notes

Table 13. Dimensions Information

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.203 REF			0.008 REF		
b	0.13	0.18	0.23	0.005	0.007	0.009
D/E	10 BSC			0.394BSC		
D_2	4.9	5.0	5.1	0.193	0.197	0.201
E_2	5.7	5.8	5.9	0.224	0.228	0.232
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：
1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

9. Ordering Information

Table 14. Ordering Information

Part Number	Package	Status
RTL8812BRH-VN-CG	QFN-88, 'Green' Package	Mass Production