Click here for production status of specific part numbers.

MAX32665–MAX32668

Low-Power Arm Cortex-M4 with FPU-Based Microcontroller with Bluetooth 5 for Wearables

General Description

DARWIN is a new breed of low-power microcontrollers built to thrive in the rapidly evolving Internet of Things (IoT). They are smart, with the biggest memories in their class and a massively scalable memory architecture. They run forever, thanks to wearable-grade power technology. They are durable enough to withstand the most advanced cyberattacks. DARWIN microcontrollers are designed to run any application imaginable—in places where you would not dream of sending other microcontrollers.

Generation UB microcontrollers are designed to handle the increasingly complex applications demanded by today's advanced battery-powered devices and wirelessly connected devices, while providing robust hardware security and Bluetooth® 5 Low Energy (BLE) radio connectivity.

The MAX32665–MAX32668 UB class microcontrollers are advanced systems-on-chips featuring an Arm® Cortex®-M4 with FPU CPU for efficient computation of complex functions and algorithms with integrated power management. They also include the newest generation Bluetooth 5 Low Energy radio with support for long range (4x) and high throughput (2Mbps) and Maxim's best-in-class hardware security suite trust protection unit (TPU). The devices offer large on-board memory with 1MB flash and up to 560KB SRAM that can be configured as 448KB SRAM with error correction coding (ECC). Split flash banks of 512KB each support seamless over the air upgrades, adding an additional degree of reliability. Memory scalability of data (SRAM) and code (flash) space is supported by two SPI execute-in-place (SPIX) interfaces.

Multiple high-speed interfaces are supported including HS-USB, secure digital interface (SD, SDIO, MMC, SDHC, and microSD™), SPI, UART, and I²C serial interfaces, and an audio subsystem supporting PDM, PCM, I²S, and TDM interfaces. An 8-input, 10-bit ADC is available to monitor analog inputs from external sensors and meters. The devices are available in 109-bump WLP (0.35mm pitch) and 121-bump CTBGA (0.65mm pitch) packages.

Applications

- Connected Home
- Industrial Sensors
- Payment/Fitness/Medical Wearables
- Telemedicine
- Gaming Devices
- Hearables

Benefits and Features

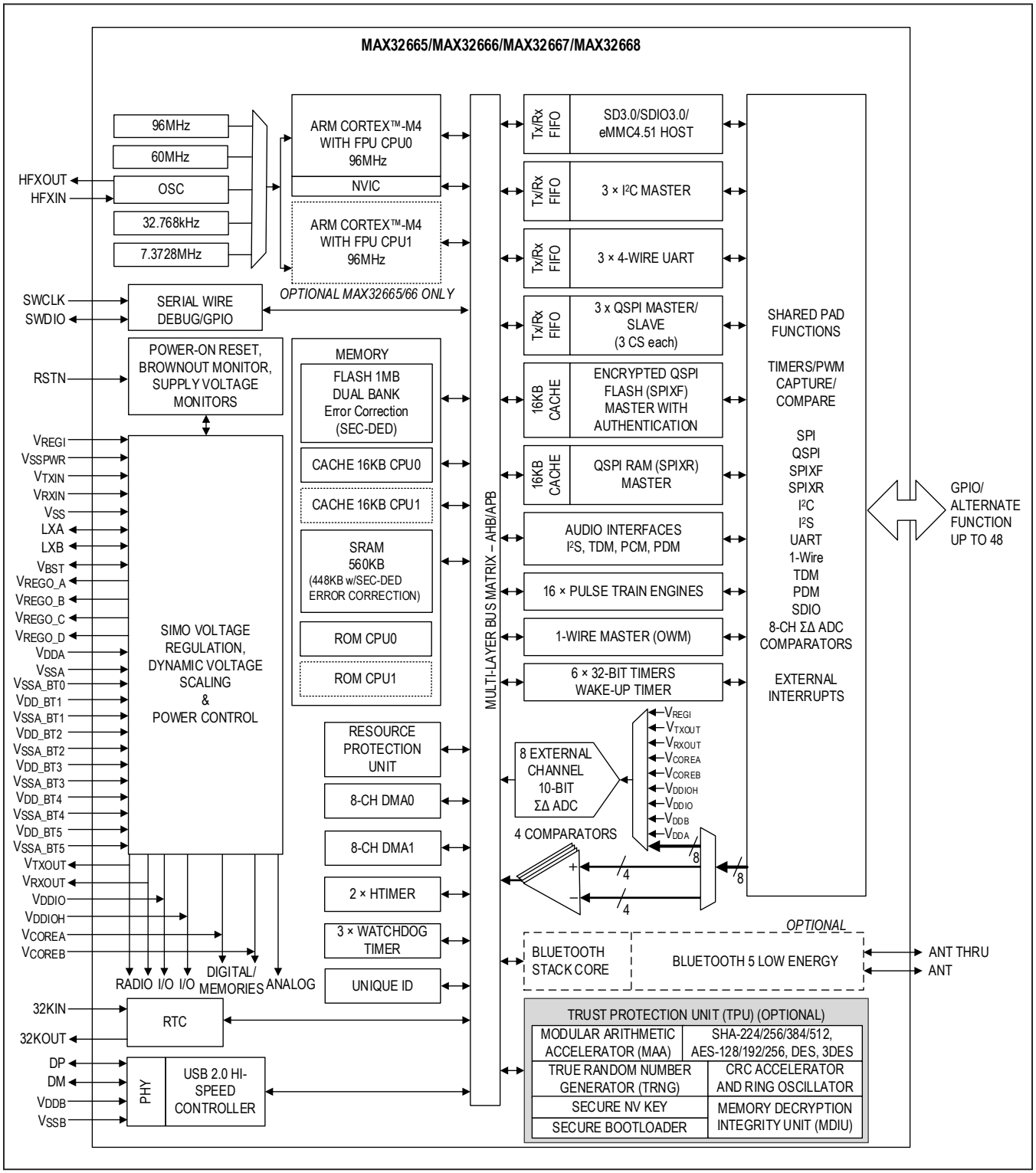
- High-Efficiency Microcontroller and Audio DSP for Wearable and Hearable Devices
  - Arm Cortex-M4 with FPU Up to 96MHz
  - Optional Second Arm Cortex-M4 with FPU Optimized for Data Processing
  - Low-Power 7.3728MHz System Clock Option
  - 1MB Flash, Organized into Dual Banks 2 x 512KB
  - 560KB (448KB ECC) SRAM; 3 x 16KB Cache
  - Optional Error Correction Code (ECC-SEC-DED) for Cache, SRAM, and Internal Flash
- Bluetooth 5 Low Energy Radio
  - Up to 2Mbps Data Throughput
  - Long Range (125kbps and 500kbps)
  - Rx Sensitivity: -95dbm; Tx Power: +9.5dbm
  - Single-Ended Antenna Connection
- Power Management Maximizes Operating Time for Battery Applications
  - Integrated SIMO SMPS for Coin-Cell Operation
  - Dynamic Voltage Scaling Minimizes Active Core Power Consumption
  - 27.3µA/MHz at 3.3V Executing from Cache
  - 12.3µA at 3.3V Retention Current for 32KB SRAM
  - Selectable SRAM Retention in Low Power Modes with RTC Enabled
- Multiple Peripherals for System Control
  - Three QSPI Master/Slave with Three Chip Selects Each, Three 4-Wire UARTs, Three I²C Master/Slave
  - QSPI (SPIXF) with Real-Time Flash Decryption
  - QSPI (SPIXR) RAM Interface Provides SRAM Expansion
  - 8-Input, 10-Bit Delta-Sigma ADC 7.8ksps
  - USB 2.0 HS Engine with Internal Transceiver
  - PDM Interface Supports Two Digital Microphones
  - I²S with TDM, Six 32-Bit Timers, Two High-Speed Timers, 1-Wire Master, Sixteen Pulse Train (PWM) Engines
  - Secure Digital Interface Supports SD3.0/SDIO3.0/eMMC4.51
- Secure Valuable IP/Data with Hardware Security
  - Trust Protection Unit (TPU) with MAA Supports Fast ECDSA and Modular Arithmetic
  - AES-128, -192, -256, DES, 3DES, Hardware Accelerator
  - TRNG Seed Generator, SHA-2 Accelerator
  - Secure Bootloader

Ordering Information *appears at end of data sheet.*

19-100411; Rev 0; 10/18

maxim integrated™

Simplified Block Diagram



Absolute Maximum Ratings

V_{COREA} ..... -0.3V to +1.21V
V_{COREB} ..... -0.3V to +1.21V
V_{DDA} ..... -0.3V to +1.98V
V_{DDIO} ..... -0.3V to +1.98V
V_{DDIOH} ..... -0.3V to +3.6V
V_{REGI} ..... -0.3V to +3.6V
V_{TXIN} ..... -0.3V to +1.9V
V_{RXIN} ..... -0.3V to +1.9V
$V_{DDA\_BT[1:5]}$ ..... -0.3V to +1V
RSTN, GPIO (V_{DDIO}) ..... -0.3V to V_{DDIO} + 0.5V
GPIO (V_{DDIOH}) ..... -0.3V to V_{DDIOH} + 0.5V
32KIN, 32KOUT ..... -0.3V to V_{DDA} + 0.2V
HFXIN, HFXOUT ..... -0.3V to V_{DDA} + 0.2V
AIN[7:0] ..... -0.3V to +3.6V
V_{DDB} ..... -0.3V to +3.6V
DM, DP ..... -0.3V to +3.6V
V_{DDIO} Combined Pins (sink) 100mA
V_{DDIOH} Combined Pins (sink) 100mA
V_{SSA} 100mA
V_{SS} 100mA
V_{SSPWR} 100mA
$V_{SSA\_BT[1:5]}$ 100mA
Output Current (sink) by Any GPIO Pin 25mA
Output Current (source) by Any GPIO Pin ..... -25mA
Continuous Package Power Dissipation
CTBGA (multilayer board) T_A = +70°C
(derate 31.0mW/°C above +70°C) 1692mW
Operating Temperature Range ..... -40°C to +105°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

109 WLP

Package Code	W1093A4+1
Outline Number	**21-100301**
Land Pattern Number	Refer to **Application Note 1891**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	38.05°C/W
Junction to Case (θ_{JC})	N/A

121 CTBGA

Package Code	X12188+6C
Outline Number	**21-0680**
Land Pattern Number	**90-0451**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	32.5°C/W
Junction to Case (θ_{JC})	8.8°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Core Input Supply Voltage A	V_{COREA}			V_{COREA} V_{RST}	1.1	1.21	V
Core Input Supply Voltage B	V_{COREB}			V_{COREB} V_{RST}	1.1	1.21	V
Input Supply Voltage, Analog	V_{DDA}			1.71	1.8	1.89	V
Input Supply Voltage, Battery	V_{REGI}			2.0	2.7	3.6	V
Input Supply Voltage, GPIO	V_{DDIO}			1.71	1.8	1.89	V
Input Supply Voltage, GPIO (High)	V_{DDIOH}			1.71	1.8	3.6	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{COREA}		0.78	0.832		V
		Monitors V_{COREB}		0.78	0.832		
		Monitors V_{DDA}		1.6	1.67		
		Monitors V_{DDB}		2.85	2.95		
		Monitors V_{DDIO}		1.6	1.67		
		Monitors V_{DDIOH}		1.6	1.67		
		Monitors V_{REGI}		1.95		2.15	
Power-On Reset Voltage	V_{POR}	Monitors V_{COREA}			0.63		V
V_{REGI} Current, Active Mode	I_{REGI_ACT}	Total current into V_{REGI} pins, f_{SYS_CLK} = 96MHz, V_{REGI} = 3.3V, CPU0 in Active mode, executing While(1) from cache, inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}, outputs source/sink 0mA			3.3		mA
V_{REGI} Current, Sleep Mode	I_{REGI_SLP}	Total current into V_{REGI} pins, f_{SYS_CLK} = 96MHz, V_{REGI} = 3.3V, CPU0 in Sleep mode, inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}, outputs source/sink 0mA			2.1		mA
V_{REGI} Current, Backup Mode	I_{REGI_BK}	Total current into V_{REGI} pins, inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}, outputs source/sink 0mA	RTC enabled, full memory retention		14.6		µA
			RTC enabled, no memory retention		7.8		
			RTC disabled, no memory retention		7.2		
			RTC disabled, full memory retention		14.4		
			RTC disabled, 32KB ECC memory retention		12.3		
			RTC disabled, 64KB ECC memory retention		12.3		

Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REGI} Fixed Current, DeepSleep Mode	I_{REGI_FDSL}	Standby state with full retention		23.2		µA
V_{REGO_X} Output Current	$V_{REGO\_X\_IOUT}$	Output current for each of the V_{REGO_X} outputs		5	50	mA
V_{REGO_X} Output Current Combined	$V_{REGO\_X\_IOUT\_TOT}$	All four V_{REGO_X} outputs combined		15	100	mA
V_{REGO_X} Output Voltage Range	$V_{REGO\_X\_RANGE}$	$V_{REGI} \geq V_{REGO\_X}$ + 200mV	0.5	1.0	1.85	V
V_{REGO_X} Efficiency	$V_{REGO\_X\_EFF}$	V_{REGI} = 2.7V, V_{REGO_X} = 1.1 V, load = 30mA		90		%
CLOCKS						
System Clock Frequency	f_{SYS_CLK}		8		96,000	kHz
System Clock Period	t_{SYS_CLK}			$1/f_{SYS\_CLK}$		ns
High-Speed Oscillator Frequency	f_{HSCLK}	Factory default, user adjustable 50MHz–96MHz	92.5	96	99.6	MHz
Low-Power Oscillator Frequency	f_{LPCLK}			60		MHz
RF Oscillator Frequency	f_{RFCLK}	32MHz crystal, C_L = 12pF, ESR ≤ 50Ω, C_0 ≤ 7pF, temperature stability ±20ppm, initial tolerance ±20ppm		32		MHz
HFXIN, HFXOUT Input Capacitance	C_{HFX_PIN}			6		pF
7MHz Oscillator Frequency	f_{7MCLK}			7.3728		MHz
RTC Input Frequency	f_{32KIN}	32kHz watch crystal, C_L = 6pF, ESR < 90kΩ, C_0 ≤ 2pF		32.768		kHz
RTC Operating Current	I_{RTC_BDSLP}	Backup or DeepSleep mode		0.39		µA
RTC Power-Up Time	t_{RTC_ON}			250		ms
Nano-Ring Oscillator Frequency	f_{NANO}			8		kHz
GENERAL-PURPOSE I/O						
Input Low Voltage for All GPIO	V_{IL_VDDIO}	V_{DDIO} selected as I/O supply			0.3 × V_{DDIO}	V
	V_{IL_VDDIOH}	V_{DDIOH} selected as I/O supply			0.3 × V_{DDIOH}	
Input Low Voltage for RSTN	V_{IL_RSTN}			0.5 x V_{COREA}		V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage for All GPIO	V_{IH_VDDIO}	V_{DDIO} selected as I/O supply	0.7 × V_{DDIO}			V
	V_{IH_VDDIOH}	V_{DDIOH} selected as I/O supply	0.7 × V_{DDIOH}			
Input High Voltage for RSTN	V_{IH_RSTN}			0.5 x V_{COREA}		V
Output Low Voltage for All GPIO	V_{OL_VDDIO}	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = 1mA		0.2	0.4	V
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = 8mA		0.2	0.4	
	V_{OL_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = 1mA		0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = 8mA		0.2	0.4	
Combined I_{OL}, All GPIO	I_{OL_TOTAL}				48	mA
Output High Voltage for All GPIO	V_{OH_VDDIO}	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = -1mA	V_{DDIO} - 0.4			V
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = -2mA	V_{DDIO} - 0.4			
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = -4mA	V_{DDIO} - 0.4			
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = -8mA	V_{DDIO} - 0.4			
	V_{OH_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = -1mA	V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = -2mA	V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = -8mA	V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = -8mA	V_{DDIOH} - 0.4			

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Combined I_{OH}, All GPIO	I_{OH_TOTAL}					-48	mA
Input Hysteresis (Schmitt)	V_{IHYS}				300		mV
Input Leakage Current Low	I_{IL}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 0V, internal pullup disabled		-100		+100	nA
Input Leakage Current High	I_{IH}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 3.6V, internal pulldown disabled		-100		+100	nA
	I_{OFF}	V_{DDIO} = 0V, V_{DDIOH} = 0V, V_{DDIO} selected as I/O supply, V_{IN} < 1.89V		-1		+1	µA
	I_{IH3V}	V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, V_{IN} = 3.6V		-2		+2	
Input Pullup Resistor RSTN	R_{PU_R}	P1M = 1			25		kΩ
		P1M = 0			1		MΩ
Input Pullup/Pulldown Resistor for All GPIOs	R_{PU1}	Normal resistance			25		kΩ
	R_{PU2}	Highest resistance			1		MΩ
ADC (DELTA-SIGMA)							
Resolution					10		Bits
ADC Clock Rate	f_{ACLK}			0.1		8	MHz
ADC Clock Period	t_{ACLK}				$1/f_{ACLK}$		µs
Input Voltage Range	V_{AIN}	AIN[7:0], ADC_DIVSEL = [00], ADC_CH_SEL = [7:0]	REF_SEL = 0, INPUT_SCALE = 0	V_{SSA} + 0.05		V_{BG}	V
		AIN[7:0], ADC_DIVSEL = [01], ADC_CH_SEL = [7:0]	REF_SCALE = 0, INPUT_SCALE = 0	V_{SSA} + 0.05		2 x V_{BG}	
		AIN[7:0], ADC_DIVSEL = [10], ADC_CH_SEL = [7:0]	REF_SCALE = 0, INPUT_SCALE = 0, V_{DDIOH} selected as the I/O supply	V_{SSA} + 0.05		V_{DDIOH}	
		AIN[7:0], ADC_DIVSEL = [11], ADC_CH_SEL = [7:0]	REF_SEL = 0, INPUT_SCALE = 0, V_{DDIOH} selected as the I/O supply	V_{SSA} + 0.05		V_{DDIOH}	
Input Impedance	R_{AIN}				30		kΩ
Analog Input Capacitance	C_{AIN}	Fixed capacitance to V_{SSA}			1		pF
		Dynamically switched capacitance			250		fF
Integral Nonlinearity	INL	Measured at 25°C, insignificant temperature drift due to architecture				±2	LSb

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Nonlinearity	DNL	Measured at 25°C, insignificant temperature drift due to architecture			±1	LSb
Offset Error	V_{OS}			±1		LSb
ADC Active Current	I_{ADC}	ADC active, reference buffer enabled, input buffer disabled		210		µA
ADC Setup Time	t_{ADC_SU}	Any power-up of ADC clock or ADC bias to CpuAdcStart			10	µs
ADC Output Latency	t_{ADC}			1067		t_{ACLK}
ADC Sample Rate	f_{ADC}				7.8	ksps
ADC Input Leakage	I_{ADC_LEAK}	ADC inactive or channel not selected		0.16		nA
Full-Scale Voltage	V_{FS}	ADC code = 0x3FF		1.2		V
Bandgap Temperature Coefficient	V_{TEMPCO}	Box method		30		ppm
COMPARATORS						
Input Offset Voltage	V_{OFFSET}			±1		mV
Input Hysteresis	V_{HYST}	AINCOMPHYST[1:0] = 00		±23		mV
		AINCOMPHYST[1:0] = 01		±50		
		AINCOMPHYST[1:0] = 10		±2		
		AINCOMPHYST[1:0] = 11		±7		
Input Voltage Range	V_{IN_CMP}	Common-mode range	0.6		1.35	V
FLASH MEMORY						
Flash Erase Time	t_{M_ERASE}	Mass erase		20		ms
	t_{P_ERASE}	Page erase		20		
Flash Programming Time per Word	t_{PROG}			16		µs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +85°C	10			years
USB						
USB Supply Voltage	V_{DDB}		3.0	3.3	3.6	V
D+, D- Pin Capacitance	C_{IN_USB}	Pin to V_{SS}		8		pF
Driver Output Resistance	R_{DRV}	Steady state drive		44 ±10%		Ω

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB/FULL SPEED						
Single-Ended Input High Voltage (DP, DM)	V_{IH_USB}		2.1			V
Single-Ended Input Low Voltage (DP, DM)	V_{IL_USB}				0.5	V
Output High Voltage (DP, DM)	V_{OH_USB}	R_L = 1.5kΩ from DP and DM to V_{SS}, I_{OH} = -4mA	2.8		V_{DDB}	V
Output Low Voltage (DP, DM)	V_{OL_USB}	R_L = 1.5kΩ from DP to V_{DDB}, I_{OL} = 4mA	V_{SS}		0.3	V
Differential Input Sensitivity	V_{DI}	|DP to DM|; system requirement, not tested	0.2			V
Common-Mode Voltage Range	V_{CM}	Includes V_{DI} range; system requirement, not tested	0.8		2.5	V
Transition Time (Rise/Fall) DP, DM	t_{RF}	C_L = 50pF	4		20	ns
Pullup Resistor on Upstream Ports	R_{PU}		1.05	1.5	1.95	kΩ
USB/HI-SPEED						
Hi-Speed Data Signaling Common-Mode Voltage Range	V_{HSCM}		-50		+500	mV
Hi-Speed Squelch Detection Threshold	V_{HSSQ}	Squelch detected		100		mV
		No squelch detected		200		
Hi-Speed Idle Level Output Voltage	V_{HSOI}		-10		+10	mV
Hi-Speed Low-Level Output Voltage	V_{HSOL}		-10		+10	mV
Hi-Speed High-Level Output Voltage	V_{HSOH}			400 ±40		mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}			900 ±200		mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}			-700 ±200		mV

Electrical Characteristics—SPI

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MASTER MODE						
SPI Master Operating Frequency	f_{MCK}	f_{SYS_CLK} = 96MHz, $f_{MCK(MAX)} = f_{SYS\_CLK}/2$			48	MHz
SPI Master SCK Period	t_{MCK}			$1/f_{MCK}$		ns
SCK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}		$t_{MCK}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Low Idle	t_{MLH}			$t_{MCK}/2$		ns
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCK}/2$		ns
SLAVE MODE						
SPI Slave Operating Frequency	f_{SCK}				48	MHz
SPI Slave SCK Period	t_{SCK}			$1/f_{SCK}$		ns
SCK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		
SSx Active to First Shift Edge	t_{SSE}			10		ns
MOSI Input to SCK Sample Edge Rise/Fall Setup	t_{SIS}			5		ns
MOSI Input from SCK Sample Edge Transition Hold	t_{SIH}			1		ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}			5		ns
SCK Inactive to SSx Inactive	t_{SSD}			10		ns
SSx Inactive Time	t_{SSH}			$1/f_{SCK}$		µs
MISO Hold Time After SSx Deassertion	t_{SLH}			10		ns

Electrical Characteristics—I²C

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STANDARD MODE						
Output Fall Time	t_{OF}	Standard mode, from $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
SCL Clock Frequency	f_{SCL}		0		100	kHz
Low Period SCL Clock	t_{LOW}		4.7			µs
High Time SCL Clock	t_{HIGH}		4.0			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		4.7			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		4.0			µs
Data Setup Time	$t_{SU;DAT}$			300		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			800		ns
Fall Time for SDA and SCL	t_F			200		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		4.0			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		4.7			µs
Data Valid Time	$t_{VD;DAT}$		3.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		3.45			µs
FAST MODE						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Low Period SCL Clock	t_{LOW}		1.3			µs
High Time SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			µs
Data Setup Time	$t_{SU;DAT}$			125		ns
Data Hold Time	$t_{HD;DAT}$			10		ns

Electrical Characteristics—I²C (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time for SDA and SCL	t_R			30		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.6			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		1.3			µs
Data Valid Time	$t_{VD;DAT}$		0.9			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9			µs
FAST MODE PLUS						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		80		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Low Period SCL Clock	t_{LOW}		0.5			µs
High Time SCL Clock	t_{HIGH}		0.26			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.26			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.26			µs
Data Setup Time	$t_{SU;DAT}$			50		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			50		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.26			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		0.5			µs
Data Valid Time	$t_{VD;DAT}$		0.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.45			µs

Electrical Characteristics—SD/SDIO/SDHC/MMC

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency in Data Transfer Mode	f_{SDHC_CLK}		0		$f_{H-SCLK}/2$	MHz
Clock Period	t_{CLK}			$1/f_{SD-HC\_CLK}$		ns
Clock Low Time	t_{WCL}			7		ns
Clock High Time	t_{WCH}			7		
Input Setup Time	t_{ISU}			5		ns
Input Hold Time	t_{IHLD}			1		ns
Output Valid Time	t_{OVLD}			5		ns
Output Hold Time	t_{OHLD}			6		ns

Electrical Characteristics—1-Wire Master

(TIming specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write 0 Low Time	t_{W0L}	Standard		60		µs
		Overdrive		8		
Write 1 Low Time	t_{W1L}	Standard		6		µs
		Standard, long line mode		8		
		Overdrive		1		
Presence Detect Sample	t_{MSP}	Standard		70		µs
		Standard, long line mode		85		
		Overdrive		9		
Read Data Value	t_{MSR}	Standard		15		µs
		Standard, long line mode		24		
		Overdrive		3		
Recovery Time	t_{REC0}	Standard		10		µs
		Standard, long line mode		20		
		Overdrive		4		
Reset Time High	t_{RSTH}	Standard		480		µs
		Overdrive		58		
Reset Time Low	t_{RSTL}	Standard		600		µs
		Overdrive		70		
Time Slot	t_{SLOT}	Standard		70		µs
		Overdrive		12		

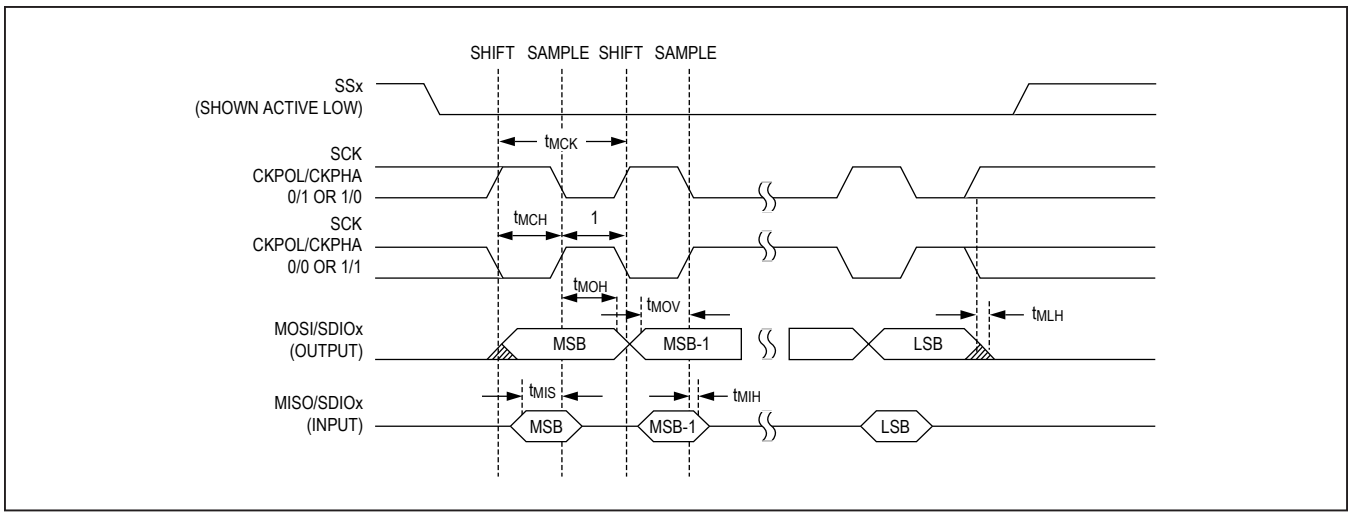


Figure 1. SPI Master Mode Timing Diagram

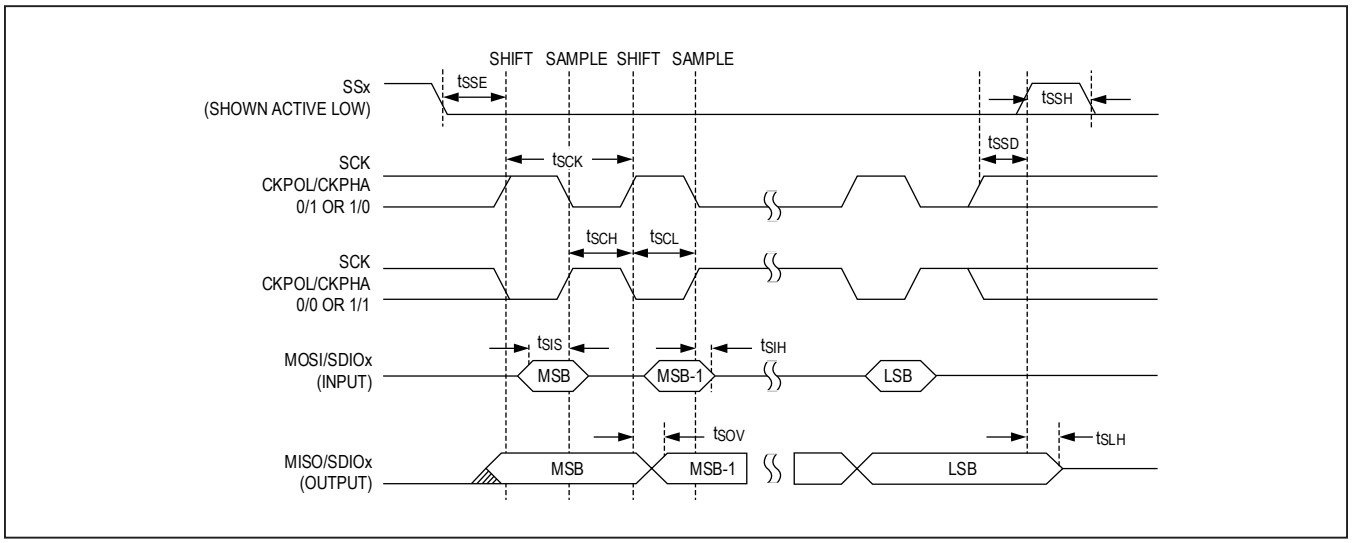


Figure 2. SPI Slave Mode Timing Diagram

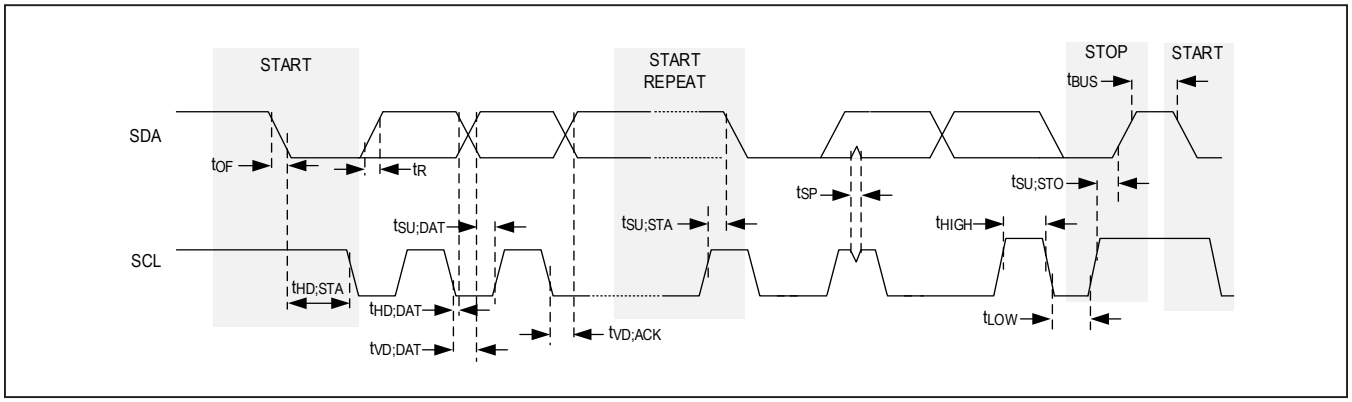


Figure 3. I²C Timing Diagram

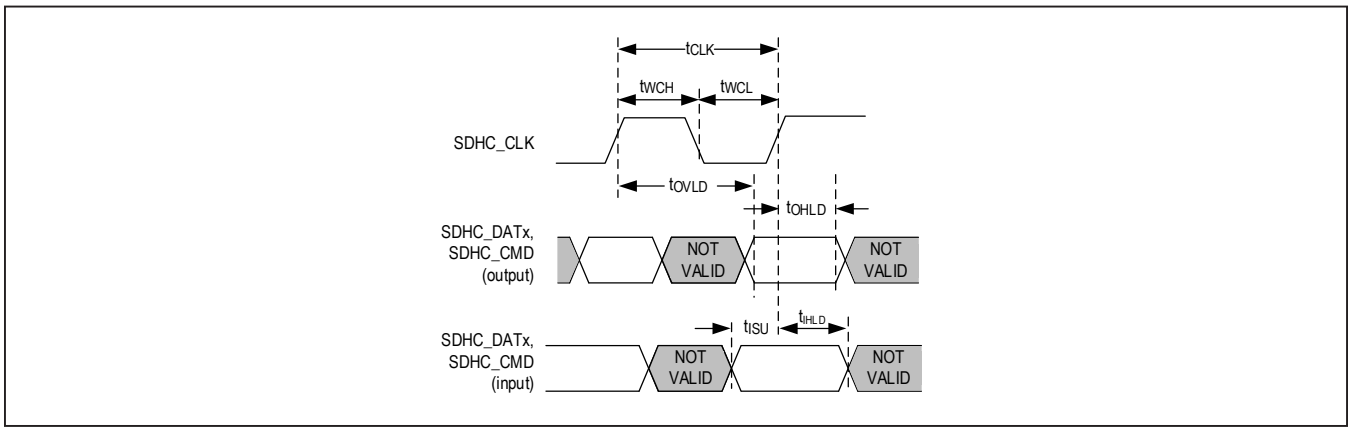


Figure 4. SD/SDIO/SDHC/MMC Timing Diagram

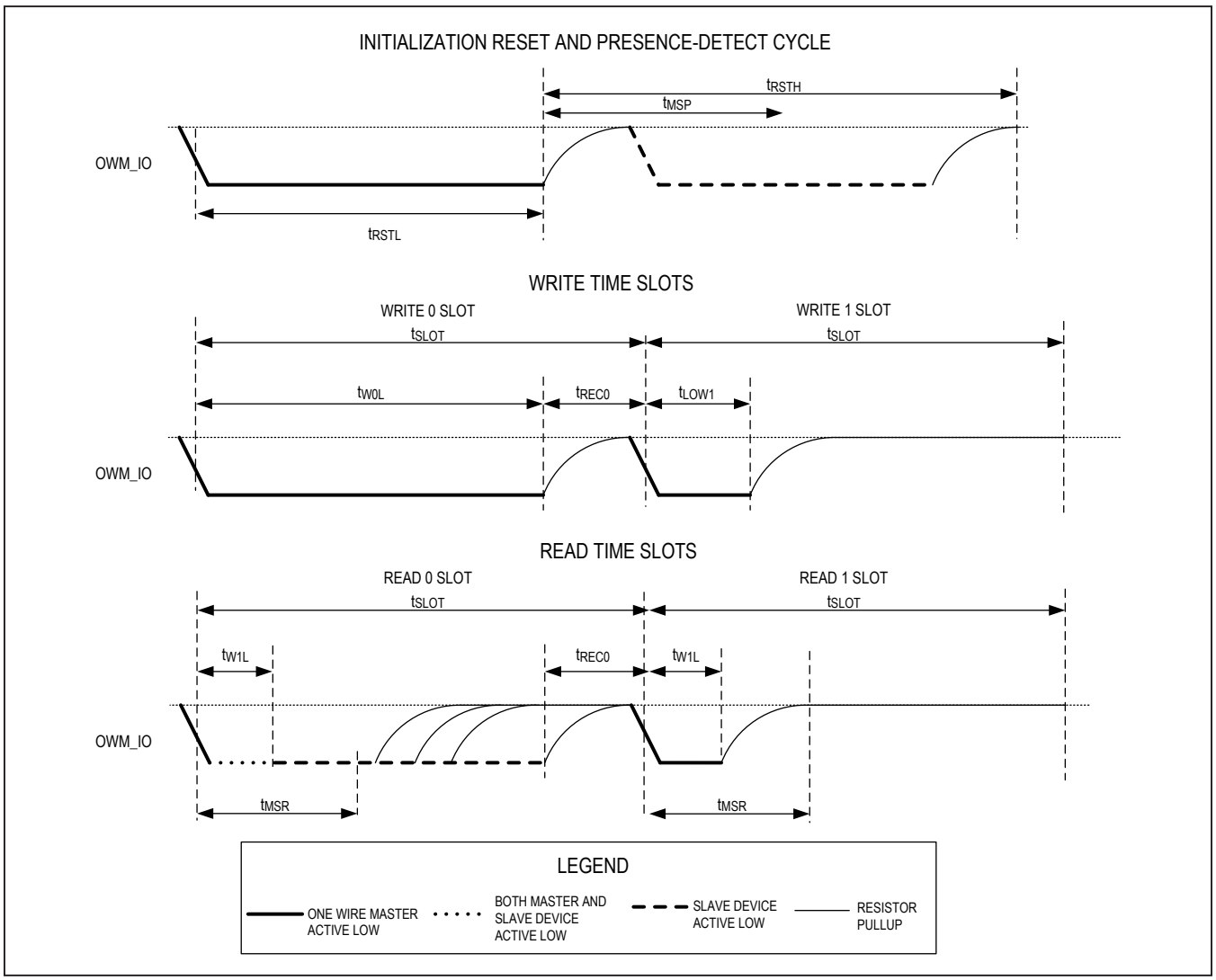


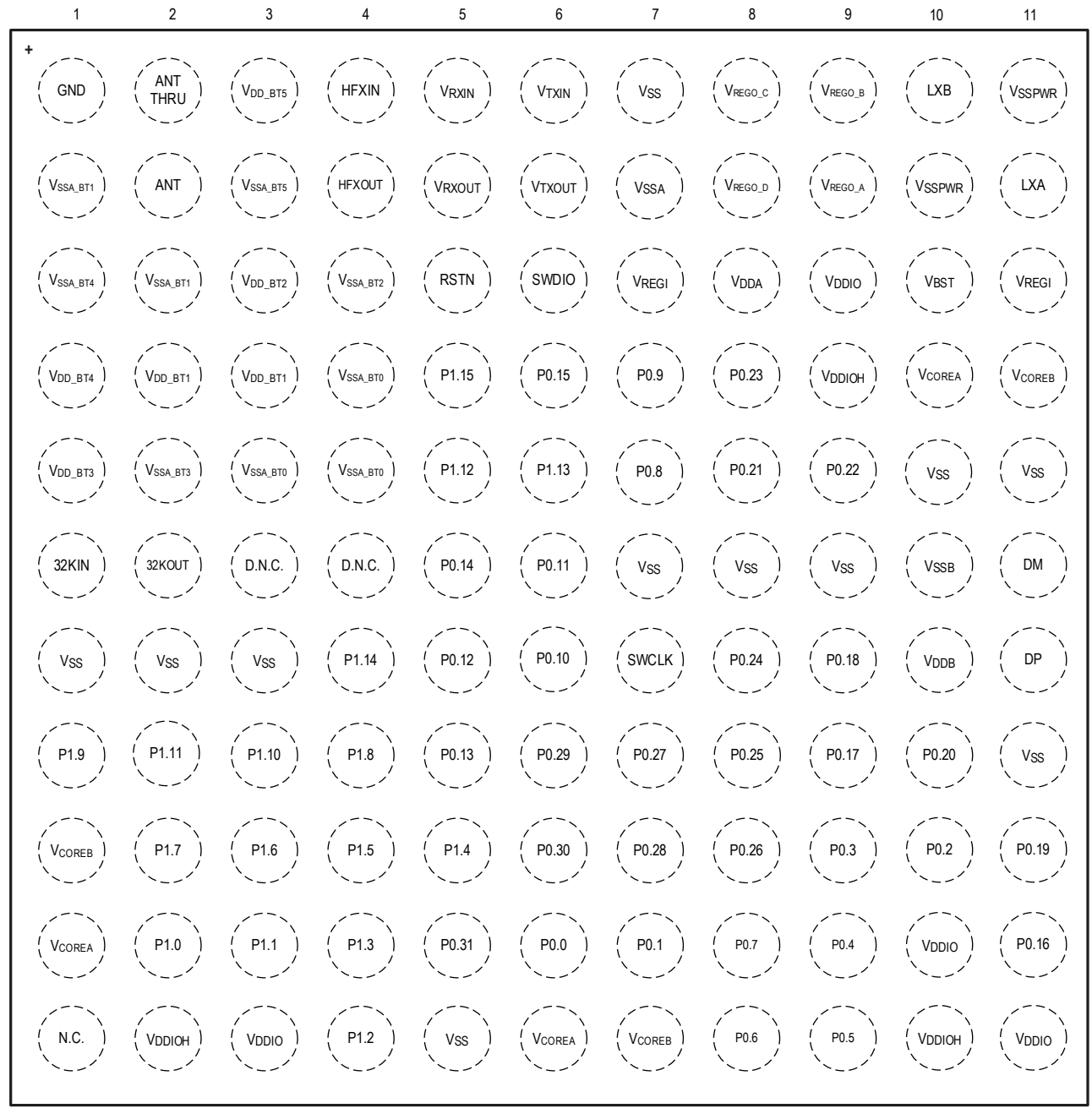
Figure 5. One-Wire Master Data Timing Diagram

Pin Configurations

109 WLP

Pin Configurations (continued)

TOP VIEW (BUMP SIDE DOWN)



121 CTBGA

Pin Description

PIN		NAME	FUNCTION
109 WLP	121 CTBGA		
POWER PINS			
H7, H11	C7, C11	V_{REGI}	Battery Power Supply. Bypass this pin to V_{SS} with 2 x 47µF capacitors placed as close as possible to the V_{REGI} and V_{SSPWR} pins.
J10, K11	A11, B10	V_{SSPWR}	Ground for the SIMO SMPS
A5, D11, F2, F3, G4, H4, K7	A7, E10, E11, F7, F8, F9, G1, G2, G3, H11, L5	V_{SS}	Digital Ground
—	A1	GND	This device pin is not connected internally to the die. Connect this device pin to the ground plane of the circuit board. Do not connect any other signal to this pin.
K6	A6	V_{TXIN}	Radio Transmitter Supply Voltage
K5	A5	V_{RXIN}	Radio Receiver Supply Voltage
J11	B11	LXA	Switching Inductor Input A. Connect a 2.2µH inductor between LXA and LXB.
K10	A10	LXB	Switching Inductor Input B. Connect a 2.2µH inductor between LXA and LXB.
H10	C10	V_{BST}	Boosted Supply Voltage for the Gate Drive of High-Side Switches. Bypass V_{BST} to LXB with a 3.3nF capacitor.
J9	B9	V_{REGO_A}	Buck Converter A Voltage Output. Bypass V_{REGO_A} with a 22µF capacitor to V_{SS} placed as close as possible to the V_{DDA} device pin.
K9	A9	V_{REGO_B}	Buck Converter B Voltage Output. Bypass V_{REGO_B} with a 22µF capacitor to V_{SS} placed as close as possible to the closest V_{COREB} device pin.
K8	A8	V_{REGO_C}	Buck Converter C Voltage Output. Bypass V_{REGO_C} with a 22µF capacitor to V_{SS} placed as close as possible to the closest V_{COREA} device pin.
J8	B8	V_{REGO_D}	Buck Converter D Voltage Output. Bypass V_{REGO_D} with a 22µF capacitor to V_{SS} placed as close as possible to the V_{RXIN} and V_{TXIN} device pins.
H8	C8	V_{DDA}	1.8V Analog/Digital Power Supply
J7	B7	V_{SSA}	Analog Ground
J6	B6	V_{TXOUT}	Radio Transmitter Supply Voltage Output. Bypass this pin to V_{SS} with a 1.0µF capacitor placed as close as possible to the package.
J5	B5	V_{RXOUT}	Radio Receiver Supply Voltage Output. Bypass this pin to V_{SS} with a 1.0µF capacitor placed as close as possible to the package.
A3, A11, B10, H9,	C9, L3, L11, K10	V_{DDIO}	GPIO Supply Voltage. Bypass this pin to V_{SS} with a 1.0µF capacitor placed as close as possible to the package.
A2, A10, G9	D9, L2, L10	V_{DDIOH}	GPIO Supply Voltage, High. $V_{DDIOH} \geq V_{DDIO}$. Bypass this pin to V_{SS} with a 1.0µF capacitor placed as close as possible to the package.
A6, B1, G10	D10, K1, L6	V_{COREA}	Digital Core Supply Voltage A
A7, C1, G11	D11, J1, L7	V_{COREB}	Digital Core Supply Voltage B
E10	G10	V_{DDB}	USB Transceiver Supply Voltage. Bypass this pin to V_{SSB} with a 1.0µF capacitor as close as possible to the package.
F10	F10	V_{SSB}	USB Transceiver Ground
J2	D2, D3	V_{DD_BT1}	0.9V Analog Power Supply for the Bluetooth Radio Low Noise Amplifier and Mixer
J3	C3	V_{DD_BT2}	0.85V Power Supply for the Bluetooth Radio Power Amplifier
G3	E1	V_{DD_BT3}	0.9V Power Supply for the Bluetooth Radio FRAC-N Divider

Pin Description (continued)

PIN		NAME	FUNCTION
109 WLP	121 CTBGA		
G1	D1	V_{DD_BT4}	0.9V Power Supply for the Bluetooth Radio Receiver Baseband
H2	A3	V_{DD_BT5}	0.9V Power Supply for the Bluetooth Radio Voltage-Controlled Oscillator
F4	D4, E3, E4	V_{SSA_BT0}	Bluetooth Radio Analog Ground 0
J1	B1, C2	V_{SSA_BT1}	Bluetooth Radio Analog Ground 1
K3	C4	V_{SSA_BT2}	Bluetooth Radio Analog Ground 2
G2	E2	V_{SSA_BT3}	Bluetooth Radio Analog Ground 3
H1	C1	V_{SSA_BT4}	Bluetooth Radio Analog Ground 4
H3	B3	V_{SSA_BT5}	Bluetooth Radio Analog Ground 5
CLOCK PINS			
E1	F2	32KOUT	32kHz Crystal Oscillator Output
F1	F1	32KIN	32kHz Crystal Oscillator Input. Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
J4	B4	HFXOUT	32MHz Crystal Oscillator Output
K4	A4	HFXIN	32MHz Crystal Oscillator Input. Connect a 32MHz crystal between HFXIN and HFXOUT for Bluetooth operation. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
USB PINS			
E11	G11	DP	USB DP Signal. This bidirectional pin carries the positive differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled.
F11	F11	DM	USB DM Signal. This bidirectional pin carries the negative differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled.
TEST PINS			
E7	G7	SWCLK	Serial Wire Debug Clock/TCK/GPIO. When TTAP_ENABLE = 1, this pin becomes the JTAG Test Clock (TCK). This pin can also be configured as a GPIO.
H6	C6	SWDIO	Serial Wire Debug I/O/TMS/GPIO. When TTAP_ENABLE = 1, this pin becomes the JTAG Mode Select (TMS). This spin can also be configured as a GPIO.
RESET PINS			
H5	C5	RSTN	Hardware Power Reset (Active-Low) Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin has an internal pullup to the V_{DDIO} supply.
GPIO AND ALTERNATE FUNCTIONS (See the *Applications Information* section for GPIO Matrix)			
B6	K6	P0.0	General-Purpose I/O, Port 0
B7	K7	P0.1	General-Purpose I/O, Port 0
C10	J10	P0.2	General-Purpose I/O, Port 0
C9	J9	P0.3	General-Purpose I/O, Port 0
B9	K9	P0.4	General-Purpose I/O, Port 0
A9	L9	P0.5	General-Purpose I/O, Port 0
A8	L8	P0.6	General-Purpose I/O, Port 0
B8	K8	P0.7	General-Purpose I/O, Port 0

Pin Description (continued)

PIN		NAME	FUNCTION
109 WLP	121 CTBGA		
F7	E7	P0.8	General-Purpose I/O, Port 0
G7	D7	P0.9	General-Purpose I/O, Port 0
E6	G6	P0.10	General-Purpose I/O, Port 0
F6	F6	P0.11	General-Purpose I/O, Port 0
E5	G5	P0.12	General-Purpose I/O, Port 0
D5	H5	P0.13	General-Purpose I/O, Port 0
F5	F5	P0.14	General-Purpose I/O, Port 0
G6	D6	P0.15	General-Purpose I/O, Port 0
B11	K11	P0.16	General-Purpose I/O, Port 0
D9	H9	P0.17	General-Purpose I/O, Port 0
E9	G9	P0.18	General-Purpose I/O, Port 0
C11	J11	P0.19	General-Purpose I/O, Port 0
D10	H10	P0.20	General-Purpose I/O, Port 0
F8	E8	P0.21	General-Purpose I/O, Port 0
F9	E9	P0.22	General-Purpose I/O, Port 0
G8	D8	P0.23	General-Purpose I/O, Port 0
E8	G8	P0.24	General-Purpose I/O, Port 0
D8	H8	P0.25	General-Purpose I/O, Port 0
C8	J8	P0.26	General-Purpose I/O, Port 0
D7	H7	P0.27	General-Purpose I/O, Port 0
C7	J7	P0.28	General-Purpose I/O, Port 0
D6	H6	P0.29	General-Purpose I/O, Port 0
C6	J6	P0.30	General-Purpose I/O, Port 0
B5	K5	P0.31	General-Purpose I/O, Port 0
A1, B2	K2	P1.0	General-Purpose I/O, Port 1
B3	K3	P1.1	General-Purpose I/O, Port 1
A4	L4	P1.2	General-Purpose I/O, Port 1
B4	K4	P1.3	General-Purpose I/O, Port 1
C5	J5	P1.4	General-Purpose I/O, Port 1
C4	J4	P1.5	General-Purpose I/O, Port 1
C3	J3	P1.6	General-Purpose I/O, Port 1
C2	J2	P1.7	General-Purpose I/O, Port 1
D4	H4	P1.8	General-Purpose I/O, Port 1
D1	H1	P1.9	General-Purpose I/O, Port 1
D3	H3	P1.10	General-Purpose I/O, Port 1
D2	H2	P1.11	General-Purpose I/O, Port 1

Pin Description (continued)

PIN		NAME	FUNCTION
109 WLP	121 CTBGA		
E2	E5	P1.12	General-Purpose I/O, Port 1
E3	E6	P1.13	General-Purpose I/O, Port 1
E4	G4	P1.14	General-Purpose I/O, Port 1
G5	D5	P1.15	General-Purpose I/O, Port 1
ANTENNA OUTPUT			
K2	B2	ANT	Antenna for Bluetooth Radio. Attach the single-ended unbalanced Bluetooth radio antenna.
—	A2	ANT THRU	The single-ended unbalanced Bluetooth radio antenna circuit board trace uses this pin as a pass-through. Do not connect any other signal to this pin.
NO CONNECT			
—	F3, F4	D.N.C.	Do Not Connect. Internally connected. Do not make any electrical connection to this pin, including power supply grounds.
—	L1	N.C.	No Connection. Not internally connected.

Detailed Description

The MAX32665-MAX32668 are Arm Cortex-M4 with FPU-based microcontrollers with 1MB flash and up to 560KB SRAM that can be configured as 448KB SRAM with error correction coding (ECC). They are ideal for wearable medical fitness applications. Optionally available is a second Arm Cortex-M4 with FPU for audio signal processing in a wireless headset/earbud application (MAX32665/MAX32666 only). The architecture includes a Bluetooth 5 Low Energy radio.

The devices feature five powerful and flexible power modes. The flash memory is split into two banks of 512KB to provide flexibility when programming over-the-air. A built-in single inductor multiple output (SIMO) switch mode power supply allows the device to be optionally self-powered by a primary lithium cell. The devices have an ECC with single error correction double error detection (SEC-DED) for flash, and SRAM providing extremely reliable code execution. Dedicated hardware runs the Bluetooth 5 Low Energy stack freeing the CPUs for data processing tasks. Built-in dynamic clock gating and firmware-controlled power gating allows the user to optimize power for the specific application. Multiple SPI, UART, and I^2C serial interfaces, 1-Wire Master, and USB 2.0 High-Speed Device interface allow for interconnection to a wide variety of external sensors. An audio subsystem supporting PDM, PCM, I^2S, and TDM. An 8-input, 10-bit ADC is available to monitor analog input from external sensors and meters.

The MAX32665/MAX32666 feature a second Arm Cortex-M4 with FPU with supporting ROM and cache. This feature supports extended data processing capabilities such as audio processing for wireless Bluetooth applications. See the *Ordering Information* for device feature detail.

The MAX32666/MAX32668 incorporate a trust protection unit (TPU) with encryption and advanced security features. These features include a modular arithmetic accelerator (MAA) for fast ECDSA, a hardware AES engine, a hardware TRNG entropy generator, a SHA-2 accelerator and a secure bootloader.

All devices are available in a 109-bump WLP with 0.35mm pitch and a 121-bump CTBGA with 0.65mm pitch packages.

Arm Cortex-M4 with FPU Processor

The Arm Cortex-M4 with FPU processors CPU0 and CPU1 are ideal for the emerging category of wearable medical and wellness applications. The architecture combines high-efficiency signal processing functionality with low power, low cost, and ease of use.

The Arm Cortex-M4 with FPU DSP supports single instruction multiple data (SIMD) path DSP extensions, providing:

- Four parallel 8-bit add/sub
- Floating point single precision
- Two parallel 16-bit add/sub
- Two parallel MACs
- 32- or 64-bit accumulate
- Signed, unsigned, data with or without saturation

Memory

Internal Flash Memory

1MB of internal flash memory provides nonvolatile storage of program and data memory. It is supported by ECC with SEC-DED.

Flash can be expanded through the SPIXF flash serial interface backed by 16KB of cache. The SPIXF flash interface can address an additional 128MB.

Internal SRAM

The internal 560KB SRAM provides low-power retention of application information in all power modes. The SRAM can be configured as 448KB with ECC SEC-DED). The SRAM can be divided into granular banks that create a flexible SRAM retention architecture. This data-retention feature is optional and configurable. This granularity allows the application to minimize its power consumption by retaining the most essential data only.

SRAM can be expanded through the SPIXR SRAM serial interface supported by 16KB of cache. The SPIXR SRAM interface can address an additional 512MB.

Secure Digital Interface

The secure digital interface (SDI) provides high-speed, high-density data storage capability for media files and large long-term data logs. This interface supports eMMC, SD, SDHC, and SDXC memory devices at transfer rates up to 24MB/s. The 7-pin interface (4 data, 1 clock, 1 command, 1 write-protect) supports the following specifications:

- SD Host Controller Standard Specification Version 3.00
- SDIO Card Specification Version 3.0
- SD Memory Card Specification Version 3.01
- SD Memory Card Security Specification Version 1.01
- MMC Specification Version 4.51

Bluetooth 5

Bluetooth 5 Low Energy Radio

Bluetooth 5 Low Energy is the latest version of the Bluetooth wireless communication standard. It is used for wireless headphones and other audio hardware, as well as for communication between various smart home and Internet of Things (IoT) devices. Devices operate in the unlicensed 2.4GHz ISM (Industrial, Scientific, Medical) band. A frequency-hopping transceiver is used to combat interference and fading. The system operates in the 2.4GHz ISM band at 2400MHz–2483.5MHz. It uses 40 RF channels. These RF channels have center frequencies 2402 + k x 2MHz, where k = 0, ..., 39.

The Bluetooth stack runs on dedicated hardware so that CPU0 and CPU1 can be free to run application code.

The features of the radio include the following:

- Higher transmit power up to +9.5dbm
- 1Mbps, 2Mbps, and Long Range coded (125kbps and 500kbps)
- Increased broadcast capability
  - Advertizing packet up to 255 bytes
- On-chip matching network to the antenna
- Provides hardware on-the-fly encryption and decryption for lower power consumption
- Low transmit current of 2.5mA at 0dbm at 3.3V
- Low receive current of 1.5mA at 3.3V
- Supports mesh networking
- Supports high-quality audio streaming (isochronous)
- Low-power proprietary mode that supports 20kbps, 40kbps, 500kbps-MSK/GFSK, 1Mpbs-GFSK

Bluetooth 5 Software Stack

A Bluetooth 5 software stack is available for application developers to quickly add support to devices. The Arm Cordio®-B50 software stack is provided in library form and provides application developers access to Bluetooth without validation and development of a software stack. The Cordio-B50 software stack interfaces to the Bluetooth link layer running on dedicated hardware. The dedicated hardware for the stack enables the ultimate in power management for IoT applications.

Cordio-B50 features the following:

- C library for linking directly into an application development tool
- Change PHY Support
  - Host selects the PHY it needs to use at any given time enabling long range or higher bandwidth only when required
  - LE 1M
  - LE Coded S = 2
  - LE Coded S = 8
  - LE 2M
- Bluetooth 5 advertising extention support for enabling next generation Bluetooth beacons
  - Larger packets and advertising channel offloading
  - Packets up to 255 octets long
  - Advertising packet chaining
  - Advertising sets
  - Periodic advertising
  - High-duty cycle nonconnectable advertising
  - Sample applications using standard profiles built on the Cordio-B50 software framework

Comparators

The eight AIN[7:0] inputs can be configured as four pairs and deployed as four independent comparators with the following features:

- Comparison events can trigger interrupts
- Events can wake the CPU from Sleep, DeepSleep, or Backup operating mode
- Can be active in all power modes

Dynamic Voltage Scaling Controller

The Dynamic Voltage Scaling (DVS) Controller works using the fixed high-speed oscillator and the V_{COREA} supply voltage to optimally operate the Arm core at the lowest practical voltage. The ability to adaptively adjust the voltage provides a significant reduction in dynamic power consumption.

The DVS Controller provides the following features:

- Controls DVS monitoring and adjustment functions
- Continuous monitoring with programmable monitor sample period
- Controlled transition to a programmable operating point
- Independent high and low operating limits for safe, bounded operation
- Independent high, center, and low operating range delay line delay monitors
- Programmable adjustment rate, when an adjustment is required
- Single clock operation
- APB interface provides IP control and status access
- Interrupt capability during error

Clocking Scheme

The high-frequency oscillator operates at a maximum frequency of 96MHz.

Optionally, five other oscillators can be selected depending upon power needs:

- 60MHz low-power oscillator (f_{LPCLK})
- 8kHz nano-ring oscillator (f_{NANO})
- 32.768kHz RTC oscillator (external crystal required)
- 7.3728MHz oscillator (f_{7MCLK})
- 32MHz RF oscillator (external crystal required) (f_{RFCLK})

This clock is the primary clock source for the digital logic and peripherals. Select the 7.3728MHz internal oscillator to optimize active power consumption. Using the 7.3727MHz oscillator allows UART communications to meet a 2% baud rate tolerance. Wake-up is possible from either the 7.3728MHz internal oscillator or the high-frequency oscillator. The device exits power-on reset using the the 60MHz oscillator.

An external 32.768kHz timebase is required when using the RTC.

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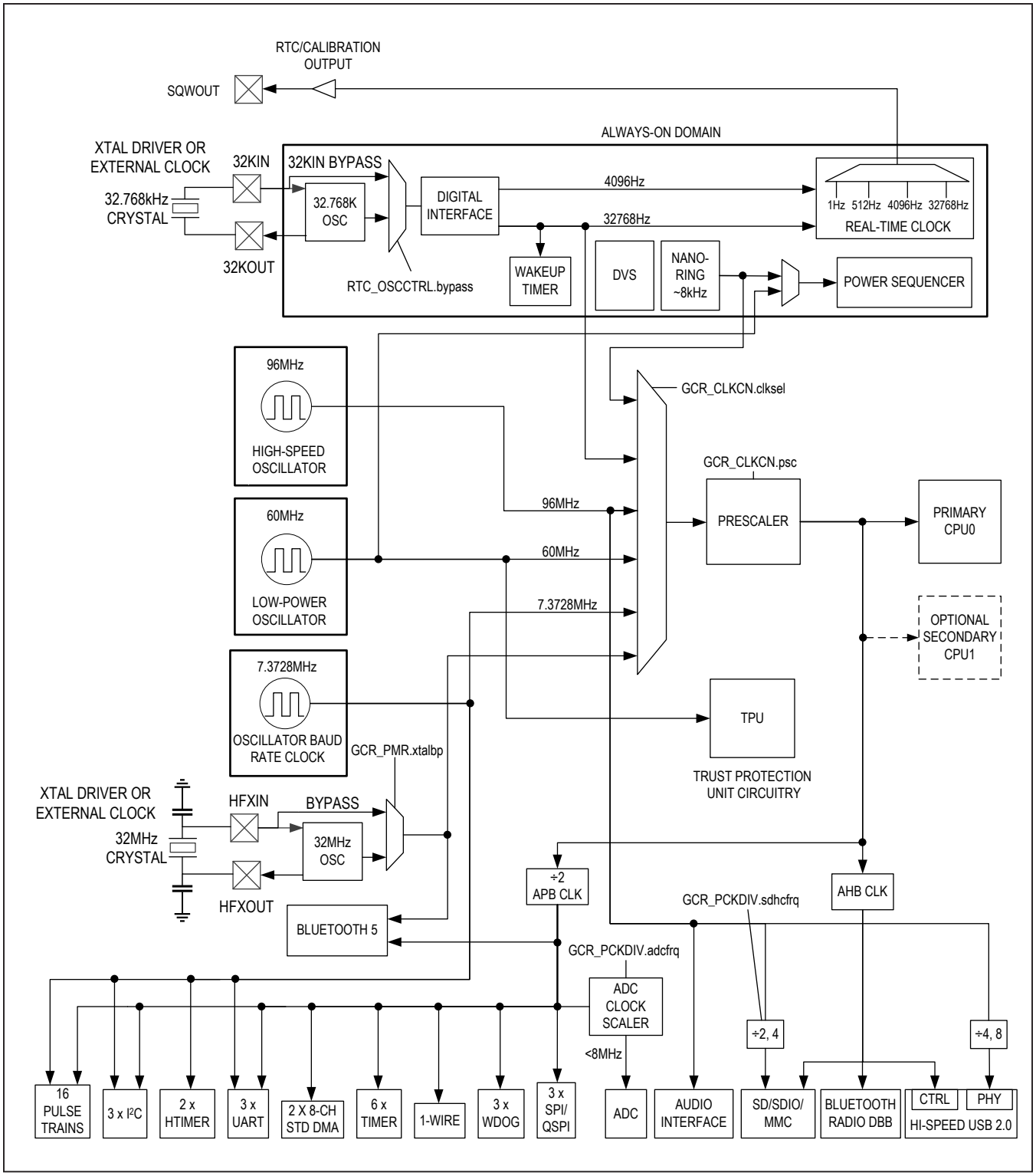

Figure 6. Clocking Scheme Diagram

General-Purpose I/O and Special Function Pins

Most general-purpose I/O (GPIO) pins share both a firmware-controlled I/O function and one or more alternate functions associated with peripheral modules. Pins can be individually enabled for GPIO or peripheral special function use. Configuring a pin as a special function usually supersedes its use as a firmware-controlled I/O. Although this multiplexing between peripheral and GPIO functions is usually static, it can also be done dynamically. The electrical characteristics of a GPIO pin are identical whether the pin is configured as an I/O or special function, except where explicitly noted in the *Electrical Characteristics* tables.

In GPIO mode, pins are logically divided into ports of 32 pins. Each pin of a port has an interrupt function that can be independently enabled, and configured as a level- or edge-sensitive interrupt. All GPIOs of a given port share the same interrupt vector.

When configured as GPIO, the following features are provided. The features can be independently enabled or disabled on a per-pin basis.

- Configurable as input, output, bidirectional, or high impedance
- Optional internal pullup resistor or internal pulldown resistor when configured as input
- Exit from low-power modes on rising or falling edge
- Selectable standard- or high-drive modes

The MAX32665–MAX32668 provide up to 50 GPIO pins.

Analog-to-Digital Converter

The 10-bit delta-sigma ADC provides an integrated reference generator and a single-ended input multiplexer. The multiplexer selects an input channel from one of the eight external analog input signals (AIN0–AIN7) or the internal power supply inputs.

The reference for the ADC can be:

- Internal 1.22V bandgap
- V_{DDA} analog supply

An optional feature allows samples captured by the ADC to be automatically compared against user-programmable high and low limits. Up to four channel limit pairs can be configured in this way. The comparison allows the ADC to trigger an interrupt (and potentially wake the CPU from a low-power sleep mode) when a captured sample goes outside the preprogrammed limit range. Since this comparison is performed directly by the sample limit monitors, it can be performed even while the CPU is is in Sleep or DeepSleep mode. The eight AIN[7:0] inputs can be configured a four pairs and deployed as four independent comparators.

The ADC measures the following voltages:

- AIN[7:0] up to 3.3V
- V_{REGI}
- V_{TXOUT}
- V_{RXOUT}
- V_{COREA}
- V_{COREB}
- V_{DDIOH}
- V_{DDIO}
- V_{DDB}
- V_{DDA}

Single-Inductor Multiple-Output Switch-Mode Power Supply (SIMO SMPS)

The SIMO SMPS built into the device provides a monolithic power supply architecture for operation from a single lithium cell. The SIMO provides four buck regulator outputs that are voltage programmable. This architecture optimizes power consumption efficiency of the device and minimizes the bill of materials for the circuit design since only a single inductor/capacitor pair is required.

Power Management

Power Management Unit

The power management unit (PMU) provides high-performance operation while minimizing power consumption. It exercises intelligent, precise control of power distribution to the CPUs and peripheral circuitry.

The PMU provides the following features:

- User-configurable system clock
- Automatic enabling and disabling of crystal oscillators based on power mode
- Multiple power domains
- Fast wake-up of powered-down peripherals when activity detected

Active Mode

In this mode, the CPU is executing application code and all digital and analog peripherals are available on demand. Dynamic clocking disables peripherals not in use, providing the optimal mix of high performance and low power consumption.

Sleep Mode

This mode consumes less power, but wakes faster because the clocks can optionally be enabled.

The device status is as follows:

- CPU is asleep.
- Peripherals are on.
- Standard DMA blocks are available for optional use.

DeepSleep Mode

This mode corresponds to the Arm Cortex-M4 with FPU DeepSleep mode. In this mode, CPU and critical peripheral configuration settings and all volatile memory is preserved.

The device status is a follows:

- CPU is off.
- The GPIO pins retain their state.
- The transition from DeepSleep to Active mode is faster than the transition from Backup mode because system initialization is not required.
- The system oscillators are all disabled to provide additional power savings over Sleep mode:
  - 96MHz high-speed oscillator
  - 60MHz low-power oscillator
  - 7.3728MHz oscillator system clock shuts down.

Backup Mode

This mode places the CPUs in a static, low-power state that supports a fast wake-up to Active mode feature.

The device status is as follows:

- CPU is off.
- Either 32KB, 64KB, or all the SRAM can be retained.
- The RTC can be enabled.

Wake-Up Sources

The sources of wakeup from the Sleep, DeepSleep, and Backup operating modes are summarized in Table 1.

Real-Time Clock

A real-time clock (RTC) keeps the time of day in absolute seconds. The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software.

The RTC provides a time-of-day alarm that can be programmed to any future value between 1 second and 12 days. When configured for long intervals, the time-of-day alarm can be used as a power-saving timer, allowing the device to remain in an extremely low-power mode, but still awaken periodically to perform assigned tasks. A second independent 32-bit 1/4096 subsecond alarm can be programmed with a tick resolution of 244µs. Both can be configured as recurring alarms. When enabled, either alarm can cause an interrupt or wake the device from most low power modes.

The time base is generated by a 32.768kHz crystal or an external clock source that must meet the electrical/timing requirements in the *Electrical Characteristics* table.

The RTC calibration feature provides the ability for user software to compensate for minor variations in the RTC oscillator, crystal, temperature, and board layout. Enabling the SQWOUT alternate function outputs a timing signal derived from the RTC. External hardware can measure the frequency and adjust the RTC frequency in increments of ±127ppm with 1ppm resolution. Under most circumstances, the oscillator does not require any calibration.

Table 1. Wake-Up Sources

OPERATING MODE	WAKE-UP SOURCE
Sleep	Interrupts (RTC, GPIO, USB, comparators, all peripherals), RSTN assertion, wake-up timer
DeepSleep	Interrupts (RTC, GPIO, USB, comparators), RSTN assertion, wake-up timer
Backup	Interrupts (RTC, GPIO, USB, comparators), RSTN assertion, wake-up timer

CRC Module

A cyclic redundancy check (CRC) hardware module provides fast calculations and data integrity checks by application software. The CRC module supports the following polynomials:

- CRC-16-CCITT
- CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$)

Programmable Timers

32-Bit Timer/Counter/PWM (TMR)

General-purpose, 32-bit timers provide timing, capture/compare, or generation of pulse-width modulated (PWM) signals with minimal software interaction. Each of the 32-bit timers can also be split into two 16-bit timers.

The timer provides the following features:

- 32-bit up/down autoreload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External pin multiplexed with GPIO for timer input, clock gating, or capture
- Timer output pin
- Configurable as 2 x 16-bit general-purpose timers
- Timer interrupt

The MAX32665–MAX32668 provides six instances of the general-purpose 32-bit timer (TMR0, TMR1, TMR2, TMR3, TMR4, and TMR5).

Watchdog Timer (WDT)

Microcontrollers are often used in harsh environments where electrical noise and electromagnetic interference (EMI) are abundant. Without proper safeguards, these can hazards can disturb device operation and corrupt program execution. One of the most effective countermeasures is the watchdog timer (WDT), which detects runaway code or system unresponsiveness.

The WDT is a 32-bit, free-running counter with a configurable prescaler. When enabled, the WDT must be periodically reset by the application software. Failure to reset the WDT within the user-configurable timeout period indicates that the application software is not operating correctly and results in a WDT timeout. A WDT timeout can trigger an interrupt, system reset, or both. Either response forces the instruction pointer to a known good location before resuming instruction execution.

The MAX32665–MAX32668 provide three instances of the WDT (WDT0, WDT1, WDT2). All three WDTs are identical and independent of each other. Each has a dedicated reset bit, reset and/or interrupt enable bits, and status flags. They all share the same timebase, which is a scaled of the version system clock, but have independent prescale values.

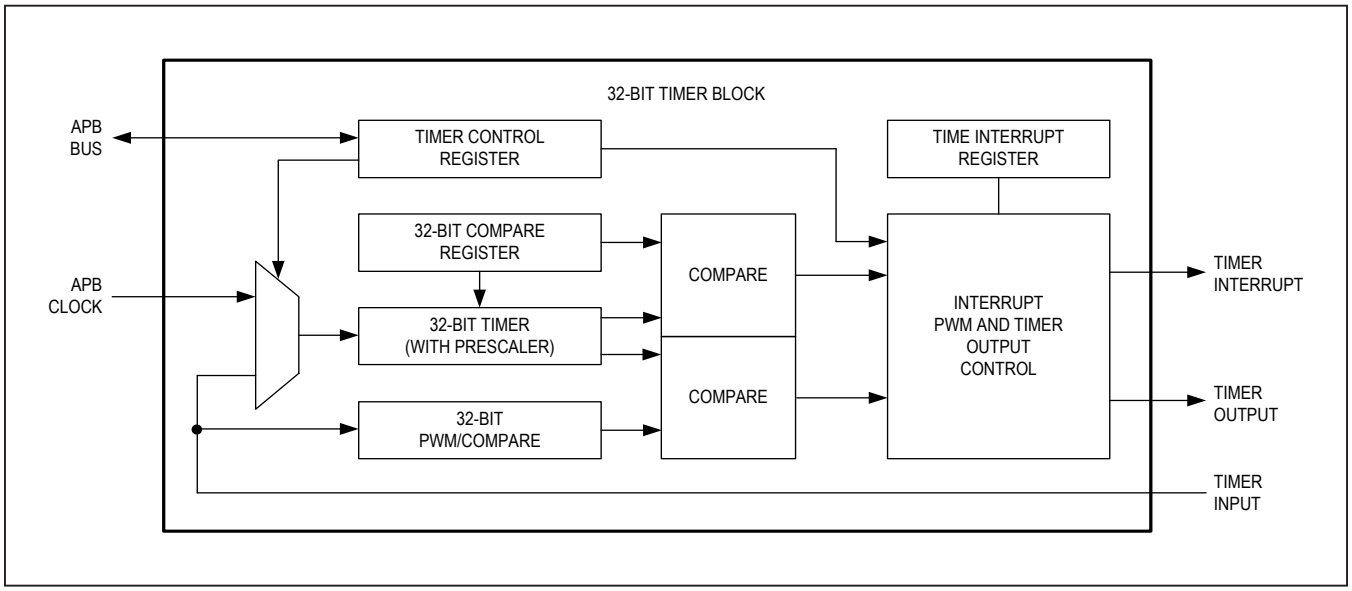

Figure 7. 32-Bit Timer

Pulse Train Engine (PT)

Multiple independent pulse train generators can provide either a square wave or a repeating pattern from 2 to 32 bits in length. Any single pulse train generator or any desired group of pulse train generators can be synchronized at the bit level allowing for multibit patterns. Each pulse train generator is independently configurable.

The pulse train generators provide the following features:

- Independently enabled
- Safe enable and disable for pulse trains without bit banding
- Multiple pin configurations allow for flexible layout
- Pulse trains can be started/synchronized independently or as a group
- Frequency of each enabled pulse train generator is also set separately, based on a divide down (divide by 2, divide by 4, divide by 8, and so on) of the input pulse train module clock
- Input pulse train module clock can be optionally configured to be independent from the system AHB clock
- Multiple repetition options
  - Single shot (nonrepeating pattern of 2 to 32 bits)
  - Pattern repeats user-configurable number of times or indefinitely
  - Termination of one pulse train loop count can restart one or more other pulse trains

The pulse train engine feature is an alternate function associated with a GPIO pin. In most cases, enabling the pulse train engine function supersedes the GPIO function.

The MAX32665–MAX32668 provide up to 16 instances of the pulse train engine peripheral (PT[15:0]).

HTIMER

The HTIMER is a 44-bit timer that is driven by the 7.3728MHz source clock resulting in a tick resolution of 135.63ns. It is programmable to provide interrupts at count comparison.

The MAX32665–MAX32668 provide two instances of the HTIMER.

Serial Peripherals

USB Controller

The integrated USB slave controller is compliant with the High-Speed (480Mb/s) USB 2.0 specification. The integrated USB physical interface (PHY) reduces board space and system cost. An integrated voltage regulator enables smart switching between the main supply and V_{DDB} when connected to a USB host controller. The USB controller supports DMA for the endpoint buffers. A total of 11 endpoint buffers are supported with configurable selection of IN or OUT in addition to endpoint 0.

Audio Interface

The audio interface allows the device to communicate with external audio devices using standard I2S pulse-coded modulation (PCM) and pulse density modulation (PDM) audio interfaces. This allows audio algorithms to be run such as dynamic speaker management (DSM) or ambient noise cancellation (ANC).

I2S PCM mode features the following:

- Single 4-wire I2S PCM interface allowing transmit and receive of audio data and is intended to connect to speaker driver devices
- Four transmit channels and eight receive channels are supported to allow 4-channel DSM
- Support two PDM receive channels at the same time as PCM support
- Sample rates from 8kHz to 192kHz

PDM mode features the following:

- Up to two PDM transmit channels at 3.072MHz
- Up to two PDM receive channels at 3.072MHz
- Interpolation and decimation filtering to save MIPS in the DSP

I2C Interface

The I2C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many, or many-to-many communications medium. The I2C master/slave interface to a wide variety of I2C-compatible peripherals. These engines support standard mode, fast mode, and fast mode plus I2C speeds. It provides the following features:

- Master or slave mode operation
- Supports standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive receive mode
- Tx FIFO preloading
- Support for clock stretching to allow slower slave devices to operate on higher speed buses
- Multiple transfer rates
  - Standard mode: 100kbps
  - Fast mode: 400kbps
  - Fast mode plus: 1000kbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 8 bytes
- Transmitter FIFO depth of 8 bytes

The MAX32665–MAX32668 provide three instances of the I2C interface (I2C0, I2C1, I2C2).

Serial Peripheral Interface

The serial peripheral interface (SPI) is a highly configurable, flexible, and efficient synchronous interface among multiple SPI devices on a single bus. The bus uses a single clock signal and multiple data signals, and one or more slave select lines to address only the intended target device. The SPI operates independently and requires minimal processor overhead.

The provided SPI peripherals can operate in either slave or master mode and provide the following features:

- SPI modes 0, 1, 2, 3 for single-bit communication
- 3- or 4-wire mode for single-bit slave device communication
- Full-duplex operation in single-bit, 4-wire mode
- Dual and quad data modes supported
- Multiple slave select lines on some instances
- Multimaster mode fault detection
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- 32-byte transmit and receive FIFOs
- Slave select assertion and deassertion timing with respect to leading/trailing SCK edge

The MAX32665–MAX32668 provide three instances of the SPI interface (SPI0, SPI1, SPI2).

SPI Execute in Place (SPIX) Master

There are two SPI execute in place (SPIX) master interfaces. One is dedicated for SRAM (SPIXR) and one is dedicated for flash (SPIXF) with dedicated slave selects. This allows the CPU to transparently execute instructions stored in an external SPI memory device. Instructions fetched through the SPI master are cached just like instructions fetched from internal program memory. The SPI SRAM master provides write-through capability. These two SPI execute in place master interfaces can also be used to access large amounts of external static data that would otherwise reside in internal data memory.

Table 2. SPI Configuration Options

INSTANCE	DATA	SLAVE SELECT LINES		MAXIMUM FREQUENCY (MASTER MODE) (MHz)	MAXIMUM FREQUENCY (SLAVE MODE) (MHz)
		109 WLP	121 CTBGA		
SPI0	3-wire, 4-wire, dual, or quad data support	3	3	48	48
SPI1	3-wire, 4-wire, dual, or quad data support	3	3	48	48
SPI2	3-wire, 4-wire, dual, or quad data support	3	3	48	48

UART

The universal asynchronous receiver-transmitter (UART) interface supports full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry standard request to send (RTS) and clear to send (CTS) flow control signaling. Each UART is individually programmable.

The UART supports the following features:

- Baud rate generation with ±2% optionally utilizing the 7.3727MHz relaxation oscillator
- 2-wire interface or 4-wire interface with flow control
- 32-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Interrupts available for frame error, parity error, CTS, Rx FIFO overrun and FIFO full/partially full conditions
- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th bit parity support
- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Maximum baud rate 4000kB
- Two DMA channels can be connected (read and write FIFOs)
- Programmable word size (5 bits to 8 bits)

The MAX32665–MAX32668 provide three instances of the UART peripheral (UART0, UART1, and UART2).

1-Wire Master (OWM)

Maxim's 1-wire bus consists of one signal that carries data and also supplies power to the slave devices and a ground return. The bus master communicates serially with one or more slave devices through the bidirectional, multidrop 1-Wire bus. The single contact serial interface is ideal for communication networks requiring minimal interconnection.

The provided 1-Wire master supports the following features:

- Single contact for control and operation
- Unique factory identifier for any 1-Wire device
- Multiple device capability on a single line

The OWM supports both standard (15.6 kbps) and overdrive (110 kbps) speeds.

Standard DMA Controller

The standard DMA controller allows automatic one-way data transfer between two entities. These entities can be either memories or peripherals. The transfers are done without using CPU resources. The following transfer modes are supported:

- 8-channel
- Peripheral to data memory
- Data memory to peripheral
- Data memory to data memory
- Event support

All DMA transactions consist of an AHB burst read into the DMA FIFO followed immediately by an AHB burst write from the FIFO.

The MAX32665–MAX32668 provide two instances of the standard DMA controller.

Table 3. UART Configuration Options

INSTANCE	FLOW CONTROL		MAXIMUM BAUD RATE (kb)
	109 WLP	121 CTBGA	
UART0	YES	YES	4000
UART1	YES	YES	4000
UART2	YES	YES	4000

Trusted Protection Unit (TPU)

True Random Number Generator (TRNG)

Random numbers are a vital part of a secure application, providing random numbers that can be used for cryptographic seeds or strong encryption keys to ensure data privacy.

Software can use random numbers to trigger asynchronous events that result in nondeterministic behavior. This is helpful in thwarting replay attacks or key search approaches. An effective true random number generator (TRNG) must be continuously updated by a high-entropy source.

The provided TRNG is continuously driven by a physically-unpredictable entropy source. It generates a 128-bit true random number in 128 system clock cycles.

The TRNG can support the system-level validation of many security standards such as FIPS 140-2, PCI-PED, and Common Criteria. Contact Maxim for details of compliance with specific standards.

MAA

The provided high-speed, hardware-based modulo arithmetic accelerator (MAA) performs mathematical computations that support strong cryptographic algorithms. These include:

- 2048-bit DSA
- 4096-bit RSA
- Elliptic curve public key infrastructure

AES

The dedicated hardware-based AES engine supports the following algorithms:

- AES-128
- AES-192
- AES-256

The AES keys are automatically generated by the engine and stored in dedicated flash to protect against tampering. Key generation and storage is transparent to the user.

SHA-2

SHA-2 is a cryptographic hash function. It authenticates user data and verifies its integrity. It is used for digital signatures.

The device provides a hardware SHA-2 engine for fast computation of digests supporting:

- SHA-224
- SHA-256
- SHA-384
- SHA-512

Memory Decryption Integrity Unit (MDIU)

The external SPI flash can optionally be encrypted for additional security. Data can be transparently encrypted when it is loaded and decrypted on the fly. Encryption keys are stored in the always-on domain and preserved as as long as V_{COREA} is present.

Secure Bootloader

The secure bootloader provides a secure, authenticated communication channel with a system host. The secure communication protocol (SCP) allows the programming of internal and external memory.

The secure bootloader provides the following features:

- Life cycle management
- Trusted boot authentication through ECDSA P-256, RSA 2048, and RSA 4096
- Preprogrammed Maxim manufacturer root key (MRK)
- Programmable customer root key (CRK)
- Support for 2048- or 4096-bit RSA digital signature

Applications Information

Table 4. GPIO and Alternate Function Matrix

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2	ALTERNATE FUNCTION 3	ALTERNATE FUNCTION 4	GPIOOUT_ ENABLE	TTAP_ ENABLE
P0.0	SPIXF_SS0		UART2_CTS	TMR0		
P0.1	SPIXF_MOSI/ SDIO0		UART2_TX	TMR1		
P0.2	SPIXF_MISO/ SDIO1		UART2_RX	TMR2		
P0.3	SPIXF_SCK		UART2_RTS	TMR3		
P0.4	SPIXF_SDIO2		OWM_IO	TMR4		
P0.5	SPIXF_SDIO3		OWM_PE	TMR5		
P0.6	I2C0_SCL		SWDIO2	TMR0		
P0.7	I2C0_SDA		SWCLK2	TMR1		
P0.8	SPIXR_SS0	QSPI0_SS0	UART0_CTS	TMR2		
P0.9	SPIXR_MOSI/ SDIO0	QSPI0_MOSI/ SDIO0	UART0_TX	TMR3		
P0.10	SPIXR_MISO/ SDIO1	QSPI0_MISO/ SDIO1	UART0_RX	TMR4		
P0.11	SPIXR_SCK	QSPI0_SCK	UART0_RTS	TMR5		
P0.12	SPIXR_SDIO2	QSPI0_SDIO2	OWM_IO	TMR0		
P0.13	SPIXR_SDIO3	QSPI0_SDIO3	OWM_PE	TMR1		
P0.14	I2C1_SCL	QSPI0_SS1		TMR2		
P0.15	I2C1_SDA	QSPI0_SS2		TMR3		
P0.16	AIN0/AIN0P	QSPI1_SS0	OWM_IO	TMR4		
P0.17	AIN1/AIN0N	QSPI1_MOSI/ SDIO0	OWM_PE	TMR5		
P0.18	AIN2/AIN1P	QSPI1_MISO/ SDIO1		TMR0	PDOWN	
P0.19	AIN3/AIN1N	QSPI1_SCK		TMR1	SQWOUT	
P0.20	AIN4/AIN2P	QSPI1_SDIO2	UART1_RX	TMR2		
P0.21	AIN5/AIN2N	QSPI1_SDIO3	UART1_TX	TMR3		
P0.22	AIN6/AIN3P	QSPI1_SS1	UART1_CTS	TMR4		
P0.23	AIN7/AIN3N	QSPI1_SS2	UART1_RTS	TMR5		
P0.24	PCM_LRCLK	QSPI2_SS0	OWM_IO	TMR0		
P0.25	PCM_DOUT	QSPI2_MOSI/ SDIO0	OWM_PE	TMR1		
P0.26	PCM_DIN	QSPI2_MISO/ SDIO1		TMR2	PDOWN	
P0.27	PCM_BCLK	QSPI2_SCK		TMR3	SQWOUT	
P0.28	PDM_DATA2	QSPI2_SDIO2	UART2_RX	TMR4		

Table 4. GPIO and Alternate Function Matrix (continued)

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2	ALTERNATE FUNCTION 3	ALTERNATE FUNCTION 4	GPIOOUT_ ENABLE	TTAP_ ENABLE
P0.29	PDM_DATA3	QSPI2_SDIO3	UART2_TX	TMR5		
P0.30	PDM_RX_CLK	QSPI2_SS1	UART2_CTS	TMR0		
P0.31	PDM_MCLK	QSPI2_SS2	UART2_RTS	TMR1		
P1.0	SDHC_DAT3		SDMA_TMS	PT0		
P1.1	SDHC_CMD		SDMA_TDO	PT1		
P1.2	SDHC_DAT0		SDMA_TDI	PT2		
P1.3	SDHC_CLK		SDMA_TCK	PT3		
P1.4	SDHC_DAT1		UART0_RX	PT4		
P1.5	SDHC_DAT2		UART0_TX	PT5		
P1.6	SDHC_WP		UART0_CTS	PT6		
P1.7	SDHC_CDN		UART0_RTS	PT7		
P1.8	QSPI0_SS0			PT8		
P1.9	QSPI0_MOSI/ SDIO0			PT9		
P1.10	QSPI0_MISO/ SDIO1			PT10		
P1.11	QSPI0_SCK			PT11		
P1.12	QSPI0_SDIO2		UART1_RX	PT12		
P1.13	QSPI0_SDIO3		UART1_TX	PT13		
P1.14	I2C2_SCL		UART1_CTS	PT14		JTAG TDI
P1.15	I2C2_SDA		UART1_RTS	PT15		JTAG TDO

Ordering Information

PART	BLE	ARM CORTEX-M4 CPU	SRAM SIZE	ECC	SECURITY	PIN-PACKAGE
MAX32665GWP+*	No	Dual	560KB	Yes	No	109 WLP
MAX32665GWP+T*	No	Dual	560KB	Yes	No	109 WLP
MAX32665GWPBT+*	Yes	Dual	560KB	Yes	No	109 WLP
MAX32665GWPBT+T*	Yes	Dual	560KB	Yes	No	109 WLP
MAX32665GXM+*	No	Dual	560KB	Yes	No	121 CTBGA
MAX32665GXM+T*	No	Dual	560KB	Yes	No	121 CTBGA
MAX32665GXMBT+*	Yes	Dual	560KB	Yes	No	121 CTBGA
MAX32665GXMBT+T*	Yes	Dual	560KB	Yes	No	121 CTBGA
MAX32666GWP+	No	Dual	560KB	Yes	Yes	109 WLP
MAX32666GWP+T	No	Dual	560KB	Yes	Yes	109 WLP
MAX32666GWPBT+*	Yes	Dual	560KB	Yes	Yes	109 WLP
MAX32666GWPBT+T*	Yes	Dual	560KB	Yes	Yes	109 WLP
MAX32666GXM+*	No	Dual	560KB	Yes	Yes	121 CTBGA
MAX32666GXM+T*	No	Dual	560KB	Yes	Yes	121 CTBGA
MAX32666GXMBT+*	Yes	Dual	560KB	Yes	Yes	121 CTBGA
MAX32666GXMBT+T*	Yes	Dual	560KB	Yes	Yes	121 CTBGA
MAX32667GWP+*	No	Single	192KB	No	No	109 WLP
MAX32667GWP+T*	No	Single	192KB	No	No	109 WLP
MAX32667GWPBT+*	Yes	Single	192KB	No	No	109 WLP
MAX32667GWPBT+T*	Yes	Single	192KB	No	No	109 WLP
MAX32667GXM+*	No	Single	192KB	No	No	121 CTBGA
MAX32667GXM+T*	No	Single	192KB	No	No	121 CTBGA
MAX32667GXMBT+*	Yes	Single	192KB	No	No	121 CTBGA
MAX32667GXMBT+T*	Yes	Single	192KB	No	No	121 CTBGA
MAX32668GWP+*	No	Single	192KB	No	Yes	109 WLP
MAX32668GWP+T*	No	Single	192KB	No	Yes	109 WLP
MAX32668GWPBT+*	Yes	Single	192KB	No	Yes	109 WLP
MAX32668GWPBT+T*	Yes	Single	192KB	No	Yes	109 WLP
MAX32668GXM+*	No	Single	192KB	No	Yes	121 CTBGA
MAX32668GXM+T*	No	Single	192KB	No	Yes	121 CTBGA
MAX32668GXMBT+*	Yes	Single	192KB	No	Yes	121 CTBGA
MAX32668GXMBT+T*	Yes	Single	192KB	No	Yes	121 CTBGA

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel. Full reel.

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/18	Initial release	—

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.