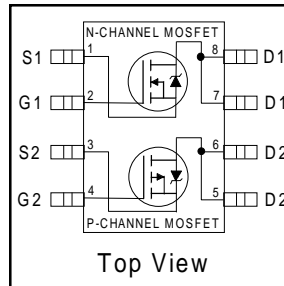


IRF7507

HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- Dual N and P Channel MOSFET
- Very Small SOIC Package
- Low Profile (<1.1mm)
- Available in Tape & Reel
- Fast Switching

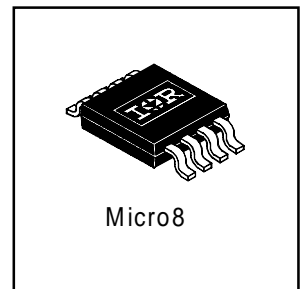


	N-Ch	P-Ch
V_{DS}	20V	-20V
$R_{DS(on)}$	0.135 Ω	0.27 Ω

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The new Micro8 package, with half the footprint area of the standard SO-8, provides the smallest footprint available in an SOIC outline. This makes the Micro8 an ideal device for applications where printed circuit board space is at a premium. The low profile (<1.1mm) of the Micro8 will allow it to fit easily into extremely thin application environments such as portable electronics and PCMCIA cards.



Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	20	-20	V
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, V_{GS}	2.4	-1.7	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, V_{GS}	1.9	-1.4	
I_{DM}	Pulsed Drain Current ^①	19	-14	
$P_D @ T_A = 25^\circ\text{C}$	Maximum Power Dissipation ^④	1.25		W
$P_D @ T_A = 70^\circ\text{C}$	Maximum Power Dissipation ^④	0.8		W
	Linear Derating Factor	10		mW/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 12		V
V_{GSM}	Gate-to-Source Voltage Single Pulse $t_p < 10\mu\text{s}$	16		V
dv/dt	Peak Diode Recovery dv/dt ^②	5.0	-5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		$^\circ\text{C}$
	Soldering Temperature, for 10 seconds	240 (1.6mm from case)		

Thermal Resistance

	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ^④	100	$^\circ\text{C}/\text{W}$

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Parameter	Description	N-Ch	P-Ch	Min.	Typ.	Max.	Units	Conditions
				—	—	—		
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	N-Ch	P-Ch	20	—	—	V	V _{GS} = 0V, I _D = 250μA
				-20	—	—		V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	N-Ch	P-Ch	—	0.041	—	V/°C	Reference to 25°C, I _D = 1mA
				—	-0.012	—		Reference to 25°C, I _D = -1mA
R _{DS(ON)}	Static Drain-to-Source On-Resistance	N-Ch	P-Ch	—	0.085	0.14	Ω	V _{GS} = 4.5V, I _D = 1.7A ③
				—	0.120	0.20		V _{GS} = 2.7V, I _D = 0.85A ③
				—	0.17	0.27		V _{GS} = -4.5V, I _D = -1.2A ③
				—	0.28	0.40		V _{GS} = -2.7V, I _D = -0.6A ③
V _{GS(th)}	Gate Threshold Voltage	N-Ch	P-Ch	0.7	—	—	V	V _{DS} = V _{GS} , I _D = 250μA
				-0.7	—	—		V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Transconductance	N-Ch	P-Ch	2.6	—	—	S	V _{DS} = 10V, I _D = 0.85A ③
				1.3	—	—		V _{DS} = -10V, I _D = -0.6A ③
I _{DSS}	Drain-to-Source Leakage Current	N-Ch	P-Ch	—	—	1.0	μA	V _{DS} = 16V, V _{GS} = 0V
				—	—	-1.0		V _{DS} = -16V, V _{GS} = 0V
				—	—	25		V _{DS} = 16V, V _{GS} = 0V, T _J = 125°C
				—	—	-25		V _{DS} = -16V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	N-P		—	—	±100		V _{GS} = ± 12V
Q _g	Total Gate Charge	N-Ch	P-Ch	—	5.3	8.0		N-Channel
				—	5.4	8.2		I _D = 1.7A, V _{DS} = 16V, V _{GS} = 4.5V
Q _{gs}	Gate-to-Source Charge	N-Ch	P-Ch	—	0.84	1.3	nC	P-Channel
				—	0.96	1.4		
Q _{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	P-Ch	—	2.2	3.3		
				—	2.4	3.6		
t _{d(on)}	Turn-On Delay Time	N-Ch	P-Ch	—	5.7	—		N-Channel
				—	9.1	—		
t _r	Rise Time	N-Ch	P-Ch	—	24	—		P-Channel
				—	35	—		
t _{d(off)}	Turn-Off Delay Time	N-Ch	P-Ch	—	15	—	ns	
				—	38	—		
t _f	Fall Time	N-Ch	P-Ch	—	16	—		
				—	43	—		
C _{iss}	Input Capacitance	N-Ch	P-Ch	—	260	—		N-Channel
				—	240	—		
C _{oss}	Output Capacitance	N-Ch	P-Ch	—	130	—		P-Channel
				—	130	—		
C _{rss}	Reverse Transfer Capacitance	N-Ch	P-Ch	—	61	—		
				—	64	—		

Source-Drain Ratings and Characteristics

Parameter	Description	N-Ch	P-Ch	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	N-Ch	P-Ch	—	—	1.25	A	
				—	—	-1.25		
I _{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	P-Ch	—	—	19		
				—	—	-14		
V _{SD}	Diode Forward Voltage	N-Ch	P-Ch	—	—	1.2	V	T _J = 25°C, I _S = 1.7A, V _{GS} = 0V ③
				—	—	-1.2		T _J = 25°C, I _S = -1.2A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	N-Ch	P-Ch	—	39	59	ns	N-Channel
				—	52	78		
Q _{rr}	Reverse Recovery Charge	N-Ch	P-Ch	—	37	56	nC	T _J = 25°C, I _F = 1.7A, di/dt = 100A/μs
				—	63	95		

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 21)

② N-Channel I_{SD} ≤ 1.7A, di/dt ≤ 66A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
P-Channel I_{SD} ≤ -1.2A, di/dt ≤ 100A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C

③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

④ Surface mounted on FR-4 board, t ≤ 10sec.

N - Channel

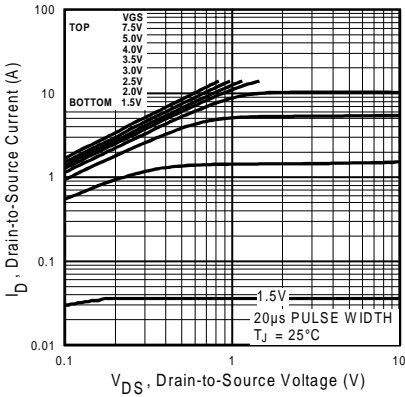


Fig 1. Typical Output Characteristics

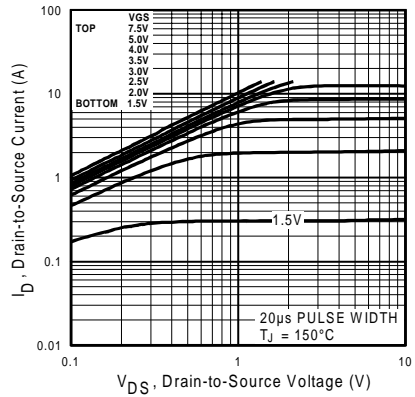


Fig 2. Typical Output Characteristics

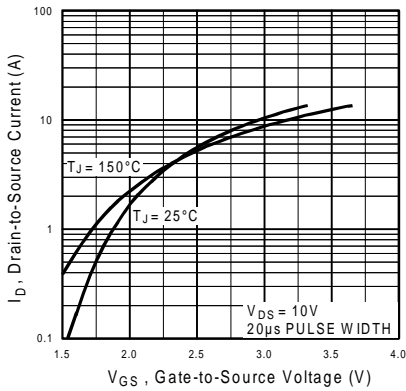


Fig 3. Typical Transfer Characteristics

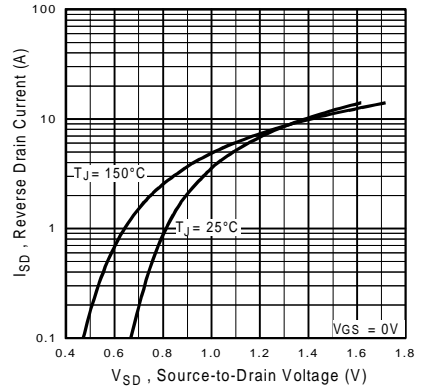


Fig 4. Typical Source-Drain Diode Forward Voltage

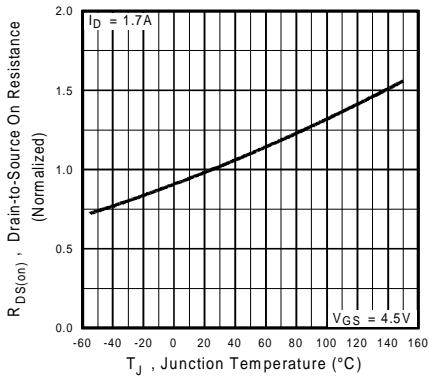


Fig 5. Normalized On-Resistance Vs. Temperature

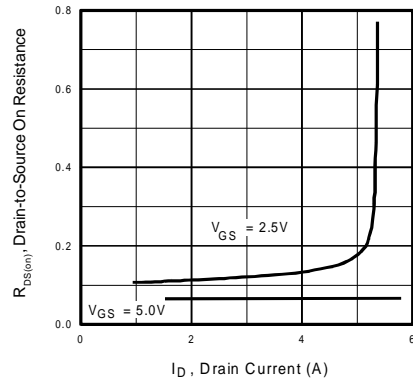


Fig 6. Typical On-Resistance Vs. Drain Current

IRF7507

N - Channel

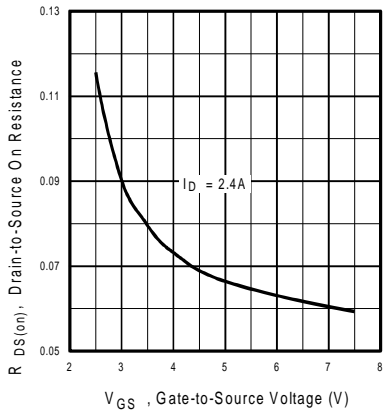


Fig 7. Typical On-Resistance Vs. Gate Voltage

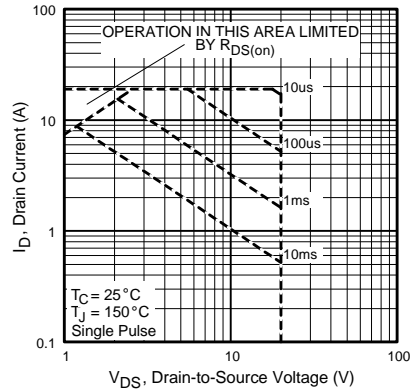


Fig 8. Maximum Safe Operating Area

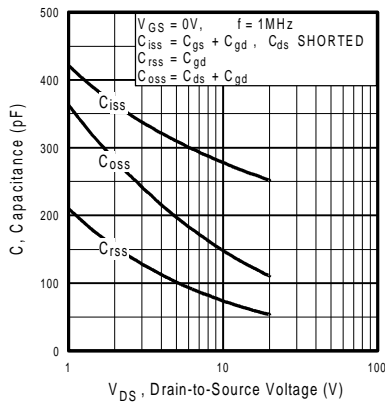


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

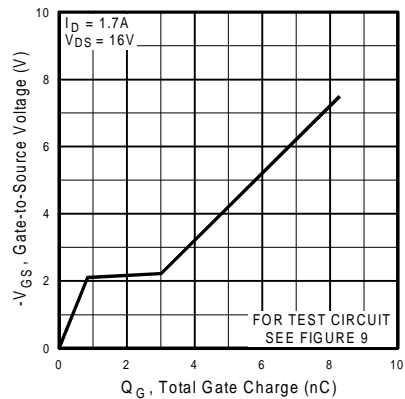


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

P - Channel

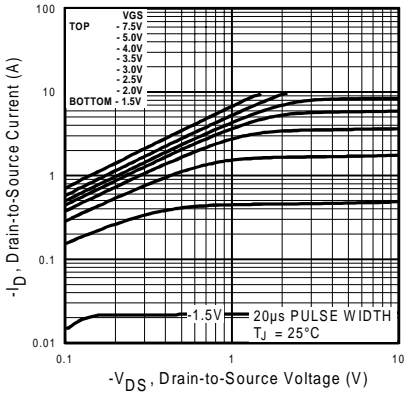


Fig 11. Typical Output Characteristics

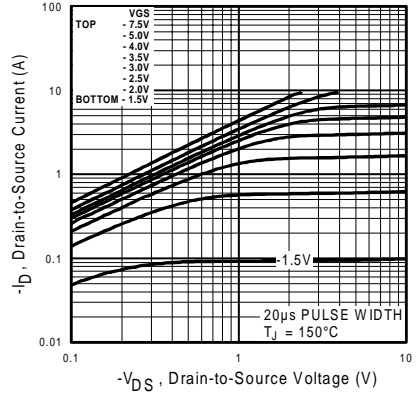


Fig 12. Typical Output Characteristics

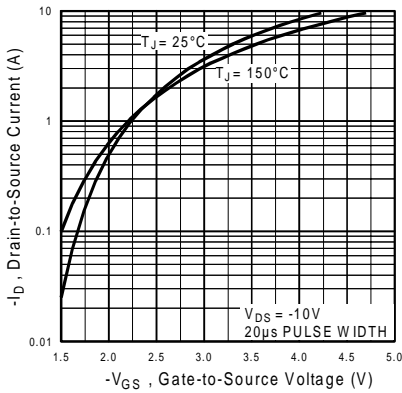


Fig 13. Typical Transfer Characteristics

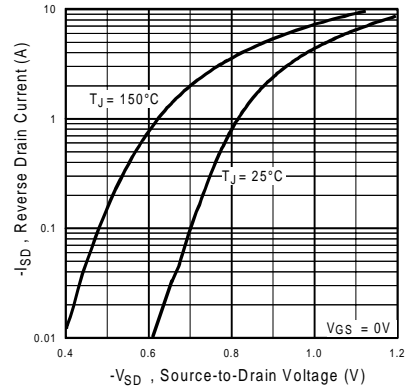


Fig 14. Typical Source-Drain Diode Forward Voltage

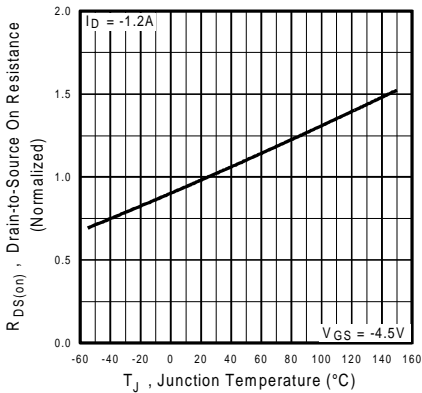


Fig 15. Normalized On-Resistance Vs. Temperature

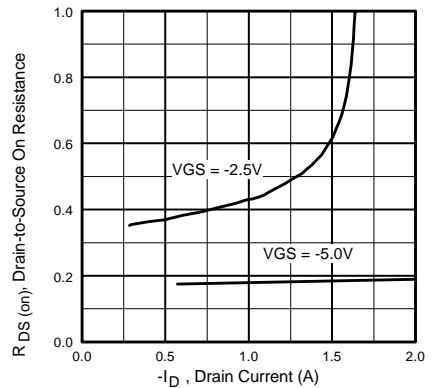


Fig 16. Typical On-Resistance Vs. Drain Current

P - Channel

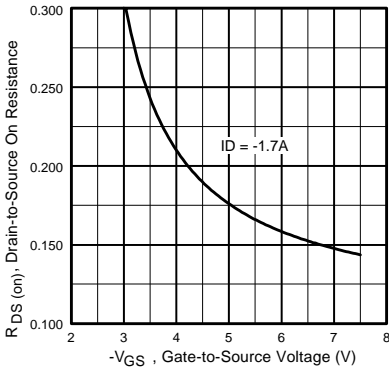


Fig 17. Typical On-Resistance Vs. Gate Voltage

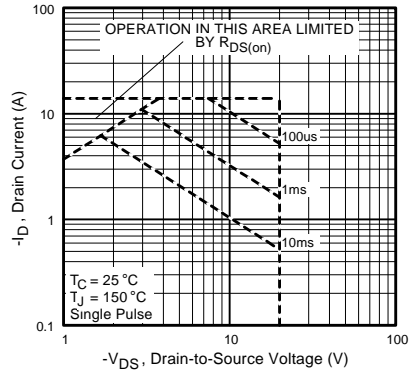


Fig 18. Maximum Safe Operating Area

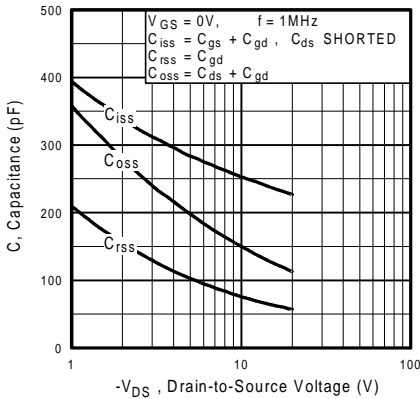


Fig 19. Typical Capacitance Vs. Drain-to-Source Voltage

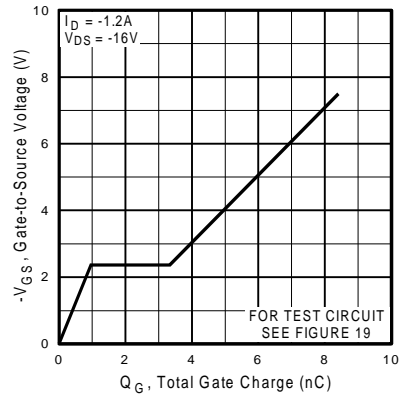


Fig 20. Typical Gate Charge Vs. Gate-to-Source Voltage

N-P - Channel

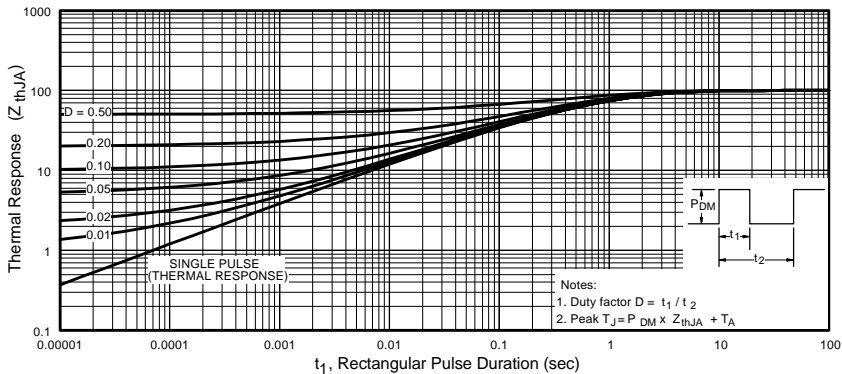
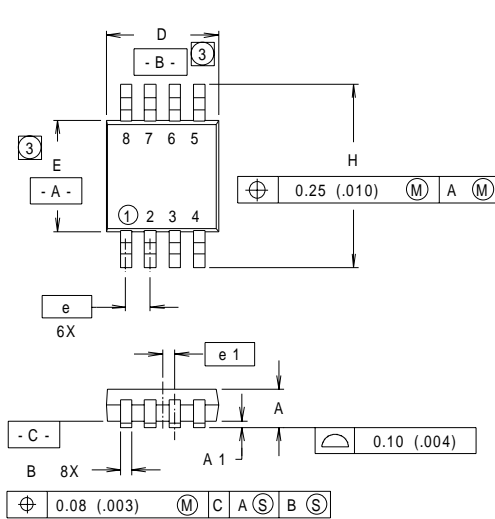


Fig 21. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

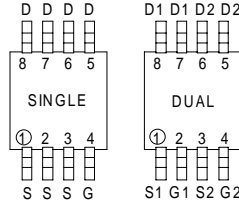
Package Outline

Micro8 Outline

Dimensions are shown in millimeters (inches)

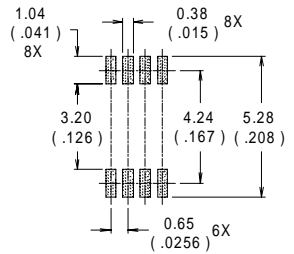


LEAD ASSIGNMENTS



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.036	.044	0.91	1.11
A1	.004	.008	0.10	0.20
B	.010	.014	0.25	0.36
C	.005	.007	0.13	0.18
D	.116	.120	2.95	3.05
e	.0256 BASIC		0.65 BASIC	
e1	.0128 BASIC		0.33 BASIC	
E	.116	.120	2.95	3.05
H	.188	.198	4.78	5.03
L	.016	.026	0.41	0.66
θ	0°	6°	0°	6°

RECOMMENDED FOOTPRINT



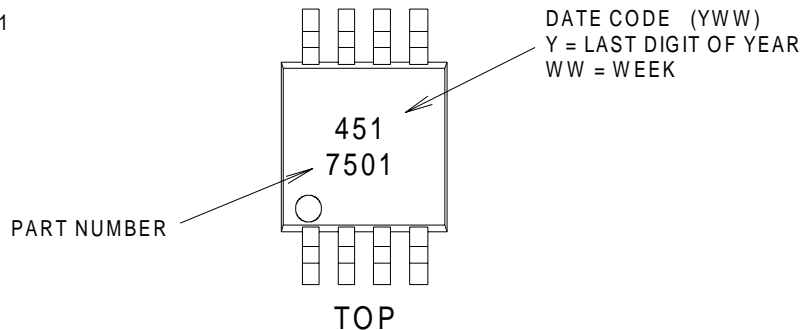
NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
- 2 CONTROLLING DIMENSION : INCH.
- 3 DIMENSIONS DO NOT INCLUDE MOLD FLASH.

Part Marking Information

Micro8

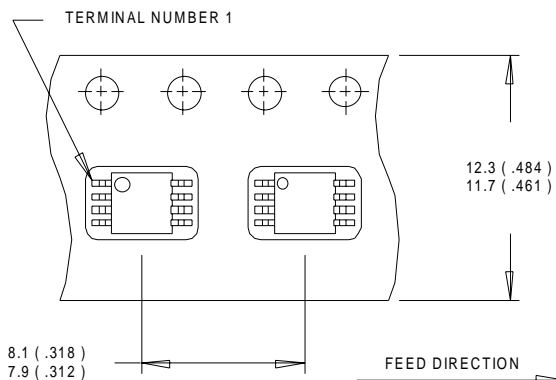
EXAMPLE : THIS IS AN IRF7501



Tape & Reel Information

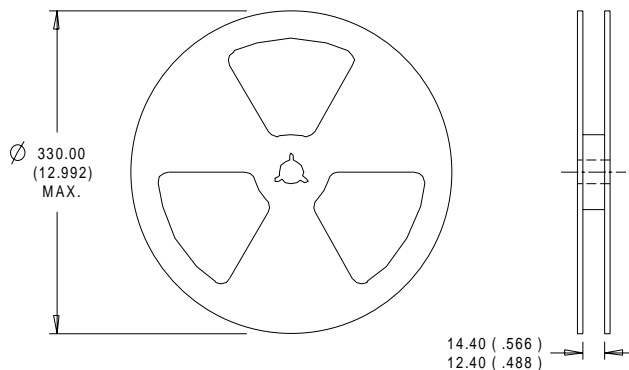
Micro8

Dimensions are shown in millimeters (inches)



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.
2. CONTROLLING DIMENSION : MILLIMETER.



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

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IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630

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