

## 2.9 nV/sqrt(Hz) Low Noise, Precision, RRIO Amplifier

Check for Samples: [LMP7731](#)

### FEATURES

(Typical Values,  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}$ )

- **Input Voltage Noise**
  - $f = 3\text{ Hz}$   $3.3\text{ nV}/\sqrt{\text{Hz}}$
  - $f = 1\text{ kHz}$   $2.9\text{ nV}/\sqrt{\text{Hz}}$
- **CMRR 130 dB**
- **Open Loop Gain 130 dB**
- **GBW 22 MHz**
- **Slew Rate 2.4 V/ $\mu\text{s}$**
- **THD @  $f = 10\text{ kHz}$ ,  $A_V = +1$ ,  $R_L = 2\text{ k}\Omega$  0.001%**
- **Supply Current per Channel 2.2 mA**
- **Supply Voltage Range 1.8V to 5.5V**
- **Operating Temperature Range  $-40^\circ\text{C}$  to  $125^\circ\text{C}$**
- **Input Bias Current  $\pm 1.5\text{ nA}$**
- **RRIO**

### APPLICATIONS

- **Gas Analysis Instruments**
- **Photometric Instrumentation**
- **Medical Instrumentation**

### DESCRIPTION

The LMP7731 is a single, low noise, rail-to-rail input and output, low voltage amplifier. The LMP7731 is part of the LMP™ precision amplifier family and is ideal for precision and low noise applications with low voltage requirements.

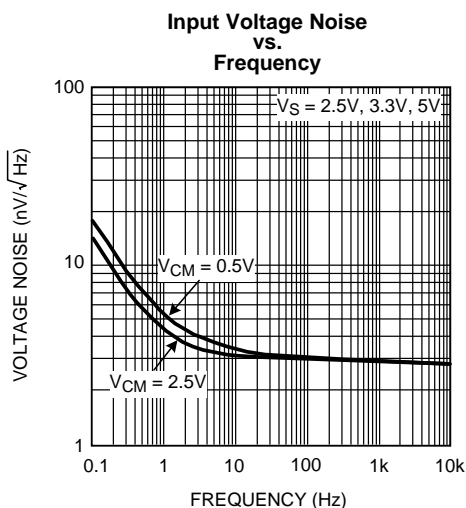
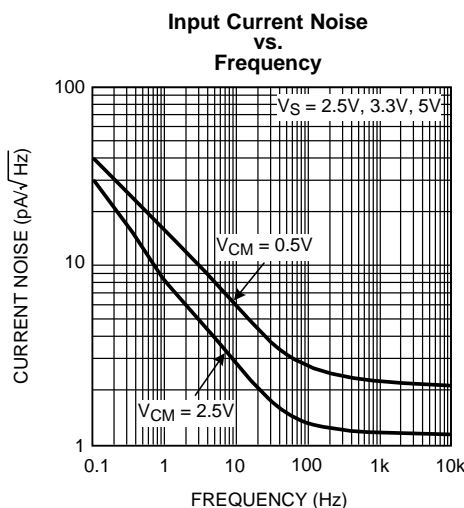
This operational amplifier offers low voltage noise of  $2.9\text{ nV}/\sqrt{\text{Hz}}$  with a  $1/f$  corner of only 3 Hz. The LMP7731 has bipolar input stages with a bias current of only 1.5 nA. This low input bias current, complemented by the very low level of voltage noise, makes the LMP7731 an excellent choice for photometry applications.

The LMP7731 provides a wide GBW of 22 MHz while consuming only 2 mA of current. This high gain bandwidth along with the high open loop gain of 130 dB enables accurate signal conditioning in applications with high closed loop gain requirements.

The LMP7731 has a supply voltage range of 1.8V to 5.5V, making it an ideal choice for battery operated portable applications.

The LMP7731 is offered in the space saving 5-Pin SOT-23 and 8-Pin SOIC packages.

### Typical Performance Characteristics


**Figure 1.**

**Figure 2.**


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings <sup>(1)(2)</sup>

ESD Tolerance <sup>(3)</sup>	Human Body Model	Inputs pins only	2000V
		All other pins	2000V
	Machine Model		200V
	Charge Device Model		1000V
V <sub>IN</sub> Differential			±2V
Supply Voltage (V <sub>S</sub> = V <sup>+</sup> – V <sup>-</sup> )			6.0V
Storage Temperature Range			-65°C to 150°C
Junction Temperature <sup>(4)</sup>			+150°C max
Soldering Information	Infrared or Convection (20 sec)		235°C
	Wave Soldering Lead Temp. (10 sec)		260°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
- (4) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> – T<sub>A</sub>) / θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PC Board.

### Operating Ratings <sup>(1)</sup>

Temperature Range		-40°C to 125°C
Supply Voltage (V <sub>S</sub> = V <sup>+</sup> – V <sup>-</sup> )		1.8V to 5.5V
Package Thermal Resistance (θ <sub>JA</sub> )	5-Pin SOT-23	265°C/W
	8-Pin SOIC	190°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.

### 2.5V Electrical Characteristics <sup>(1)</sup>

Unless otherwise specified, all limits are ensured for T<sub>A</sub> = 25°C, V<sup>+</sup> = 2.5V, V<sup>-</sup> = 0V, V<sub>CM</sub> = V<sup>+</sup>/2, R<sub>L</sub> > 10 kΩ to V<sup>+</sup>/2. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
V <sub>OS</sub>	Input Offset Voltage <sup>(4)</sup>	V <sub>CM</sub> = 2.0V		±9	±500 <b>±600</b>	µV
		V <sub>CM</sub> = 0.5V		±9	±500 <b>±600</b>	
TCV <sub>OS</sub>	Input Offset Voltage Temperature Drift	V <sub>CM</sub> = 2.0V		±0.5	±5.5	µV/°C
		V <sub>CM</sub> = 0.5V		±0.2	±5.5	
I <sub>B</sub>	Input Bias Current	V <sub>CM</sub> = 2.0V		±1	±30 <b>±45</b>	nA
		V <sub>CM</sub> = 0.5V		±12	±50 <b>±75</b>	

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T<sub>J</sub> = T<sub>A</sub>. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T<sub>J</sub> > T<sub>A</sub>. Absolute maximum Ratings indicate junction temperature limits beyond which the device maybe permanently degraded, either mechanically or electrically.
- (2) All limits are specified by testing, statistical analysis or design.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
- (4) Ambient production test is performed at 25°C with a variance of ±3°C.

## 2.5V Electrical Characteristics <sup>(1)</sup> (continued)

Unless otherwise specified, all limits are ensured for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 2.5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V^+/2$ ,  $R_L > 10\text{ k}\Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
$I_{\text{OS}}$	Input Offset Current	$V_{\text{CM}} = 2.0\text{V}$		$\pm 1$	$\pm 50$ <b><math>\pm 75</math></b>	nA
		$V_{\text{CM}} = 0.5\text{V}$		$\pm 11$	$\pm 60$ <b><math>\pm 80</math></b>	
$\text{TCI}_{\text{OS}}$	Input Offset Current Drift	$V_{\text{CM}} = 0.5\text{V}$ and $V_{\text{CM}} = 2.0\text{V}$		0.0474		nA/ $^\circ\text{C}$
CMRR	Common Mode Rejection Ratio	$0.15\text{V} \leq V_{\text{CM}} \leq 0.7\text{V}$ $0.23\text{V} \leq V_{\text{CM}} \leq 0.7\text{V}$	101 <b>89</b>	120		dB
		$1.5\text{V} \leq V_{\text{CM}} \leq 2.35\text{V}$ $1.5\text{V} \leq V_{\text{CM}} \leq 2.27\text{V}$	105 <b>99</b>	129		
PSRR	Power Supply Rejection Ratio	$2.5\text{V} \leq V^+ \leq 5\text{V}$	111 <b>105</b>	129		dB
		$1.8\text{V} \leq V^+ \leq 5.5\text{V}$		117		
CMVR	Common Mode Voltage Range	Large Signal CMRR $\geq 80\text{ dB}$	0		2.5	V
$A_{\text{VOL}}$	Open Loop Voltage Gain	$R_L = 10\text{ k}\Omega$ to $V^+/2$ $V_{\text{OUT}} = 0.5\text{V}$ to $2.0\text{V}$	112 <b>104</b>	130		dB
		$R_L = 2\text{ k}\Omega$ to $V^+/2$ $V_{\text{OUT}} = 0.5\text{V}$ to $2.0\text{V}$	109 <b>90</b>	119		
$V_{\text{OUT}}$	Output Voltage Swing High	$R_L = 10\text{ k}\Omega$ to $V^+/2$		4	50 <b>75</b>	mV from either rail
		$R_L = 2\text{ k}\Omega$ to $V^+/2$		13	50 <b>75</b>	
	Output Voltage Swing Low	$R_L = 10\text{ k}\Omega$ to $V^+/2$		6	50 <b>75</b>	
		$R_L = 2\text{ k}\Omega$ to $V^+/2$		9	50 <b>75</b>	
$I_{\text{OUT}}$	Output Current	Sourcing, $V_{\text{OUT}} = V^+/2$ $V_{\text{IN}}(\text{diff}) = 100\text{ mV}$	22 <b>12</b>	31		mA
		Sinking, $V_{\text{OUT}} = V^+/2$ $V_{\text{IN}}(\text{diff}) = -100\text{ mV}$	15 <b>10</b>	44		
$I_{\text{S}}$	Supply Current (Per Channel)	$V_{\text{CM}} = 2.0\text{V}$		2.0	2.7 <b>3.4</b>	mA
		$V_{\text{CM}} = 0.5\text{V}$		2.3	3.1 <b>3.9</b>	
SR	Slew Rate	$A_V = +1$ , $C_L = 10\text{ pF}$ , $R_L = 10\text{ k}\Omega$ to $V^+/2$ , $V_O = 2 V_{\text{PP}}$		2.4		V/ $\mu\text{s}$
GBW	Gain Bandwidth	$C_L = 20\text{ pF}$ , $R_L = 10\text{ k}\Omega$ to $V^+/2$		21		MHz
$G_M$	Gain Margin	$C_L = 20\text{ pF}$ , $R_L = 10\text{ k}\Omega$ to $V^+/2$		14		dB
$\Phi_M$	Phase Margin	$C_L = 20\text{ pF}$ , $R_L = 10\text{ k}\Omega$ to $V^+/2$		60		deg
$R_{\text{IN}}$	Input Resistance	Differential Mode		38		k $\Omega$
		Common Mode		151		M $\Omega$
THD+N	Total Harmonic Distortion + Noise	$A_V = 1$ , $f = 1\text{ kHz}$ , Amplitude = 1V		0.002		%
$e_n$	Input Referred Voltage Noise Density	$f = 1\text{ kHz}$ , $V_{\text{CM}} = 2.0\text{V}$		3		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$ , $V_{\text{CM}} = 0.5\text{V}$		3		
	Input Voltage Noise	0.1 Hz to 10 Hz		75		nV $_{\text{PP}}$
$i_n$	Input Referred Current Noise Density	$f = 1\text{ kHz}$ , $V_{\text{CM}} = 2.0\text{V}$		1.1		pA/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$ , $V_{\text{CM}} = 0.5\text{V}$		2.3		

### 3.3V Electrical Characteristics <sup>(1)</sup>

Unless otherwise specified, all limits are ensured for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 3.3\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V^+/2$ ,  $R_L > 10\text{ k}\Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
$V_{\text{OS}}$	Input Offset Voltage <sup>(4)</sup>	$V_{\text{CM}} = 2.5\text{V}$		$\pm 6$	$\pm 500$ <b><math>\pm 600</math></b>	$\mu\text{V}$
		$V_{\text{CM}} = 0.5\text{V}$		$\pm 6$	$\pm 500$ <b><math>\pm 600</math></b>	
$\text{TCV}_{\text{OS}}$	Input Offset Voltage Temperature Drift	$V_{\text{CM}} = 2.5\text{V}$		$\pm 0.5$	$\pm 5.5$	$\mu\text{V}/^\circ\text{C}$
		$V_{\text{CM}} = 0.5\text{V}$		$\pm 0.2$	$\pm 5.5$	
$I_{\text{B}}$	Input Bias Current	$V_{\text{CM}} = 2.5\text{V}$		$\pm 1.5$	$\pm 30$ <b><math>\pm 45</math></b>	nA
		$V_{\text{CM}} = 0.5\text{V}$		$\pm 13$	$\pm 50$ <b><math>\pm 77</math></b>	
$I_{\text{OS}}$	Input Offset Current	$V_{\text{CM}} = 2.5\text{V}$		$\pm 1$	$\pm 50$ <b><math>\pm 70</math></b>	nA
		$V_{\text{CM}} = 0.5\text{V}$		$\pm 11$	$\pm 60$ <b><math>\pm 80</math></b>	
$\text{TCI}_{\text{OS}}$	Input Offset Current Drift	$V_{\text{CM}} = 0.5\text{V}$ and $V_{\text{CM}} = 2.5\text{V}$		0.048		$\text{nA}/^\circ\text{C}$
CMRR	Common Mode Rejection Ratio	$0.15\text{V} \leq V_{\text{CM}} \leq 0.7\text{V}$ $0.23\text{V} \leq V_{\text{CM}} \leq 0.7\text{V}$	101 <b>89</b>	120		dB
		$1.5\text{V} \leq V_{\text{CM}} \leq 3.15\text{V}$ $1.5\text{V} \leq V_{\text{CM}} \leq 3.07\text{V}$	105 <b>99</b>	130		
PSRR	Power Supply Rejection Ratio	$2.5\text{V} \leq V^+ \leq 5.0\text{V}$	111 <b>105</b>	129		dB
		$1.8\text{V} \leq V^+ \leq 5.5\text{V}$		117		
CMVR	Common Mode Voltage Range	Large Signal CMRR $\geq 80\text{ dB}$	0		3.3	V
$A_{\text{VOL}}$	Open Loop Voltage Gain	$R_L = 10\text{ k}\Omega$ to $V^+/2$ $V_{\text{OUT}} = 0.5\text{V}$ to $2.8\text{V}$	112 <b>104</b>	130		dB
		$R_L = 2\text{ k}\Omega$ to $V^+/2$ $V_{\text{OUT}} = 0.5\text{V}$ to $2.8\text{V}$	110 <b>92</b>	119		
$V_{\text{OUT}}$	Output Voltage Swing High	$R_L = 10\text{ k}\Omega$ to $V^+/2$		5	50 <b>75</b>	mV from either rail
		$R_L = 2\text{ k}\Omega$ to $V^+/2$		14	50 <b>75</b>	
	Output Voltage Swing Low	$R_L = 10\text{ k}\Omega$ to $V^+/2$		9	50 <b>75</b>	
		$R_L = 2\text{ k}\Omega$ to $V^+/2$		13	50 <b>75</b>	
$I_{\text{OUT}}$	Output Current	Sourcing, $V_{\text{OUT}} = V^+/2$ $V_{\text{IN}}(\text{diff}) = 100\text{ mV}$	28 <b>22</b>	45		mA
		Sinking, $V_{\text{OUT}} = V^+/2$ $V_{\text{IN}}(\text{diff}) = -100\text{ mV}$	25 <b>20</b>	48		
$I_{\text{S}}$	Supply Current (Per Channel)	$V_{\text{CM}} = 2.5\text{V}$		2.1	2.8 <b>3.5</b>	mA
		$V_{\text{CM}} = 0.5\text{V}$		2.4	3.2 <b>4.0</b>	
SR	Slew Rate	$A_V = +1$ , $C_L = 10\text{ pF}$ , $R_L = 10\text{ k}\Omega$ to $V^+/2$ , $V_{\text{OUT}} = 2 V_{\text{PP}}$		2.4		$\text{V}/\mu\text{s}$

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ . Absolute maximum Ratings indicate junction temperature limits beyond which the device maybe permanently degraded, either mechanically or electrically.
- (2) All limits are specified by testing, statistical analysis or design.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
- (4) Ambient production test is performed at  $25^\circ\text{C}$  with a variance of  $\pm 3^\circ\text{C}$ .

### 3.3V Electrical Characteristics <sup>(1)</sup> (continued)

Unless otherwise specified, all limits are ensured for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 3.3\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V^+/2$ ,  $R_L > 10\text{ k}\Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
GBW	Gain Bandwidth	$C_L = 20\text{ pF}$ , $R_L = 10\text{ k}\Omega$ to $V^+/2$		22		MHz
$G_M$	Gain Margin	$C_L = 20\text{ pF}$ , $R_L = 10\text{ k}\Omega$ to $V^+/2$		14		dB
$\Phi_M$	Phase Margin	$C_L = 20\text{ pF}$ , $R_L = 10\text{ k}\Omega$ to $V^+/2$		62		deg
$R_{\text{IN}}$	Input Resistance	Differential Mode		38		k $\Omega$
		Common Mode		151		M $\Omega$
THD+N	Total Harmonic Distortion + Noise	$A_V = 1$ , $f = 1\text{ kHz}$ , Amplitude = 1V,		0.002		%
$e_n$	Input Referred Voltage Noise Density	$f = 1\text{ kHz}$ , $V_{\text{CM}} = 2.5\text{V}$		2.9		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$ , $V_{\text{CM}} = 0.5\text{V}$		2.9		
	Input Voltage Noise	0.1 Hz to 10 Hz		65		nV <sub>PP</sub>
$i_n$	Input Referred Current Noise Density	$f = 1\text{ kHz}$ , $V_{\text{CM}} = 2.5\text{V}$		1.1		pA/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$ , $V_{\text{CM}} = 0.5\text{V}$		2.1		

### 5V Electrical Characteristics <sup>(1)</sup>

Unless otherwise specified, all limits are ensured for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V^+/2$ ,  $R_L > 10\text{ k}\Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
$V_{\text{OS}}$	Input Offset Voltage <sup>(4)</sup>	$V_{\text{CM}} = 4.5\text{V}$		$\pm 6$	$\pm 500$ <b><math>\pm 600</math></b>	$\mu\text{V}$
		$V_{\text{CM}} = 0.5\text{V}$		$\pm 6$	$\pm 500$ <b><math>\pm 600</math></b>	
TCV <sub>OS</sub>	Input Offset Voltage Temperature Drift	$V_{\text{CM}} = 4.5\text{V}$		$\pm 0.5$	$\pm 5.5$	$\mu\text{V}/^\circ\text{C}$
		$V_{\text{CM}} = 0.5\text{V}$		$\pm 0.2$	$\pm 5.5$	
$I_B$	Input Bias Current	$V_{\text{CM}} = 4.5\text{V}$		$\pm 1.5$	$\pm 30$ <b><math>\pm 50</math></b>	nA
		$V_{\text{CM}} = 0.5\text{V}$		$\pm 14$	$\pm 50$ <b><math>\pm 85</math></b>	
$I_{\text{OS}}$	Input Offset Current	$V_{\text{CM}} = 4.5\text{V}$		$\pm 1$	$\pm 50$ <b><math>\pm 70</math></b>	nA
		$V_{\text{CM}} = 0.5\text{V}$		$\pm 11$	$\pm 65$ <b><math>\pm 80</math></b>	
TCI <sub>OS</sub>	Input Offset Current Drift	$V_{\text{CM}} = 0.5\text{V}$ and $V_{\text{CM}} = 4.5\text{V}$		0.0482		nA/ $^\circ\text{C}$
CMRR	Common Mode Rejection Ratio	$0.15\text{V} \leq V_{\text{CM}} \leq 0.7\text{V}$	101	120		dB
		$0.23\text{V} \leq V_{\text{CM}} \leq 0.7\text{V}$	<b>89</b>			
		$1.5\text{V} \leq V_{\text{CM}} \leq 4.85\text{V}$ $1.5\text{V} \leq V_{\text{CM}} \leq 4.77\text{V}$	105 <b>99</b>	130		
PSRR	Power Supply Rejection Ratio	$2.5\text{V} \leq V^+ \leq 5\text{V}$	111 <b>105</b>	129		dB
		$1.8\text{V} \leq V^+ \leq 5.5\text{V}$		117		
CMVR	Common Mode Voltage Range	Large Signal CMRR $\geq 80\text{ dB}$	0		5	V
$A_{\text{VOL}}$	Open Loop Voltage Gain	$R_L = 10\text{ k}\Omega$ to $V^+/2$ $V_{\text{OUT}} = 0.5\text{V}$ to $4.5\text{V}$	112 <b>104</b>	130		dB
		$R_L = 2\text{ k}\Omega$ to $V^+/2$ $V_{\text{OUT}} = 0.5\text{V}$ to $4.5\text{V}$	110 <b>94</b>	119		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ . Absolute maximum Ratings indicate junction temperature limits beyond which the device maybe permanently degraded, either mechanically or electrically.

(2) All limits are specified by testing, statistical analysis or design.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

(4) Ambient production test is performed at  $25^\circ\text{C}$  with a variance of  $\pm 3^\circ\text{C}$ .

### 5V Electrical Characteristics <sup>(1)</sup> (continued)

Unless otherwise specified, all limits are ensured for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2$ ,  $R_L > 10\text{ k}\Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
$V_{OUT}$	Output Voltage Swing High	$R_L = 10\text{ k}\Omega$ to $V^+/2$		8	50 <b>75</b>	mV from either rail
		$R_L = 2\text{ k}\Omega$ to $V^+/2$		24	50 <b>75</b>	
	Output Voltage Swing Low	$R_L = 10\text{ k}\Omega$ to $V^+/2$		9	50 <b>75</b>	
		$R_L = 2\text{ k}\Omega$ to $V^+/2$		23	50 <b>75</b>	
$I_{OUT}$	Output Current	Sourcing, $V_{OUT} = V^+/2$ $V_{IN}(\text{diff}) = 100\text{ mV}$	33 <b>27</b>	47		mA
		Sinking, $V_{OUT} = V^+/2$ $V_{IN}(\text{diff}) = -100\text{ mV}$	30 <b>25</b>	49		
$I_S$	Supply Current (Per Channel)	$V_{CM} = 4.5\text{V}$		2.2	3.0 <b>3.7</b>	mA
		$V_{CM} = 0.5\text{V}$		2.5	3.4 <b>4.2</b>	
SR	Slew Rate	$A_V = +1$ , $C_L = 10\text{ pF}$ , $R_L = 10\text{ k}\Omega$ to $V^+/2$ , $V_{OUT} = 2 V_{PP}$		2.4		V/ $\mu\text{s}$
GBW	Gain Bandwidth	$C_L = 20\text{ pF}$ , $R_L = 10\text{ k}\Omega$ to $V^+/2$		22		MHz
$G_M$	Gain Margin	$C_L = 20\text{ pF}$ , $R_L = 10\text{ k}\Omega$ to $V^+/2$		12		dB
$\Phi_M$	Phase Margin	$C_L = 20\text{ pF}$ , $R_L = 10\text{ k}\Omega$ to $V^+/2$		65		deg
$R_{IN}$	Input Resistance	Differential Mode		38		k $\Omega$
		Common Mode		151		M $\Omega$
THD+N	Total Harmonic Distortion + Noise	$A_V = 1$ , $f = 1\text{ kHz}$ , Amplitude = 1V		0.001		%
$e_n$	Input Referred Voltage Noise Density	$f = 1\text{ kHz}$ , $V_{CM} = 4.5\text{V}$		2.9		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$ , $V_{CM} = 0.5\text{V}$		2.9		
	Input Voltage Noise	0.1 Hz to 10 Hz		78		nV $_{PP}$
$i_n$	Input Referred Current Noise Density	$f = 1\text{ kHz}$ , $V_{CM} = 4.5\text{V}$		1.1		pA/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$ , $V_{CM} = 0.5\text{V}$		2.2		

### Connection Diagrams

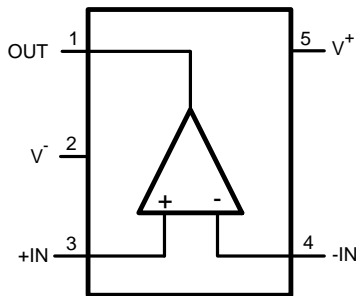


Figure 3. 5-Pin SOT-23 Top View

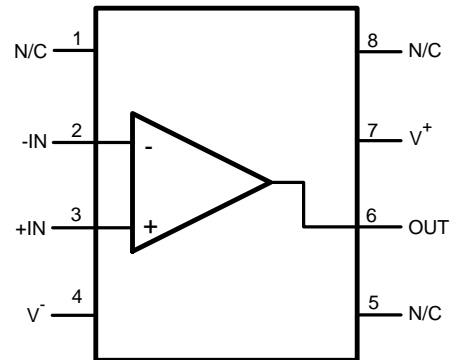


Figure 4. 8-Pin SOIC Top View

### Typical Performance Characteristics

Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $R_L > 10\text{ k}\Omega$ ,  $V_{CM} = V_S/2$ .

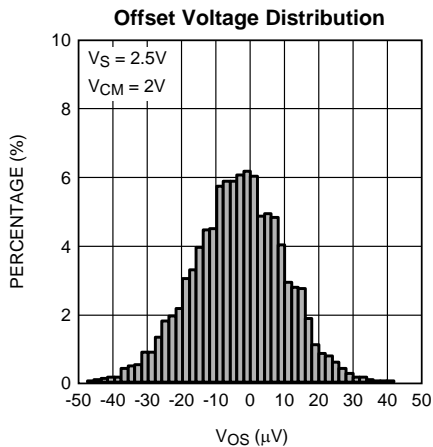


Figure 5.

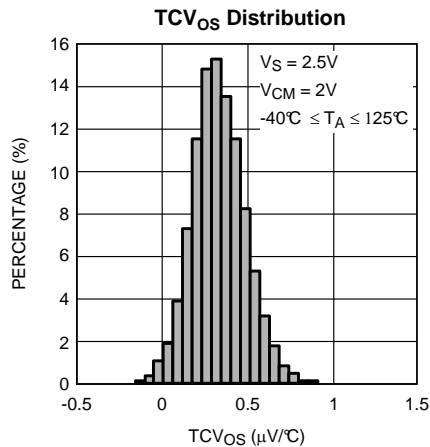


Figure 6.

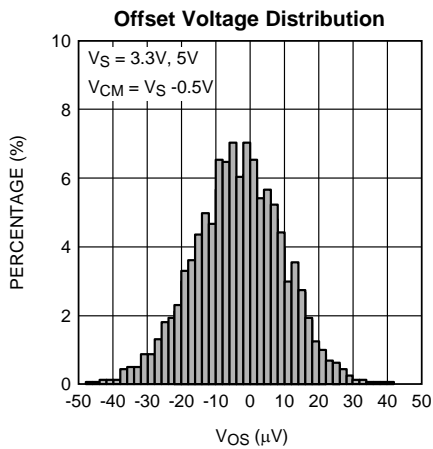


Figure 7.

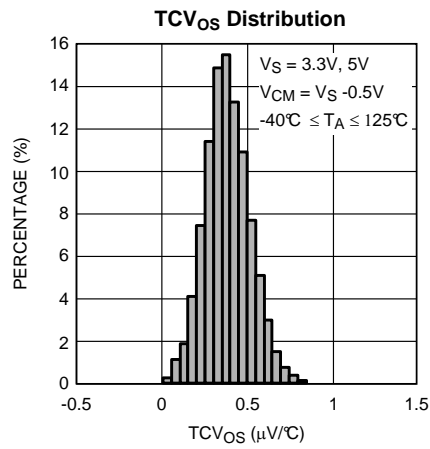


Figure 8.

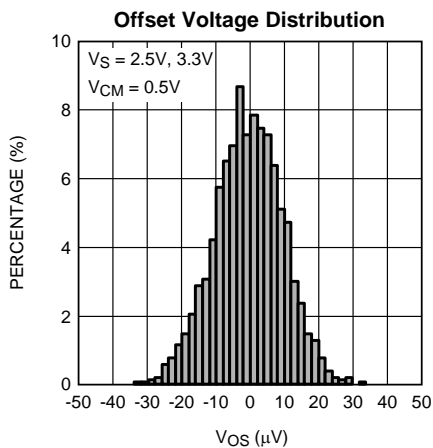


Figure 9.

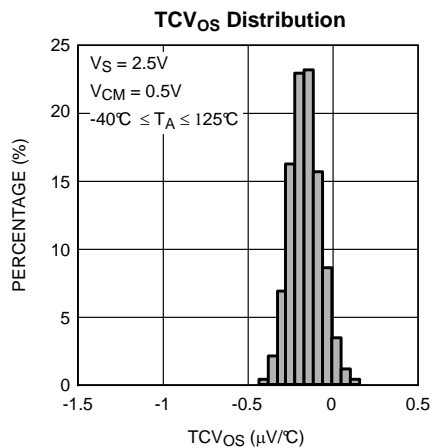


Figure 10.

### Typical Performance Characteristics (continued)

Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $R_L > 10\text{ k}\Omega$ ,  $V_{CM} = V_S/2$ .

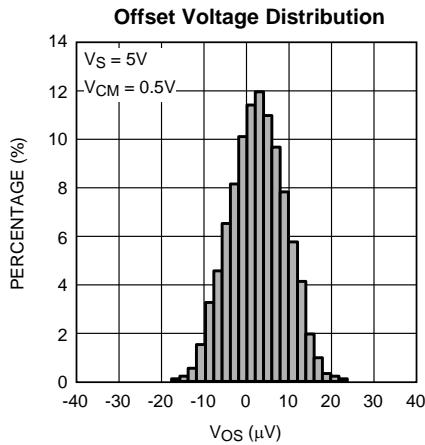


Figure 11.

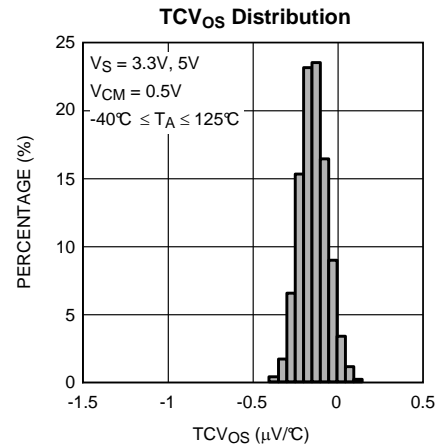


Figure 12.

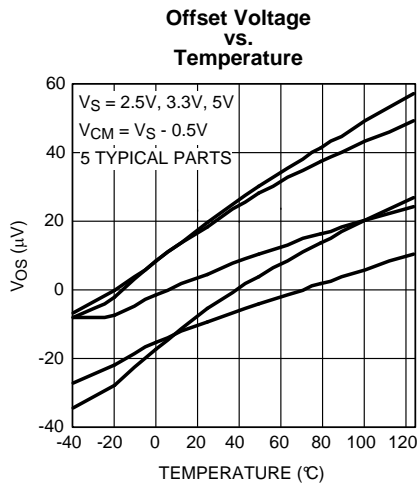


Figure 13.

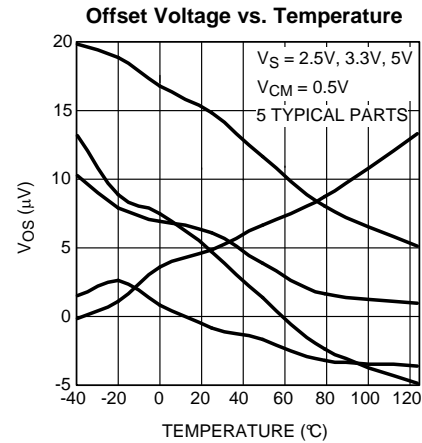


Figure 14.

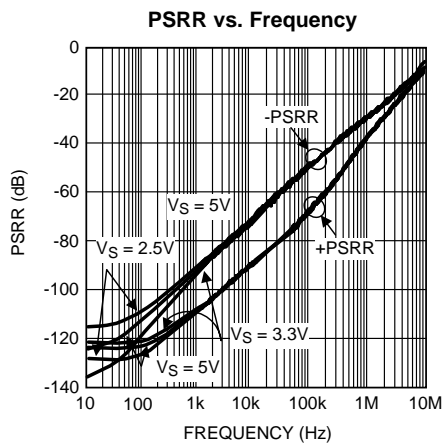


Figure 15.

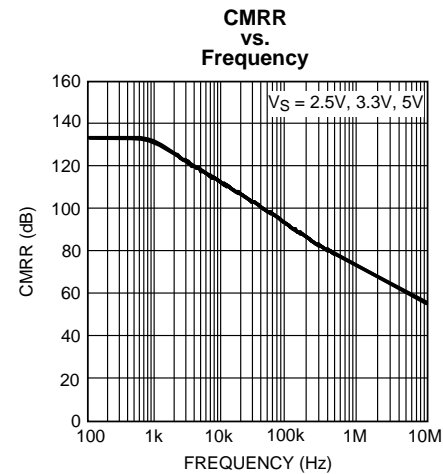


Figure 16.



**Typical Performance Characteristics (continued)**

Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $R_L > 10\text{ k}\Omega$ ,  $V_{CM} = V_S/2$ .

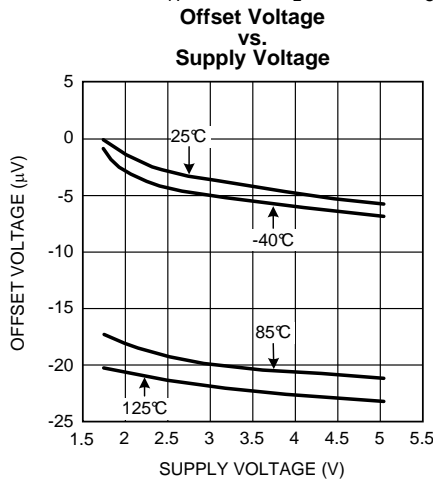


Figure 17.

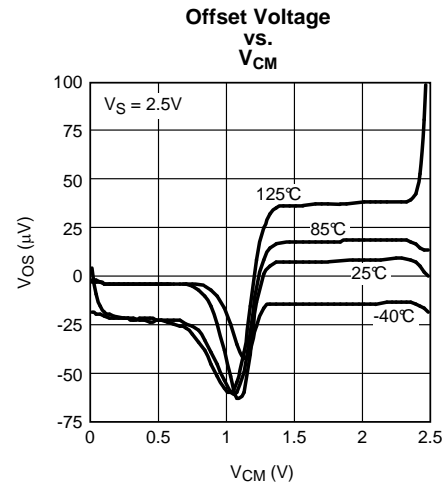


Figure 18.

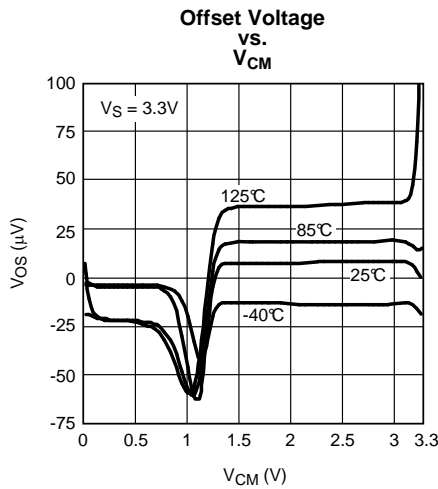


Figure 19.

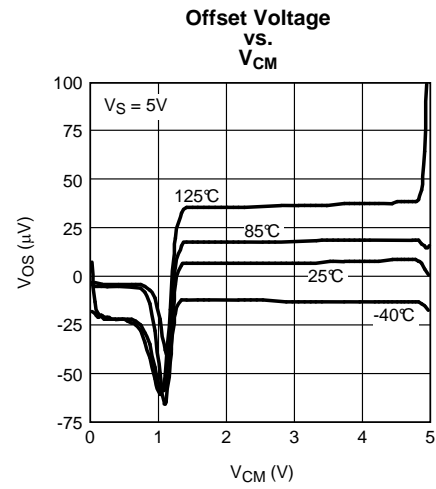


Figure 20.

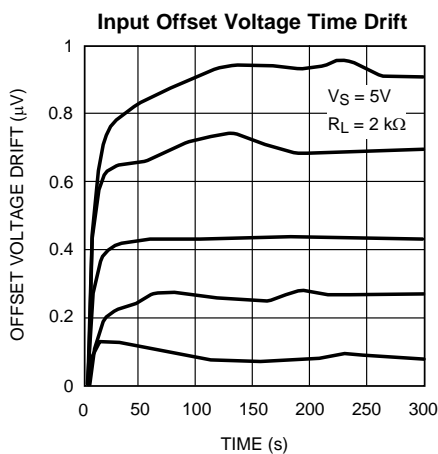


Figure 21.

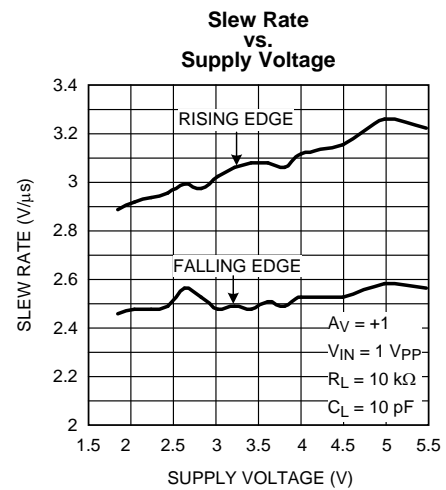
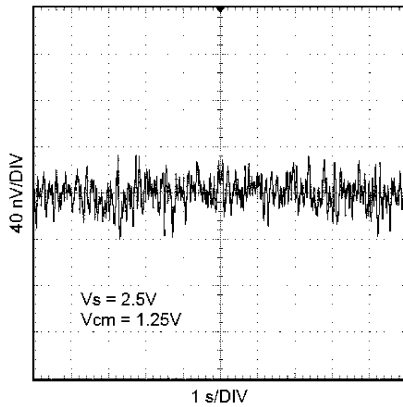


Figure 22.

**Typical Performance Characteristics (continued)**

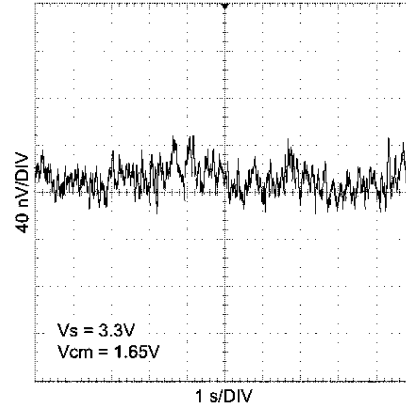
Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $R_L > 10\text{ k}\Omega$ ,  $V_{CM} = V_S/2$ .

**Time Domain Voltage Noise**



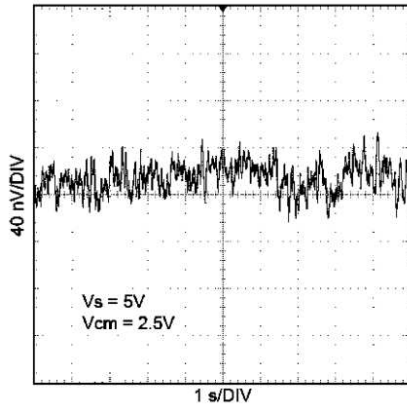
**Figure 23.**

**Time Domain Voltage Noise**



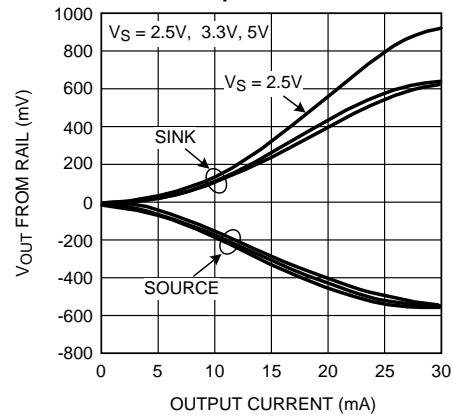
**Figure 24.**

**Time Domain Voltage Noise**



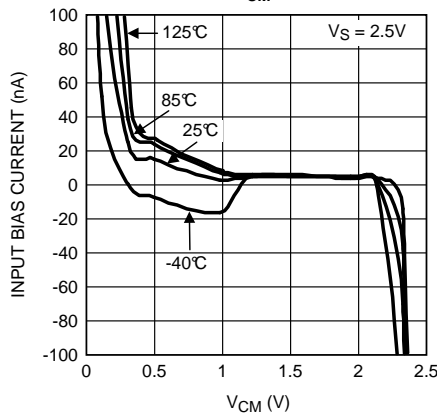
**Figure 25.**

**Output Voltage vs. Output Current**



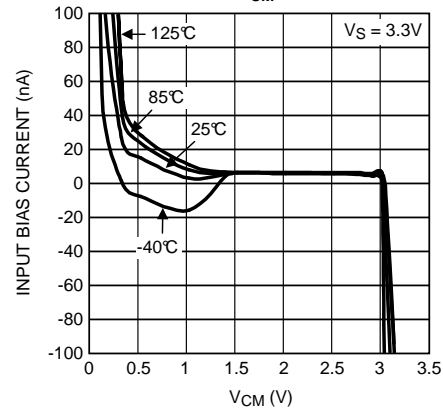
**Figure 26.**

**Input Bias Current vs. V<sub>CM</sub>**



**Figure 27.**

**Input Bias Current vs. V<sub>CM</sub>**



**Figure 28.**

Typical Performance Characteristics (continued)

Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $R_L > 10\text{ k}\Omega$ ,  $V_{CM} = V_S/2$ .

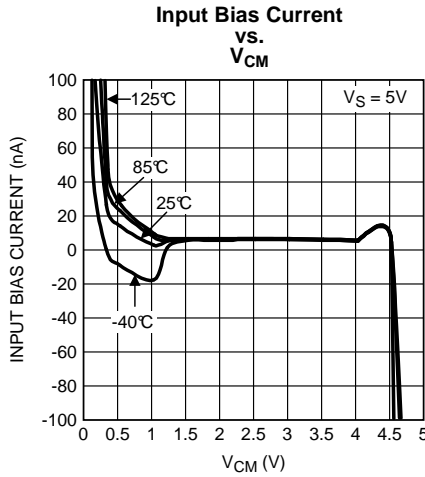


Figure 29.

Open Loop Frequency Response Over Temperature

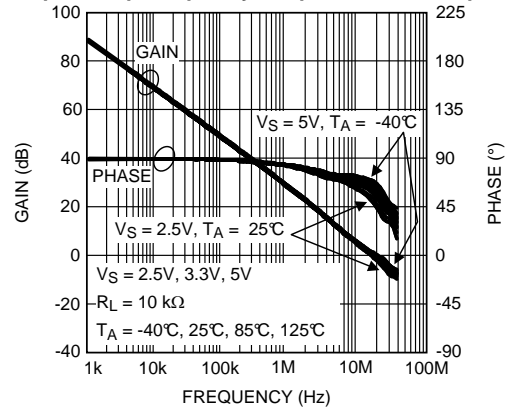


Figure 30.

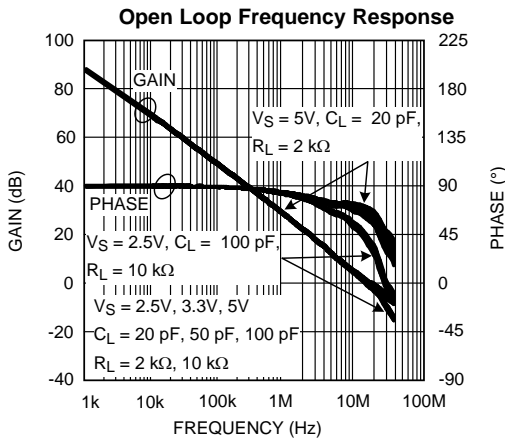


Figure 31.

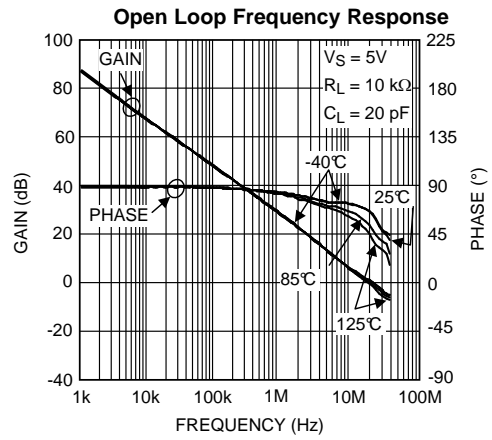


Figure 32.

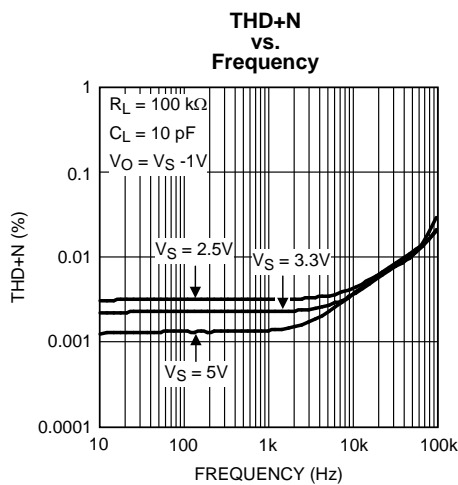


Figure 33.

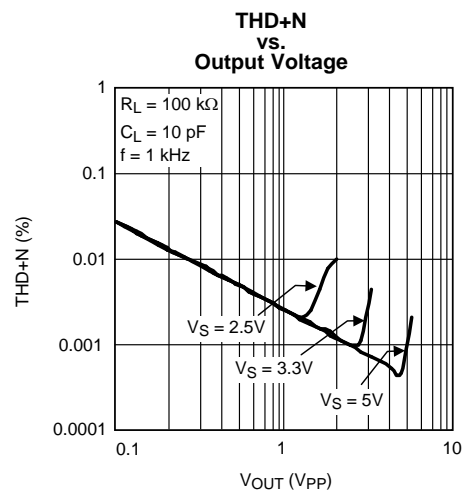
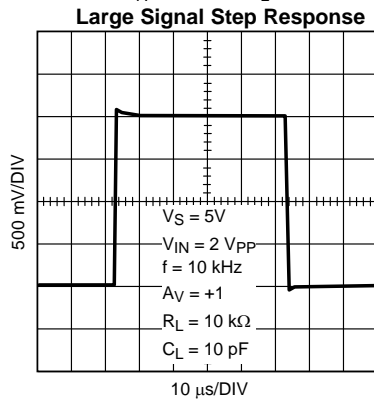


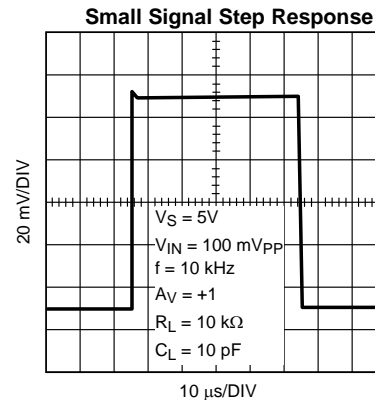
Figure 34.

**Typical Performance Characteristics (continued)**

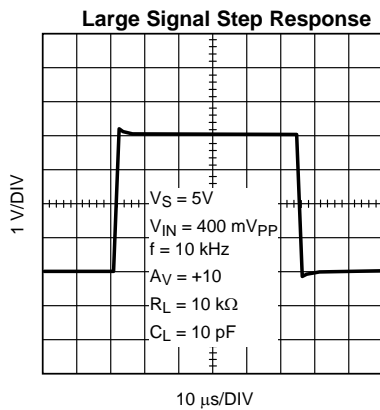
Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $R_L > 10\text{ k}\Omega$ ,  $V_{CM} = V_S/2$ .



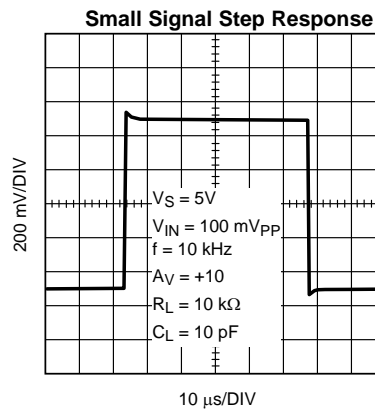
**Figure 35.**



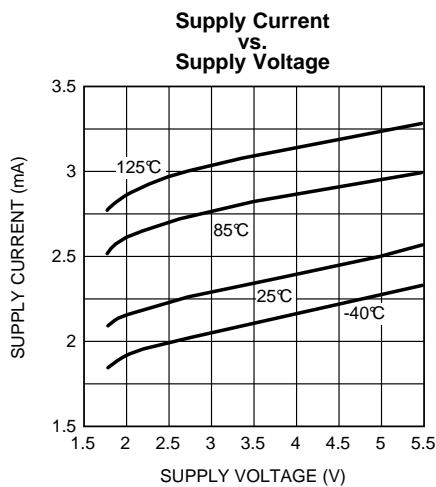
**Figure 36.**



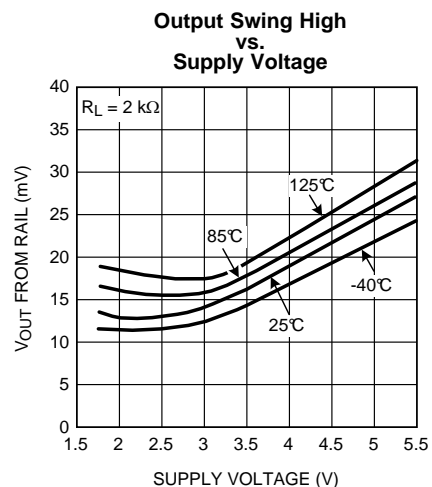
**Figure 37.**



**Figure 38.**



**Figure 39.**

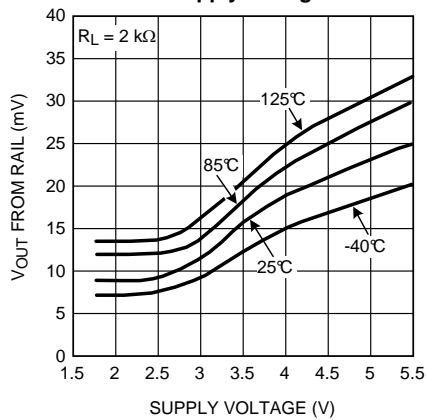


**Figure 40.**

**Typical Performance Characteristics (continued)**

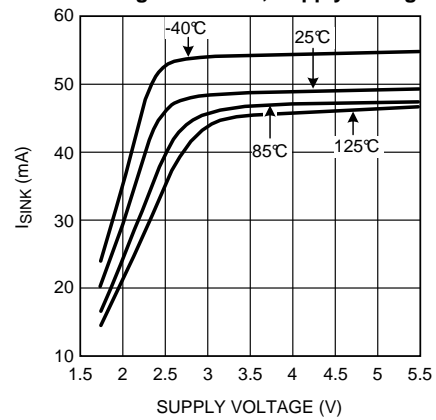
Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $R_L > 10\text{ k}\Omega$ ,  $V_{CM} = V_S/2$ .

**Output Swing Low vs. Supply Voltage**



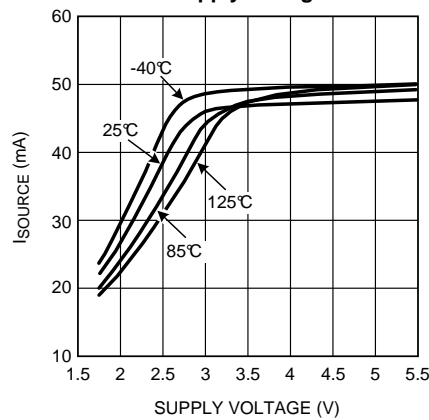
**Figure 41.**

**Sinking Current vs. Supply Voltage**



**Figure 42.**

**Sourcing Current vs. Supply Voltage**



**Figure 43.**

## APPLICATION INFORMATION

### LMP7731

The LMP7731 is a single, low noise, rail-to-rail input and output, and low voltage amplifier.

The low input voltage noise of only  $2.9 \text{ nV}/\sqrt{\text{Hz}}$  with a  $1/f$  corner at 3 Hz makes the LMP7731 ideal for sensor applications where DC accuracy is of importance.

The LMP7731 has a high gain bandwidth of 22 MHz. This wide bandwidth enables use of the amplifier at higher gain settings while retaining usable bandwidth for the application. This is particularly beneficial when system designers need to use sensors with very limited output voltage range as it allows larger gains in one stage which in turn increases the signal to noise ratio.

The LMP7731 has proprietary input bias cancellation circuitry on the input stages. This allows the LMP7731 to have only about 1.5 nA bias current with a bipolar input stage. This low input bias current, paired with the inherent lower input voltage noise of bipolar input stages makes the LMP7731 an excellent choice for precision applications. The combination of low input bias current, and low input voltage noise enables the user to achieve unprecedented accuracy and higher signal integrity.

Texas Instruments is heavily committed to precision amplifiers and the market segment they serve. Technical support and extensive characterization data are available for sensitive applications or applications with a constrained error budget.

The LMP7731 is offered in the space saving 5-Pin SOT-23 and 8-Pin SOIC packages. These small packages are ideal solutions for area constrained PC boards and portable electronics.

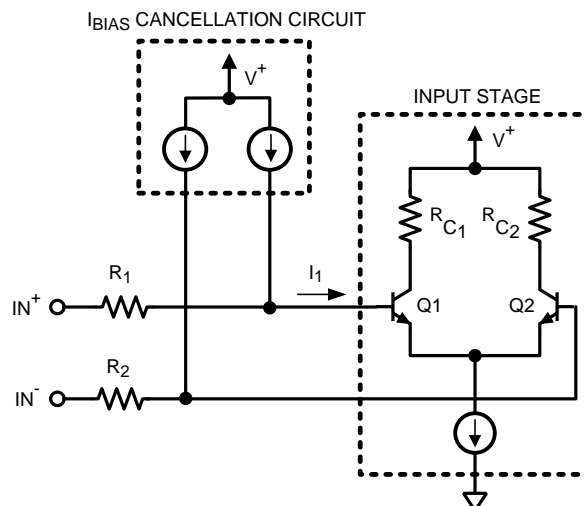
### INPUT BIAS CURRENT CANCELLATION

The LMP7731 has proprietary input bias current cancellation circuitry on their input stages.

The LMP7731 has rail-to-rail input. This is achieved by having two input stages in parallel. [Figure 44](#) shows only one of the input stages as the circuitry is symmetrical for both stages.

[Figure 44](#) shows that as the common mode voltage gets closer to one of the extreme ends, current  $I_1$  significantly increases. This increased current shows as an increase in voltage drop across resistor  $R_1$  equal to  $I_1 \cdot R_1$  on  $\text{IN}^+$  of the amplifier. This voltage contributes to the offset voltage of the amplifier. When common mode voltage is in the mid-range, the transistors are operating in the linear region and  $I_1$  is significantly small. The voltage drop due to  $I_1$  across  $R_1$  can be ignored as it is orders of magnitude smaller than the amplifier's input offset voltage.

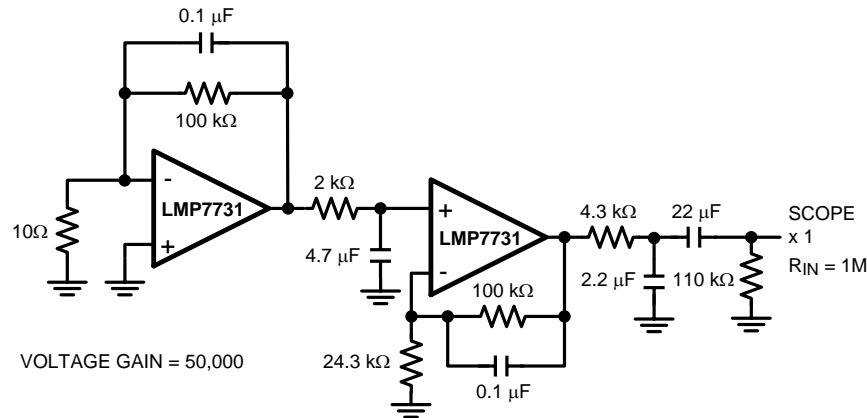
As the common mode voltage gets closer to one of the rails, the offset voltage generated due to  $I_1$  increases and becomes comparable to the amplifiers offset voltage.



**Figure 44. Input Bias Current Cancellation**

## INPUT VOLTAGE NOISE MEASUREMENT

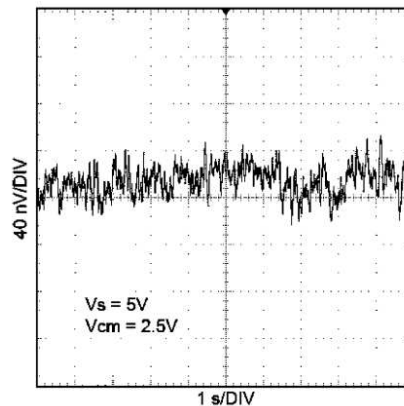
The LMP7731 has very low input voltage noise. The peak-to-peak input voltage noise of the LMP7731 can be measured using the test circuit shown in [Figure 45](#)



**Figure 45. 0.1 Hz to 10 Hz Noise Test Circuit**

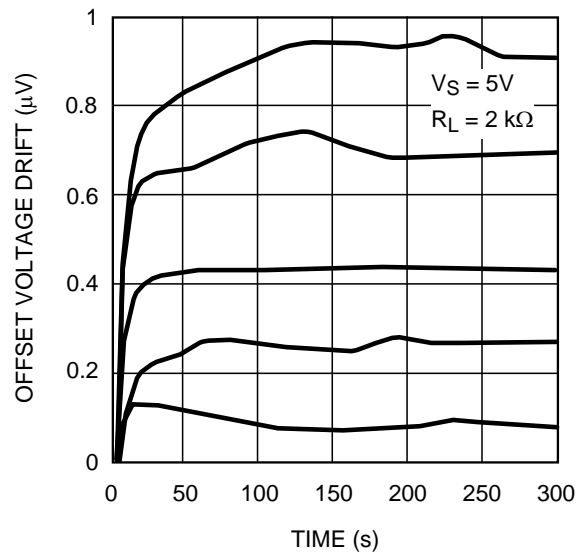
The frequency response of this noise test circuit at the 0.1 Hz corner is defined by only one zero. The test time for the 0.1 Hz to 10 Hz noise measurement using this configuration should not exceed 10 seconds, as this time limit acts as an additional zero to reduce or eliminate the noise contributions of noise from frequencies below 0.1 Hz.

[Figure 46](#) shows typical peak-to-peak noise for the LMP7731 measured with the circuit in [Figure 45](#) for the LMP7731.



**Figure 46. 0.1 Hz to 10 Hz Input Voltage Noise**

Measuring the very low peak-to-peak noise performance of the LMP7731, requires special testing attention. In order to achieve accurate results, the device should be warmed up for at least five minutes. This is so that the input offset voltage of the op amp settles to a value. During this warm up period, the offset can typically change by a few  $\mu\text{V}$  because the chip temperature increases by about  $30^\circ\text{C}$ . If the 10 seconds of the measurement is selected to include this warm up time, some of this temperature change might show up as the measured noise. [Figure 47](#) shows the start-up drift of five typical LMP7731 units.

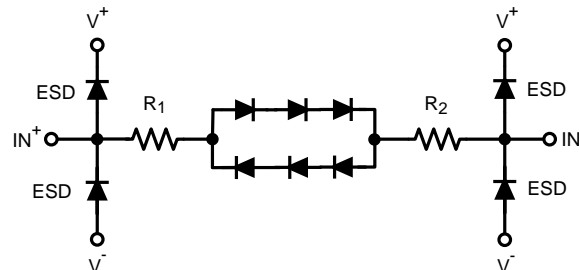


**Figure 47. Start-Up Input Offset Voltage Drift**

During the peak-to-peak noise measurement, the LMP7731 must be shielded. This prevents offset variations due to airflow. Offset can vary by a few nV due to this airflow and that can invalidate measurements of input voltage noise with a magnitude which is in the same range. For similar reasons, sudden motions must also be restricted in the vicinity of the test area. The feed-through which results from this motion could increase the observed noise value which in turn would invalidate the measurement.

## DIODES BETWEEN THE INPUTS

The LMP7731 has a set of anti-parallel diodes between the input pins as shown in [Figure 48](#). These diodes are present to protect the input stage of the amplifier. At the same time, they limit the amount of differential input voltage that is allowed on the input pins. A differential signal larger than the voltage needed to turn on the diodes might cause damage to the diodes. The differential voltage between the input pins should be limited to  $\pm 3$  diode drops or the input current needs to be limited to  $\pm 20$  mA.



**Figure 48. Anti-Parallel Diodes between Inputs**

## DRIVING AN ADC

Analog to Digital Converters, ADCs, usually have a sampling capacitor on their input. When the ADC's input is directly connected to the output of the amplifier a charging current flows from the amplifier to the ADC. This charging current causes a momentary glitch that can take some time to settle. There are different ways to minimize this effect. One way is to slow down the sampling rate. This method gives the amplifier sufficient time to stabilize its output. Another way to minimize the glitch caused by the switch capacitor is to have an external capacitor connected to the input of the ADC. This capacitor is chosen so that its value is much larger than the internal switching capacitor and it will hence provide the voltage needed to quickly and smoothly charge the



ADC's sampling capacitor. Since this large capacitor will be loading the output of the amplifier as well, an isolation resistor is needed between the output of the amplifier and this capacitor. The isolation resistor,  $R_{ISO}$ , separates the additional load capacitance from the output of the amplifier and will also form a low-pass filter and can be designed to provide noise reduction as well as anti-aliasing. The drawback to having  $R_{ISO}$  is that it reduces signal swing since there is some voltage drop across it.

Figure 49 (a) shows the ADC directly connected to the amplifier. To minimize the glitch in this setting, a slower sample rate needs to be used. Figure 49 (b) shows  $R_{ISO}$  and an external capacitor used to minimize the glitch.

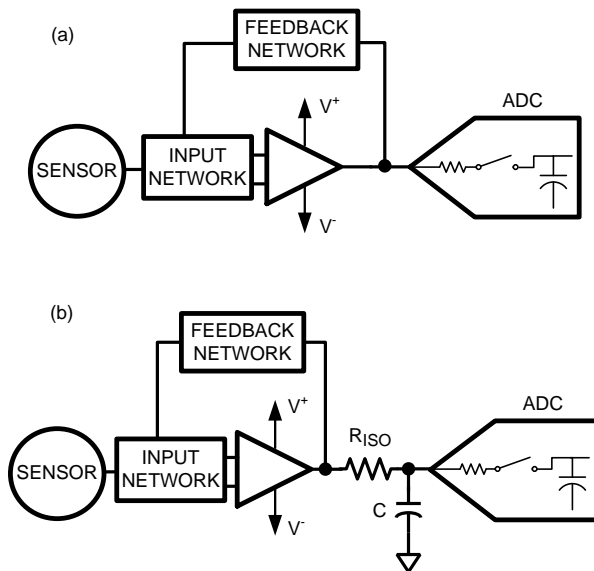


Figure 49. Driving an ADC

### REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">17</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMP7731MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMP77 31MA	<a href="#">Samples</a>
LMP7731MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMP77 31MA	<a href="#">Samples</a>
LMP7731MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AY3A	<a href="#">Samples</a>
LMP7731MFE/NOPB	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AY3A	<a href="#">Samples</a>
LMP7731MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AY3A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP7731MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP7731MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7731MFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7731MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP7731MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP7731MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMP7731MFE/NOPB	SOT-23	DBV	5	250	210.0	185.0	35.0
LMP7731MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

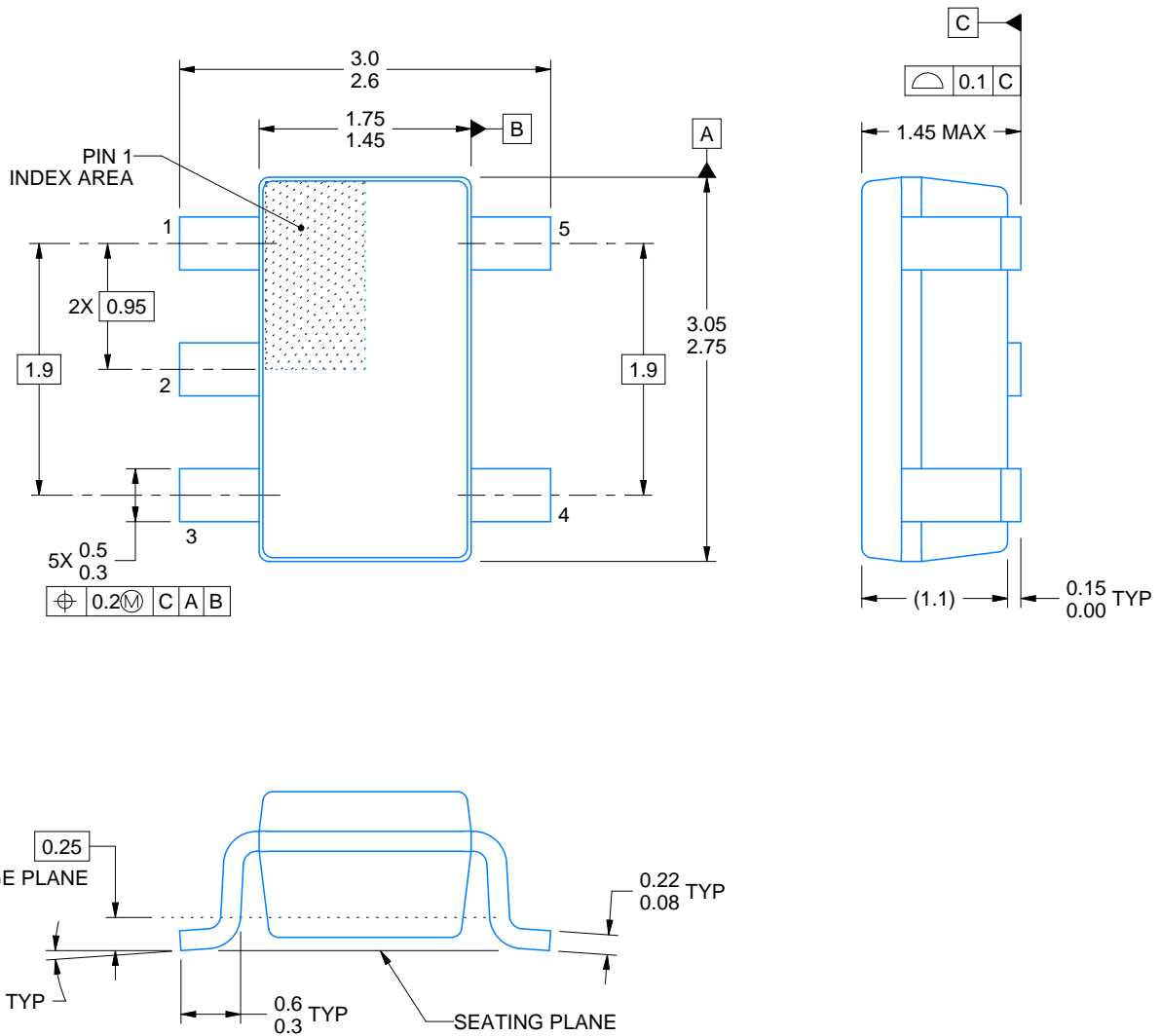
DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/D 11/2018

NOTES:

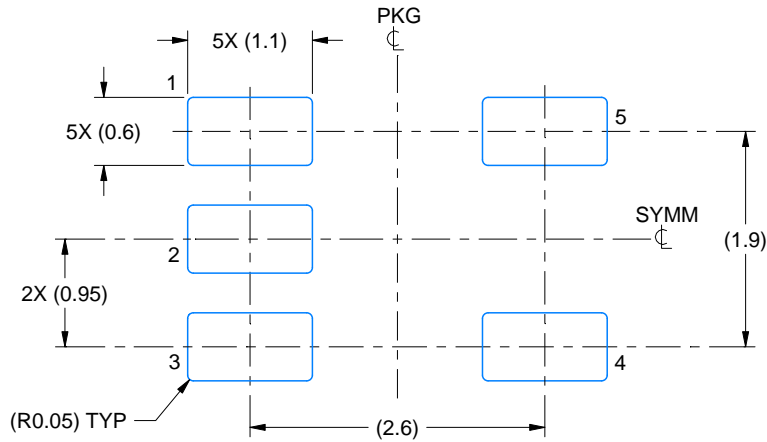
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

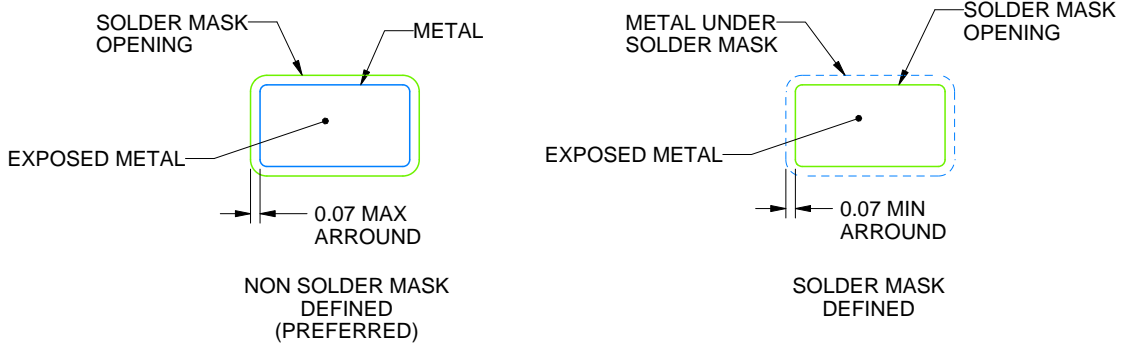
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

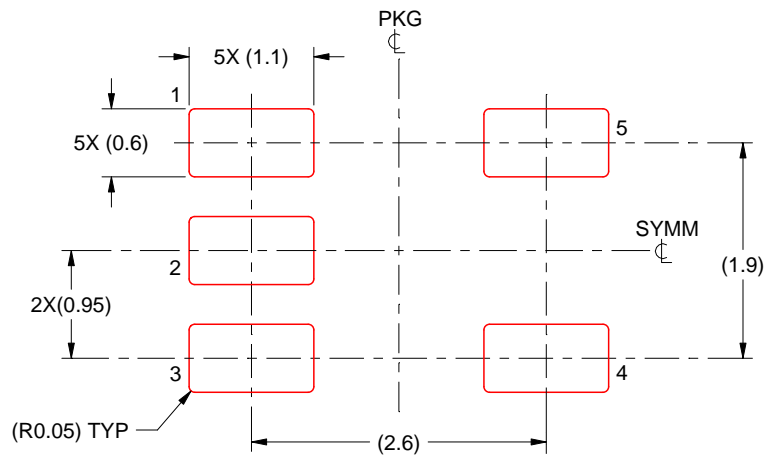
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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