LM8365 Micropower Undervoltage-Sensing Circuit With Programmable Output Delay

1 Features

- Extremely-Low Quiescent Current: 0.62 µA at V_{IN} = 2.6 V
- High Accuracy Threshold Voltage (±2.5%)
- Open-Drain Output
- Programmable Output Delay by External Capacitor (130 ms Typical With 0.1 µF)
- Input Voltage Range: 1 V to 6 V
- Pin-for-Pin Compatible With MC33465

2 Applications

- Portable Electronics
- Low-Battery Detection
- Microprocessor Reset Controllers
- Power Fail Indicators
- Battery Backup Detection

3 Description

The LM8365 device is a micropower undervoltage sensing circuit that is ideal for use in battery-powered microprocessor based systems, where extended battery life is a key requirement.

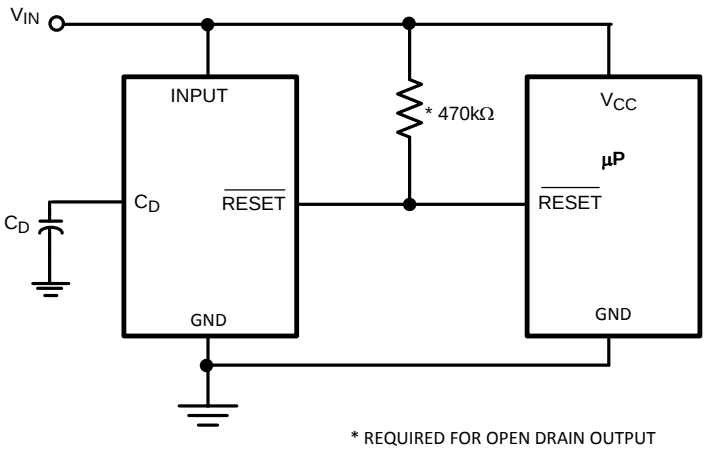
Threshold voltages of 2.7 V and 4.5 V are available with an active-low, open-drain output. These devices feature a very-low quiescent current of 0.65 µA typical. The LM8365 features a highly accurate voltage reference, a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation, a time delayed output which can be programmed by the system designer, and specified Reset operation down to 1 V with extremely-low standby current.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM8365	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Microprocessor $\overline{\text{Reset}}$ Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2013) to Revision C — **Page**

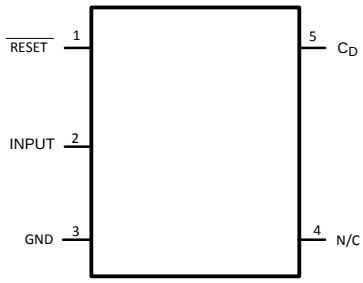
- Added, updated, or revised the following sections in accordance with new datasheet standards: *Description*, *Pin Configuration and Functions*, *Specifications*, , *Detailed Description*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, *Mechanical, Packaging, and Ordering Information*. ... 1
- Removed all references of the 22 Suffix and 30 Suffix from the *Electrical Characteristics* table ... 5
- Removed all references of the LM8365BCLMF30 in the *Typical Characteristics* section ... 7

Changes from Revision A (April 2013) to Revision B — **Page**

- Changed layout of National Data Sheet to TI format ... 11

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
C_D	5	O	Delay Capacitor Pin
GND	3	—	Ground
INPUT	2	I	Input Supply
N/C	4	—	No Connection
$\overline{\text{RESET}}$	1	O	Active Low Reset Output

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2).

		MIN	MAX	UNIT
Supply voltage		−0.3	6.5	V
$\overline{\text{RESET}}$ output voltage		−0.3	6.5	V
$\overline{\text{RESET}}$ output current		70		mA
Mounting temperature	Lead temp. (soldering 10 sec)		260	°C
	Junction temperature		125	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±200 V may actually have higher performance.

6.3 Recommended Operating Conditions (1)

	MIN	MAX	UNIT
Temperature	−40	85	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC (1)		LM8365 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	191.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	144.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified, all limits specified for T_A = 25°C.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{DET-}	Detector threshold voltage	High-to-low state output (V_{IN} decreasing)	27 suffix	2.633	2.7	2.767	V
			45 suffix	4.388	4.5	4.613	
V_{HYS}	Detector threshold hysteresis	V_{IN} increasing	27 suffix	0.081	0.135	0.189	V
			45 suffix	0.135	0.225	0.315	
ΔVdet/ΔT	Detector threshold voltage temperature coefficient				±100		PPM/°C
V_{OL}	$\overline{\text{RESET}}$ output voltage	Open-drain I_{SINK} = 1 mA			0.25	0.5	V
I_{OL}	$\overline{\text{RESET}}$ output sink current	V_{IN} = 1.5 V, V_{OL} = 0.5 V		1	2.5		mA
I_{OH}	$\overline{\text{RESET}}$ output source current	V_{IN} = 4.5 V, V_{OL} = 2.4 V		1	7		mA
I_{CD}	Delay pin output sink current	V_{IN} = 1.5 V, V_{CD} = 0.5 V		0.2	1.8		mA
R_D	Delay resistance			0.5	1	2	MΩ
V_{IN}	Operating input voltage range			1		6	V
I_{IN}	Quiescent input current	27 suffix	V_{IN} = 2.6 V		0.62	0.9	μA
			V_{IN} = 4.7 V		0.75	1.3	
		45 suffix	V_{IN} = 4.34 V		0.7	1	
			V_{IN} = 6 V		0.85	1.4	

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.

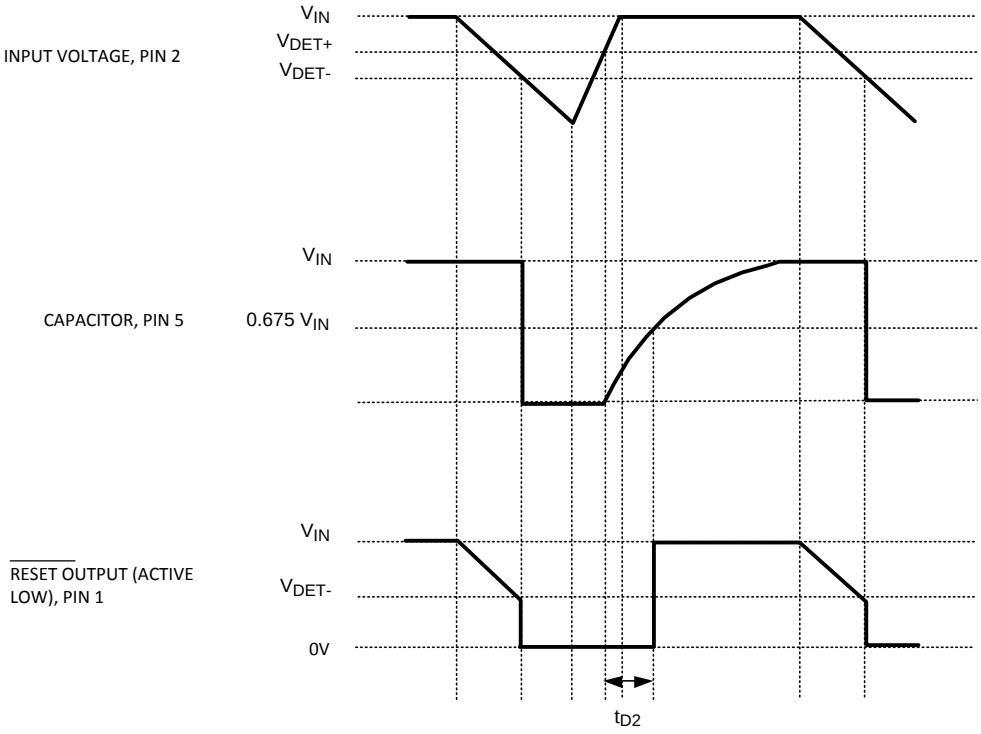


Figure 1. Timing Waveforms

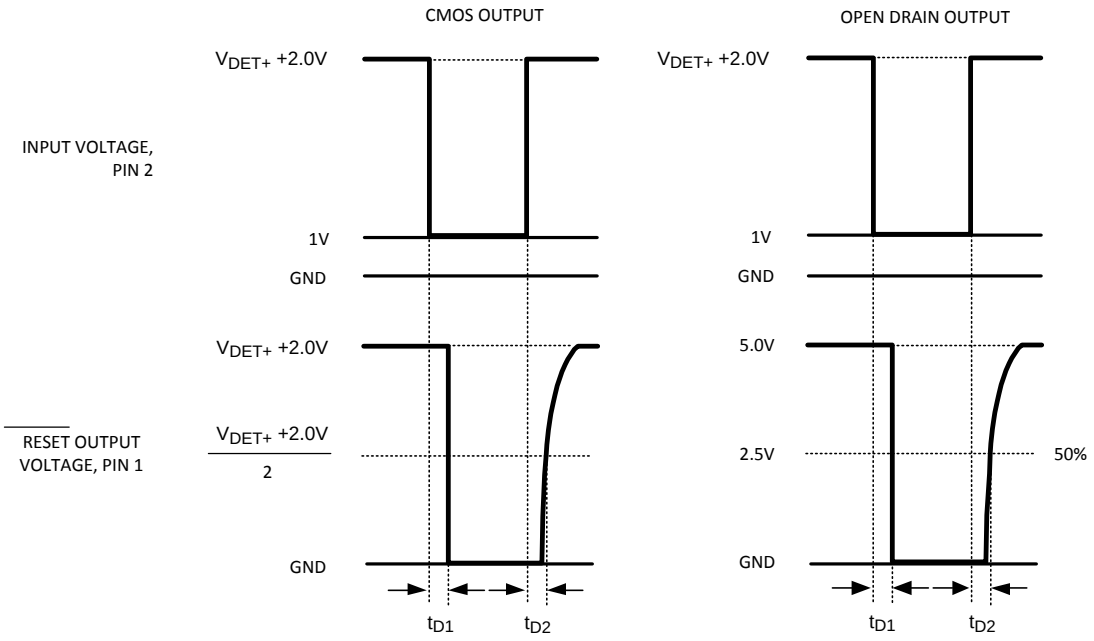


Figure 2. Propagation Delay Timing Diagrams

6.6 Typical Characteristics

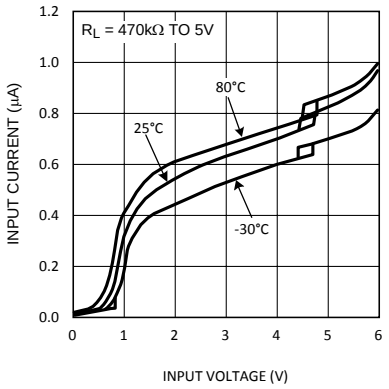


Figure 3. Input Current vs Input Voltage LM8365BALMF45

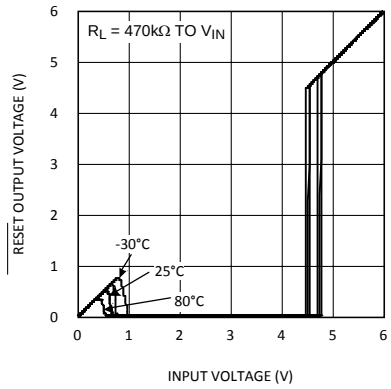


Figure 4. $\overline{\text{Reset}}$ Output Voltage vs Input Voltage LM8365BALMF45

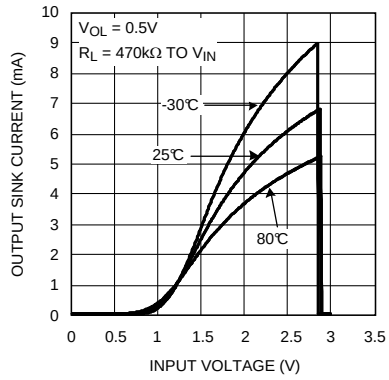


Figure 5. $\overline{\text{Reset}}$ Output Sink Current vs Input Voltage LM8365BALMF27

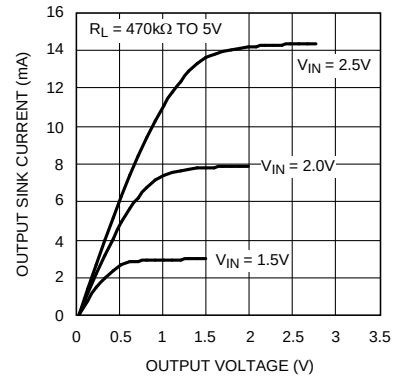


Figure 6. $\overline{\text{Reset}}$ Output Sink Current vs $\overline{\text{Reset}}$ Output Voltage LM8365BALMF45

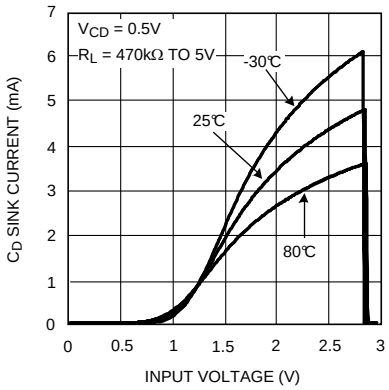


Figure 7. C_D Sink Current vs Input Voltage LM8365BALMF27

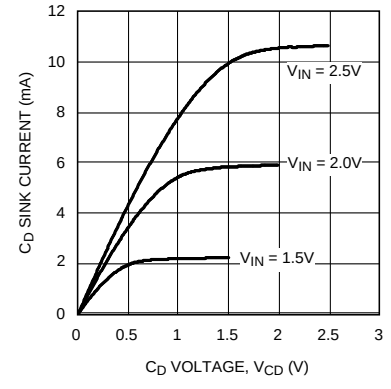


Figure 8. C_D Sink Current vs C_D Voltage

Typical Characteristics (continued)

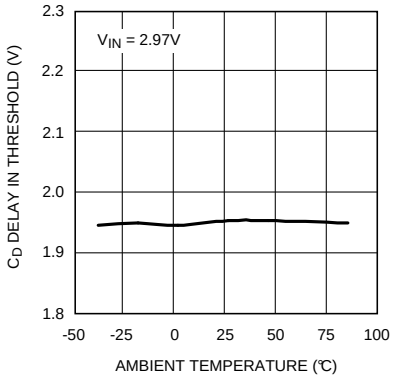


Figure 9. C_D Delay Pin Threshold Voltage vs Temperature LM8365BALMF27

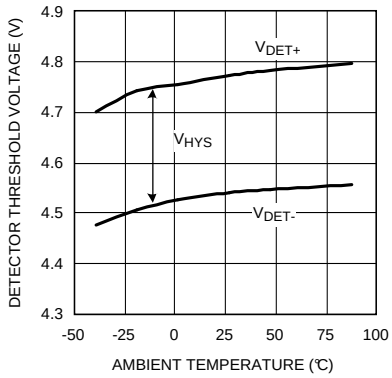


Figure 10. Detector Threshold Voltage vs Temperature LM8365BALMF45

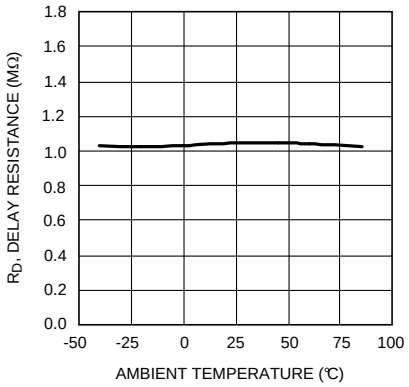


Figure 11. Delay Resistance vs Temperature

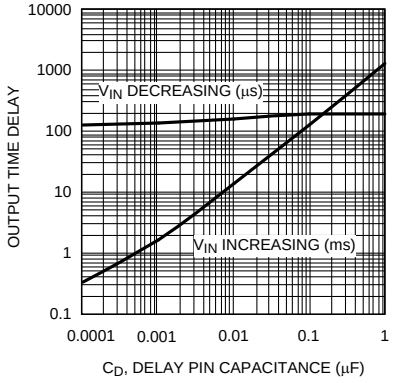


Figure 12. Output Time Delay vs Capacitance

7 Detailed Description

7.1 Overview

The LM8365 ultra-low current voltage detector was designed to monitor voltages and to provide an indication when the monitored voltage, V_{IN}, dropped below a precisely trimmed threshold voltage. The voltage detector of the LM8365 drives a time delay generator that may be programmed for fixed lengths of time depending on the application needs. This characteristic is displayed in the typical operating timing diagram in Figure 1.

7.2 Functional Block Diagram

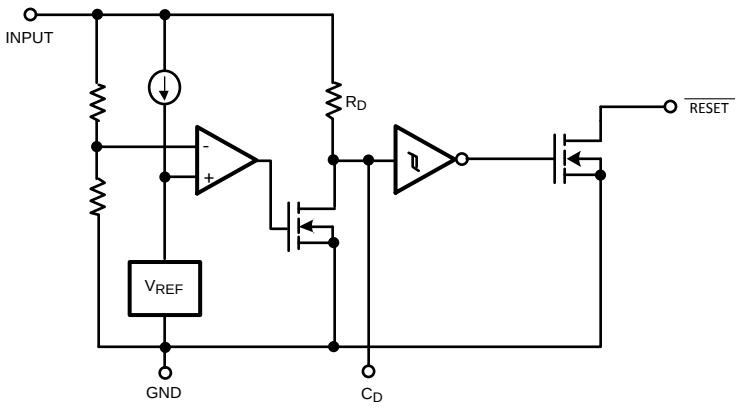


Figure 13. Open-Drain Output

7.3 Feature Description

V_{IN} is the voltage that is being monitored and as it decreases passed the precisely trimmed threshold V_{DET-}, the Active Low $\overline{\text{RESET}}$ output drops to a Logic Low state and the C_D pin drops to 0 V. During this state the external capacitor connected to the C_D pin is immediately discharged by an internal N-Channel MOSFET. When V_{IN} increases above the threshold V_{DET+} (V_{DET-} + V_{HYS}) the capacitor connected to the C_D pin starts to charge up to V_{IN} through an internal pullup resistor R_D. Once the capacitor has charged up past the internal Delay Pin Threshold, which is typically 0.675 V_{IN}, the $\overline{\text{RESET}}$ output will revert back to it's original state. The LM8365 have built-in hysteresis to help prevent erratic reset operation when the input voltage crosses the threshold.

The LM8365 has a wide variety of applications that can take advantage of its precision and low current consumption to monitor Input voltages even though it was designed as a reset controller in portable microprocessor based systems. It is a very cost-effective and space-saving device that will protect your more expensive investments of microprocessors and other devices that need a specified supply voltage and time delay for proper operation.

The propagation delay time for the LM8365 is measured using a 470-kΩ pullup resistor connected to from the $\overline{\text{RESET}}$ output pin to 5 V in addition to a 10-pF capacitive load connected from the same pin to GND. Figure 2 shows the timing diagram for the measurement for the propagation delay. V_{DET+} is equal to the sum of the detector threshold, V_{DET-}, and the built in hysteresis, V_{HYS}. t_{D1} is the propagation time from High-to-Low and t_{D2} is the propagation from Low-to-High.

7.4 Device Functional Modes

7.4.1 $\overline{\text{Reset}}$ Output Low

When V_{IN} decreases below the precisely trimmed threshold V_{DET-}, the C_D pin voltage will drop to 0 V and the $\overline{\text{Reset}}$ pin will output low.

7.4.2 $\overline{\text{Reset}}$ Output High

When V_{IN} increases above the precisely trimmed threshold V_{DET+} (V_{DET-} + V_{HYS}), the capacitor connected to the C_D pin starts to charge up to V_{IN} through an internal pull-up resistor R_D. Once the capacitor has charged up past the internal Delay Pin Threshold, which is typically 0.675 V_{IN}, the $\overline{\text{RESET}}$ output will be pulled high, assuming an external pullup resistor is connected from $\overline{\text{Reset}}$ to V_{IN}.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM8365 is a supervisor that is ideal for use in battery powered microprocessor based systems. With an external delay capacitor, C_D, a time delay can be accurately programmed to allow for use in many types of applications. The LM8365 can ensure system reliability and ensures that a connected microprocessor will operate only when a minimum V_{IN} supply is satisfied.

8.2 Typical Application

The LM8365 can be used as a simple supervisor circuit to monitor the input supply to a microprocessor as shown in Figure 14.

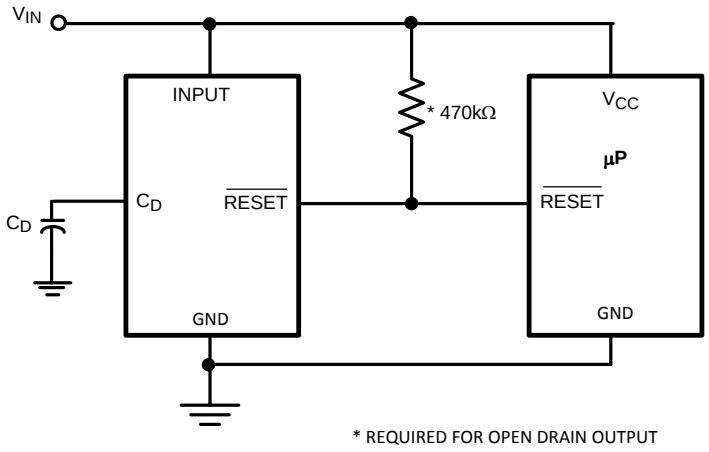


Figure 14. Microprocessor $\overline{\text{Reset}}$ Circuit

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Supply voltage range	1 V to 6 V
$\overline{\text{Reset}}$ Output voltage, high	Input Supply
$\overline{\text{Reset}}$ Output voltage, low	0 V
Output Time delay, C_D = 0.1 µF	130 ms
Output Time delay, C_D = 1 µF	1.2 s

8.2.2 Detailed Design Procedure

The Bill of Materials shown in Table 2 reflects the components used on the LM8365EVM. A layout of the EVM can be seen in Figure 19.

Table 2. Bill of Materials

DESIGNATOR	DESCRIPTION	PART NUMBER	QUANTITY	MANUFACTURER
U1	LM8365, 2.7V Threshold	LM8365	1	Texas Instruments
R1	470K Resistor, 0603	CRCW0603470KJNEA	1	Vishay
C1	0.01µF Capacitor, 0603	GRM188R71C103KA01D	1	MuRata
C2	0.1µF Capacitor, 0805	GRM219R71C104KA01D	1	MuRata
C3	1µF Capacitor, 0805	C0805C105K4RACTU	1	Kemet
C4	Input Capacitor	–	0	–

8.2.3 Application Curves

Two capacitor values for C_D (0.1 µF and 1 µF) are used as examples to show the programmability of the output time delay as shown in Figure 15 and Figure 16.

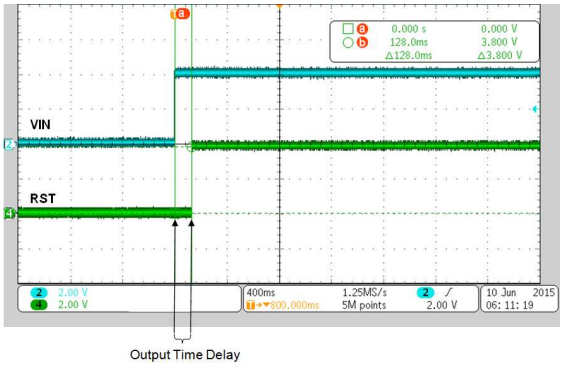


Figure 15. 0.1-µF Capacitor Programmed Delay

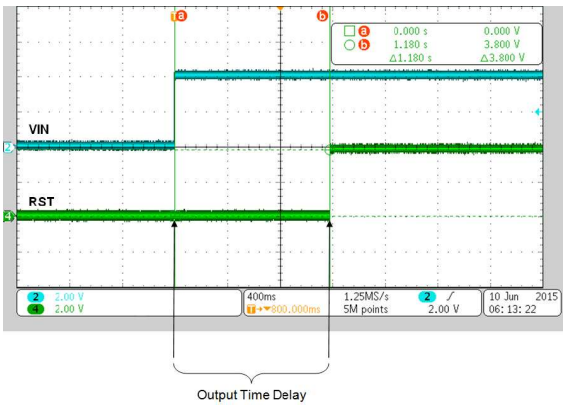


Figure 16. 1-µF Capacitor Programmed Delay

8.3 System Examples

The LM8365 can be used as a missing pulse detector. As shown in Figure 17, if a high-to-low transition pulse were to be missing, the C_D voltage would continue to increase until it reaches its threshold of 0.675 × V_{IN}, causing the Reset pin to output high and signal a missing pulse.

System Examples (continued)

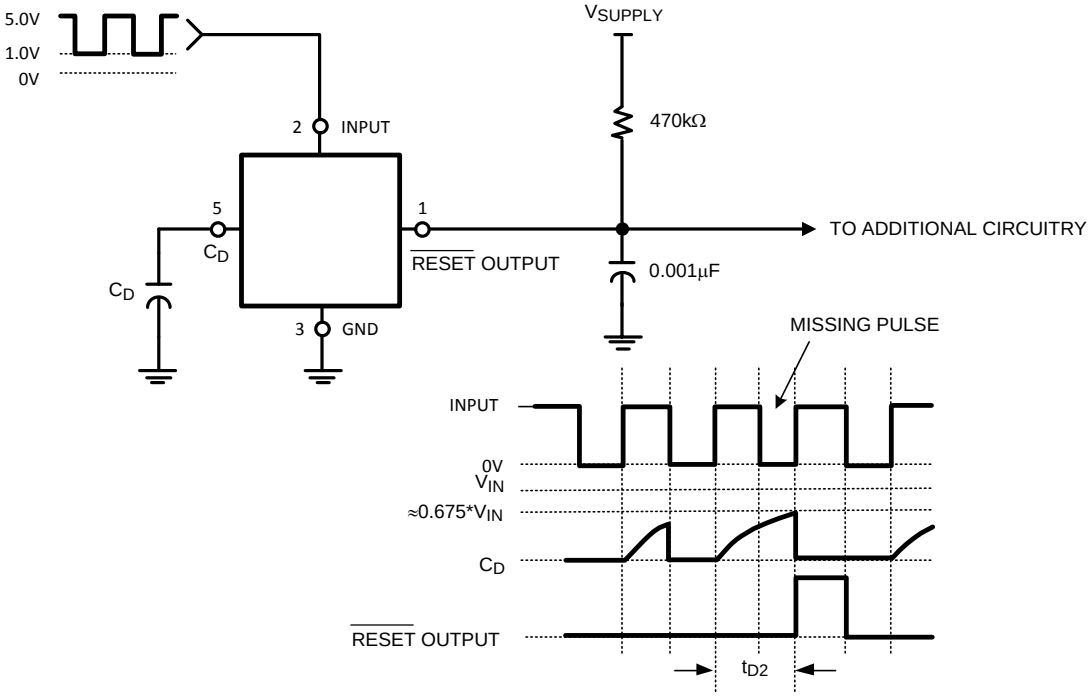


Figure 17. Missing Pulse Detector Using LM8365BALMF45

9 Power Supply Recommendations

The input of the LM8365 is designed to handle up to the supply voltage absolute maximum rating of 6.5 V. If the input supply is susceptible to any large transients above the maximum rating, then extra precautions should be taken. An input capacitor is recommended to avoid false Reset output triggers due to noise.

10 Layout

10.1 Layout Guidelines

- Place the input capacitor as close as possible to the IC.
- Keep traces short between the IC and the C_D capacitor to ensure the timing delay is as accurate as possible.

10.2 Layout Example

Figure 18 and Figure 19 are layout examples for the LM8365, which is taken from the LM8365EVM. For information on the operation and schematic of the EVM, see the *LM8365EVM User's Guide* (SNVU493).

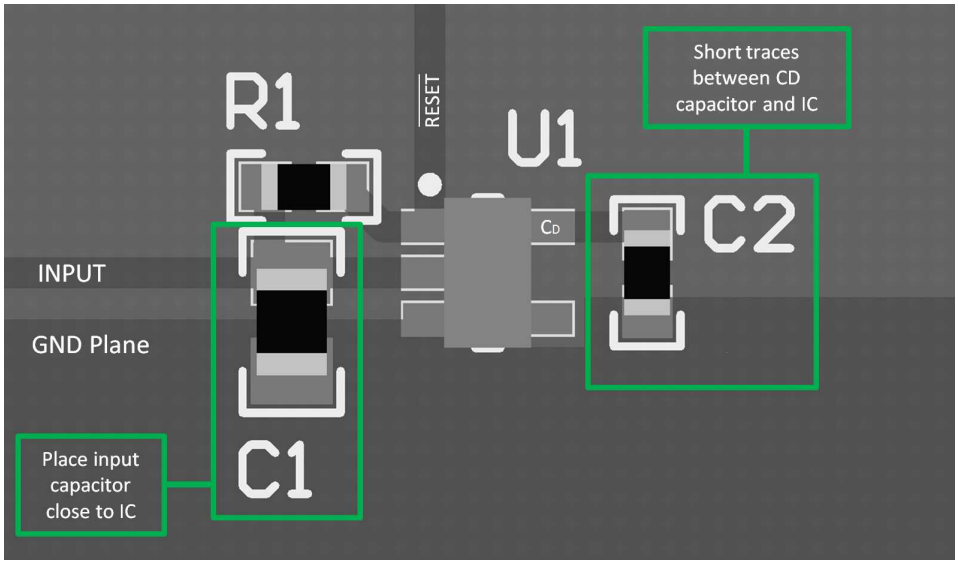


Figure 18. Layout Example

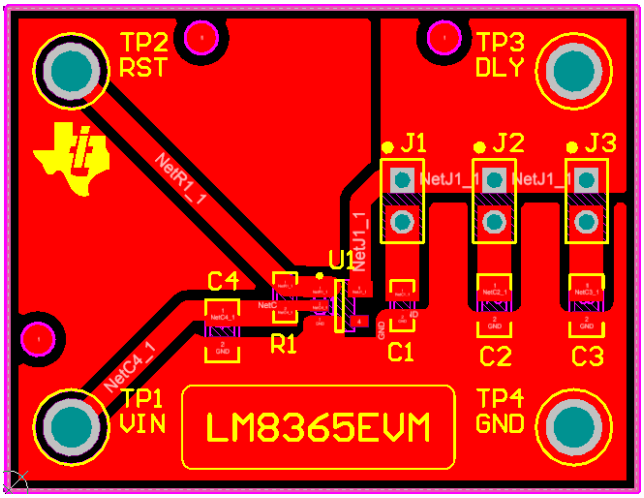


Figure 19. Top Layer Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

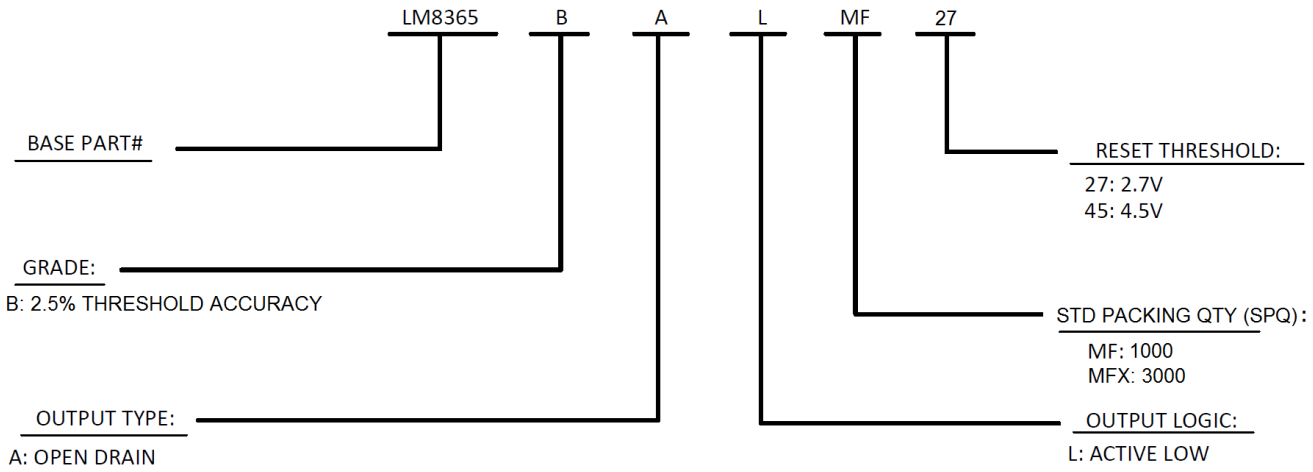


Figure 20. LM8365 IC Nomenclature

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

LM8365EVM User's Guide, SNVU493

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM8365BALMF27/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	F07A	Samples
LM8365BALMFX27/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	F07A	Samples
LM8365BALMFX45/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	F06A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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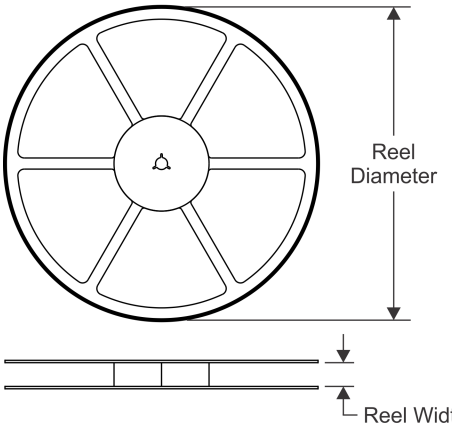
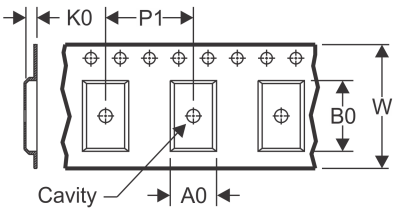
TAPE AND REEL INFORMATION

REEL DIMENSIONS

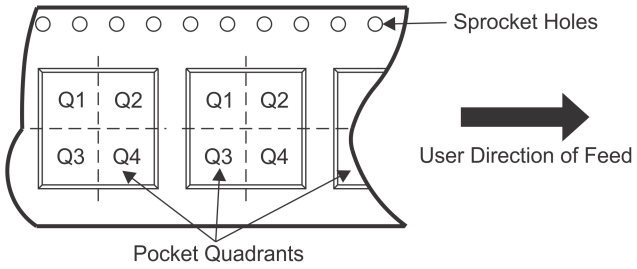


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

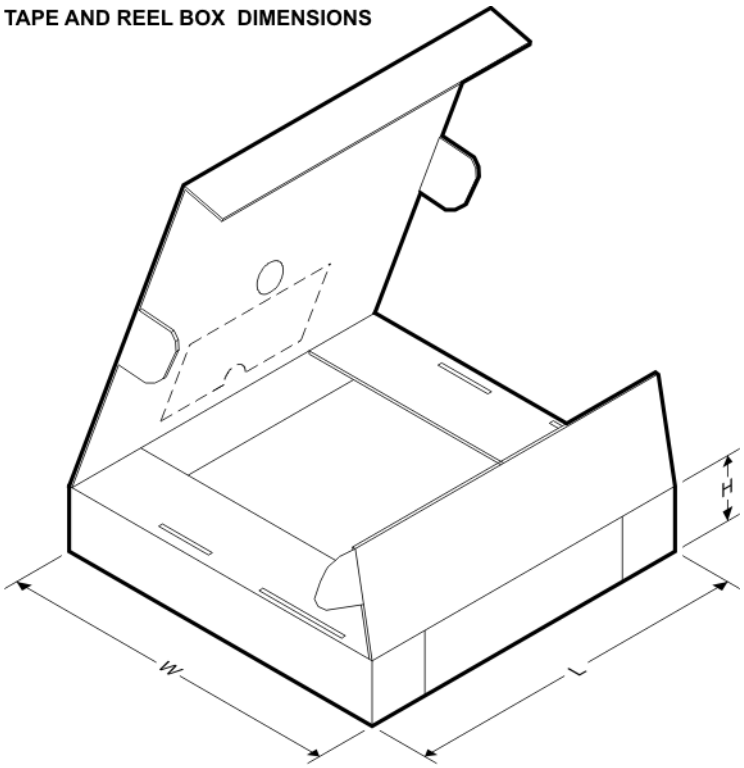
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM8365BALMF27/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM8365BALMFX27/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM8365BALMFX45/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

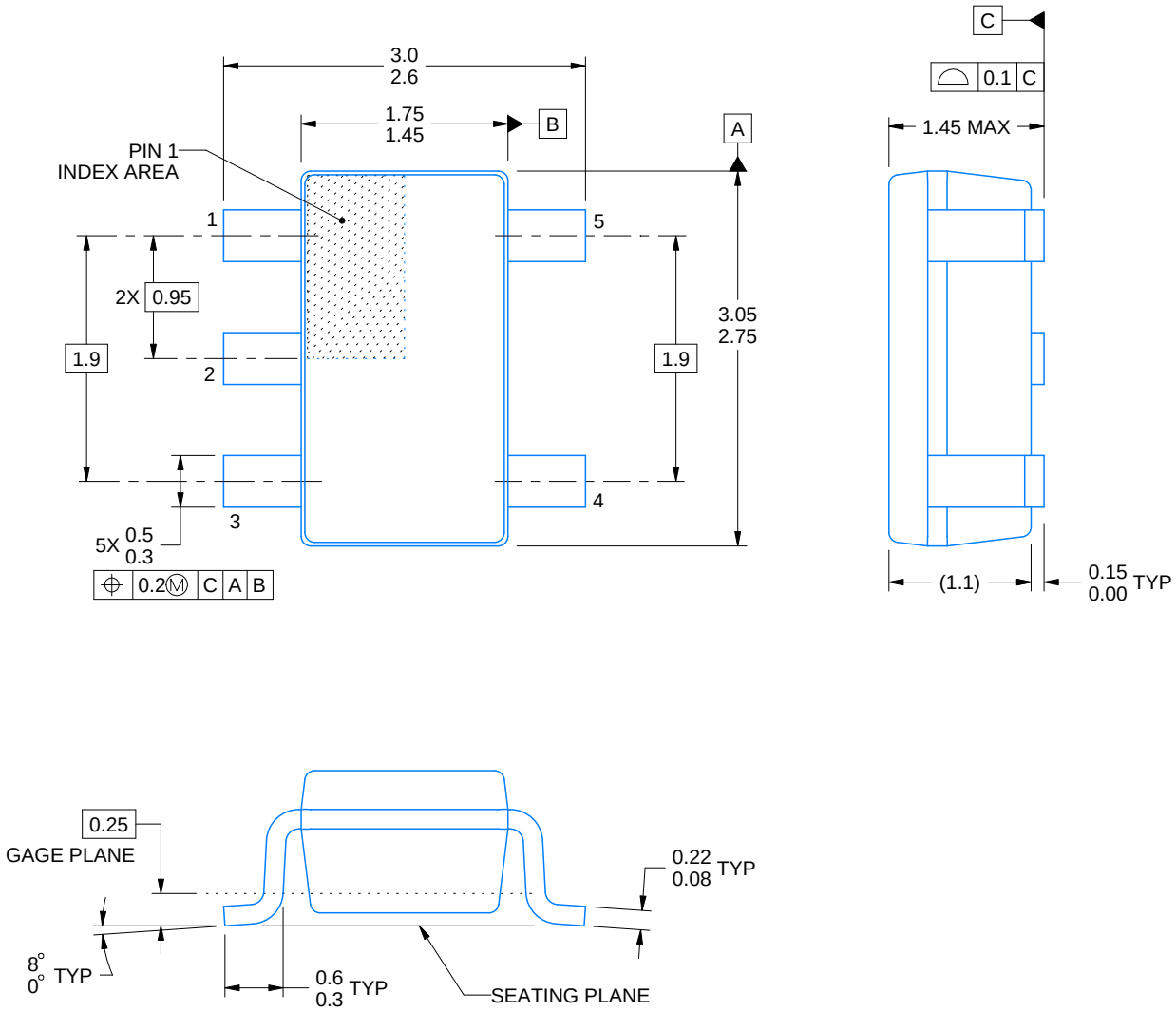
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM8365BALMF27/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM8365BALMFX27/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM8365BALMFX45/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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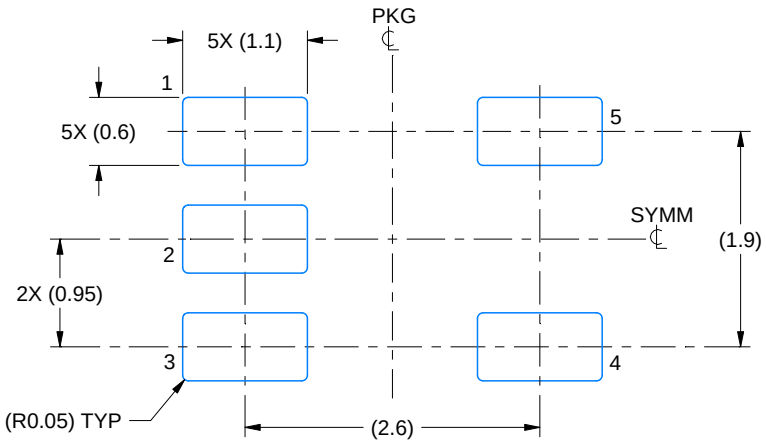
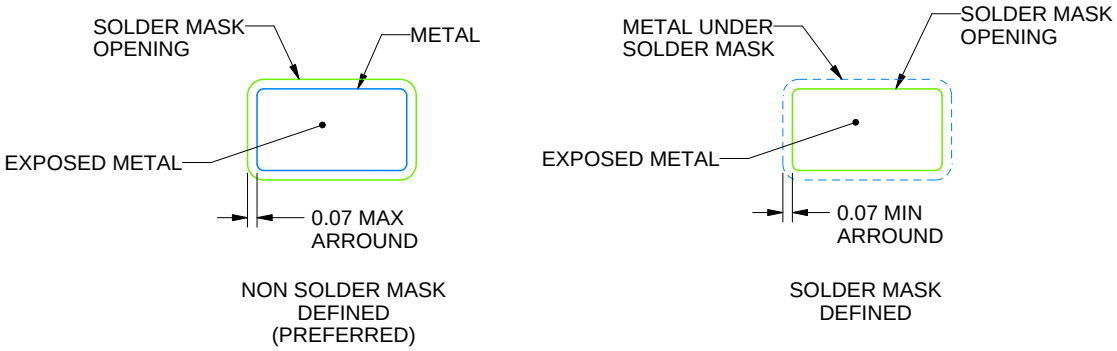
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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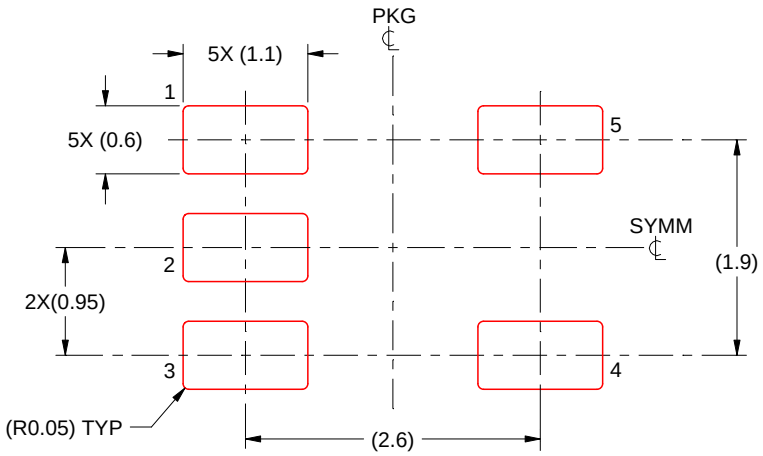
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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