



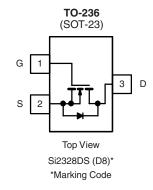
# N-Channel 100-V (D-S) MOSFET

| PRODUCT SUMMARY     |                                 |                    |  |  |
|---------------------|---------------------------------|--------------------|--|--|
| V <sub>DS</sub> (V) | $R_{DS(on)}\left(\Omega\right)$ | I <sub>D</sub> (A) |  |  |
| 100                 | 0.250 at V <sub>GS</sub> = 10 V | 1.5                |  |  |

#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Available
- 100 % R<sub>g</sub> Tested
   TrenchFET<sup>®</sup> Power MOSFET





Ordering Information: Si2328DS-T1-E3 (Lead (Pb)-free)

Si2328DS-T1-GE3 (Lead (Pb)-free and Halogen-free)

| <b>ABSOLUTE MAXIMUM RATINGS</b>                                 | T <sub>A</sub> = 25 °C, unle | ss otherwise r                    | noted       |              |      |  |
|---|------------------------------|-----------------------------------|-------------|--------------|------|--|
| Parameter   |                              | Symbol                            | 5 s         | Steady State | Unit |  |
| Drain-Source Voltage  |                              | V <sub>DS</sub>                   | 100         |              | V    |  |
| Gate-Source Voltage   |                              | V <sub>GS</sub>                   | ± 20        |              |      |  |
| Continuous Dunin Comment /T 450 00\8                            | T <sub>A</sub> = 25 °C       | 1-                                | 1.5         | 1.15         |      |  |
| Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup> | T <sub>A</sub> = 70 °C       | - I <sub>D</sub>                  | 1.2         | 0.92         |      |  |
| Pulsed Drain Current <sup>b</sup>                               |                              | I <sub>DM</sub>                   | 6           |              | Α    |  |
| Avalanche Current <sup>b</sup>                                  | L = 0.1 mH                   | I <sub>AS</sub>                   | 6<br>1.8    |              |      |  |
| Single Avalanche Energy   | L=0.1 IIII                   | E <sub>AS</sub>                   |             |              | mJ   |  |
| Continuous Source Current (Diode Conduction) <sup>a</sup>       |                              | I <sub>S</sub>                    | 0.6         |              | Α    |  |
| David Discission  | T <sub>A</sub> = 25 °C       | P <sub>D</sub>                    | 1.25        | 0.73         | W    |  |
| Power Dissipation <sup>a</sup>                                  | T <sub>A</sub> = 70 °C       | '`D                               | 0.80        | 0.47         |      |  |
| Operating Junction and Storage Temperature Range                |                              | T <sub>J</sub> , T <sub>stg</sub> | - 55 to 150 |              | °C   |  |

| THERMAL RESISTANCE RATINGS               |              |                     |         |         |      |
|--|--------------|---------------------|---------|---------|------|
| Parameter                                |              | Symbol              | Typical | Maximum | Unit |
| Mariana la Antica de Antica de           | t ≤ 5 s      | - R <sub>thJA</sub> | 80      | 100     | °C/W |
| Maximum Junction-to-Ambient <sup>a</sup> | Steady State |                     | 130     | 170     |      |
| Maximum Junction-to-Foot                 | Steady State |                     | 45      | 55      |      |

Notes:
a. Surface Mounted on 1" x 1" FR4 board.
b. Pulse width limited by maximum junction temperature.

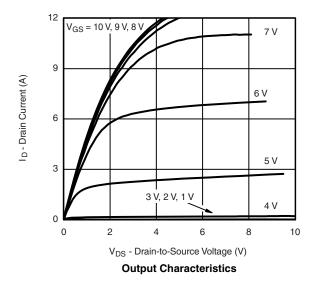
# Vishay Siliconix

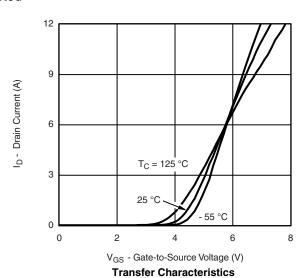


| SPECIFICATIONS T <sub>A</sub> = 25 °    | °C, unless          | otherwise noted  |        |       |       |      |  |
|---|---------------------|--|--------|-------|-------|------|--|
|   |                     |  | Limits |       |       |      |  |
| Parameter                               | Symbol              | Test Conditions  | Min.   | Тур.  | Max.  | Unit |  |
| Static                                  |                     |  |        |       |       |      |  |
| Drain-Source Breakdown Voltage          | $V_{DS}$            | $V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$                             | 100    |       |       | V    |  |
| Gate-Threshold Voltage                  | $V_{GS(th)}$        | $V_{DS} = V_{GS}$ , $I_D = 250 \mu A$                                  | 2      | 2     | 4     | v    |  |
| Gate-Body Leakage                       | I <sub>GSS</sub>    | $V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$                      |        |       | ± 100 | nA   |  |
| Zana Oata Walkana Busin Oamant          |                     | V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V                         |        |       | 1     |      |  |
| Zero Gate Voltage Drain Current         | I <sub>DSS</sub>    | V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C |        |       | 75    | μΑ   |  |
| On-State Drain Current <sup>a</sup>     | I <sub>D(on)</sub>  | $V_{DS} \ge 15 \text{ V}, V_{GS} = 10 \text{ V}$                       | 6      |       |       | Α    |  |
| Drain-Source On-Resistance <sup>a</sup> | R <sub>DS(on)</sub> | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.5 A                         |        | 0.195 | 0.250 | Ω    |  |
| Forward Transconductance <sup>a</sup>   | 9 <sub>fs</sub>     | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1.5 A                         |        | 4     |       | S    |  |
| Diode Forward Voltage                   | $V_{SD}$            | I <sub>S</sub> = 1.0 A, V <sub>GS</sub> = 0 V                          |        | 0.8   | 1.2   | V    |  |
| Dynamic <sup>b</sup>                    |                     |  |        |       |       |      |  |
| Total Gate Charge                       | $Q_g$               |  |        | 3.3   | 4.0   |      |  |
| Gate-Source Charge                      | $Q_{gs}$            | $V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 1.5 \text{ A}$  |        | 0.47  |       | nC   |  |
| Gate-Drain Charge                       | $Q_{gd}$            |  |        | 1.45  |       |      |  |
| Gate Resistance                         | $R_g$               |  | 0.5    |       | 2.4   | Ω    |  |
| Switching                               |                     |  |        |       |       |      |  |
| Turn-On Delay Time                      | t <sub>d(on)</sub>  |  |        | 7     | 11    |      |  |
| Rise Time                               | t <sub>r</sub>      | $V_{DD}$ = 50 V, $R_L$ = 33 $\Omega$                                   |        | 11    | 17    |      |  |
| Turn-Off Delay Time                     | t <sub>d(off)</sub> | $I_D \cong 0.2 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 6 \Omega$      |        | 9     | 15    | ns   |  |
| Fall Time                               | t <sub>f</sub>      |  |        | 10    | 15    |      |  |
| Source-Drain Reverse Recovery Time      | t <sub>rr</sub>     | I <sub>F</sub> = 1.5 A, dI/dt = 100 A/μs                               |        | 50    | 100   |      |  |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

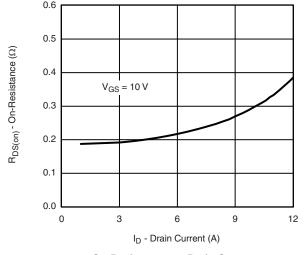




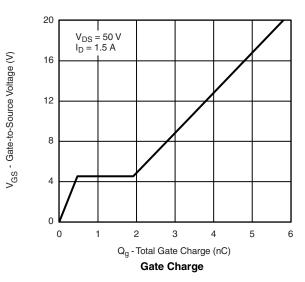
Notes: a. Pulse test: PW  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %. b. Guaranteed by design, not subject to production testing.

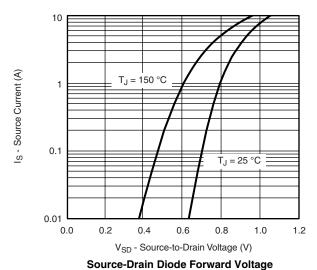


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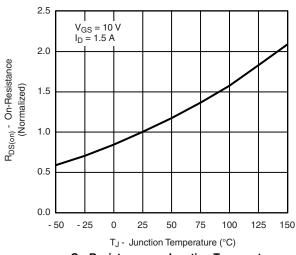


#### On-Resistance vs. Drain Current

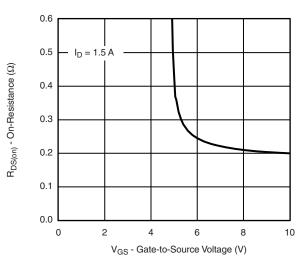




250 200  $\mathsf{C}_{\mathsf{iss}}$ C - Capacitance (pF) 150 100 50  $C_{oss}$  $\mathsf{C}_{\mathsf{rss}}$ 0 0 20 40 60 80 100



On-Resistance vs. Junction Temperature

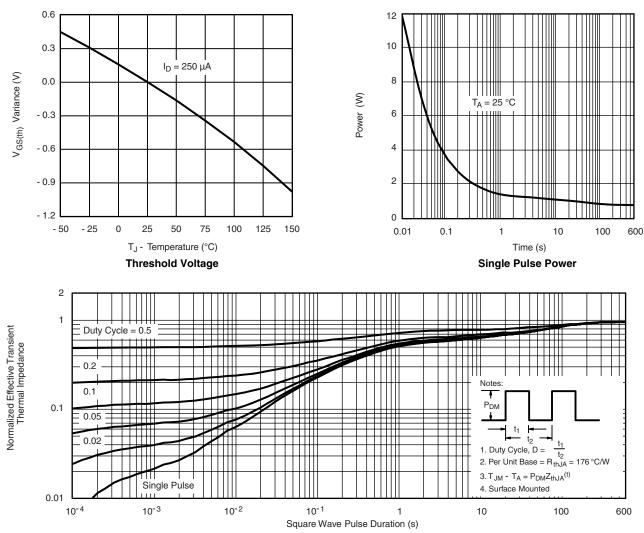


On-Resistance vs. Gate-to-Source Voltage

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### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?71796">www.vishay.com/ppg?71796</a>.



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