

## LM3409, -Q1, LM3409HV, -Q1 P-FET Buck Controller for High-Power LED Drivers

### 1 Features

- LM3409-Q1 and LM3409HV-Q1 are Automotive Grade Products: AEC-Q100 Grade 1 Qualified
- 2- $\Omega$ , 1-A Peak MOSFET Gate Drive
- $V_{IN}$  Range: 6 V to 42 V (LM3409, LM3409-Q1)
- $V_{IN}$  Range: 6 V to 75 V (LM3409HV, LM3409HV-Q1)
- Differential, High-Side Current Sense
- Cycle-by-Cycle Current Limit
- No Control Loop Compensation Required
- 10,000:1 PWM Dimming Range
- 250:1 Analog Dimming Range
- Supports All-Ceramic Output Capacitors and Capacitor-less Outputs
- Low-Power Shutdown and Thermal Shutdown
- Thermally Enhanced 10-Pin, HVSSOP Package

### 2 Applications

- LED Driver
- Constant Current Source
- Automotive Lighting
- General Illumination

### 3 Description

The LM3409, LM3409-Q1, LM3409HV, and LM3409HV-Q1 are P-channel MOSFET (PFET) controllers for step-down (buck) current regulators. They offer wide input voltage range, high-side differential current sense with low adjustable threshold voltage and fast output enable/disable function and a thermally enhanced 10-pin, HVSSOP package. These features combine to make the LM3409 family of devices ideal for use as constant current sources for driving LEDs where forward currents up to 5 A are easily achievable.

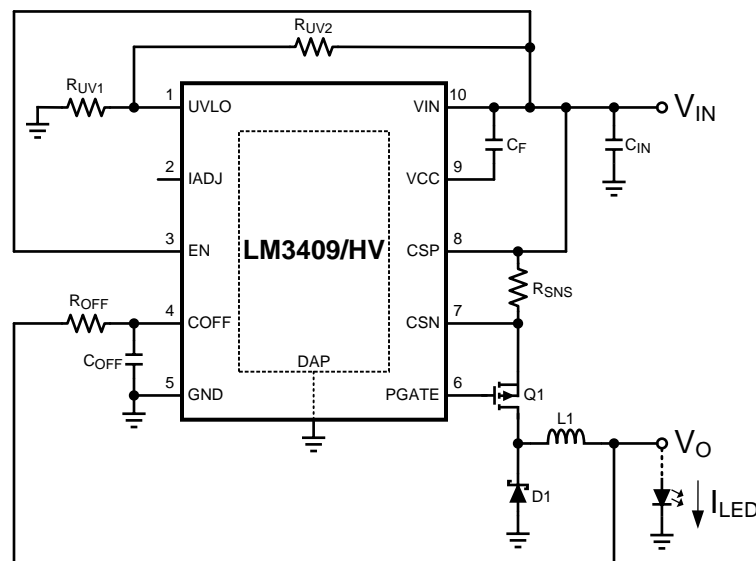
The LM3409 devices use constant off-time (COFT) control to regulate an accurate constant current without the need for external control loop compensation. Analog and PWM dimming are easy to implement and result in a highly linear dimming range with excellent achievable contrast ratios. Programmable UVLO, low-power shutdown, and thermal shutdown complete the feature set.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3409	HVSSOP (10)	3.00 mm × 3.00 mm
	PDIP (14)	19.177 mm × 6.35 mm
LM3409-Q1	HVSSOP (10)	3.00 mm × 3.00 mm
LM3409HV		
LM3409HV-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Typical Application Schematic



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision K (July 2014) to Revision L</b>	<b>Page</b>
• Corrected package family reference in <a href="#">Features</a> section .....	<b>1</b>
• Corrected package family reference in Device Information table.....	<b>1</b>
• Added <a href="#">Device Comparison</a> table .....	<b>3</b>
• Corrected typographical error in package name reference in <a href="#">Pin Configuration and Functions</a> section .....	<b>3</b>
• Corrected typographical error in <a href="#">Absolute Maximum Ratings</a> table .....	<b>4</b>
• Corrected typographical error in package name reference in <a href="#">ESD Ratings</a> table .....	<b>4</b>
• Corrected package family reference in <a href="#">Thermal Information</a> table.....	<b>5</b>

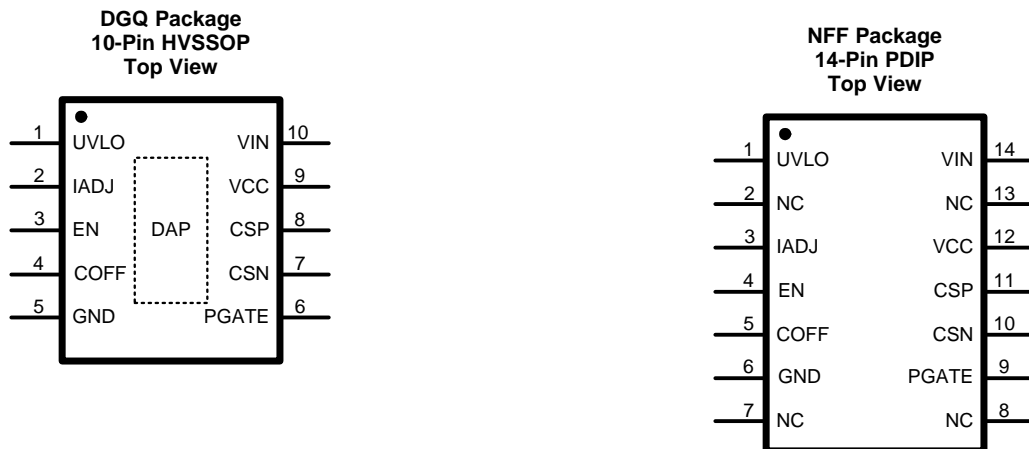
<b>Changes from Revision J (May 2013) to Revision K</b>	<b>Page</b>
• Added <a href="#">ESD Ratings</a> table, <a href="#">Feature Description</a> section, <a href="#">Device Functional Modes</a> , <a href="#">Application and Implementation</a> section, <a href="#">Power Supply Recommendations</a> section, <a href="#">Layout</a> section, <a href="#">Device and Documentation Support</a> section, and <a href="#">Mechanical, Packaging, and Orderable Information</a> section .....	<b>1</b>

<b>Changes from Revision I (May 2013) to Revision J</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format .....	<b>1</b>

## 5 Device Comparison Table

ORDERABLE NUMBER	MAXIMUM INPUT VOLTAGE (V)	AEC-Q100 GRADE 1 QUALIFIED
LM3409	42	N
LM3409-Q1		Y
LM3409HV	75	N
LM3409HV-Q1		Y

## 6 Pin Configuration and Functions



### Pin Functions

PIN			DESCRIPTION
NAME	PDIP	HVSSOP	
UVLO	1	1	Input undervoltage lockout. Connect to a resistor divider from $V_{IN}$ and GND. Turn-on threshold is 1.24 V and hysteresis for turnoff is provided by a 22 $\mu$ A current source.
IADJ	3	2	Analog LED current adjust. Apply a voltage from 0 to 1.24 V, connect a resistor to GND, or leave open to set the current sense threshold voltage.
EN	4	3	Logic level enable and PWM dimming. Apply a voltage >1.74 V to enable device, a PWM signal to dim, or a voltage < 0.5 V for low-power shutdown.
COFF	5	4	Off-time programming. Connect resistor from $V_O$ , capacitor to GND to set off-time.
GND	6	5	Connect to system ground.
PGATE	9	6	Gate drive. Connect to gate of external P-channel MOSFET.
CSN	10	7	Negative current sense. Connect to negative side of sense resistor.
CSP	11	8	Positive current sense. Connect to positive side of sense resistor (also to $V_{IN}$ ).
VCC	12	9	$V_{IN}$ -referenced linear regulator output. Connect at least a 1- $\mu$ F ceramic capacitor to $V_{IN}$ . The regulator provides power for the P-channel MOSFET drive.
VIN	14	10	Input voltage. Connect to the input voltage.
Thermal pad	—	—	Connect to GND pin. Place 4 to 6 vias from thermal pad to GND plane.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

		MIN	MAX	UNIT
VIN, EN, UVLO to GND	LM3409, LM3409-Q1	-0.3	45	V
	LM3409HV, LM3409HV-Q1	-0.3	76	
VIN to VCC, PGATE		-0.3	7	V
VIN to PGATE for 100 ns		-2.8	9.5	V
VIN to CSP, CSN		-0.3	0.3	V
COFF to GND		-0.3	4	V
COFF Current continuous			±1	mA
IADJ Current continuous			±5	mA
Junction temperature			150	°C
Soldering information	Lead temperature (Soldering, 10 s)		260	°C
	Infrared and convection reflow (15 s)		260	°C
Storage temperature, T <sub>stg</sub>		-65	125	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.

### 7.2 ESD Ratings

		VALUE	UNIT
<b>LM3409 IN DGQ AND NFF PACKAGES</b>			
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±1000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000	
<b>LM3409-Q1 IN DGQ AND NFF PACKAGES</b>			
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(3)(4)</sup>	±2000	V
	Charged device model (CDM), per AEC Q100-011	±1000	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
- AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
- The human body model is a 100 pF capacitor discharged through a 1.5-kΩ resistor into each pin.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>IN</sub>	LM3409, LM3409-Q1	6	42	V
	LM3409HV, LM3409HV-Q1	6	75	
Junction temperature range, T <sub>J</sub>		-40	125	°C

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM3409, LM3409-Q1, LM3409HV, LM3409HV-Q1	LM3409	UNIT
		DGQ (HVSSOP)	NFF (PDIP)	
		10 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54.4	49	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.7	36.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.8	28.9	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	3.9	21.1	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	33.5	28.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

$V_{IN} = 24\text{ V}$  unless otherwise indicated. Typical values and limits appearing in plain type apply for  $T_A = T_J = 25^\circ\text{C}$  <sup>(1)</sup>. Data sheet minimum and maximum specification limits are specified by design, test, or statistical analysis.

PARAMETER		TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(1)</sup>	MAX <sup>(2)</sup>	UNIT
<b>PEAK CURRENT COMPARATOR</b>						
$V_{CST}$	$V_{CSP} - V_{CSN}$ average peak current threshold <sup>(3)</sup>	$V_{ADJ} = 1\text{ V}$	188	198	208	mV
		$V_{ADJ} = V_{ADJ-OC}$	231	246	261	
$A_{ADJ}$	$V_{ADJ}$ to $V_{CSP} - V_{CSN}$ threshold gain	$0.1 < V_{ADJ} < 1.2\text{ V}$ $V_{ADJ} = V_{ADJ-OC}$		0.2		V/V
$V_{ADJ-OC}$	IADJ pin open circuit voltage		1.189	1.243	1.297	V
$I_{ADJ}$	IADJ pin current		3.8	5	6.4	$\mu\text{A}$
$t_{DEL}$	CSN pin falling delay	CSN fall - PGATE rise		38		ns
<b>SYSTEM CURRENTS</b>						
$I_{IN}$	Operating input current	Not switching		2		mA
$I_{SD}$	Shutdown input current	EN = 0 V		110		$\mu\text{A}$
<b>PFET DRIVER</b>						
$R_{PGATE}$	Driver output resistance	Sourcing 50 mA		2		$\Omega$
		Sinking 50 mA		2		
<b>VCC REGULATOR</b>						
$V_{CC}$	VIN pin voltage - VCC pin voltage	$V_{IN} > 9\text{ V}$ $0 < I_{CC} < 20\text{ mA}$	5.5	6	6.5	V
$V_{CC-UVLO}$	$V_{CC}$ undervoltage lockout threshold	$V_{CC}$ increasing		3.73		V
$V_{CC-HYS}$	$V_{CC}$ UVLO hysteresis	$V_{CC}$ decreasing		283		mV
$I_{CC-LIM}$	$V_{CC}$ regulator current limit		30	45		mA
<b>OFF-TIMER AND ON-TIMER</b>						
$V_{OFT}$	Off-time threshold		1.122	1.243	1.364	V
$t_{D-OFF}$	COFF threshold to PGATE falling delay			25		ns
$t_{ON-MIN}$	Minimum ON-time			115	211	ns
$t_{OFF-MAX}$	Maximum OFF-time			300		$\mu\text{s}$
<b>UNDERVOLTAGE LOCKOUT</b>						
$I_{UVLO}$	UVLO pin current	$V_{UVLO} = 1\text{ V}$		10		nA
$V_{UVLO-R}$	Rising UVLO threshold		1.175	1.243	1.311	V
$I_{UVLO-HYS}$	UVLO hysteresis current			22		$\mu\text{A}$
<b>ENABLE</b>						
$I_{EN}$	EN pin current			10		nA
$V_{EN-TH}$	EN pin threshold	$V_{EN}$ rising			1.74	V
		$V_{EN}$ falling	.5			
$V_{EN-HYS}$	EN pin hysteresis			420		mV
$t_{EN-R}$	EN pin rising delay	EN rise - PGATE fall		42		ns
$t_{EN-F}$	EN pin falling delay	EN fall - PGATE rise		21		ns

(1) Typical values represent most likely parametric norms at the conditions specified and are not ensured.

(2) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Texas Instrument's Average Outgoing Quality Level (AOQL).

(3) The current sense threshold limits are calculated by averaging the results from the two polarities of the high-side differential amplifier.

## 7.6 Typical Characteristics

$T_A = 25\text{ }^\circ\text{C}$ ,  $V_{IN} = 24\text{ V}$ , and characteristics are identical for LM3409 and LM3409HV unless otherwise specified.

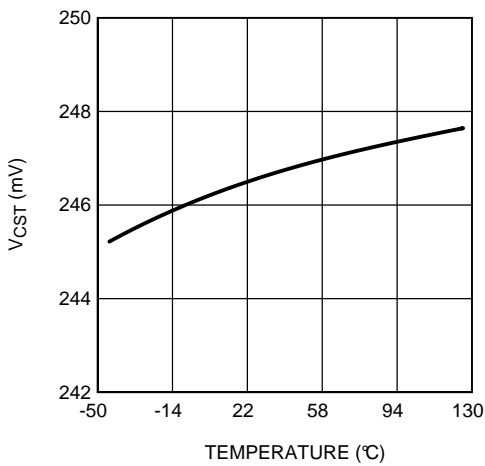


Figure 1.  $V_{cst}$  vs Junction Temperature

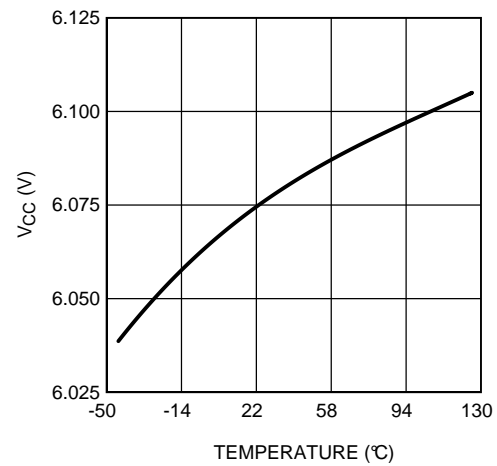


Figure 2.  $V_{cc}$  vs Junction Temperature

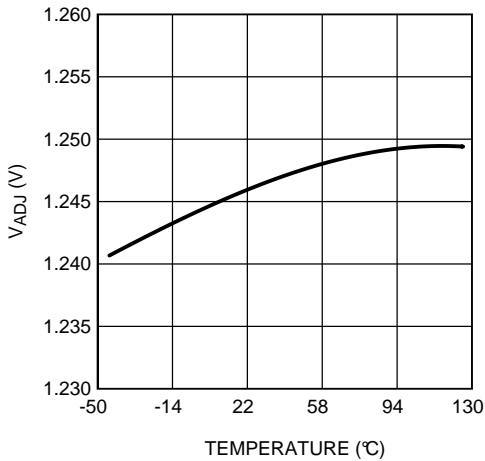


Figure 3.  $V_{adj}$  vs Junction Temperature

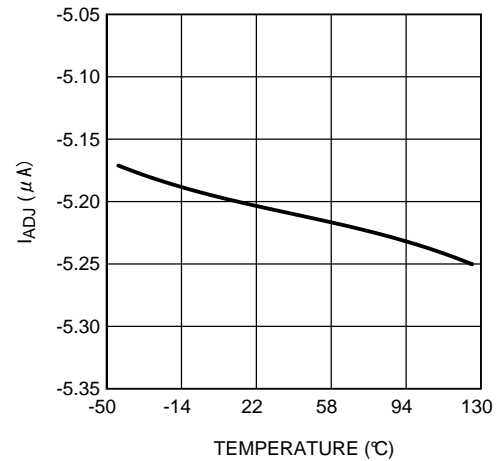


Figure 4.  $I_{adj}$  vs Junction Temperature

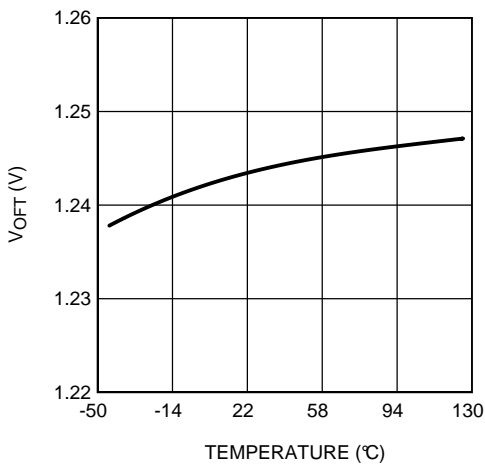


Figure 5.  $V_{oft}$  vs Junction Temperature

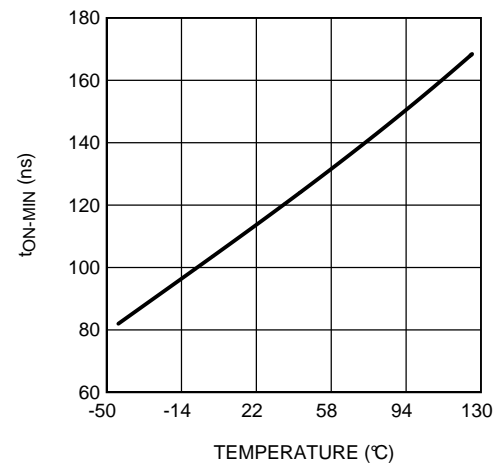


Figure 6.  $t_{on-min}$  vs Junction Temperature

### Typical Characteristics (continued)

$T_A = 25\text{ }^\circ\text{C}$ ,  $V_{IN} = 24\text{ V}$ , and characteristics are identical for LM3409 and LM3409HV unless otherwise specified.

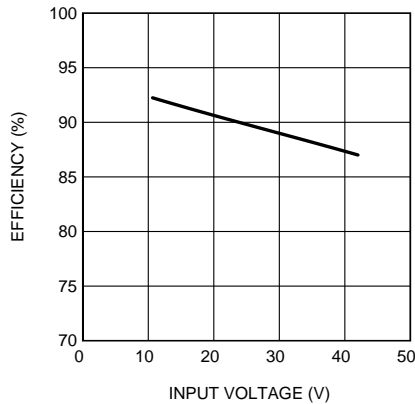


Figure 7. LM3409 Efficiency vs Input Voltage  $V_O = 17\text{ V}$  (5 LEDs);  $I_{LED} = 2\text{ A}$

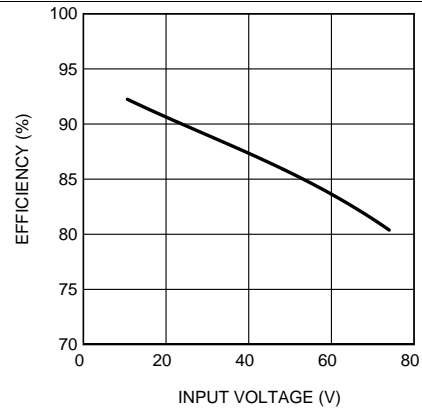


Figure 8. LM3409HV Efficiency vs Input Voltage  $V_O = 17\text{ V}$  (5 LEDs);  $I_{LED} = 2\text{ A}$

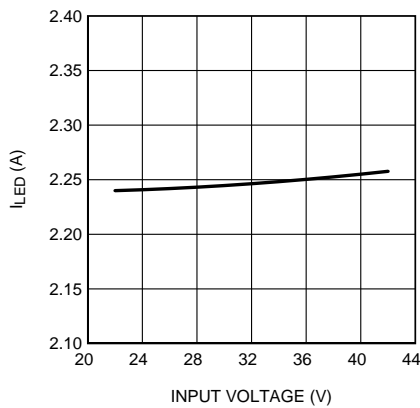


Figure 9. LM3409 LED Current vs Input Voltage  $V_O = 17\text{ V}$  (5 LEDs)

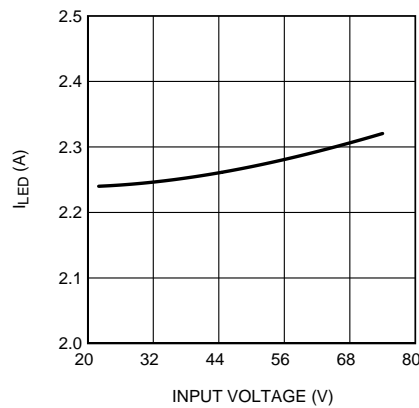


Figure 10. LM3409HV LED Current vs Input Voltage  $V_O = 17\text{ V}$  (5 LEDs)

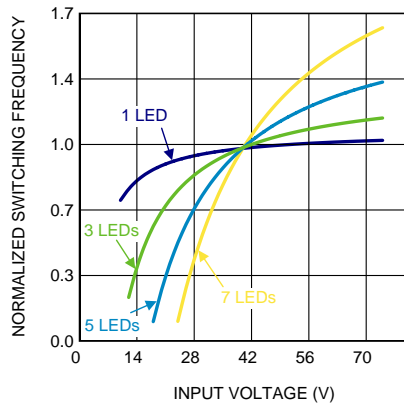


Figure 11. Normalized Switching Frequency vs Input Voltage

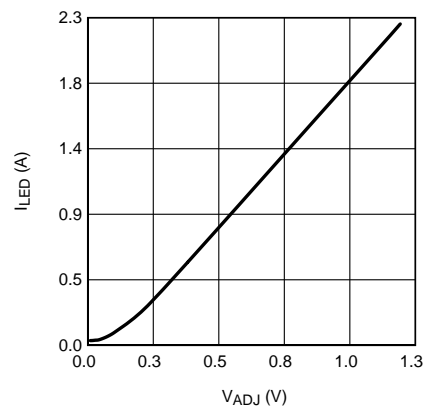


Figure 12. Amplitude Dimming Using IADJ Pin  $V_O = 17\text{ V}$  (5 LEDs);  $V_{IN} = 24\text{ V}$



Typical Characteristics (continued)

$T_A = 25\text{ }^\circ\text{C}$ ,  $V_{IN} = 24\text{ V}$ , and characteristics are identical for LM3409 and LM3409HV unless otherwise specified.

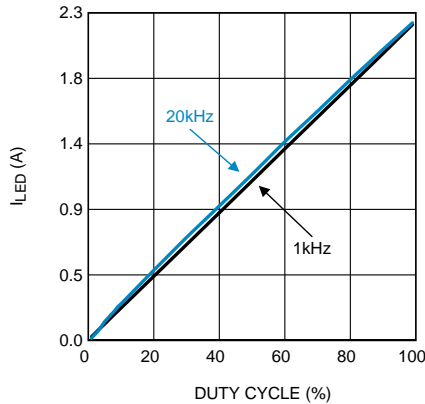


Figure 13. Internal EN Pin PWM Dimming  $V_O = 17\text{ V}$  (5 LEDs);  $V_{IN} = 24\text{ V}$

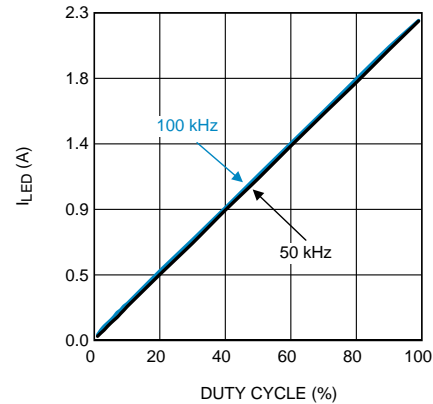
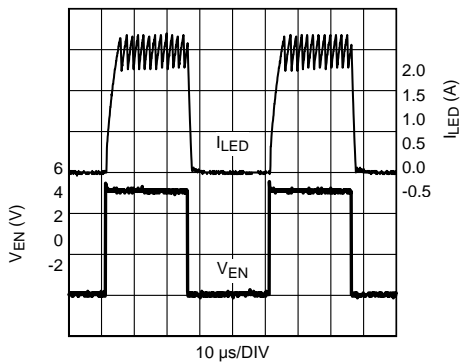
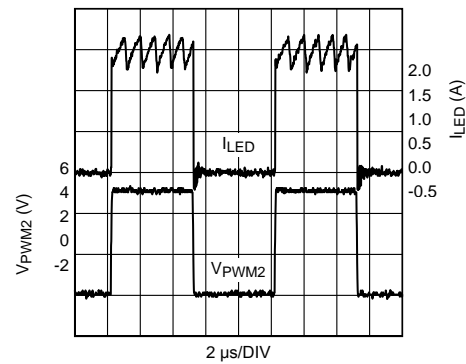


Figure 14. External Parallel FET PWM Dimming  $V_O = 17\text{ V}$  (5 LEDs);  $V_{IN} = 24\text{ V}$



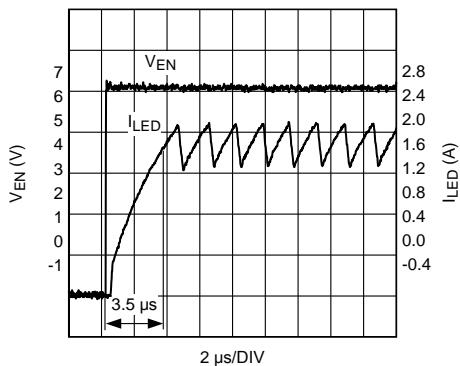
NOTE: The waveforms were acquired using the standard evaluation board from AN-1953 (SNVA390).

Figure 15. 20 kHz 50% EN Pin PWM Dimming  $V_O = 42\text{ V}$  (12 LEDs);  $V_{IN} = 48\text{ V}$



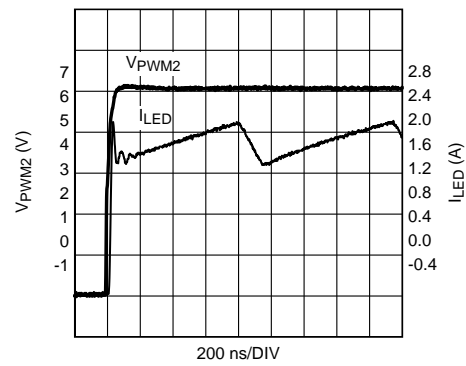
NOTE: The waveforms were acquired using the standard evaluation board from AN-1953 (SNVA390).

Figure 16. 100 kHz 50% External FET PWM Dimming  $V_O = 42\text{ V}$  (12 LEDs);  $V_{IN} = 48\text{ V}$



NOTE: The waveforms were acquired using the standard evaluation board from AN-1953 (SNVA390).

Figure 17. 20 kHz 50% EN Pin PWM Dimming (Rising Edge)  $V_O = 42\text{ V}$  (12 LEDs);  $V_{IN} = 48\text{ V}$



The waveforms were acquired using the standard evaluation board from AN-1953 (SNVA390).

Figure 18. 100 kHz 50% External FET PWM Dimming (Rising Edge)  $V_O = 42\text{ V}$  (12 LEDs);  $V_{IN} = 48\text{ V}$

## 8 Detailed Description

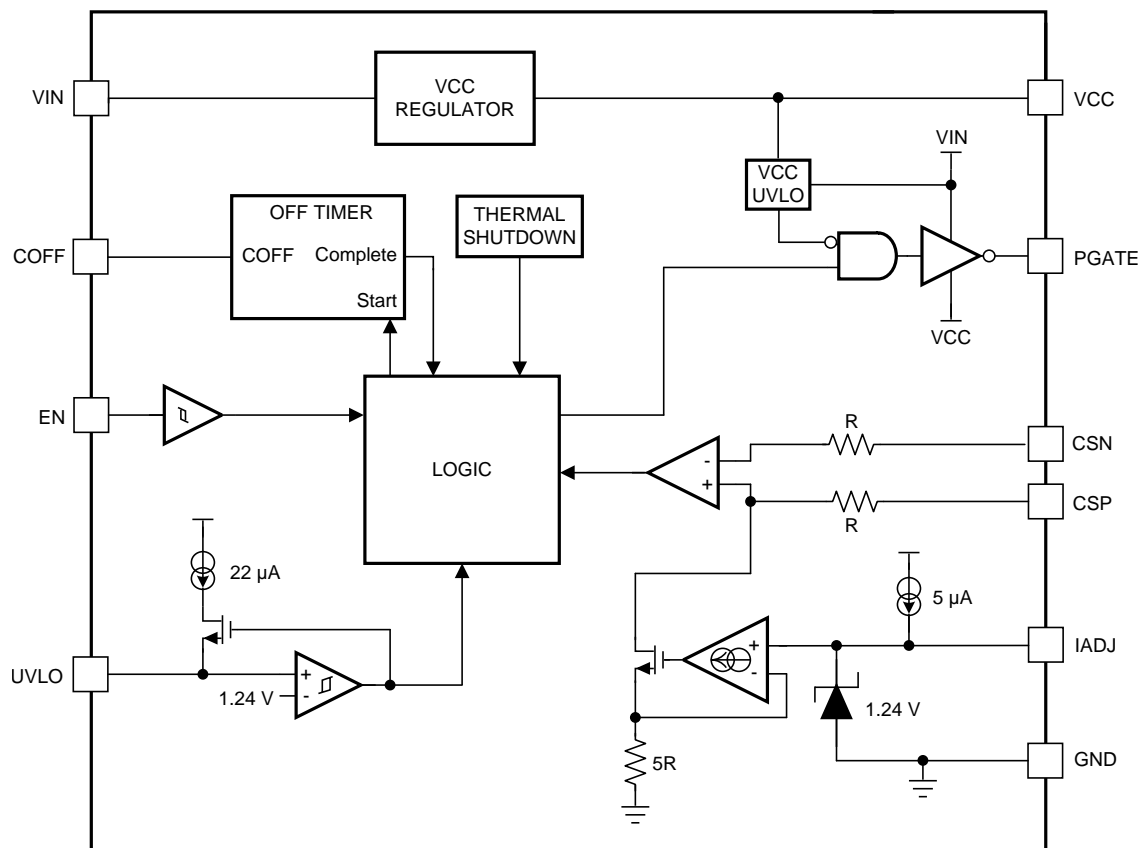
### 8.1 Overview

The LM3409/09HV are P-channel MOSFET (PFET) controllers for step-down (buck) current regulators which are ideal for driving LED loads. They have wide input voltage range allowing for regulation of a variety of LED loads. The high-side differential current sense, with low adjustable threshold voltage, provides an excellent method for regulating output current while maintaining high system efficiency.

The LM3409/09HV uses a Controlled Off-Time (COFT) architecture that allows the converter to be operated in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) with no external control loop compensation, while providing an inherent cycle-by-cycle current limit. The adjustable current sense threshold provides the capability to amplitude (analog) dim the LED current over the full range and the fast output enable/disable function allows for high frequency PWM dimming using no external components.

When designing, the maximum attainable LED current is not internally limited because the LM3409/09HV is a controller. Instead it is a function of the system operating point, component choices, and switching frequency allowing the LM3409/09HV to easily provide constant currents up to 5A. This simple controller contains all the features necessary to implement a high-efficiency versatile LED driver.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Buck Current Regulators

The buck regulator is unique among non-isolated topologies due to the direct connection of the inductor to the load during the entire switching cycle. An inductor will control the rate of change of current that flows through it, therefore a direct connection to the load is excellent for current regulation. A buck current regulator, using the LM3409/09HV, is shown in the [Application and Implementation](#) section. During the time that the PFET (Q1) is turned on ( $t_{ON}$ ), the input voltage charges up the inductor (L1). When Q1 is turned off ( $t_{OFF}$ ), the re-circulating diode (D1) becomes forward biased and L1 discharges. During both intervals, the current is supplied to the load keeping the LEDs forward biased. [Figure 19](#) shows the inductor current ( $i_L(t)$ ) waveform for a buck converter operating in CCM.

The average inductor current ( $I_L$ ) is equal to the average output LED current ( $I_{LED}$ ), therefore if  $I_L$  is tightly controlled,  $I_{LED}$  will be well regulated. As the system changes input voltage or output voltage, duty cycle (D) is varied to regulate  $I_L$  and ultimately  $I_{LED}$ . For any buck regulator, D is simply the conversion ratio divided by the efficiency ( $\eta$ ):

$$D = \frac{V_O}{\eta \times V_{IN}} \quad (1)$$

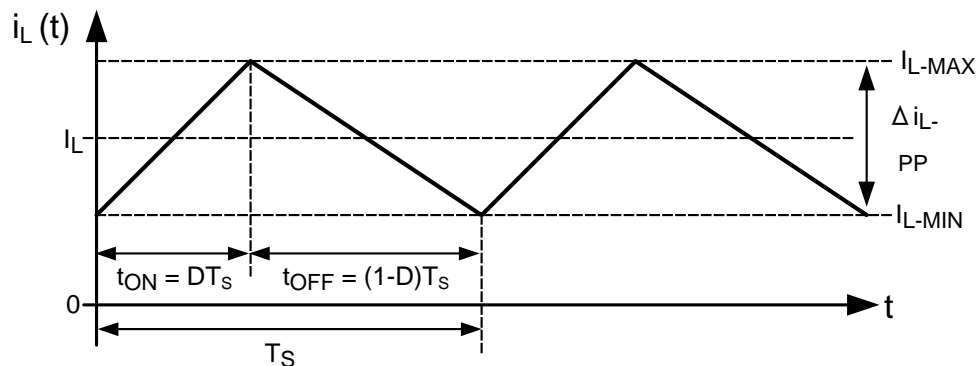


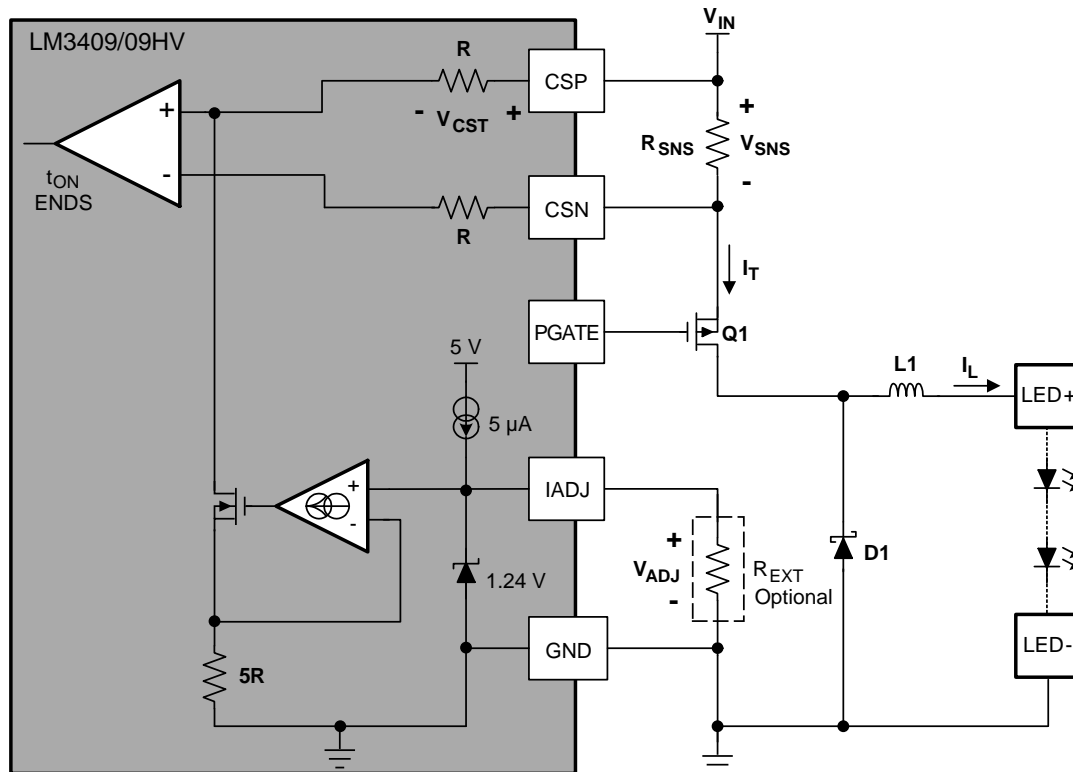
Figure 19. Ideal CCM Buck Converter Inductor Current  $i_L(t)$

### 8.3.2 Controlled Off-Time (COFT) Architecture

The COFT architecture is used by the LM3409/09HV to control  $I_{LED}$ . It is a combination of peak current detection and a one-shot off-timer that varies with output voltage. D is indirectly controlled by changes in both  $t_{OFF}$  and  $t_{ON}$ , which vary depending on the operating point. This creates a variable switching frequency over the entire operating range. This type of hysteretic control eliminates the need for control loop compensation necessary in many switching regulators, simplifying the design process and providing fast transient response.

#### 8.3.2.1 Adjustable Peak Current Control

At the beginning of a switching period, PFET Q1 is turned on and inductor current increases. Once peak current is detected, Q1 is turned off, the diode D1 forward biases, and inductor current decreases. [Figure 20](#) shows how peak current detection is accomplished using the differential voltage signal created as current flows through the current setting resistor ( $R_{SNS}$ ). The voltage across  $R_{SNS}$  ( $V_{SNS}$ ) is compared to the adjustable current sense threshold ( $V_{CST}$ ) and Q1 is turned off when  $V_{SNS}$  exceeds  $V_{CST}$ , providing that  $t_{ON}$  is greater than the minimum possible  $t_{ON}$  (typically 115ns).

**Feature Description (continued)**

**Figure 20. Peak Current Control Circuit**

There are three different methods to set the current sense threshold ( $V_{CST}$ ) using the multi-function IADJ pin:

1. IADJ pin left open:  $5\ \mu\text{A}$  internal current source biases the Zener diode and clamps the IADJ pin voltage ( $V_{ADJ}$ ) at 1.24 V causing the maximum threshold voltage:

$$V_{CST} = \frac{V_{ADJ}}{5 \times R} \times R = \frac{V_{ADJ}}{5} = \frac{1.24\text{V}}{5} = 248\ \text{mV} \quad (2)$$

2. External voltage ( $V_{ADJ}$ ) of 0 V to 1.24 V: Apply to the IADJ pin to adjust  $V_{CST}$  from 0V to 248mV. If the  $V_{ADJ}$  voltage is adjustable, analog dimming can be achieved.
3. External resistor ( $R_{EXT}$ ) placed from IADJ pin to ground:  $5\ \mu\text{A}$  current source sets the  $V_{ADJ}$  voltage and corresponding threshold voltage:

$$V_{CST} = \frac{V_{ADJ}}{5} = \frac{5\ \mu\text{A} \times R_{EXT}}{5} = 1\ \mu\text{A} \times R_{EXT} \quad (3)$$

**8.3.2.2 Controlled Off-Time**

Once Q1 is turned off, it remains off for a constant time ( $t_{OFF}$ ) which is preset by an external resistor ( $R_{OFF}$ ), an external capacitor ( $C_{OFF}$ ), and the output voltage ( $V_O$ ) as shown in [Figure 21](#). Because  $I_{LED}$  is tightly regulated,  $V_O$  will remain nearly constant over widely varying input voltage and temperature yielding a nearly constant  $t_{OFF}$ .

Feature Description (continued)

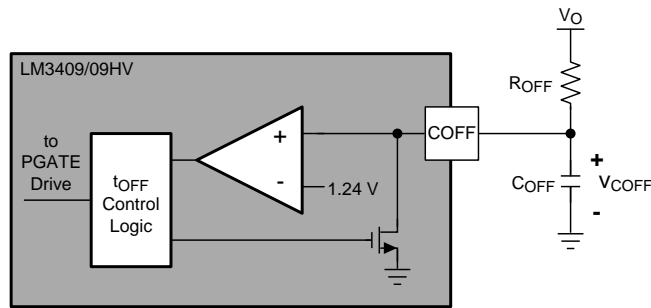


Figure 21. Off-Time Control Circuit

At the start of  $t_{OFF}$ , the voltage across  $C_{OFF}$  ( $v_{COFF}(t)$ ) is zero and the capacitor begins charging according to the time constant provided by  $R_{OFF}$  and  $C_{OFF}$ . When  $v_{COFF}(t)$  reaches the off-time threshold ( $V_{OFT} = 1.24\text{ V}$ ), then the off-time is terminated and  $v_{COFF}(t)$  is reset to zero.  $t_{OFF}$  is calculated as follows:

$$t_{OFF} = -R_{OFF} \times (C_{OFF} + 20\text{ pF}) \times \ln\left(1 - \frac{1.24\text{ V}}{V_O}\right) \quad (4)$$

In reality, there is typically 20 pF parasitic capacitance at the off-timer pin in parallel with  $C_{OFF}$ , which is accounted for in the calculation of  $t_{OFF}$ . Also, it should be noted that the  $t_{OFF}$  equation has a preceding negative sign because the result of the logarithm should be negative for a properly designed circuit. The resulting  $t_{OFF}$  is a positive value as long as  $V_O > 1.24\text{ V}$ . If  $V_O < 1.24\text{ V}$ , the off-timer cannot reach  $V_{OFT}$  and an internally limited maximum off-time (typically 300  $\mu\text{s}$ ) will occur.

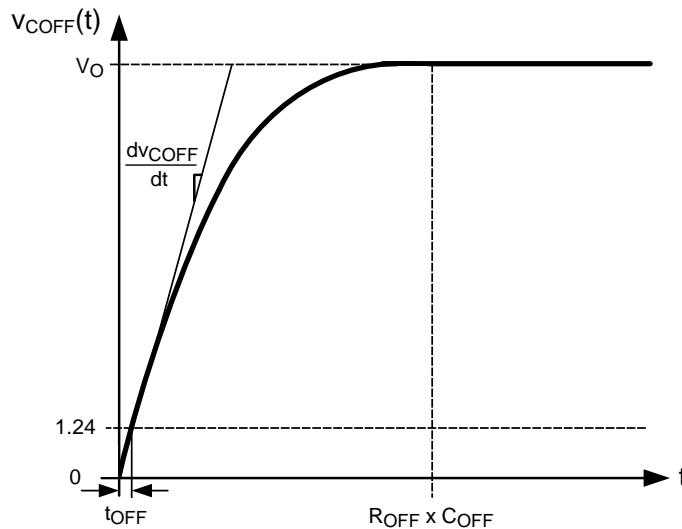


Figure 22. Exponential Charging Function  $v_{COFF}(t)$

Although the  $t_{OFF}$  equation is non-linear,  $t_{OFF}$  is actually very linear in most applications. Ignoring the 20-pF parasitic capacitance at the  $C_{OFF}$  pin,  $v_{COFF}(t)$  is plotted in Figure 22. The time derivative of  $v_{COFF}(t)$  can be calculated to find a linear approximation to the  $t_{OFF}$  equation:

$$\frac{dv_{COFF}(t)}{dt} = \frac{V_O}{R_{OFF} \times C_{OFF}} e^{-\left(\frac{t_{OFF}}{R_{OFF} \times C_{OFF}}\right)} \quad (5)$$

When  $t_{OFF} \ll R_{OFF} \times C_{OFF}$  (equivalent to when  $V_O \gg 1.24\text{ V}$ ), the slope of the function is essentially linear and  $t_{OFF}$  can be approximated as a current source charging  $C_{OFF}$ :

**Feature Description (continued)**

$$t_{OFF} \approx \frac{1.24V \times R_{OFF} \times C_{OFF}}{V_O} \quad (6)$$

Using the actual  $t_{OFF}$  equation, the inductor current ripple ( $\Delta i_{L-PP}$ ) of a buck current regulator operating in CCM is:

$$\Delta i_{L-PP} = \frac{-V_O \times R_{OFF} \times (C_{OFF} + 20 \text{ pF}) \times \ln\left(1 - \frac{1.24V}{V_O}\right)}{L1} \quad (7)$$

Using the  $t_{OFF}$  approximation, the equation is reduced to:

$$\Delta i_{L-PP} \approx \frac{1.24 \times R_{OFF} \times C_{OFF}}{L1} \quad (8)$$

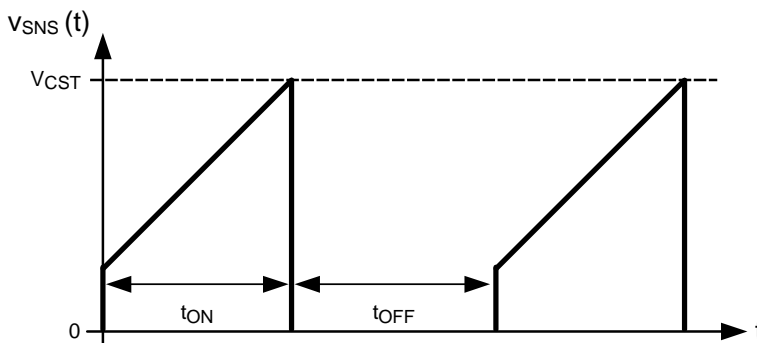
**NOTE**

$\Delta i_{L-PP}$  is independent of both  $V_{IN}$  and  $V_O$  when in CCM.

The  $\Delta i_{L-PP}$  approximation only depends on  $R_{OFF}$ ,  $C_{OFF}$ , and  $L1$ , therefore the ripple is essentially constant over the operating range as long as  $V_O \gg 1.24V$  (when the  $t_{OFF}$  approximation is valid). An exception to the  $t_{OFF}$  approximation occurs if the IADJ pin is used to analog dim. As the LED/inductor current decreases, the converter will eventually enter DCM and the ripple will decrease with the peak current threshold. The approximation shows how the LM3409/09HV achieves constant ripple over a wide operating range, however  $t_{OFF}$  should be calculated using the actual equation first presented.

**8.3.3 Average LED Current**

For a buck converter, the average LED current is simply the average inductor current.



**Figure 23. Sense Voltage  $v_{SNS}(t)$**

Using the COFT architecture, the peak transistor current ( $I_{T-MAX}$ ) is sensed as shown in [Figure 23](#), which is equal to the peak inductor current ( $I_{L-MAX}$ ) given by the following equation:

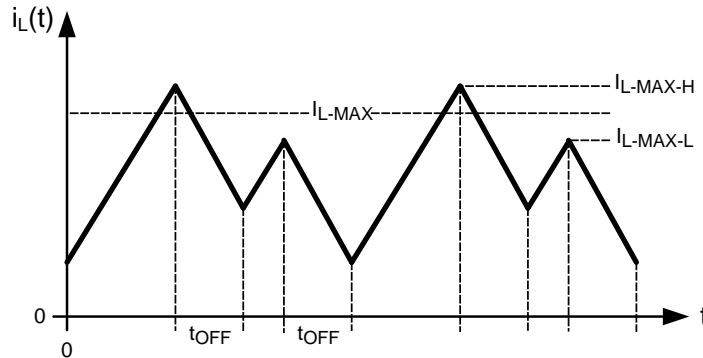
$$I_{L-MAX} = I_{T-MAX} = \frac{V_{CST}}{R_{SNS}} = \frac{V_{ADJ}}{5 \times R_{SNS}} \quad (9)$$

Because  $I_{L-MAX}$  is set using peak current control and  $\Delta i_{L-PP}$  is set using the controlled off-timer,  $I_L$  and correspondingly  $I_{LED}$  can be calculated as follows:

$$I_{LED} = I_L = I_{L-MAX} - \frac{\Delta i_{L-PP}}{2} = \frac{V_{ADJ}}{5 \times R_{SNS}} - \frac{V_O \times t_{OFF}}{2 \times L1} \quad (10)$$

## Feature Description (continued)

The threshold voltage  $V_{CST}$  seen by the high-side sense comparator is affected by the comparator's input offset voltage, which causes an error in the calculation of  $I_{L-MAX}$  and ultimately  $I_{LED}$ . To mitigate this problem, the polarity of the comparator inputs is swapped every cycle, which causes the actual  $I_{L-MAX}$  to alternate between two peak values ( $I_{L-MAXH}$  and  $I_{L-MAXL}$ ), equidistant from the theoretical  $I_{L-MAX}$  as shown in Figure 24.  $I_{LED}$  remains accurate through this averaging.



**Figure 24. Inductor Current  $i_L(t)$  Showing  $I_{L-MAX}$  Offset**

### 8.3.4 Inductor Current Ripple

Because the LM3409/09HV swaps the polarity of the differential current sense comparator every cycle, a minimum inductor current ripple ( $\Delta i_{L-PP}$ ) is necessary to maintain accurate  $I_{LED}$  regulation. Referring to Figure 24, the first  $t_{ON}$  is terminated at the higher of the two polarity-swapped thresholds (corresponding to  $I_{L-MAXH}$ ). During the following  $t_{OFF}$ ,  $i_L$  decreases until the second  $t_{ON}$  begins. If  $t_{OFF}$  is too short, then as the second  $t_{ON}$  begins,  $i_L$  will still be above the lower peak current threshold (corresponding to  $I_{L-MAXL}$ ) and a minimum  $t_{ON}$  pulse will follow. This will result in degraded  $I_{LED}$  regulation. The minimum inductor current ripple ( $\Delta i_{L-PP-MIN}$ ) should adhere to the following equation to ensure accurate  $I_{LED}$  regulation:

$$\Delta i_{L-PP-MIN} > \frac{24 \text{ mV}}{R_{SNS}} \quad (11)$$

### 8.3.5 Switching Frequency

The switching frequency is dependent upon the actual operating point ( $V_{IN}$  and  $V_O$ ).  $V_O$  will remain relatively constant for a given application, therefore the switching frequency will vary with  $V_{IN}$  (frequency increases as  $V_{IN}$  increases). The target switching frequency ( $f_{SW}$ ) at the nominal operating point is selected based on the tradeoffs between efficiency (better at low frequency) and solution size/cost (smaller at high frequency). The off-time of the LM3409/09HV can be programmed for switching frequencies up to 5 MHz (theoretical limit imposed by minimum  $t_{ON}$ ). In practice, switching frequencies higher than 1MHz may be difficult to obtain due to gate drive limitations, high input voltage, and thermal considerations.

At CCM operating points,  $f_{SW}$  is defined as:

$$f_{SW} = \frac{1-D}{t_{OFF}} = \frac{1 - \left( \frac{V_O}{\eta \times V_{IN}} \right)}{t_{OFF}} \quad (12)$$

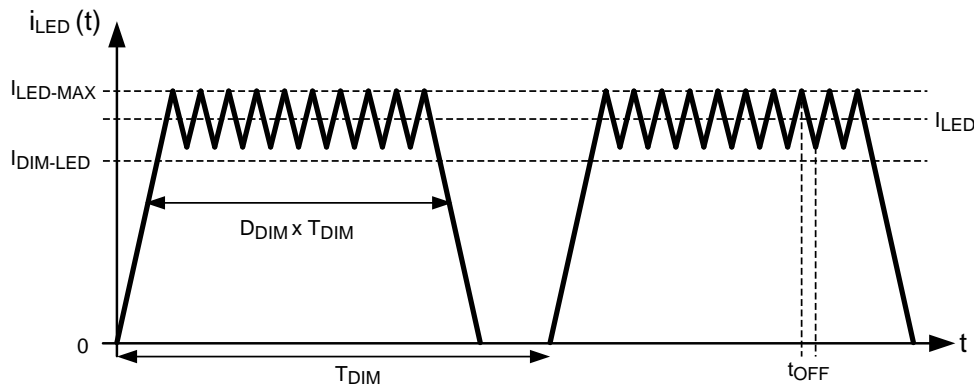
At DCM operating points,  $f_{SW}$  is defined as:

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}} = \frac{1}{\left( \frac{I_{L-MAX} \times L_1}{V_{IN} - V_O} \right) + t_{OFF}} \quad (13)$$

## Feature Description (continued)

In the CCM equation, it is apparent that the efficiency ( $\eta$ ) factors into the switching frequency calculation. Efficiency is hard to estimate and, because switching frequency varies with input voltage, accuracy in setting the nominal switching frequency is not critical. Therefore, a general rule of thumb for the LM3409/09HV is to assume an efficiency between 85% and 100%. When approximating efficiency to target a nominal switching frequency, the following condition must be met:

$$\eta > \frac{V_O}{V_{IN}} \quad (14)$$



**Figure 25. LED Current  $i_{LED}(t)$  During EN Pin PWM Dimming**

### 8.3.6 PWM Dimming Using the EN Pin

The enable pin (EN) is a TTL compatible input for PWM dimming of the LED. A logic low (below 0.5V) at EN will disable the internal driver and shut off the current flow to the LED array. While the EN pin is in a logic low state the support circuitry (driver, bandgap,  $V_{CC}$  regulator) remains active to minimize the time needed to turn the LED array back on when the EN pin sees a logic high (above 1.74 V).

Figure 25 shows the LED current ( $i_{LED}(t)$ ) during PWM dimming where duty cycle ( $D_{DIM}$ ) is the percentage of the dimming period ( $T_{DIM}$ ) that the PFET is switching. For the remainder of  $T_{DIM}$ , the PFET is disabled. The resulting dimmed average LED current ( $I_{DIM-LED}$ ) is:

$$I_{DIM-LED} = D_{DIM} \times I_{LED} \quad (15)$$

The LED current rise and fall times (which are limited by the slew rate of the inductor as well as the delay from activation of the EN pin to the response of the external PFET) limit the achievable  $T_{DIM}$  and  $D_{DIM}$ . In general, dimming frequency should be at least one order of magnitude lower than the steady state switching frequency to prevent aliasing. However, for good linear response across the entire dimming range, the dimming frequency may need to be even lower.

### 8.3.7 High Voltage Negative BIAS Regulator

The LM3409/09HV contains an internal linear regulator where the steady state VCC pin voltage is typically 6.2 V below the voltage at the VIN pin. The VCC pin should be bypassed to the VIN pin with at least 1 $\mu$ F of ceramic capacitance connected as close as possible to the IC.



## Feature Description (continued)

### 8.3.8 External Parallel FET PWM Dimming

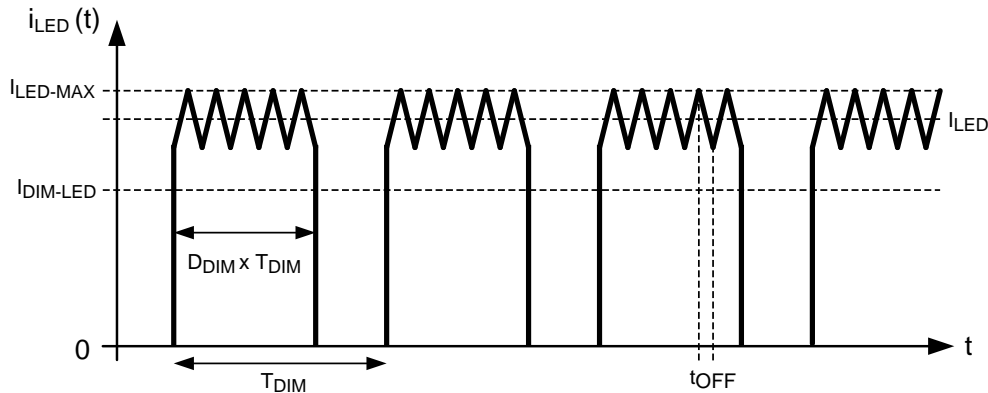


Figure 26. Ideal LED Current  $i_{LED}(t)$  During Parallel FET Dimming

Any buck topology LED driver is a good candidate for parallel FET dimming because high slew rates are achievable, due to the fact that no output capacitance is required. This allows for much higher dimming frequencies than are achievable using the EN pin. When using external parallel FET dimming, a situation can arise where maximum off-time occurs due to a shorted output. To mitigate this situation, a secondary voltage ( $V_{DD}$ ) should be used as shown in Figure 27.

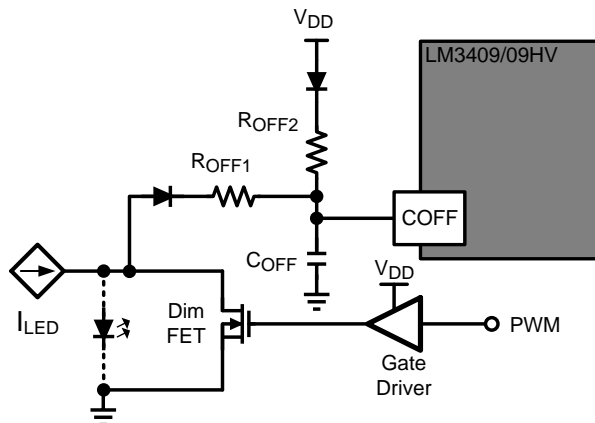


Figure 27. External Parallel FET Dimming Circuit

A small diode is connected in series with the off time resistor calculated for nominal operation from the output,  $R_{OFF1}$ . Then connect a small diode from the secondary voltage along with another resistor,  $R_{OFF2}$ . The secondary voltage can be any voltage as long as it is greater than 2V. The value of  $R_{OFF2}$  can be calculated using Equation 16.

$$R_{OFF2} = \frac{R_{OFF1} \times V_{DD}}{I_{LED} \times R_{DS(on)}} \quad (16)$$

The ideal LED current waveform  $i_{LED}(t)$  during parallel FET PWM dimming is very similar to the EN pin PWM dimming shown previously. The LED current does not rise and fall infinitely fast as shown in Figure 26 however with this method, only the speed of the parallel Dim FET ultimately limits the dimming frequency and dimming duty cycle. This allows for much faster PWM dimming than can be attained with the EN pin.

## 8.4 Device Functional Modes

### 8.4.1 Low-Power Shutdown

The LM3409/09HV can be placed into a low-power shutdown (typically 110  $\mu$ A) by grounding the EN terminal (any voltage below 0.5 V) until  $V_{CC}$  drops below the  $V_{CC}$  UVLO threshold (typically 3.73 V). During normal operation this terminal should be tied to a voltage above 1.74 V and below absolute maximum input voltage rating.

### 8.4.2 Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. The threshold for thermal shutdown is 160°C with 15°C of hysteresis (both values typical). During thermal shutdown the PFET and driver are disabled.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.1.1 Input Undervoltage Lockout (UVLO)

Undervoltage lockout is set with a resistor divider from  $V_{IN}$  to GND and is compared against a 1.24V threshold as shown in Figure 28. Once the input voltage is above the preset UVLO rising threshold (and assuming the part is enabled), the internal circuitry becomes active and a 22 $\mu$ A current source at the UVLO pin is turned on. This extra current provides hysteresis to create a lower UVLO falling threshold. The resistor divider is chosen to set both the UVLO rising and falling thresholds.

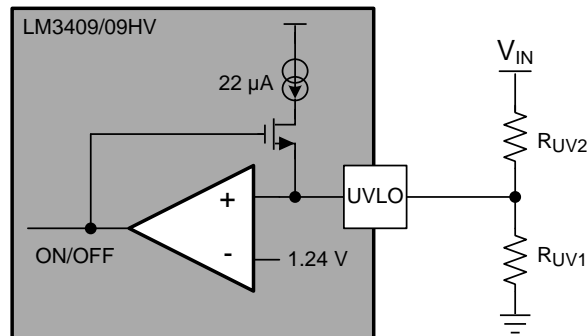


Figure 28. UVLO Circuit

The turn-on threshold ( $V_{TURN-ON}$ ) is defined as follows:

$$V_{TURN-ON} = \frac{1.24V \times (R_{UV1} + R_{UV2})}{R_{UV1}} \quad (17)$$

The hysteresis ( $V_{HYS}$ ) is defined as follows:

$$V_{HYS} = R_{UV2} \times 22\mu A \quad (18)$$

#### 9.1.2 Operation Near Dropout

Because the power MOSFET is a PFET, the LM3409/09HV can be operated into dropout which occurs when the input voltage is approximately equal to output voltage. Once the input voltage drops below the nominal output voltage, the switch remains constantly on ( $D=1$ ) causing the output voltage to decrease with the input voltage. In normal operation, the average LED current is regulated to the peak current threshold minus half of the ripple. As the converter goes into dropout, the LED current is exactly at the peak current threshold because it is no longer switching. This causes the LED current to increase by half of the set ripple current as it makes the transition into dropout. Therefore, the inductor current ripple should be kept as small as possible (while remaining above the previously established minimum) and output capacitance should be added to help maintain good line regulation when approaching dropout.

## Application Information (continued)

### 9.1.3 LED Ripple Current

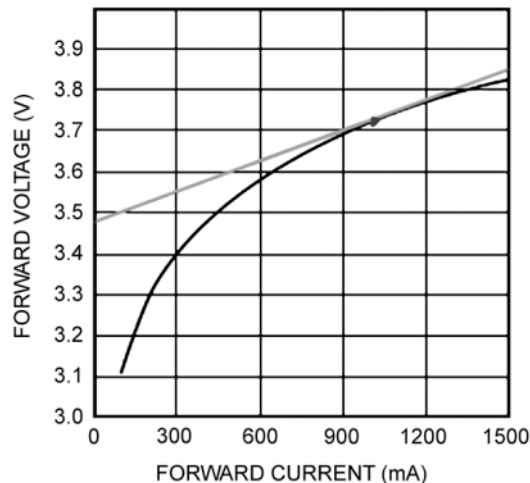
Selection of the ripple current through the LED array is analogous to the selection of output ripple voltage in a standard voltage regulator. Where the output voltage ripple in a voltage regulator is commonly  $\pm 1\%$  to  $\pm 5\%$  of the DC output voltage, LED manufacturers generally recommend values for  $\Delta i_{LED-PP}$  ranging from  $\pm 5\%$  to  $\pm 20\%$  of  $I_{LED}$ . For a nominal system operating point, a larger  $\Delta i_{LED-PP}$  specification can reduce the necessary inductor size and/or allow for smaller output capacitors (or no output capacitors at all) which helps to minimize the total solution size and cost. On the other hand, a smaller  $\Delta i_{LED-PP}$  specification would require more output inductance, a higher switching frequency, or additional output capacitance.

### 9.1.4 Buck Converters without Output Capacitors

Because current is being regulated, not voltage, a buck current regulator is free of load current transients, therefore output capacitance is not needed to supply the load and maintain output voltage. This is very helpful when high frequency PWM dimming the LED load. When no output capacitor is used, the same design equations that govern  $\Delta i_{L-PP}$  also apply to  $\Delta i_{LED-PP}$ .

### 9.1.5 Buck Converters With Output Capacitors

A capacitor placed in parallel with the LED load can be used to reduce  $\Delta i_{LED-PP}$  while keeping the same average current through both the inductor and the LED array. With an output capacitor, the inductance can be lowered, making the magnetics smaller and less expensive. Alternatively, the circuit can be run at lower frequency with the same inductor value, improving the efficiency and increasing the maximum allowable average output voltage. A parallel output capacitor is also useful in applications where the inductor or input voltage tolerance is poor. Adding a capacitor that reduces  $\Delta i_{LED-PP}$  to well below the target provides headroom for changes in inductance or  $V_{IN}$  that might otherwise push the maximum  $\Delta i_{LED-PP}$  too high.



**Figure 29. Calculating Dynamic Resistance  $r_D$**

Output capacitance ( $C_O$ ) is determined knowing the desired  $\Delta i_{LED-PP}$  and the LED dynamic resistance ( $r_D$ ).  $r_D$  can be calculated as the slope of the LED's exponential DC characteristic at the nominal operating point as shown in Figure 29. Simply dividing the forward voltage by the forward current at the nominal operating point will give an incorrect value that is 5x to 10x too high. Total dynamic resistance for a string of  $n$  LEDs connected in series can be calculated as the  $r_D$  of one device multiplied by  $n$ . The following equations can then be used to estimate  $\Delta i_{LED-PP}$  when using a parallel capacitor:

$$\Delta i_{LED-PP} = \frac{\Delta i_{L-PP}}{1 + \frac{r_D}{Z_C}} \quad (19)$$

$$Z_C = \frac{1}{2 \times \pi \times f_{SW} \times C_O} \quad (20)$$

## Application Information (continued)

In general,  $Z_C$  should be at least half of  $r_D$  to effectively reduce the ripple. Ceramic capacitors are the best choice for the output capacitors due to their high ripple current rating, low ESR, low cost, and small size compared to other types. When selecting a ceramic capacitor, special attention must be paid to the operating conditions of the application. Ceramic capacitors can lose one-half or more of their capacitance at their rated DC voltage bias and also lose capacitance with extremes in temperature. Make sure to check any recommended de-ratings and also verify if there is any significant change in capacitance at the operating voltage and temperature.

### 9.1.6 Output Overvoltage Protection

Because the LM3409/09HV controls a buck current regulator, there is no inherent need to provide output overvoltage protection. If the LED load is opened, the output voltage will only rise as high as the input voltage plus any ringing due to the parasitic inductance and capacitance present at the output node. If a ceramic output capacitor is used in the application, it should have a minimum rating equal to the input voltage. Ringing seen at the output node should not damage most ceramic capacitors, due to their high ripple current rating.

### 9.1.7 Input Capacitors

Input capacitors are selected using requirements for minimum capacitance and RMS ripple current. The PFET current during  $t_{ON}$  is approximately  $I_{LED}$ , therefore the input capacitors discharge the difference between  $I_{LED}$  and the average input current ( $I_{IN}$ ) during  $t_{ON}$ . During  $t_{OFF}$ , the input voltage source charges up the input capacitors with  $I_{IN}$ . The minimum input capacitance ( $C_{IN-MIN}$ ) is selected using the maximum input voltage ripple ( $\Delta V_{IN-MAX}$ ) which can be tolerated.  $\Delta V_{IN-MAX}$  is equal to the change in voltage across  $C_{IN}$  during  $t_{ON}$  when it supplies the load current. A good starting point for selection of  $C_{IN}$  is to use  $\Delta V_{IN-MAX}$  of 2% to 10% of  $V_{IN}$ .  $C_{IN-MIN}$  can be selected as follows:

$$C_{IN-MIN} = \frac{I_{LED} \times t_{ON}}{\Delta V_{IN-MAX}} = \frac{I_{LED} \times \left( \frac{1}{f_{SW}} - t_{OFF} \right)}{\Delta V_{IN-MAX}} \quad (21)$$

An input capacitance at least 75% greater than the calculated  $C_{IN-MIN}$  value is recommended. To determine the RMS input current rating ( $I_{IN-RMS}$ ) the following approximation can be used:

$$I_{IN-RMS} = I_{LED} \times \sqrt{D \times (1 - D)} = I_{LED} \times f_{SW} \times \sqrt{t_{ON} \times t_{OFF}} \quad (22)$$

Because this approximation assumes there is no inductor ripple current, the value should be increased by 10-30% depending on the amount of ripple that is expected. Ceramic capacitors are the best choice for input capacitors for the same reasons mentioned in the [Buck Converters With Output Capacitors](#) section. Careful selection of the capacitor requires checking capacitance ratings at the nominal operating voltage and temperature.

### 9.1.8 P-Channel MOSFET (PFET)

The LM3409/09HV requires an external PFET (Q1) as the main power MOSFET for the switching regulator. Q1 should have a voltage rating at least 15% higher than the maximum input voltage to ensure safe operation during the ringing of the switch node. In practice all switching converters have some ringing at the switch node due to the diode parasitic capacitance and the lead inductance. The PFET should also have a current rating at least 10% higher than the average transistor current ( $I_T$ ):

$$I_T = D \times I_{LED} \quad (23)$$

The power rating is verified by calculating the power loss ( $P_T$ ) using the RMS transistor current ( $I_{T-RMS}$ ) and the PFET on-resistance ( $R_{DS-ON}$ ):

$$I_{T-RMS} = I_{LED} \times \sqrt{D \times \left( 1 + \frac{1}{12} \times \left( \frac{\Delta i_{L-PP}}{I_{LED}} \right)^2 \right)} \quad (24)$$

$$P_T = I_{T-RMS}^2 \times R_{DS-ON} \quad (25)$$

## Application Information (continued)

It is important to consider the gate charge of Q1. As the input voltage increases from a nominal voltage to its maximum input voltage, the COFT architecture will naturally increase the switching frequency. The dominant switching losses are determined by input voltage, switching frequency, and PFET total gate charge ( $Q_g$ ). The LM3409/09HV must provide and remove charge  $Q_g$  from the input capacitance of Q1 to turn it on and off. This occurs more often at higher switching frequencies which requires more current from the internal regulator, thereby increasing internal power dissipation and eventually causing the LM3409/09HV to thermally cycle. For a given range of operating points the only effective way to reduce these switching losses is to minimize  $Q_g$ .

A good rule of thumb is to limit  $Q_g < 30\text{nC}$  (if the switching frequency remains below 300kHz for the entire operating range then a larger  $Q_g$  can be considered). If a PFET with small  $R_{DS-ON}$  and a high voltage rating is required, there may be no choice but to use a PFET with  $Q_g > 30\text{nC}$ .

When using a PFET with  $Q_g > 30\text{nC}$ , the bypass capacitor ( $C_F$ ) should not be connected to the VIN pin. This will ensure that peak current detection through  $R_{SNS}$  is not affected by the charging of the PFET input capacitance during switching, which can cause false triggering of the peak detection comparator. Instead,  $C_F$  should be connected from the VCC pin to the CSN pin which will cause a small DC offset in  $V_{CST}$  and ultimately  $I_{LED}$ , however it avoids the problematic false triggering.

In general, the PFET should be chosen to meet the  $Q_g$  specification whenever possible, while minimizing  $R_{DS-ON}$ . This will minimize power losses while ensuring the part functions correctly over the full operating range.

### 9.1.9 Re-Circulating Diode

A re-circulating diode (D1) is required to carry the inductor current during  $t_{OFF}$ . The most efficient choice for D1 is a Schottky diode due to low forward voltage drop and near-zero reverse recovery time. Similar to Q1, D1 must have a voltage rating at least 15% higher than the maximum input voltage to ensure safe operation during the ringing of the switch node and a current rating at least 10% higher than the average diode current ( $I_D$ ):

$$I_D = (1 - D) \times I_{LED} \quad (26)$$

The power rating is verified by calculating the power loss through the diode. This is accomplished by checking the typical diode forward voltage ( $V_D$ ) from the I-V curve on the product data sheet and calculating as follows:

$$P_D = I_D \times V_D \quad (27)$$

In general, higher current diodes have a lower  $V_D$  and come in better performing packages minimizing both power losses and temperature rise.

## 9.2 Typical Applications

### 9.2.1 EN PIN PWM Dimming Application for 10 LEDs

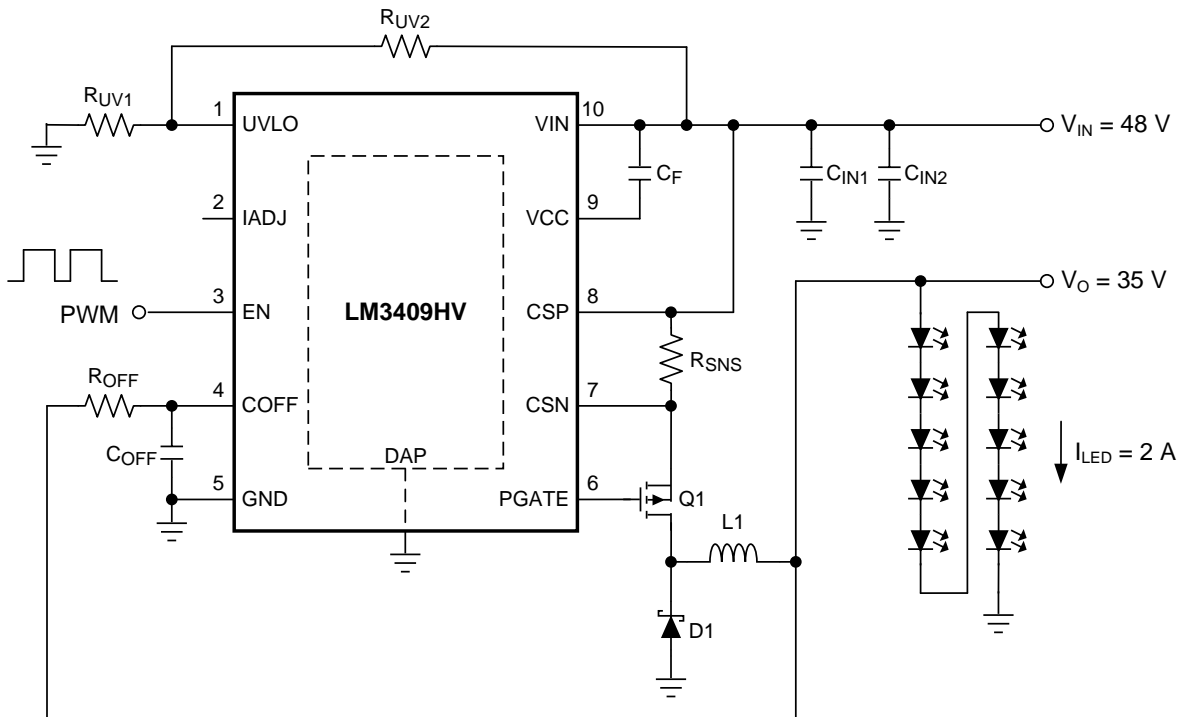


Figure 30. EN PIN PWM Dimming Application for 10 LEDs Schematic

#### 9.2.1.1 Design Requirements

$$f_{SW} = 525 \text{ kHz}$$

$$V_{IN} = 48 \text{ V}; V_{IN-MAX} = 75 \text{ V}$$

$$V_O = 35 \text{ V}$$

$$I_{LED} = 2 \text{ A}$$

$$\Delta i_{LED-PP} = \Delta i_{L-PP} = 1 \text{ A}$$

$$\Delta v_{IN-PP} = 1.44 \text{ V}$$

$$V_{TURN-ON} = 10 \text{ V}; V_{HYS} = 1.1 \text{ V}$$

$$\eta = 0.95$$

#### 9.2.1.2 Detailed Design Procedure

Table 1. Design 1 Bill of Materials

QTY	PART ID	PART VALUE	MANUFACTURER	PART NUMBER
1	LM3409HV/LM3409QHVMY	Buck controller	TI	LM3409HVVMY/LM3409QHVMY
2	C <sub>IN1</sub> , C <sub>IN2</sub>	2 $\mu$ F X7R 10% 100 V	MURATA	GRM43ER72A225KA01L
1	C <sub>F</sub>	1 $\mu$ F X7R 10% 16 V	TDK	C1608X7R1C105K
1	C <sub>OFF</sub>	470 $\mu$ F X7R 10% 50 V	TDK	C1608X7R1H471K
1	Q1	PMOS 100 V 3.8 A	ZETEX	ZXMP10A18KTC
1	D1	Schottky 100 V 3 A	VISHAY	SS3H10-E3/57T
1	L1	15 $\mu$ H 20% 4.2 A	TDK	SLF12565T-150M4R2

**Typical Applications (continued)**
**Table 1. Design 1 Bill of Materials (continued)**

QTY	PART ID	PART VALUE	MANUFACTURER	PART NUMBER
1	R <sub>OFF</sub>	24.9 kΩ 1%	VISHAY	CRCW060324K9FKEA
1	R <sub>UV1</sub>	6.98 kΩ 1%	VISHAY	CRCW06036K98FKEA
1	R <sub>UV2</sub>	49.9 kΩ 1%	VISHAY	CRCW060349K9FKEA
1	R <sub>SNS</sub>	0.1 Ω 1% 1W	VISHAY	WSL2512R1000FEA

**9.2.1.2.1 Nominal Switching Frequency**

 Assume C<sub>OFF</sub> = 470 pF and η = 0.95. Solve for R<sub>OFF</sub>:

$$R_{OFF} = \frac{-\left(1 - \frac{V_o}{\eta \times V_{IN}}\right)}{(C_{OFF} + 20 \text{ pF}) \times f_{SW} \times \ln\left(1 - \frac{1.24V}{V_o}\right)}$$

$$R_{OFF} = \frac{-\left(1 - \frac{35V}{0.95 \times 48V}\right)}{490 \text{ pF} \times 525 \text{ kHz} \times \ln\left(1 - \frac{1.24V}{35V}\right)} = 25.1 \text{ k}\Omega \quad (28)$$

 The closest 1% tolerance resistor is 24.9 kΩ; therefore, the actual t<sub>OFF</sub> and target f<sub>SW</sub> are:

$$t_{OFF} = -(C_{OFF} + 20 \text{ pF}) \times R_{OFF} \times \ln\left(1 - \frac{1.24V}{V_o}\right)$$

$$t_{OFF} = -490 \text{ pF} \times 24.9 \text{ k}\Omega \times \ln\left(1 - \frac{1.24V}{35V}\right) = 440 \text{ ns} \quad (29)$$

$$f_{SW} = \frac{1 - \left(\frac{V_o}{\eta \times V_{IN}}\right)}{t_{OFF}} = \frac{1 - \left(\frac{35V}{0.95 \times 48V}\right)}{440 \text{ ns}} = 528 \text{ kHz} \quad (30)$$

The chosen components from step 1 are:

$$C_{OFF} = 470 \text{ pF}$$

$$R_{OFF} = 24.9 \text{ k}\Omega$$

(31)

**9.2.1.2.2 Inductor Ripple Current**

Solve for L1:

$$L1 = \frac{V_o \times t_{OFF}}{\Delta i_{L-PP}} = \frac{35V \times 440 \text{ ns}}{1A} = 15.4 \mu\text{H} \quad (32)$$

 The closest standard inductor value is 15 μH therefore the actual Δi<sub>L-PP</sub> is:

$$\Delta i_{L-PP} = \frac{V_o \times t_{OFF}}{L1} = \frac{35V \times 440 \text{ ns}}{15 \mu\text{H}} = 1.027A \quad (33)$$

The chosen component from step 2 is:

$$L1 = 15 \mu\text{H}$$

(34)



### 9.2.1.2.3 Average LED Current

Determine  $I_{L-MAX}$ :

$$I_{L-MAX} = I_{LED} + \frac{\Delta i_{L-PP}}{2} = 2A + \frac{1.027A}{2} = 2.51A \quad (35)$$

Assume  $V_{ADJ} = 1.24V$  and solve for  $R_{SNS}$ :

$$R_{SNS} = \frac{V_{ADJ}}{5 \times I_{L-MAX}} = \frac{1.24V}{5 \times 2.51A} = 0.099\Omega \quad (36)$$

The closest 1% tolerance resistor is 0.1  $\Omega$  therefore the  $I_{LED}$  is:

$$I_{LED} = \frac{V_{ADJ}}{5 \times R_{SNS}} - \frac{\Delta i_{L-PP}}{2}$$

$$I_{LED} = \frac{1.24V}{5 \times 0.099\Omega} - \frac{1.027A}{2} = 1.97A \quad (37)$$

The chosen component from step 3 is:

$$\boxed{R_{SNS} = 0.1\Omega} \quad (38)$$

### 9.2.1.2.4 Output Capacitance

No output capacitance is necessary.

### 9.2.1.2.5 Input Capacitance

Determine  $t_{ON}$ :

$$t_{ON} = \frac{1}{f_{SW}} - t_{OFF} = \frac{1}{528 \text{ kHz}} - 440 \text{ ns} = 1.45\mu\text{s} \quad (39)$$

Solve for  $C_{IN-MIN}$ :

$$C_{IN-MIN} = \frac{I_{LED} \times t_{ON}}{\Delta V_{IN-PP}} = \frac{1.97A \times 1.45\mu\text{s}}{1.44V} = 1.98\mu\text{F} \quad (40)$$

Choose  $C_{IN}$ :

$$C_{IN} = C_{IN-MIN} \times 2 = 3.96\mu\text{F} \quad (41)$$

Determine  $I_{IN-RMS}$ :

$$I_{IN-RMS} = I_{LED} \times f_{SW} \times \sqrt{t_{ON} \times t_{OFF}}$$

$$I_{IN-RMS} = 1.97A \times 528 \text{ kHz} \times \sqrt{1.45\mu\text{s} \times 440 \text{ ns}} = 831 \text{ mA} \quad (42)$$

The chosen components from step 5 are:

$$\boxed{C_{IN1} = C_{IN2} = 2.2\mu\text{F}} \quad (43)$$

### 9.2.1.2.6 PFET

Determine minimum Q1 voltage rating and current rating:

$$V_{T-MAX} = V_{IN-MAX} = 75V \quad (44)$$

$$I_T = D \times I_{LED} = \frac{V_O \times I_{LED}}{V_{IN} \times \eta} = \frac{35V \times 1.97A}{48V \times 0.95} = 1.51A \quad (45)$$

A 100 V, 3.8 A PFET is chosen with  $R_{DS-ON} = 19 \text{ m}\Omega$  and  $Q_g = 20 \text{ nC}$ . Determine  $I_{T-RMS}$  and  $P_T$ :

$$I_{T-RMS} = I_{LED} \times \sqrt{D \times \left( 1 + \frac{1}{12} \times \left( \frac{\Delta i_{L-PP}}{I_{LED}} \right)^2 \right)}$$

$$I_{T-RMS} = 1.97A \times \sqrt{\frac{35V}{48V \times 0.95} \times \left( 1 + \frac{1}{12} \times \left( \frac{1.027A}{1.97A} \right)^2 \right)}$$

$$I_{T-RMS} = 1.74A \tag{46}$$

$$P_T = I_{T-RMS}^2 \times R_{DS(ON)} = 1.74A^2 \times 190\text{ m}\Omega = 577\text{ mW} \tag{47}$$

The chosen component from step 6 is:

$$\boxed{Q1 \rightarrow 3.8A, 100V, DPAK} \tag{48}$$

### 9.2.1.2.7 Diode

Determine minimum D1 voltage rating and current rating:

$$V_{D-MAX} = V_{IN-MAX} = 75V \tag{49}$$

$$I_D = (1-D) \times I_{LED} = \left( 1 - \frac{V_O}{V_{IN} \times \eta} \right) \times I_{LED}$$

$$I_D = \left( 1 - \frac{35V}{48V \times 0.95} \right) \times 1.97A = 457\text{ mA} \tag{50}$$

A 100-V, 3-A diode is chosen with  $V_D = 750\text{ mV}$ . Determine  $P_D$ :

$$P_D = I_D \times V_D = 457\text{ mA} \times 750\text{ mV} = 343\text{ mW} \tag{51}$$

The chosen component from step 7 is:

$$\boxed{D1 \rightarrow 3A, 100V, SMC} \tag{52}$$

### 9.2.1.2.8 Input UVLO

Solve for  $R_{UV2}$ :

$$R_{UV2} = \frac{V_{HYS}}{22\ \mu A} = \frac{1.1V}{22\ \mu A} = 50\text{ k}\Omega \tag{53}$$

The closest 1% tolerance resistor is 49.9 k $\Omega$  therefore  $V_{HYS}$  is:

$$V_{HYS} = R_{UV2} \times 22\ \mu A = 49.9\text{ k}\Omega \times 22\ \mu A = 1.1V \tag{54}$$

Solve for  $R_{UV1}$ :

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN-ON} - 1.24V} = \frac{1.24V \times 49.9\text{ k}\Omega}{10V - 1.24V} = 7.06\text{ k}\Omega \tag{55}$$

The closest 1% tolerance resistor is 6.98 k $\Omega$  therefore  $V_{TURN-ON}$  is:

$$V_{TURN-ON} = \frac{1.24V \times (R_{UV1} + R_{UV2})}{R_{UV1}}$$

$$V_{TURN-ON} = \frac{1.24V \times (6.98\text{ k}\Omega + 49.9\text{ k}\Omega)}{6.98\text{ k}\Omega} = 10.1V \tag{56}$$

The chosen components from step 8 are:

$$\begin{matrix} R_{UV1} = 6.98\text{k}\Omega \\ R_{UV2} = 49.9\text{k}\Omega \end{matrix}$$

(57)

**9.2.1.2.9 IADJ Connection Method**

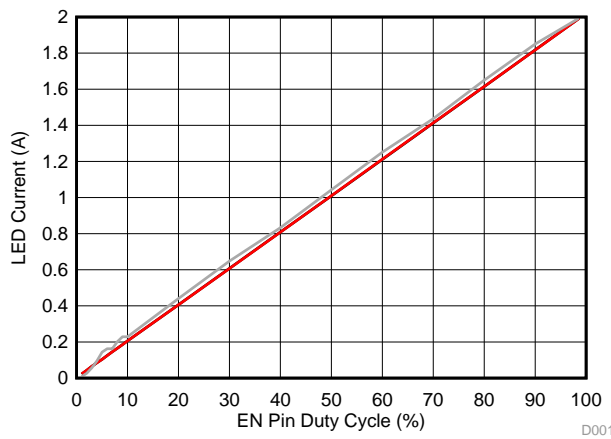
The IADJ pin is left open forcing  $V_{ADJ} = 1.24\text{ V}$ .

**9.2.1.2.10 PWM Dimming Method**

PWM dimming signal pair is applied to the EN pin and GND at  $f_{DIM} = 1\text{ kHz}$ .

**9.2.1.3 Application Curve**

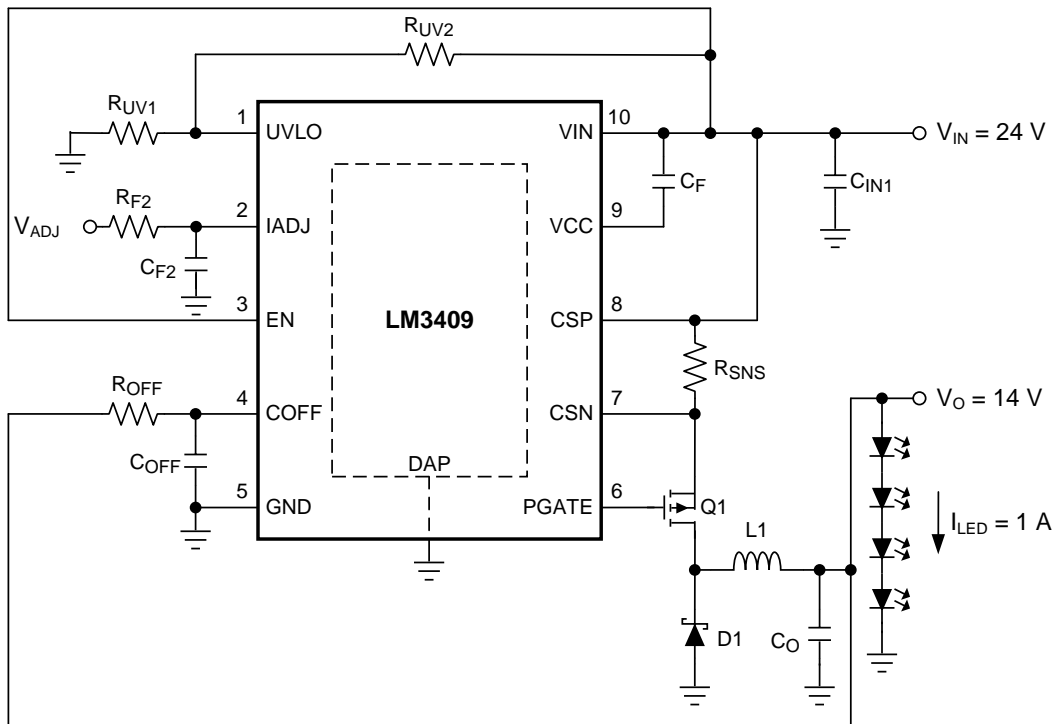
Figure 31 shows the LED current versus EN pin PWM duty cycle for the application.



Black = 200 Hz    Red = 1 kHz    Gray = 20 kHz

**Figure 31. EN Pin PWM Dimming**

## 9.2.2 Analog Dimming Application for 4 LEDs



### 9.2.2.1 Design Requirements

$$f_{SW} = 500 \text{ kHz}$$

$$V_{IN} = 24 \text{ V}; V_{IN-MAX} = 42 \text{ V}$$

$$V_O = 14 \text{ V}$$

$$I_{LED} = 1 \text{ A}$$

$$\Delta i_{L-PP} = 450 \text{ mA}; \Delta i_{LED-PP} = 50 \text{ mA}$$

$$\Delta V_{IN-PP} = 1 \text{ V}$$

$$V_{TURN-ON} = 10 \text{ V}; V_{HYS} = 1.1 \text{ V}$$

$$\eta = 0.90$$

### 9.2.2.2 Detailed Design Procedure

**Table 2. Design 2 Bill of Materials**

QTY	PART ID	PART VALUE	MANUFACTURER	PART NUMBER
1	LM3409/LM3409Q	Buck controller	TI	LM3409MY/LM3409QMY
2	C <sub>IN1</sub>	4.7- $\mu$ F X7R 10% 50 V	MURATA	GRM55ER71H475MA01L
1	C <sub>F</sub>	1- $\mu$ F X7R 10% 16 V	TDK	C1608X7R1C105K
1	C <sub>F2</sub>	0.1- $\mu$ F X7R 10% 16 V	TDK	C1608X7R1C104K
1	C <sub>OFF</sub>	470-pF X7R 10% 50 V	TDK	C1608X7R1H471K
1	C <sub>O</sub>	2.2- $\mu$ F X7R 10% 50 V	MURATA	GRM43ER71H225MA01L
1	Q1	PMOS 70 V 5.7 A	ZETEX	ZXMP7A17KTC
1	D1	Schottky 60 V 5 A	COMCHIP	CDBC560-G
1	L1	22 $\mu$ H 20% 4.2 A	TDK	SLF12575T-220M4R0
1	R <sub>F2</sub>	1 k $\Omega$ 1%	VISHAY	CRCW06031K00FKEA

**Table 2. Design 2 Bill of Materials (continued)**

QTY	PART ID	PART VALUE	MANUFACTURER	PART NUMBER
1	R <sub>OFF</sub>	15.4 kΩ 1%	VISHAY	CRCW060315K4FKEA
1	R <sub>UV1</sub>	6.98 kΩ 1%	VISHAY	CRCW06036K98FKEA
1	R <sub>UV2</sub>	49.9 kΩ 1%	VISHAY	CRCW060349K9FKEA
1	R <sub>SNS</sub>	0.2 Ω 1% 1W	VISHAY	WSL2512R2000FEA

**9.2.2.2.1 Nominal Switching Frequency**

Assume C<sub>OFF</sub> = 470 pF and η = 0.90. Solve for R<sub>OFF</sub>:

$$R_{OFF} = \frac{-\left(1 - \frac{V_O}{\eta \times V_{IN}}\right)}{C_{OFF} + 20 \text{ pF} \times f_{SW} \times \ln\left(1 - \frac{1.24V}{V_O}\right)}$$

$$R_{OFF} = \frac{-\left(1 - \frac{14V}{0.90 \times 24V}\right)}{490 \text{ pF} \times 500 \text{ kHz} \times \ln\left(1 - \frac{1.24V}{14V}\right)} = 15.5 \text{ k}\Omega \quad (58)$$

The closest 1% tolerance resistor is 15.4 kΩ; therefore, the actual t<sub>OFF</sub> and target f<sub>SW</sub> are:

$$t_{OFF} = -(C_{OFF} + 20 \text{ pF}) \times R_{OFF} \times \ln\left(1 - \frac{1.24V}{V_O}\right)$$

$$t_{OFF} = -490 \text{ pF} \times 15.4 \text{ k}\Omega \times \ln\left(1 - \frac{1.24V}{14V}\right) = 700 \text{ ns} \quad (59)$$

$$f_{SW} = \frac{1 - \left(\frac{V_O}{\eta \times V_{IN}}\right)}{t_{OFF}} = \frac{1 - \left(\frac{14V}{0.90 \times 24V}\right)}{700 \text{ ns}} = 503 \text{ kHz} \quad (60)$$

The chosen components from step 1 are:

$$\begin{aligned} C_{OFF} &= 470 \text{ pF} \\ R_{OFF} &= 15.4 \text{ k}\Omega \end{aligned}$$

(61)

**9.2.2.2.2 Inductor Ripple Current**

Solve for L1:

$$L1 = \frac{V_O \times t_{OFF}}{\Delta i_{L-PP}} = \frac{14V \times 700 \text{ ns}}{450 \text{ mA}} = 21.8 \mu\text{H} \quad (62)$$

The closest standard inductor value is 22 μH; therefore, the actual Δi<sub>L-PP</sub> is:

$$\Delta i_{L-PP} = \frac{V_O \times t_{OFF}}{L1} = \frac{14V \times 700 \text{ ns}}{22 \mu\text{H}} = 445 \text{ mA} \quad (63)$$

The chosen component from step 2 is:

$$L1 = 22 \mu\text{H}$$

(64)

### 9.2.2.2.3 Average LED Current

Determine  $I_{L-MAX}$ :

$$I_{L-MAX} = I_{LED} + \frac{\Delta i_{L-PP}}{2} = 1A + \frac{445 \text{ mA}}{2} = 1.22A \quad (65)$$

Assume  $V_{ADJ} = 1.24 \text{ V}$  and solve for  $R_{SNS}$ :

$$R_{SNS} = \frac{V_{ADJ}}{5 \times I_{L-MAX}} = \frac{1.24V}{5 \times 1.22A} = 0.203\Omega \quad (66)$$

The closest 1% tolerance resistor is  $0.2 \Omega$  therefore  $I_{LED}$  is:

$$I_{LED} = \frac{V_{ADJ}}{5 \times R_{SNS}} - \frac{\Delta i_{L-PP}}{2} = \frac{1.24V}{5 \times 0.2\Omega} - \frac{445 \text{ mA}}{2} = 1.02A \quad (67)$$

The chosen component from step 3 is:

$$\boxed{R_{SNS} = 0.2\Omega} \quad (68)$$

### 9.2.2.2.4 Output Capacitance

Assume  $r_D = 2 \Omega$  and determine  $Z_C$ :

$$Z_C = \frac{r_D \times \Delta i_{LED-PP}}{\Delta i_{L-PP} - \Delta i_{LED-PP}} = \frac{2\Omega \times 50 \text{ mA}}{450 \text{ mA} - 50 \text{ mA}} = 250 \text{ m}\Omega \quad (69)$$

Solve for  $C_{O-MIN}$  and :

$$C_{O-MIN} = \frac{1}{2 \times \pi \times f_{SW} \times Z_C}$$

$$C_{O-MIN} = \frac{1}{2 \times \pi \times 503 \text{ kHz} \times 250 \text{ m}\Omega} = 1.27 \mu\text{F} \quad (70)$$

Choose  $C_O$ :

$$C_O = C_{O-MIN} \times 1.75 = 2.2 \mu\text{F} \quad (71)$$

The chosen component from step 5 is:

$$\boxed{C_O = 2.2 \mu\text{F}} \quad (72)$$

### 9.2.2.2.5 Input Capacitance

Determine  $t_{ON}$ :

$$t_{ON} = \frac{1}{f_{SW}} - t_{OFF} = \frac{1}{503 \text{ kHz}} - 700 \text{ ns} = 1.29 \mu\text{s} \quad (73)$$

Solve for  $C_{IN-MIN}$ :

$$C_{IN-MIN} = \frac{I_{LED} \times t_{ON}}{\Delta V_{IN-PP}} = \frac{1.02A \times 1.29 \mu\text{s}}{720 \text{ mV}} = 1.82 \mu\text{F} \quad (74)$$

Choose  $C_{IN}$ :

$$C_{IN} = C_{IN-MIN} \times 2 = 3.64 \mu\text{F} \quad (75)$$

Determine  $I_{IN-RMS}$ :

$$I_{IN-RMS} = I_{LED} \times f_{SW} \times \sqrt{t_{ON} \times t_{OFF}}$$

$$I_{IN-RMS} = 1.02A \times 503 \text{ kHz} \times \sqrt{1.29 \mu\text{s} \times 700 \text{ ns}} = 486 \text{ mA} \quad (76)$$

The chosen component from step 5 is:

$$C_{IN} = 4.7 \mu\text{F} \quad (77)$$

#### 9.2.2.2.6 PFET

Determine minimum Q1 voltage rating and current rating:

$$V_{T-MAX} = V_{IN-MAX} = 42V \quad (78)$$

$$I_T = D \times I_{LED} = \frac{V_O \times I_{LED}}{V_{IN} \times \eta} = \frac{14V \times 1.02A}{24V \times 0.90} = 660 \text{ mA} \quad (79)$$

A 70V, 5.7 A PFET is chosen with  $R_{DS-ON} = 190 \text{ m}\Omega$  and  $Q_g = 20 \text{ nC}$ . Determine  $I_{T-RMS}$  and  $P_T$ :

$$I_{T-RMS} = I_{LED} \times \sqrt{D \times \left(1 + \frac{1}{12} \times \left(\frac{\Delta I_{L-PP}}{I_{LED}}\right)^2\right)}$$

$$I_{T-RMS} = 1.02A \times \sqrt{\frac{14V}{24V \times 0.90} \times \left(1 + \frac{1}{12} \times \left(\frac{445 \text{ mA}}{1.02A}\right)^2\right)}$$

$$I_{T-RMS} = 830 \text{ mA} \quad (80)$$

$$P_T = I_{T-RMS}^2 \times R_{DS-ON} = 830 \text{ mA}^2 \times 190 \text{ m}\Omega = 129 \text{ mW} \quad (81)$$

The chosen component from step 6 is:

$$Q1 \rightarrow 5.7A, 70V, \text{ DPAK} \quad (82)$$

#### 9.2.2.2.7 Diode

Determine minimum D1 voltage rating and current rating:

$$V_{D-MAX} = V_{IN-MAX} = 42V \quad (83)$$

$$I_D = (1 - D) \times I_{LED} = \left(1 - \frac{V_O}{V_{IN} \times \eta}\right) \times I_{LED}$$

$$I_D = \left(1 - \frac{14V}{24V \times 0.90}\right) \times 1.02A = 358 \text{ mA} \quad (84)$$

A 60 V, 5 A diode is chosen with  $V_D = 750 \text{ mV}$ . Determine  $P_D$ :

$$P_D = I_D \times V_D = 358 \text{ mA} \times 750 \text{ mV} = 268 \text{ mW} \quad (85)$$

The chosen component from step 7 is:

$$D1 \rightarrow 5A, 60V, \text{ SMC} \quad (86)$$

#### 9.2.2.2.8 Input UVLO

Solve for  $R_{UV2}$ :

$$R_{UV2} = \frac{V_{HYS}}{22 \mu\text{A}} = \frac{1.1V}{22 \mu\text{A}} = 50 \text{ k}\Omega \quad (87)$$

The closest 1% tolerance resistor is 49.9 kΩ therefore  $V_{HYS}$  is:

$$V_{HYS} = R_{UV2} \times 22 \mu A = 49.9 \text{ k}\Omega \times 22 \mu A = 1.1V \quad (88)$$

Solve for  $R_{UV1}$ :

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN-ON} - 1.24V} = \frac{1.24V \times 49.9 \text{ k}\Omega}{10V - 1.24V} = 7.06 \text{ k}\Omega \quad (89)$$

The closest 1% tolerance resistor is 6.98 kΩ therefore  $V_{TURN-ON}$  is:

$$V_{TURN-ON} = \frac{1.24V \times (R_{UV1} + R_{UV2})}{R_{UV1}}$$

$$V_{TURN-ON} = \frac{1.24V \times (6.98 \text{ k}\Omega + 49.9 \text{ k}\Omega)}{6.98 \text{ k}\Omega} = 10.1V \quad (90)$$

The chosen components from step 8 are:

$R_{UV1} = 6.98 \text{ k}\Omega$ $R_{UV2} = 49.9 \text{ k}\Omega$
--

(91)

#### 9.2.2.2.9 IADJ Connection Method

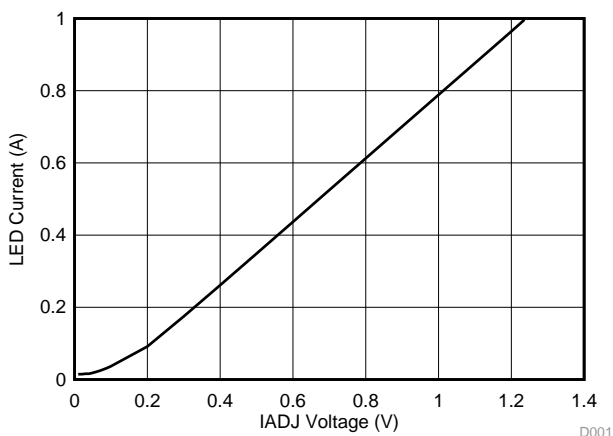
The IADJ pin is connected to an external voltage source and varied from 0 – 1.24 V to dim. An RC filter ( $R_{F2} = 1 \text{ k}\Omega$  and  $C_{F2} = 0.1 \mu F$ ) is used as recommended.

#### 9.2.2.2.10 PWM Dimming Method

No PWM dimming is necessary.

#### 9.2.2.3 Application Curve

Figure 32 shows the LED current versus IADJ voltage for the application.



**Figure 32. Analog Dimming Profile**



### 9.2.3 LM3409 Buck Converter Application

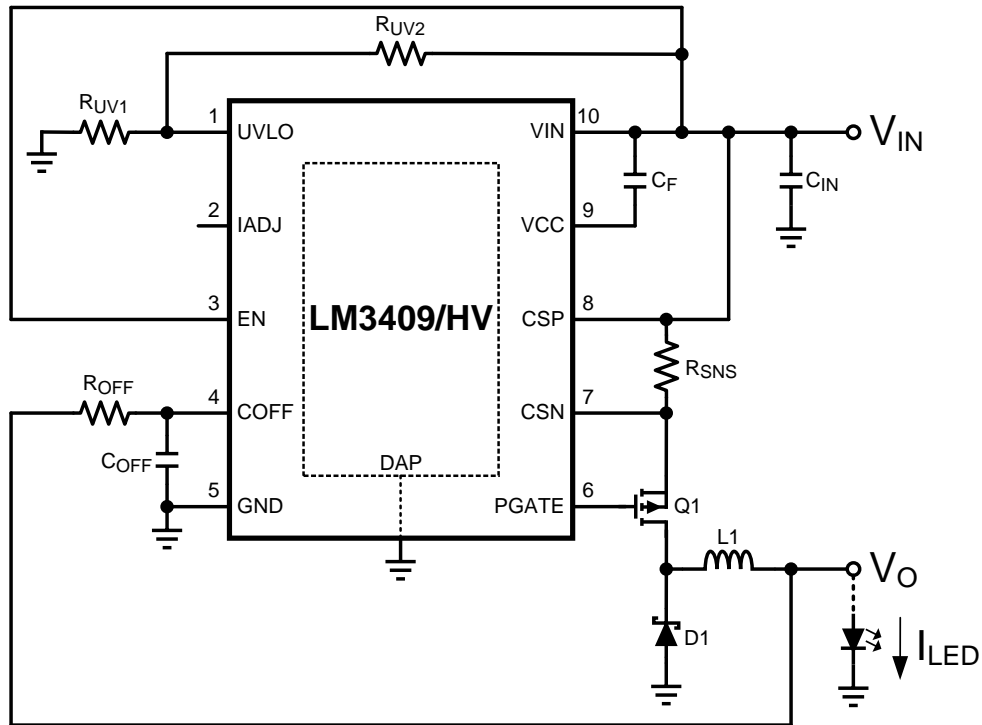


Figure 33. LM3409 Buck Converter Simplified Schematic

#### 9.2.3.1 Design Requirements

Nominal input voltage:  $V_{IN}$

Maximum input voltage:  $V_{IN-MAX}$

Nominal output voltage (number of LEDs x forward voltage):  $V_O$

LED string dynamic resistance:  $r_D$

Switching frequency (at nominal  $V_{IN}$ ,  $V_O$ ):  $f_{SW}$

Average LED current:  $I_{LED}$

Inductor current ripple:  $\Delta i_{L-PP}$

LED current ripple:  $\Delta i_{LED-PP}$

Input voltage ripple:  $\Delta v_{IN-PP}$

UVLO characteristics:  $V_{TURN-ON}$  and  $V_{HYS}$

Expected efficiency:  $\eta$

#### 9.2.3.2 Detailed Design Procedure

##### 9.2.3.2.1 Nominal Switching Frequency

Calculate switching frequency ( $f_{SW}$ ) at the nominal operating point ( $V_{IN}$  and  $V_O$ ). Assume a  $C_{OFF}$  value (from 470 pF to 1 nF) and a system efficiency ( $\eta$ ). Solve for  $R_{OFF}$ :

$$R_{\text{OFF}} = \frac{-\left(1 - \frac{V_O}{\eta \times V_{\text{IN}}}\right)}{(C_{\text{OFF}} + 20 \text{ pF}) \times f_{\text{SW}} \times \ln\left(1 - \frac{1.24\text{V}}{V_O}\right)} \quad (92)$$

### 9.2.3.2.2 Inductor Ripple Current

Set the inductor ripple current ( $\Delta i_{\text{L-PP}}$ ) by solving for the appropriate inductor (L1):

$$L1 = \frac{V_O \times t_{\text{OFF}}}{\Delta i_{\text{L-PP}}} \quad (93)$$

### 9.2.3.2.3 Average LED Current

Set the average LED current ( $I_{\text{LED}}$ ) by first solving for the peak inductor current ( $I_{\text{L-MAX}}$ ):

$$I_{\text{L-MAX}} = I_{\text{LED}} + \frac{\Delta i_{\text{L-PP}}}{2} \quad (94)$$

Peak inductor current is detected across the sense resistor ( $R_{\text{SNS}}$ ). In most cases, assume the maximum value ( $V_{\text{ADJ}} = 1.24 \text{ V}$ ) at the IADJ pin and solve for  $R_{\text{SNS}}$ :

$$R_{\text{SNS}} = \frac{V_{\text{ADJ}}}{5 \times I_{\text{L-MAX}}} \quad (95)$$

If the calculated  $R_{\text{SNS}}$  is far from a standard value, the beginning of the process can be iterated to choose a new  $R_{\text{OFF}}$ , L1, and  $R_{\text{SNS}}$  value that is a closer fit. The easiest way to approach the iterative process is to change the nominal  $f_{\text{SW}}$  target knowing that the switching frequency varies with operating conditions anyways.

Another method for finding a standard  $R_{\text{SNS}}$  value is to change the  $V_{\text{ADJ}}$  value. However, this would require an external voltage source or a resistor from the IADJ pin to GND as explained in the [Adjustable Peak Current Control](#) section of this data sheet.

### 9.2.3.2.4 Output Capacitance

A minimum output capacitance ( $C_{\text{O-MIN}}$ ) may be necessary to reduce  $\Delta i_{\text{LED-PP}}$  below  $\Delta i_{\text{L-PP}}$ . With the specified  $\Delta i_{\text{LED-PP}}$  and the known dynamic resistance ( $r_{\text{D}}$ ) of the LED string, solve for the required impedance ( $Z_{\text{C}}$ ) for  $C_{\text{O-MIN}}$ :

$$Z_{\text{C}} = \frac{r_{\text{D}} \times \Delta i_{\text{LED-PP}}}{\Delta i_{\text{L-PP}} - \Delta i_{\text{LED-PP}}} \quad (96)$$

Solve for  $C_{\text{O-MIN}}$ :

$$C_{\text{O-MIN}} = \frac{1}{2 \times \pi \times f_{\text{SW}} \times Z_{\text{C}}} \quad (97)$$

### 9.2.3.2.5 Input Capacitance

Set the input voltage ripple ( $\Delta v_{\text{IN-PP}}$ ) by solving for the required minimum capacitance ( $C_{\text{IN-MIN}}$ ):

$$C_{\text{IN-MIN}} = \frac{I_{\text{LED}} \times t_{\text{ON}}}{\Delta v_{\text{IN-PP}}} = \frac{I_{\text{LED}} \times \left(\frac{1}{f_{\text{SW}}} - t_{\text{OFF}}\right)}{\Delta v_{\text{IN-PP}}} \quad (98)$$

The necessary RMS input current rating ( $I_{\text{IN-RMS}}$ ) is:

$$I_{\text{IN-RMS}} = I_{\text{LED}} \times f_{\text{SW}} \times \sqrt{t_{\text{ON}} \times t_{\text{OFF}}} \quad (99)$$

### 9.2.3.2.6 PFET

The PFET voltage rating should be at least 15% higher than the maximum input voltage ( $V_{IN-MAX}$ ) and current rating should be at least 10% higher than the average PFET current ( $I_T$ ):

$$I_T = D \times I_{LED} \quad (100)$$

Given a PFET with on-resistance ( $R_{DS-ON}$ ), solve for the RMS transistor current ( $I_{T-RMS}$ ) and power dissipation ( $P_T$ ):

$$I_{T-RMS} = I_{LED} \times \sqrt{D \times \left( 1 + \frac{1}{12} \times \left( \frac{\Delta i_{L-PP}}{I_{LED}} \right)^2 \right)} \quad (101)$$

$$P_T = I_{T-RMS}^2 \times R_{DS-ON} \quad (102)$$

### 9.2.3.2.7 Diode

The Schottky diode needs a voltage rating similar to the PFET. Higher current diodes with a lower forward voltage are suggested. Given a diode with forward voltage ( $V_D$ ), solve for the average diode current ( $I_D$ ) and power dissipation ( $P_D$ ):

$$I_D = (1 - D) \times I_{LED} \quad (103)$$

$$P_D = I_D \times V_D \quad (104)$$

### 9.2.3.2.8 Input UVLO

Input UVLO is set with the turnon threshold voltage ( $V_{TURN-ON}$ ) and the desired hysteresis ( $V_{HYS}$ ). To set  $V_{HYS}$ , solve for  $R_{UV2}$ :

$$R_{UV2} = \frac{V_{HYS}}{22 \mu A} \quad (105)$$

To set  $V_{TURN-ON}$ , solve for  $R_{UV1}$ :

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN-ON} - 1.24V} \quad (106)$$

### 9.2.3.2.9 IADJ Connection Method

The IADJ pin controls the high-side current sense threshold in three ways outlined in the [Adjustable Peak Current Control](#) section.

**Method 1:** Leave IADJ pin open and  $I_{LED}$  is calculated as in the [Average LED Current](#) section of the *Design Guide*.

**Method 2:** Apply an external voltage ( $V_{ADJ}$ ) to the IADJ pin from 0 to 1.24 V to analog dim or to reduce  $I_{LED}$  as follows:

$$I_{LED} = \frac{V_{ADJ}}{5 \times R_{SNS}} - \frac{\Delta i_{L-PP}}{2} \quad (107)$$

Keep in mind that analog dimming will eventually push the converter in to DCM and the inductor current ripple will no longer be constant causing a divergence from linear dimming at low levels.

A 0.1  $\mu F$  capacitor connected from the IADJ pin to GND is recommended when using this method. It may also be necessary to have a 1k $\Omega$  series resistor with the capacitor to create an RC filter. The filter will help remove high frequency noise created by other connected circuitry.

**Method 3:** Connect an external resistor or potentiometer to GND ( $R_{EXT}$ ) and the internal 5  $\mu A$  current source will set the voltage. Again, a 0.1  $\mu F$  capacitor connected from the IADJ pin to GND is recommended. To set  $I_{LED}$ , solve for  $R_{EXT}$ :

$$R_{EXT} = \frac{\left( I_{LED} + \frac{\Delta i_{L-PP}}{2} \right) \times R_{SNS}}{1 \mu A} \quad (108)$$

#### 9.2.3.2.10 PWM Dimming Method

There are two methods to PWM dim using the LM3409/09HV:

**Method 1:** Apply an external PWM signal to the EN terminal.

**Method 2:** Perform external parallel FET shunt dimming as detailed in the [External Parallel FET PWM Dimming](#) section.

## 10 Power Supply Recommendations

Any DC output power supply may be used provided it has a high enough voltage and current range for the particular application required.

## 11 Layout

### 11.1 Layout Guidelines

The performance of any switching converter depends as much upon the layout of the PCB as the component selection. Following a few simple guidelines will maximize noise rejection and minimize the generation of EMI within the circuit.

Discontinuous currents are the most likely to generate EMI, therefore take care when routing these paths. The main path for discontinuous current in the LM3409/09HV buck converter contains the input capacitor ( $C_{IN}$ ), the recirculating diode (D1), the P-channel MOSFET (Q1), and the sense resistor ( $R_{SNS}$ ). This loop should be kept as small as possible and the connections between all three components should be short and thick to minimize parasitic inductance. In particular, the switch node (where L1, D1 and Q1 connect) should be just large enough to connect the components without excessive heating from the current it carries.

The IADJ, COFF, CSN and CSP pins are all high-impedance control inputs which couple external noise easily, therefore the loops containing these high impedance nodes should be minimized. The most sensitive loop contains the sense resistor ( $R_{SNS}$ ) which should be placed as close as possible to the CSN and CSP pins to maximize noise rejection. The off-time capacitor ( $C_{OFF}$ ) should be placed close to the COFF and GND pins for the same reason. Finally, if an external resistor ( $R_{EXT}$ ) is used to bias the IADJ pin, it should be placed close to the IADJ and GND pins, also.

In some applications the LED or LED array can be far away (several inches or more) from the LM3409/09HV, or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED array is large or separated from the rest of the converter, the output capacitor should be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.

### 11.2 Layout Example

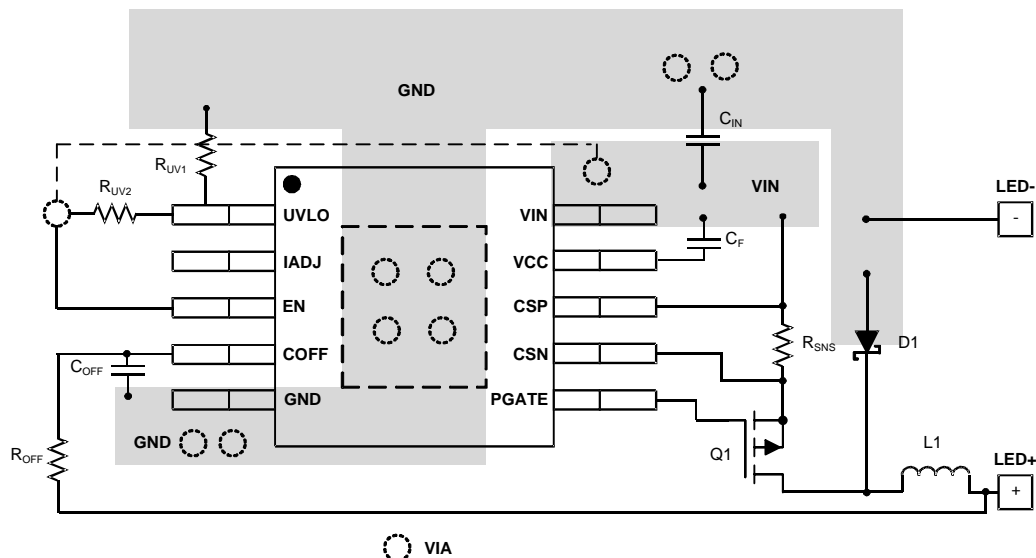


Figure 34. Layout Recommendation

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

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### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 3. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM3409	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM3409-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM3409HV	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM3409HV-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3409HVMY/NOPB	ACTIVE	HVSSOP	DGQ	10	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SYHB	<a href="#">Samples</a>
LM3409HVMYX/NOPB	ACTIVE	HVSSOP	DGQ	10	3500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SYHB	<a href="#">Samples</a>
LM3409MY/NOPB	ACTIVE	HVSSOP	DGQ	10	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SXFB	<a href="#">Samples</a>
LM3409MYX/NOPB	ACTIVE	HVSSOP	DGQ	10	3500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SXFB	<a href="#">Samples</a>
LM3409QHVMY/NOPB	ACTIVE	HVSSOP	DGQ	10	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SZEB	<a href="#">Samples</a>
LM3409QHVMYX/NOPB	ACTIVE	HVSSOP	DGQ	10	3500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SZEB	<a href="#">Samples</a>
LM3409QMY/NOPB	ACTIVE	HVSSOP	DGQ	10	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SZDB	<a href="#">Samples</a>
LM3409QMYX/NOPB	ACTIVE	HVSSOP	DGQ	10	3500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	SZDB	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LM3409, LM3409-Q1, LM3409HV, LM3409HV-Q1 :**

- Catalog: [LM3409](#), [LM3409HV](#)
- Automotive: [LM3409-Q1](#), [LM3409HV-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3409HVMY/NOPB	HVSSOP	DGQ	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3409HVMYX/NOPB	HVSSOP	DGQ	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3409MY/NOPB	HVSSOP	DGQ	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3409MYX/NOPB	HVSSOP	DGQ	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3409QHVMY/NOPB	HVSSOP	DGQ	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3409QHVMYX/NOPB	HVSSOP	DGQ	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3409QMY/NOPB	HVSSOP	DGQ	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3409QMYX/NOPB	HVSSOP	DGQ	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

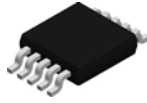
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3409HVMY/NOPB	HVSSOP	DGQ	10	1000	210.0	185.0	35.0
LM3409HVMYX/NOPB	HVSSOP	DGQ	10	3500	367.0	367.0	35.0
LM3409MY/NOPB	HVSSOP	DGQ	10	1000	210.0	185.0	35.0
LM3409MYX/NOPB	HVSSOP	DGQ	10	3500	367.0	367.0	35.0
LM3409QHVMY/NOPB	HVSSOP	DGQ	10	1000	210.0	185.0	35.0
LM3409QHVMYX/NOPB	HVSSOP	DGQ	10	3500	367.0	367.0	35.0
LM3409QMY/NOPB	HVSSOP	DGQ	10	1000	210.0	185.0	35.0
LM3409QMYX/NOPB	HVSSOP	DGQ	10	3500	367.0	367.0	35.0

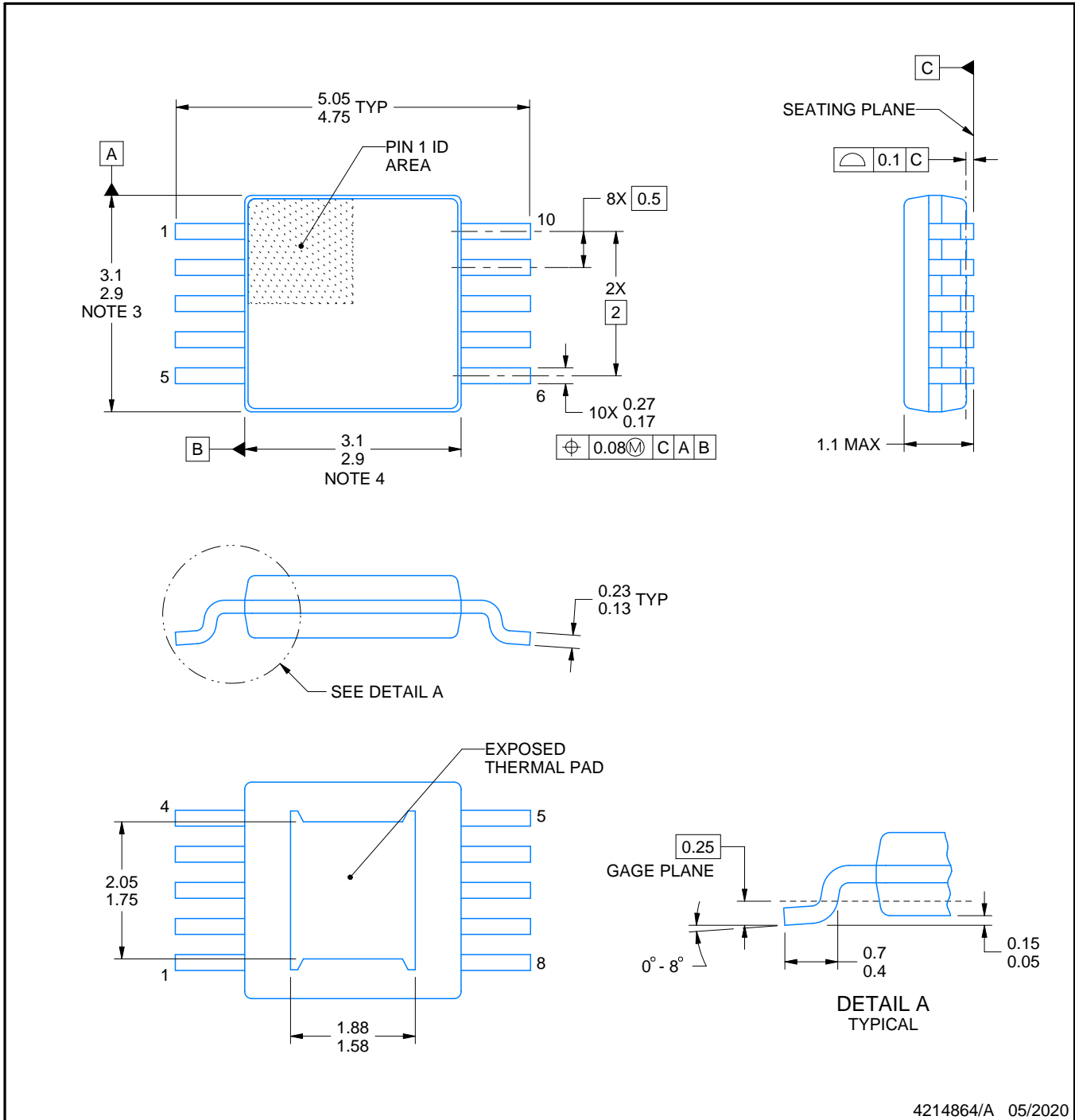
# DGQ0010A



# PACKAGE OUTLINE

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



4214864/A 05/2020

PowerPAD is a trademark of Texas Instruments.

**NOTES:**

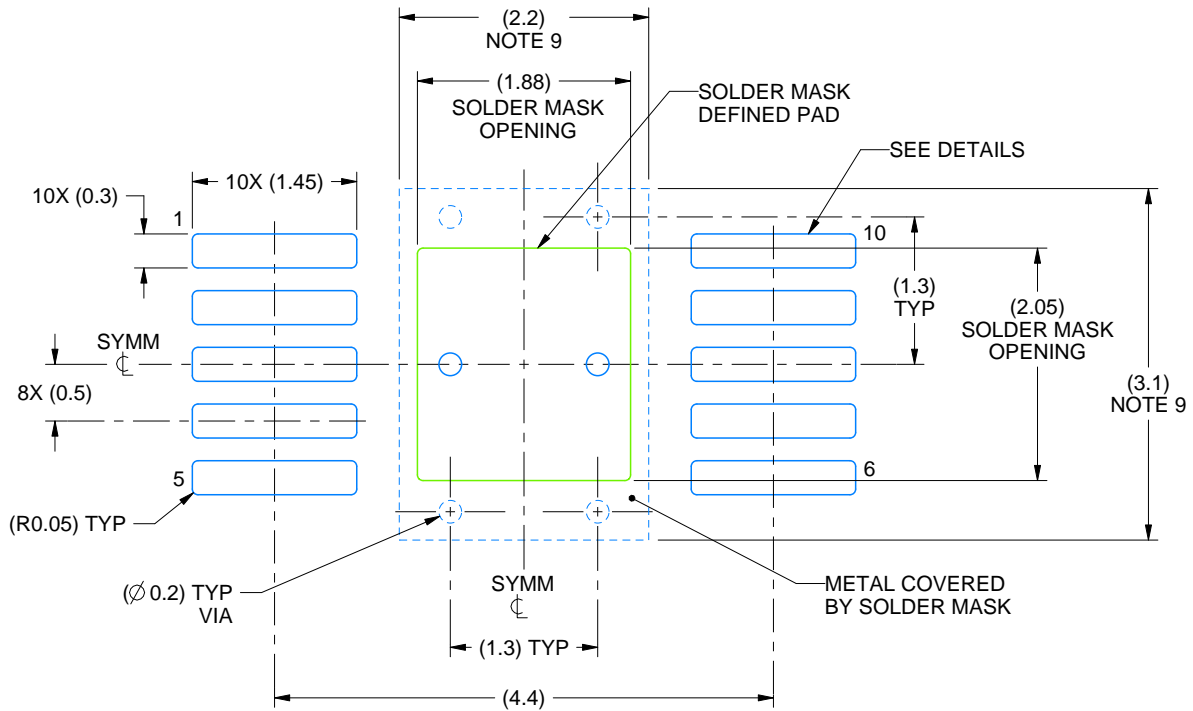
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.

# EXAMPLE BOARD LAYOUT

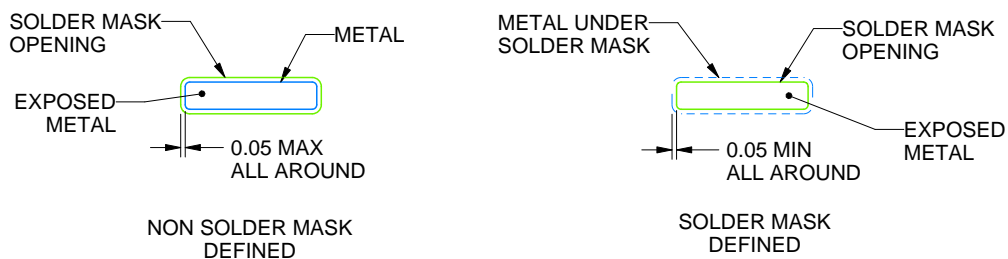
DGQ0010A

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

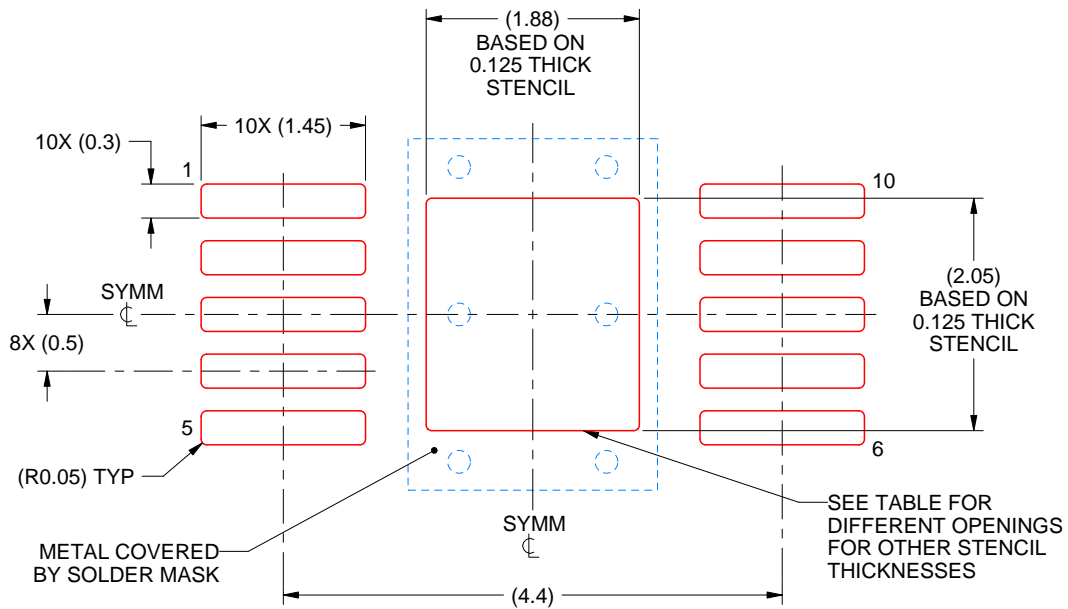
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGQ0010A

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.29
0.125	1.88 X 2.05 (SHOWN)
0.150	1.72 X 1.87
0.175	1.59 X 1.73

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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