

FEATURES

- Guaranteed $\overline{\text{RESET}}$ valid with $V_{CC} = 1V$
- 190 μA quiescent current
- Precision supply voltage monitor
4.65 V (CBM705/CBM707)
4.40 V (CBM706/CBM708)
- 200 ms reset pulse width
- Debounced TTL/CMOS manual reset input ($\overline{\text{MR}}$)
- Independent watchdog timer (CBM705/CBM706)
- 1.60 sec timeout (CBM705/CBM706)
- Active high reset output (CBM707/CBM708)
- Voltage monitor for power fail or low battery warning
- Superior upgrade for ADM705 to ADM708

APPLICATIONS

- Microprocessor systems
- Computers
- Controllers
- Intelligent instruments
- Critical microprocessor supply monitoring

GENERAL DESCRIPTION

The CBM705, CBM706, CBM707, CBM708 microprocessor supervisory circuits are suitable for monitoring 5V power supplies/batteries and microprocessor activity.

The CBM705/ CBM706 provide power-supply monitoring circuitry that generate a reset output during power-up, power-down, and brownout conditions. The reset output remains operational with V_{CC} as low as 1V. Independent watchdog monitoring circuitry is also provided. This is activated if the watchdog input has not been toggled within 1.60 sec.

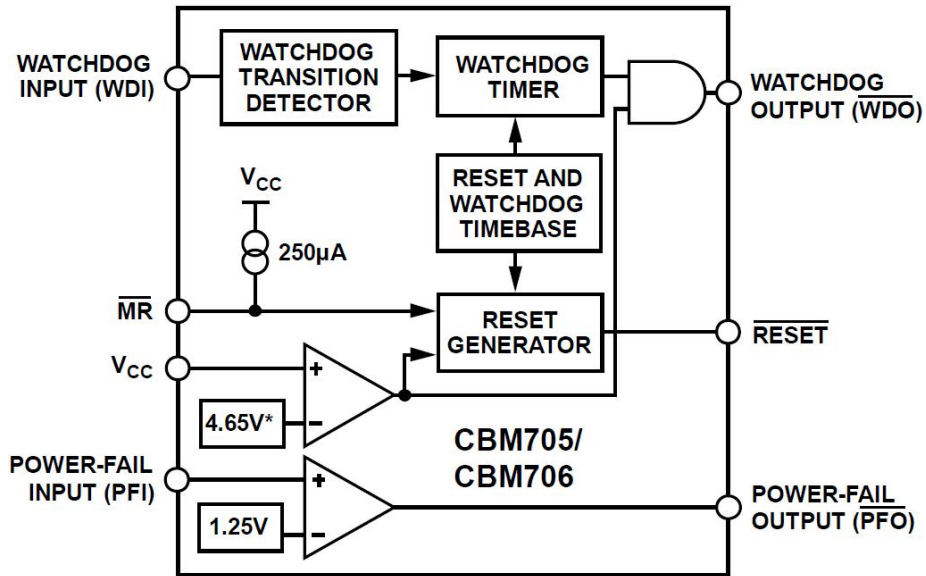
In addition, there is a 1.25V threshold detector to warn of power failures, to detect low battery conditions, or to monitor an additional power supply. An active low, debounced manual reset input ($\overline{\text{MR}}$) is also included.

The CBM705 and CBM706 are identical except for the reset threshold monitor levels, which are 4.65V and 4.40V, respectively.

The CBM707 and CBM708 provide a similar functionality to the CBM705 and CBM706 and only differ in that a watchdog timer function is not available. Instead, an active high reset output (RESET) is available as well as the active low reset output ($\overline{\text{RESET}}$). The CBM707 and CBM708 are identical except for the reset threshold monitor levels, which are 4.65V and 4.40V, respectively.

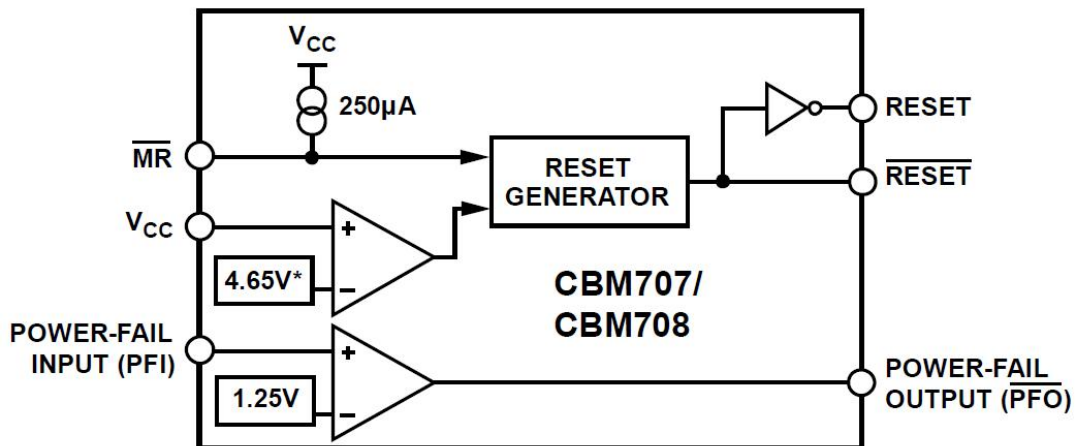
All devices are available in narrow 8-lead SOIC packages.

FUNCTIONAL BLOCK DIAGRAMS



*VOLTAGE REFERENCE = 4.65V (CBM705), 4.40V (CBM706)

Figure 1. CBM705/CBM706



* VOLTAGE REFERENCE = 4.65V (CBM707), 4.40V (CBM708)

Figure 2. CBM707/CBM708

SPECIFICATIONS

$V_{CC} = 4.75\text{ V to }5.5\text{ V}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
V_{CC} Operating Voltage Range	1.0		5.5	V	
Supply Current		190	250	μA	
LOGIC OUTPUT					
Reset Threshold	4.5	4.65	4.75	V	CBM705/CBM707
	4.25	4.40	4.50	V	CBM706/CBM708
Reset Threshold Hysteresis		40		mV	
RESET PULSE WIDTH	160	200	280	ms	
$\overline{\text{RESET}}$ OUTPUT VOLTAGE	$V_{CC}-1.5$			V	$I_{\text{SOURCE}} = 800\ \mu\text{A}$
			0.4	V	$I_{\text{SINK}} = 3.2\ \text{mA}$
			0.3	V	$V_{CC} = 1\ \text{V}$, $I_{\text{SINK}} = 50\ \mu\text{A}$
			0.3	V	$V_{CC} = 1.2\ \text{V}$, $I_{\text{SINK}} = 100\ \mu\text{A}$
RESET OUTPUT VOLTAGE	$V_{CC}-1.5$			V	CBM707/CBM708, $I_{\text{SOURCE}} = 800\ \mu\text{A}$
			0.4	V	CBM707/CBM708, $I_{\text{SINK}} = 1.2\ \text{mA}$
WATCHDOG TIMEOUT PERIOD (t_{WD})	1.00	1.60	2.25	sec	$V_{IL} = 0.4\ \text{V}$, $V_{IH} = V_{CC} \times 0.8$, $WDI = V_{CC}$
WDI Pulse Width (t_{WP})	50			ns	
WATCHDOG INPUT					
WDI Input Threshold					
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current		50	150	μA	$WDI=0\text{V}$
	-150	-50		μA	$WDI=0\text{V}$
$\overline{\text{WDO}}$ OUTPUT VOLTAGE	$V_{CC}-1.5$			V	$I_{\text{SOURCE}} = 800\ \mu\text{A}$
			0.4	V	$I_{\text{SINK}} = 1.2\ \text{mA}$
MANUAL RESET INPUT					
$\overline{\text{MR}}$ Pull-Up Current	100	250	600	μA	$\overline{\text{MR}} = 0\text{V}$
$\overline{\text{MR}}$ Pulse Width	150			ns	
MR INPUT THRESHOLD					
Logic Low			0.8	V	
Logic High	2.0			V	
$\overline{\text{MR}}$ TO RESET OUTPUT DELAY			250	ns	
POWER FAIL INPUT					
PFI Input Threshold	1.2	1.25	1.3	V	
PFI Input Current	-25	+0.01	+25	nA	
$\overline{\text{PFO}}$ OUTPUT VOLTAGE	$V_{CC}-1.5$			V	$I_{\text{SOURCE}} = 800\ \mu\text{A}$
			0.4	V	$I_{\text{SINK}} = 3.2\ \text{mA}$

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Rating
V_{CC}	-0.3 V to +6 V
All Other Inputs	-0.3V to $V_{CC}+0.3V$
Input Current	
V_{CC}	20mA
GND	20mA
Digital Output Current	20mA
Power Dissipation, N-8 PDIP	727mW
θ_{JA} Thermal Impedance	135°C
Power Dissipation, R-8 SOIC	470mW
θ_{JA} Thermal Impedance	110°C/W
Power Dissipation, RM-8 MSOP	900mW
θ_{JA} Thermal Impedance	206°C/W
Operating Temperature Range	
Industrial (Version A)	-40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Storage Temperature Range	-65°C to +150°C
ESD Rating	>4.5kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied.

Operation beyond the maximum operating conditions for extended periods may affect product reliability.



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

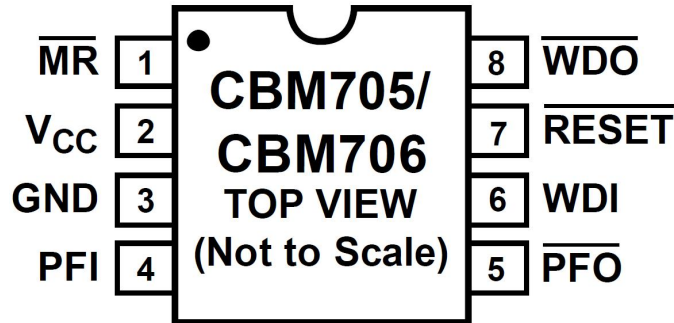
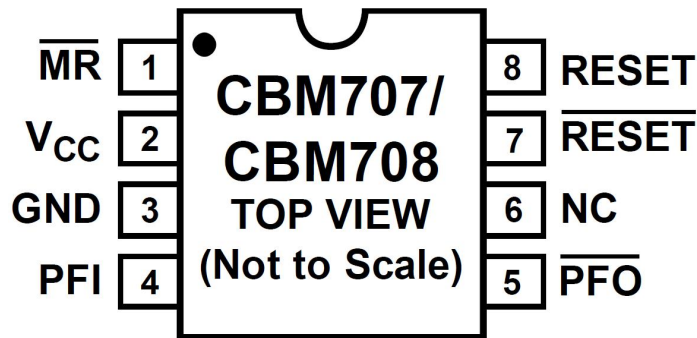
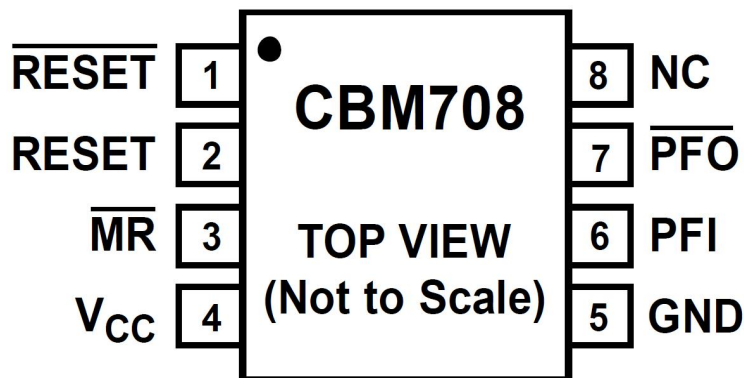


Figure 3. CBM705/CBM706 PDIP/SOIC



NC = NO CONNECT

Figure 4. CBM707/CBM708 PDIP/SOIC



NC = NO CONNECT

Figure 5. CBM708 MSOP

Pin Function Descriptions

Mnemonic	Pin Number			Description
	CBM705 CBM706	CBM707 CBM708	CBM708	
$\overline{\text{MR}}$	1	1	3	Manual Reset Input. When this pin is taken below 0.8V, a reset is generated. $\overline{\text{MR}}$ can be driven from TTL, CMOS logic, or from a manual reset switch as it is internally debounced. An internal 250 μ A pull-up current holds the input high when floating.
V_{CC}	2	2	4	5V Power Supply Input. Place a 0.1 μ F decoupling capacitor between the V_{CC} and GND pins.
GND	3	3	5	0V Ground Reference for All Signals.
PFI	4	4	6	Power Fail Input. PFI is the noninverting input to the power fail comparator. When PFI is less than 1.25V, $\overline{\text{PFO}}$ goes low. If unused, PFI must be connected to GND.
$\overline{\text{PFO}}$	5	5	7	Power Fail Output. $\overline{\text{PFO}}$ is the output from the power fail comparator. It goes low when PFI is less than 1.25V.
WDI	6	Not applicable	Not applicable	Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog timeout period, the watchdog output ($\overline{\text{WDO}}$) goes low. The timer resets with each transition at the WDI input. Either a high to low or a low to high transition clears the counter. The internal timer is also cleared whenever reset is asserted. The watchdog timer is disabled when WDI is left floating or connected to a three-state buffer.
NC	Not applicable	6	8	No Connect.
$\overline{\text{RESET}}$	7	7	1	Logic Output. $\overline{\text{RESET}}$ goes low for 200ms when triggered. It can be triggered either by V_{CC} being below the reset threshold or by a low signal on the manual reset input ($\overline{\text{MR}}$). $\overline{\text{RESET}}$ remains low whenever V_{CC} is below the reset threshold (4.65V in CBM705/CBM707, 4.40 V in CBM706/CBM708). It remains low for 200ms after V_{CC} goes above the reset threshold or $\overline{\text{MR}}$ goes from low to high. A watchdog timeout does not trigger $\overline{\text{RESET}}$ unless $\overline{\text{WDO}}$ is connected to $\overline{\text{MR}}$.
$\overline{\text{WDO}}$	8	Not applicable	Not applicable	Watchdog Output. $\overline{\text{WDO}}$ remains low until the watchdog timer is cleared. $\overline{\text{WDO}}$ also goes low during low line conditions. Whenever V_{CC} is below the reset threshold, $\overline{\text{WDO}}$ goes low if the internal $\overline{\text{WDO}}$ remains low. As soon as V_{CC} goes above the reset threshold, $\overline{\text{WDO}}$ goes high.
RESET	Not applicable	8	2	Logic Output. RESET is an active high output suitable for systems that use active high reset logic. It is the inverse of $\overline{\text{RESET}}$.

TYPICAL PERFORMANCE CHARACTERISTICS

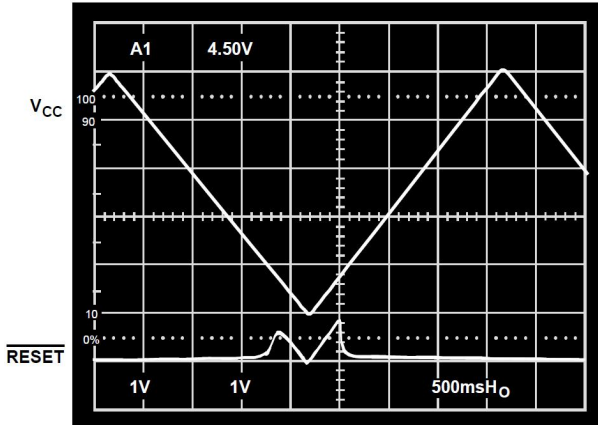


Figure 6. $\overline{\text{RESET}}$ Output Voltage vs. Supply Voltage

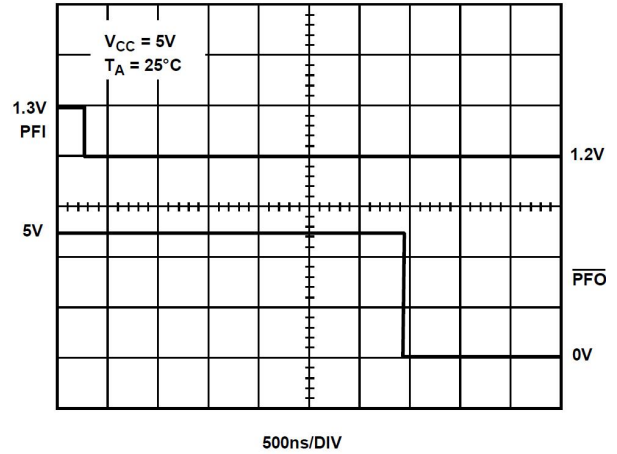


Figure 8. PFI Comparator Assertion Response Time

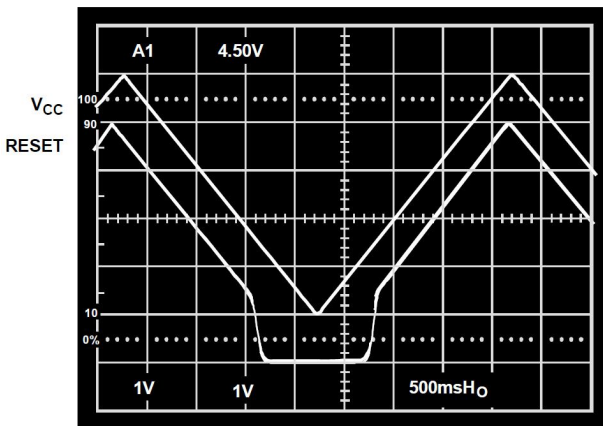


Figure 7. CBM707/CBM708 RESET Output Voltage vs. Supply Voltage

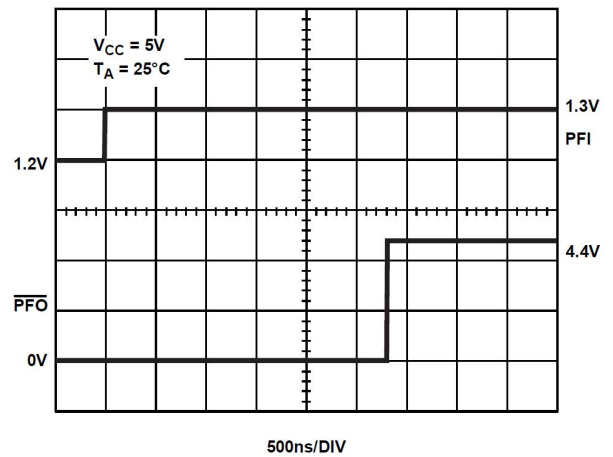


Figure 9. PFI Comparator Deassertion Response Time

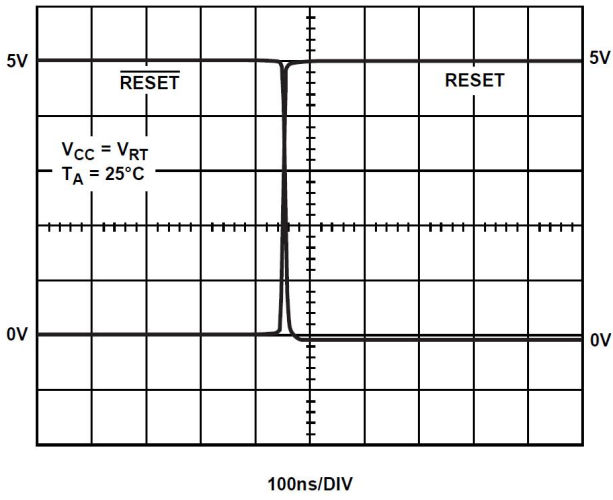


Figure 10. $\overline{\text{RESET}}$, RESET Assertion

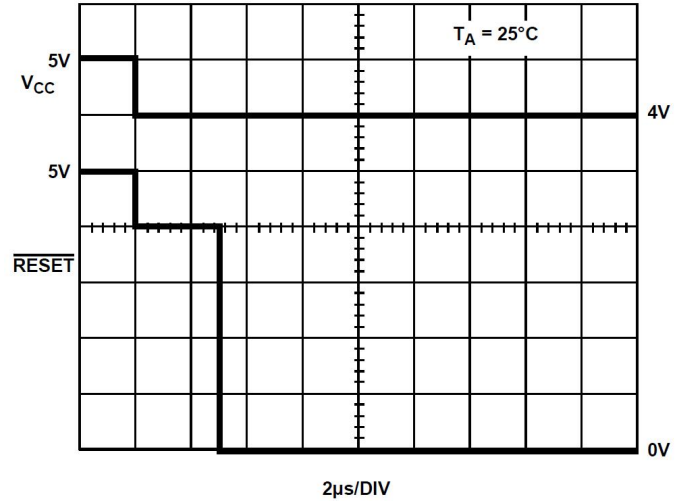


Figure 12. CBM705/CBM707 $\overline{\text{RESET}}$ Response Time

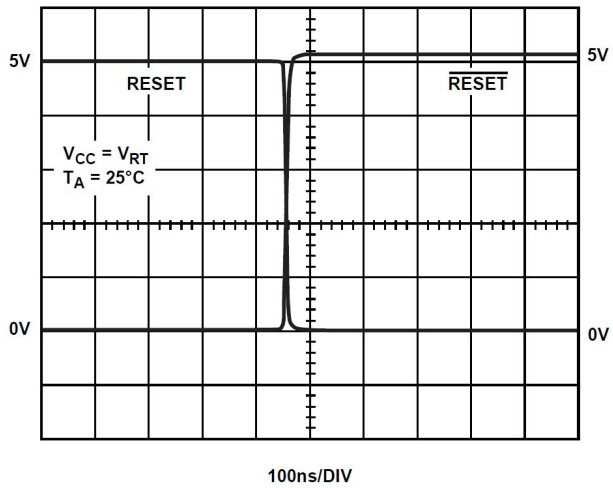


Figure 11. $\overline{\text{RESET}}$, RESET Deassertion

CIRCUIT INFORMATION

POWER FAIL RESET OUTPUT

$\overline{\text{RESET}}$ is an active low output that provides a reset signal to the microprocessor whenever the V_{CC} input is below the reset threshold. An internal timer holds $\overline{\text{RESET}}$ low for 200 ms after the voltage on V_{CC} rises above the threshold. This functions as a power-on reset signal for the microprocessor. It allows time for both the power supply and the microprocessor to stabilize after power-up. The $\overline{\text{RESET}}$ output is guaranteed to remain valid (low) with V_{CC} as low as 1V. This ensures that the microprocessor is held in a stable shutdown condition as the power supply voltage ramps up.

In addition to $\overline{\text{RESET}}$, an active high RESET output is also available on the CBM707/CBM708. This is the complement of $\overline{\text{RESET}}$ and is useful for processors requiring an active high reset signal.

MANUAL RESET

The manual reset input ($\overline{\text{MR}}$) allows other reset sources, such as a manual reset switch, to generate a processor reset. The input is effectively debounced by the timeout period (200 ms typically). The $\overline{\text{MR}}$ input is TTL-/CMOS-compatible, so it can also be driven by any logic reset output.

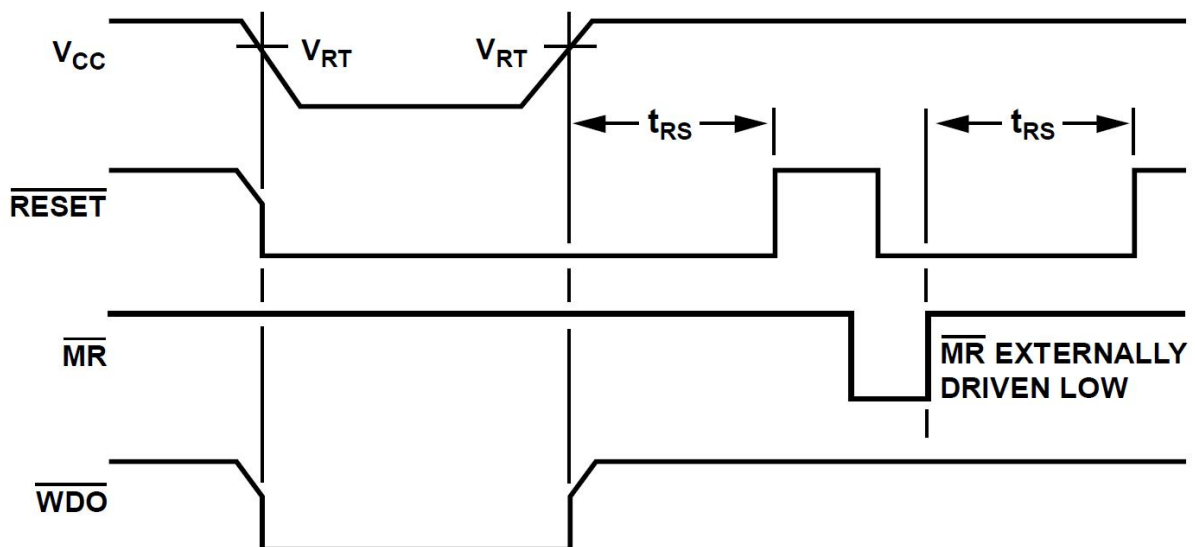


Figure 13. RESET, MR, and WDO Timing

WATCHDOG TIMER (CBM705/CBM706)

The watchdog timer circuit can monitor the activity of the micro-processor to check that it is not stalled in an indefinite loop. An output line on the processor toggles the watchdog input (WDI) line. If this line is not toggled within the timeout period (1.60 sec), then the watchdog output (\overline{WDO}) goes low. The \overline{WDO} can be connected to a nonmaskable interrupt (NMI) on the processor; therefore, if the watchdog timer times out, an interrupt is generated. The interrupt service routine then rectifies the problem.

If a \overline{RESET} signal is required when a timeout occurs, the \overline{WDO} must connect to the manual reset input (\overline{MR}).

The watchdog timer is cleared by either a high to low or a low to high transition on WDI. It is also cleared by \overline{RESET} going low; therefore, the watchdog timeout period begins after \overline{RESET} goes high.

When V_{CC} falls below the reset threshold, \overline{WDO} is forced low, whether or not the watchdog timer has timed out. Normally, this generates an interrupt, but it is overridden by \overline{RESET} going low.

The watchdog monitor can be deactivated by floating the WDI. The \overline{WDO} can then be used as a low line output because it goes low only when V_{CC} falls below the reset threshold.

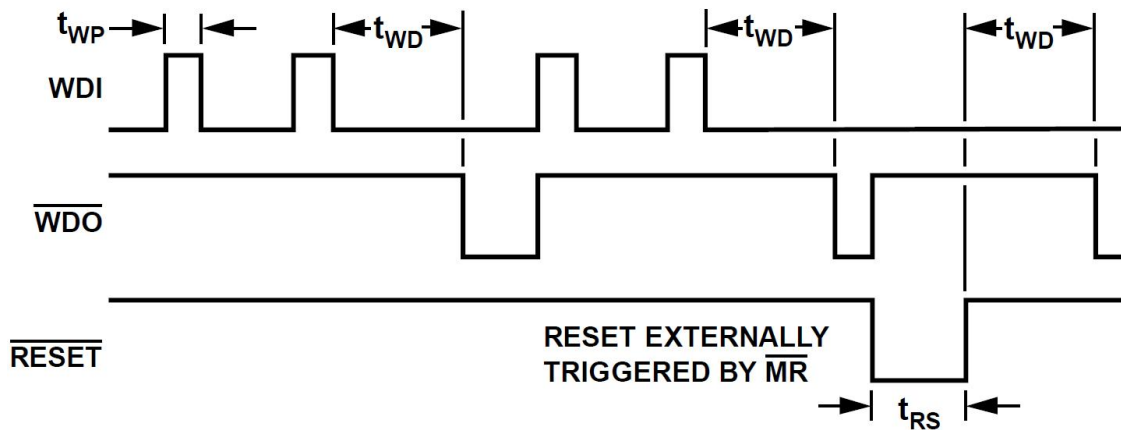


Figure 14. Watchdog Timing

POWER FAIL COMPARATOR

The power fail comparator is an independent comparator that can monitor the input power supply. The comparator inverting input is internally connected to a 1.25V reference voltage. The noninverting input is available at the PFI input. This input can monitor the input power supply via a resistive divider network. When the voltage on the PFI input drops below 1.25V, the comparator output ($\overline{\text{PFO}}$) goes low, indicating a power failure. For early warning of power failure, the comparator monitors the preregulator input by choosing an appropriate resistive divider network. The $\overline{\text{PFO}}$ output can interrupt the processor so a shutdown procedure is implemented before power is lost.

As the voltage on the PFI pin is limited to $V_{CC} + 0.3V$, it is recommended to connect the PFI pin with a Schottky diode to the $\overline{\text{RESET}}$ pin as shown in Figure 15. This helps clamping the PFI pin voltage during device power up and operation.

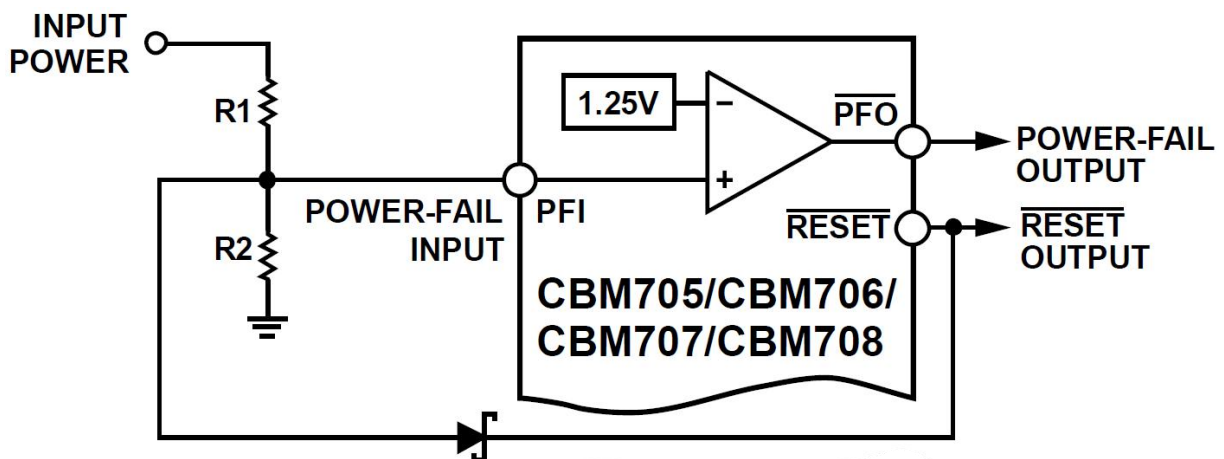


Figure 15. Power Fail Comparator

Adding Hysteresis to the Power Fail Comparator

For increased noise immunity, hysteresis can be added to the power fail comparator. Because the comparator circuit is noninverting, hysteresis can be added by connecting a resistor between the $\overline{\text{PFO}}$ output and the PFI input as shown in Figure 16.

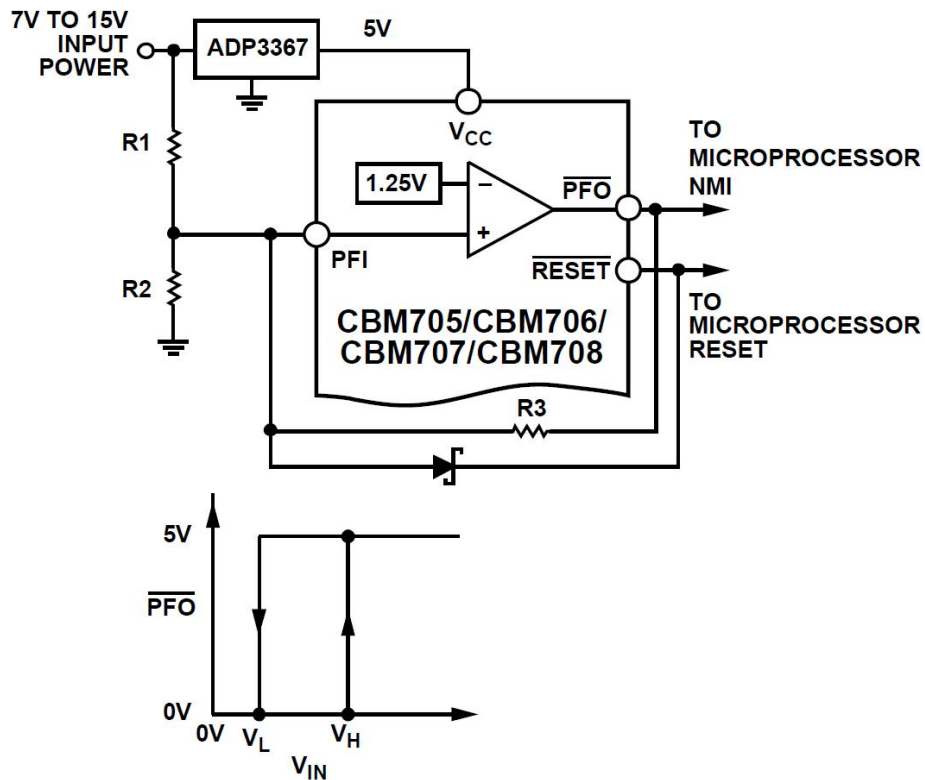


Figure 16. Adding Hysteresis to the Power Fail Comparator

When $\overline{\text{PFO}}$ is low, Resistor R3 sinks current from the summing junction at the PFI pin. When $\overline{\text{PFO}}$ is high, Resistor R3 sources current into the PFI summing junction. This results in differing trip levels for the comparator. Further noise immunity can be achieved by connecting a capacitor between PFI and GND. The equations calculate the hysteresis are as follows:

$$V_H = 1.25 \left[1 + \left(\frac{R_2 + R_3}{R_2 \times R_3} \right) R_1 \right]$$

$$V_L = 1.25 + R_1 \left(\frac{1.25}{R_2} - \frac{V_{CC} - 1.25}{R_3} \right)$$

$$V_{MID} = 1.25 \left(\frac{R_1 + R_2}{R_2} \right)$$

VALID RESET BELOW 1V V_{CC}

The CBM705/CBM706/CBM707/CBM708 are guaranteed to provide a valid reset level with V_{CC} as low as 1 V (see the Typical Performance Characteristics section). As V_{CC} drops below 1V, the internal transistor does not have sufficient drive to hold the voltage $\overline{\text{RESET}}$ at 0V. A pull-down resistor can connect externally, as shown in Figure 17, to hold the line low if required.

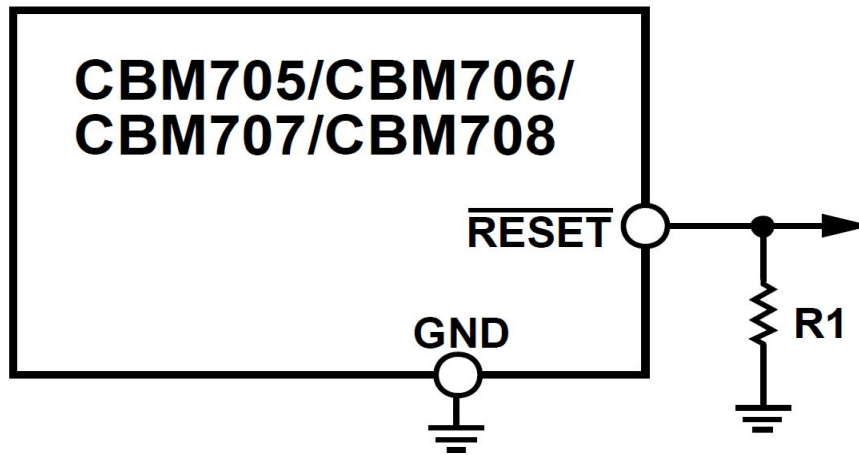


Figure 17. RESET Valid Below 1V

APPLICATIONS INFORMATION

A typical application circuit is shown in Figure 18. The un-regulated dc input supply is monitored using PFI via the resistive divider network. Resistor R1 and Resistor R2 must be selected so when the supply voltage drops below the desired level (such as 8V), the voltage on PFI drops below the 1.25V threshold, thereby generating an interrupt to the microprocessor. Monitoring the preregulator input provides additional time to execute an orderly shutdown procedure before power is lost.

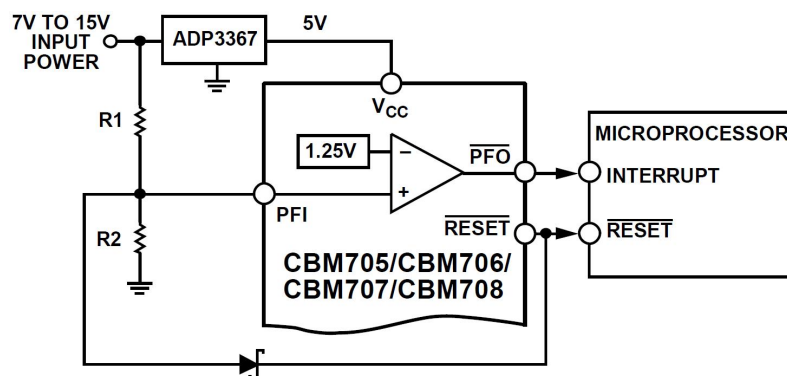


Figure 18. Typical Application Circuit

Microprocessor activity is monitored using WDI. This is driven using an output line from the processor. The software routines toggle this line at least once every 1.60 seconds. If a problem occurs and this line is not toggled, \overline{WDO} goes low and a nonmaskable interrupt is generated. This interrupt routine can clear the problem.

If in the event of inactivity on the WDI line, a system reset is required, \overline{WDO} must connect to \overline{MR} as shown in Figure 19.

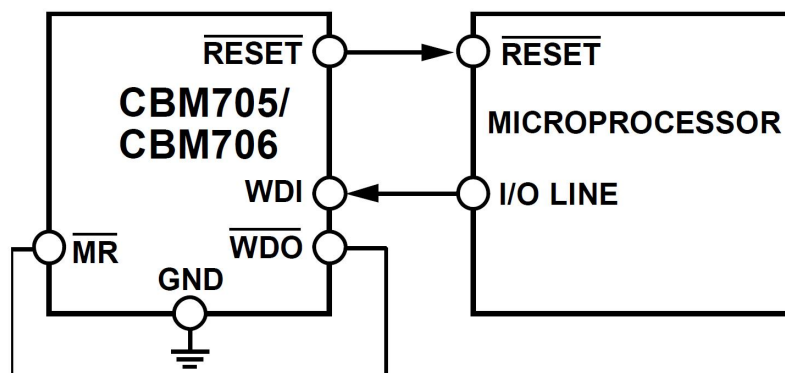


Figure 19. RESET From \overline{WDO}

MONITORING ADDITIONAL SUPPLY LEVELS

It is possible to use the power fail comparator to monitor a second supply as shown in Figure 20. The two sensing resistors, R1 and R2, are selected so the voltage on PFI drops below 1.25V at the minimum acceptable input supply. $\overline{\text{PFO}}$ can connect to $\overline{\text{MR}}$ so a reset is generated when the supply drops out of tolerance. In this case, if either supply drops out of tolerance, a reset is generated.

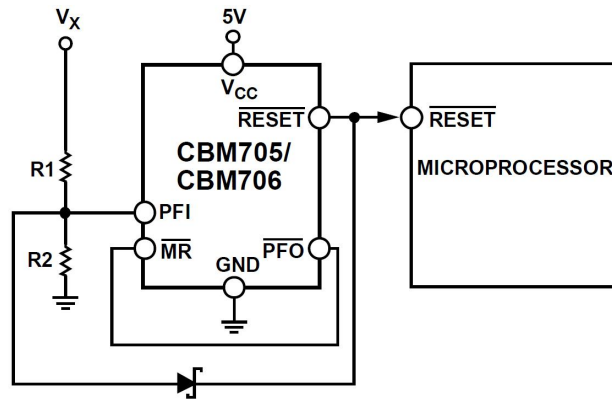


Figure 20. Monitoring 5 V and an Additional Supply, V_x

MICROPROCESSOR WITH BIDIRECTIONAL RESET

To prevent contention for microprocessors with a bidirectional reset line, a current limiting resistor must be inserted between the CBM705/ CBM706/ CBM707/ CBM708 $\overline{\text{RESET}}$ output pin and the microprocessor $\overline{\text{RESET}}$ pin. This limits the current to a safe level if there are conflicting output reset levels. A suitable resistor value is 4.7k Ω . If the reset output is required for other uses, it must be buffered, as shown in Figure 21.

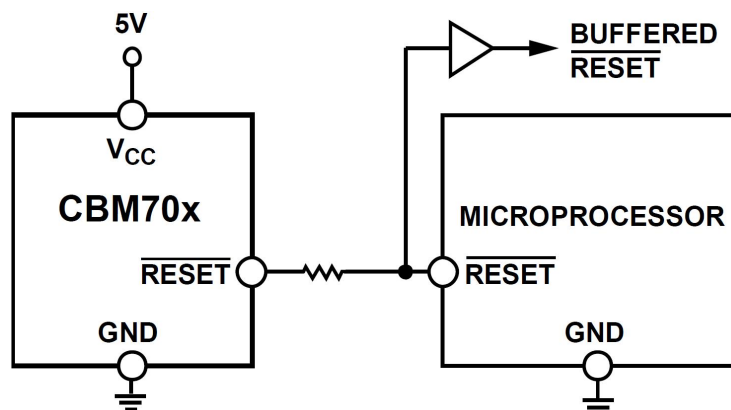
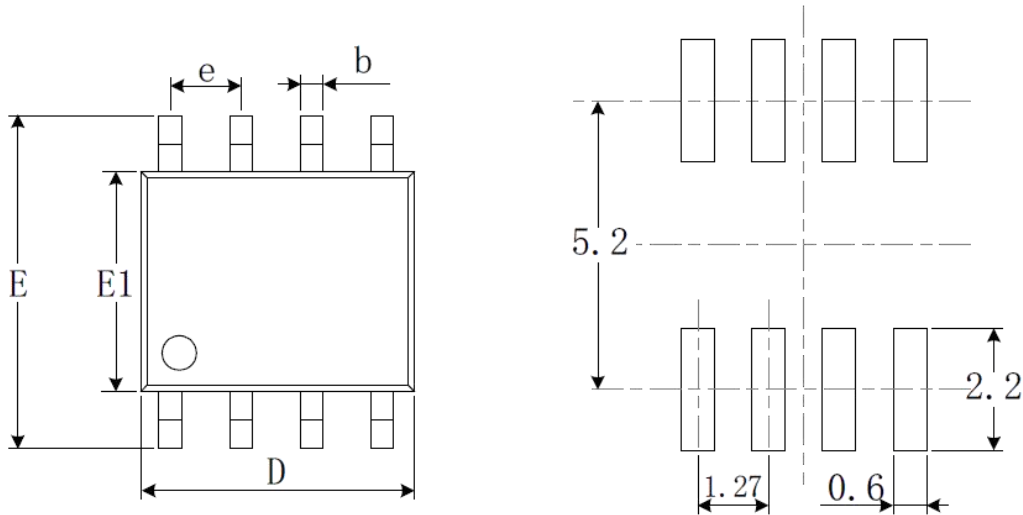


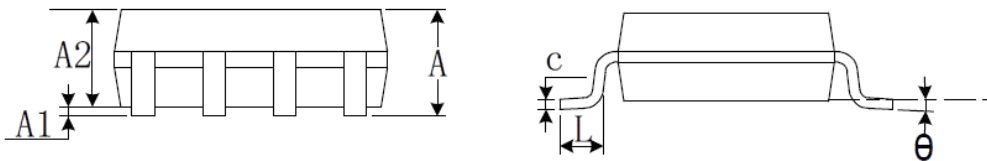
Figure 21. Bidirectional Input/Output $\overline{\text{RESET}}$

OUTLINE DIMENSIONS

SOIC-8(SOP8)

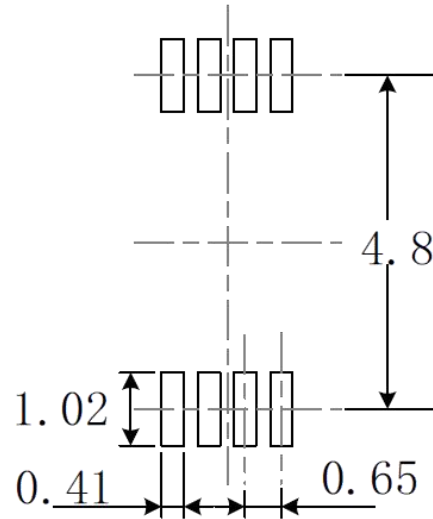
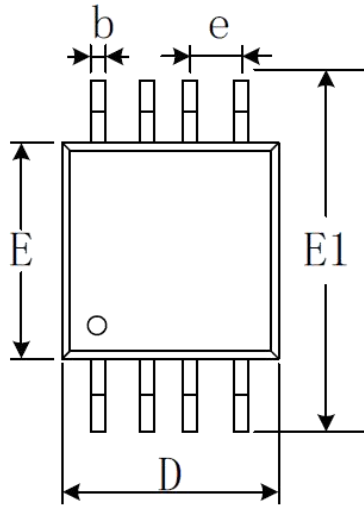


RECOMMENDED LAND PATTERN (Unit: mm)

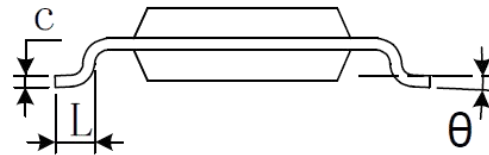
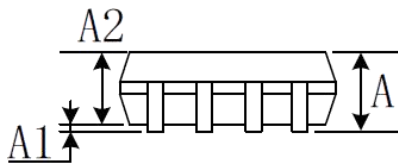


Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

MSOP-8



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

PACKAGE/ORDERING INFORMATION

PRODUCT	ORDERING NUMBER	TEMPRANGE	PACKAGE	PAKEAGE MARKING	TRANSPOT MEDIA,QUANTILY
CBM705	CBM705AS8	-40°C~125°C	SOIC-8(SOP8)	CBM705A	Tape and Reel,2500
	CBM705AMS8	-40°C~125°C	MSOP-8	705AM	Tape and Reel,3000
CBM706	CBM706AS8	-40°C~125°C	SOIC-8(SOP8)	CBM706A	Tape and Reel,2500
	CBM706AMS8	-40°C~125°C	MSOP-8	706AM	Tape and Reel,3000
CBM707	CBM707AS8	-40°C~125°C	SOIC-8(SOP8)	CBM707A	Tape and Reel,2500
	CBM707AMS8	-40°C~125°C	MSOP-8	707AM	Tape and Reel,3000
CBM708	CBM708AS8	-40°C~125°C	SOIC-8(SOP8)	CBM708A	Tape and Reel,2500
	CBM708AMS8	-40°C~125°C	MSOP-8	708AM	Tape and Reel,3000