

# SiT2002B

High Frequency, Single Chip, SOT23 Oscillator



## Features

- Any frequency between 115 MHz to 137 MHz accurate to 6 decimal places of accuracy
- Operating temperature from -40°C to 85°C.  
Refer to [SiT2019](#) for -40°C to 125°C and [SiT2021](#) for -55°C to 125°C options
- Excellent total frequency stability as low as  $\pm 20$  PPM
- Low power consumption of 4.9 mA typical at 1.8 V
- LVC MOS/LVTTL compatible output
- 5-pin SOT23-5: 2.9 mm x 2.8 mm
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free
- For AEC-Q100 oscillators, refer to [SiT2024](#) and [SiT2025](#)

## Applications

- GEAPON, network switches, routers, servers, embedded systems, industrial and medical devices
- Ethernet, PCI-E, DDR, etc.

Related products for [automotive applications](#).

For aerospace and defense applications SiTime recommends using only [Endura™ SiT2044](#).



## Electrical Specifications

**Table 1. Electrical Characteristics**

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Frequency Range</b>						
Output Frequency Range	f	115	–	137	MHz	
<b>Frequency Stability and Aging</b>						
Frequency Stability	F_stab	-20	–	+20	PPM	Inclusive of Initial tolerance at 25°C, 1st year aging at 25°C, and variations over operating temperature, rated power supply voltage and load (15 pF $\pm$ 10%).
		-25	–	+25	PPM	
		-50	–	+50	PPM	
<b>Operating Temperature Range</b>						
Operating Temperature Range (Ambient)	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
<b>Supply Voltage and Current Consumption</b>						
Supply Voltage	Vdd	1.62	1.8	1.98	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.7	3.0	3.3	V	
		2.97	3.3	3.63	V	
		2.25	–	3.63	V	
Current Consumption	Idd	–	6.2	7.5	mA	No load condition, f = 125 MHz, Vdd = 2.8 V, 3.0 V, 3.3 V or 2.25 to 3.63 V
		–	5.5	6.4	mA	No load condition, f = 125 MHz, Vdd = 2.5 V
		–	4.9	5.6	mA	No load condition, f = 125 MHz, Vdd = 1.8 V
OE Disable Current	I_od	–	–	4.3	mA	Vdd = 2.5 V to 3.3 V, OE = Low, Output in high Z state
		–	–	4.1	mA	Vdd = 1.8 V, OE = Low, Output in high Z state
Standby Current	I_std	–	2.6	4.3	$\mu$ A	Vdd = 2.8 V to 3.3 V, $\overline{ST}$ = Low, Output is weakly pulled down
		–	1.4	2.5	$\mu$ A	Vdd = 2.5 V, $\overline{ST}$ = Low, Output is weakly pulled down
		–	0.6	1.3	$\mu$ A	Vdd = 1.8 V, $\overline{ST}$ = Low, Output is weakly pulled down

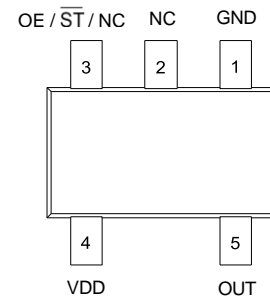
**Table 1. Electrical Characteristics (continued)**

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>LVC MOS Output Characteristics</b>						
Duty Cycle	DC	45	–	55	%	All Vdds
Rise/Fall Time	Tr, Tf	–	1.0	2.0	ns	Vdd = 2.5 V, 2.8 V, 3.0 V or 3.3 V, 20% - 80%
		–	1.3	2.5	ns	Vdd = 1.8 V, 20% - 80%
		–	1.0	2.0	ns	Vdd = 2.25 V - 3.63 V, 20% - 80%
Output High Voltage	VOH	90%	–	–	Vdd	IOH = -4 mA (Vdd = 3.0 V or 3.3 V) IOH = -3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOH = -2 mA (Vdd = 1.8 V)
Output Low Voltage	VOL	–	–	10%	Vdd	IOL = 4 mA (Vdd = 3.0 V or 3.3 V) IOL = 3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOL = 2 mA (Vdd = 1.8 V)
<b>Input Characteristics</b>						
Input High Voltage	VIH	70%	–	–	Vdd	Pin 1, OE or $\overline{ST}$
Input Low Voltage	VIL	–	–	30%	Vdd	Pin 1, OE or $\overline{ST}$
Input Pull-up Impedance	Z_in	50	87	150	kΩ	Pin 1, OE logic high or logic low, or $\overline{ST}$ logic high
		2	–	–	MΩ	Pin 1, $\overline{ST}$ logic low
<b>Startup and Resume Timing</b>						
Startup Time	T_start	–	–	5	ms	Measured from the time Vdd reaches its rated minimum value
Enable/Disable Time	T_oe	–	–	130	ns	f = 115 MHz. For other frequencies, T_oe = 100 ns + 3 * clock periods
Resume Time	T_resume	–	–	5	ms	Measured from the time $\overline{ST}$ pin crosses 50% threshold
<b>Jitter</b>						
RMS Period Jitter	T_jitt	–	1.9	3	ps	f = 125 MHz, Vdd = 2.5 V, 2.8 V, 3.0 V or 3.3 V
		–	1.6	4	ps	f = 125 MHz, Vdd = 1.8 V
Peak-to-peak Period Jitter	T_pk	–	12	20	ps	f = 125 MHz, Vdd = 2.5 V, 2.8 V, 3.0 V or 3.3 V
		–	14	30	ps	f = 125 MHz, Vdd = 1.8 V
RMS Phase Jitter (random)	T_phj	–	0.5	0.9	ps	Integration bandwidth = 900 kHz to 7.5 MHz
		–	1.3	2	ps	Integration bandwidth = 12 kHz to 20 MHz

**Table 2. Pin Description**

Pin	Symbol		Functionality
1	GND	Power	Electrical ground
2	NC	No Connect	No connect
3	OE / $\overline{ST}$ / NC	Output Enable	H <sup>[1]</sup> : specified frequency output L: output is high impedance. Only output driver is disabled.
		Standby	H or Open <sup>[1]</sup> : specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std.
		No Connect	Any voltage between 0 and Vdd or Open <sup>[1]</sup> : Specified frequency output. Pin 3 has no function.
4	VDD	Power	Power supply voltage <sup>[2]</sup>
5	OUT	Output	Oscillator output

**Top View**



**Figure 1. Pin Assignments**

**Notes:**

1. In OE or  $\overline{ST}$  mode, a pull-up resistor of 10 kΩ or less is recommended if pin 3 is not externally driven. If pin 3 needs to be left floating, use the NC option.
2. A capacitor of value 0.1 μF or higher between Vdd and GND is required.

**Table 3. Absolute Maximum Limits**

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
Vdd	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Junction Temperature <sup>[3]</sup>	–	150	°C

Note:

- Exceeding this temperature for extended period of time may damage the device.

**Table 4. Thermal Consideration<sup>[4]</sup>**

Package	$\theta_{JA}$ , 4 Layer Board (°C/W)	$\theta_{JC}$ , Bottom (°C/W)
SOT23-5	421	175

Note:

- Refer to JESD51 for  $\theta_{JA}$  and  $\theta_{JC}$  definitions, and reference layout used to determine the  $\theta_{JA}$  and  $\theta_{JC}$  values in the above table.

**Table 5. Maximum Operating Junction Temperature<sup>[5]</sup>**

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	80°C
85°C	95°C

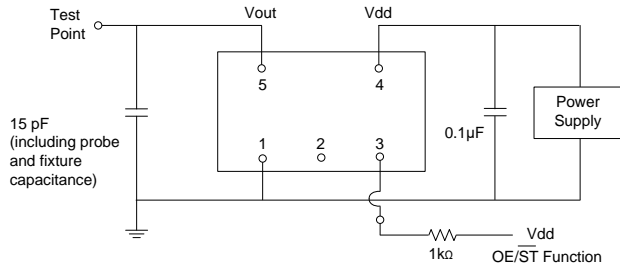
Note:

- Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

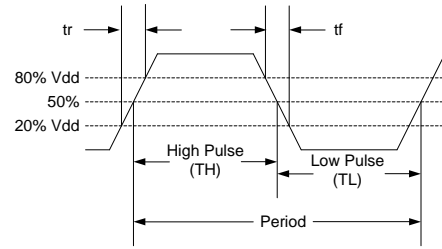
**Table 6. Environmental Compliance**

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method2002
Mechanical Vibration	MIL-STD-883F, Method2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method2003
Moisture Sensitivity Level	MSL1 @ 260°C

### Test Circuit and Waveform



**Figure 2. Test Circuit<sup>[6]</sup>**

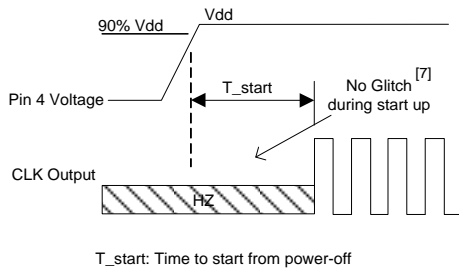


**Figure 3. Output Waveform<sup>[6]</sup>**

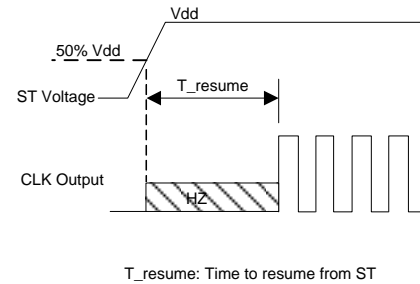
**Note:**

6. Duty Cycle is computed as  $Duty\ Cycle = TH/Period$ .

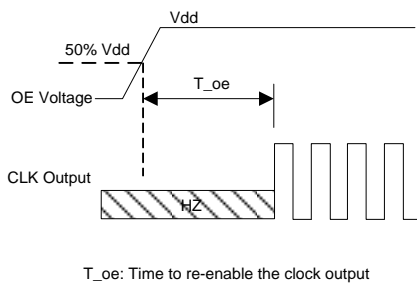
### Timing Diagrams



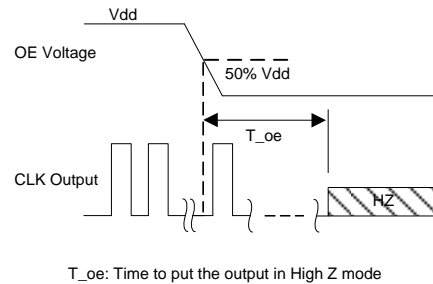
**Figure 4. Startup Timing (OE/ST Mode)**



**Figure 5. Standby Resume Timing (ST Mode Only)**



**Figure 6. OE Enable Timing (OE Mode Only)**

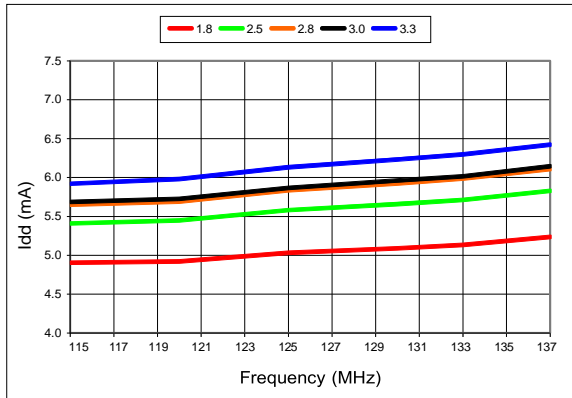


**Figure 7. OE Disable Timing (OE Mode Only)**

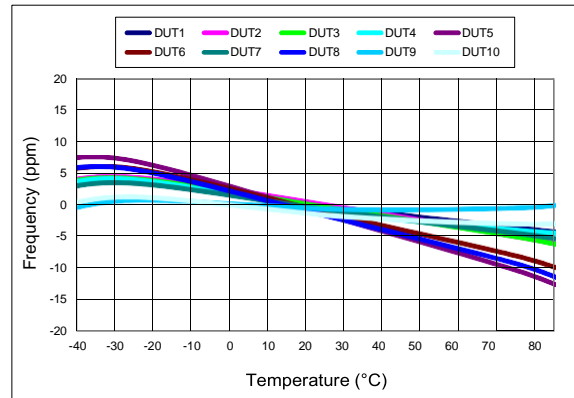
**Note:**

7. SiT2002 has “no runt” pulses and “no glitch” output during startup or resume.

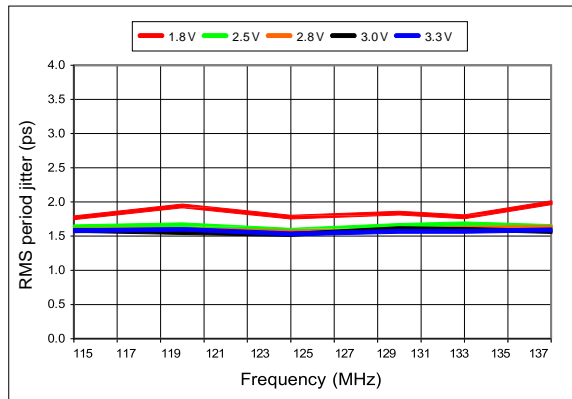
**Performance Plots<sup>[8]</sup>**



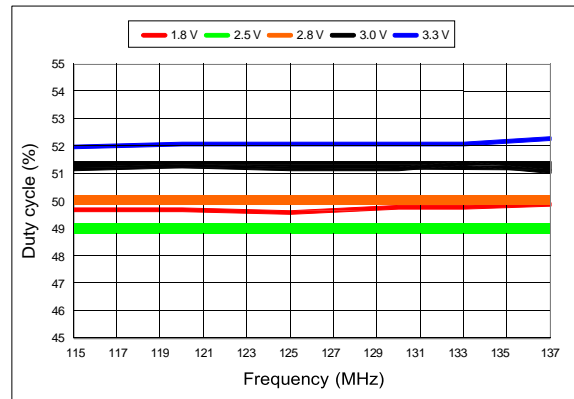
**Figure 8. Idd vs Frequency**



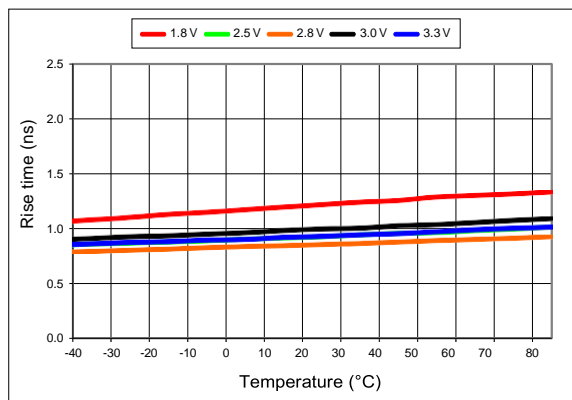
**Figure 9. Frequency vs Temperature, 1.8V**



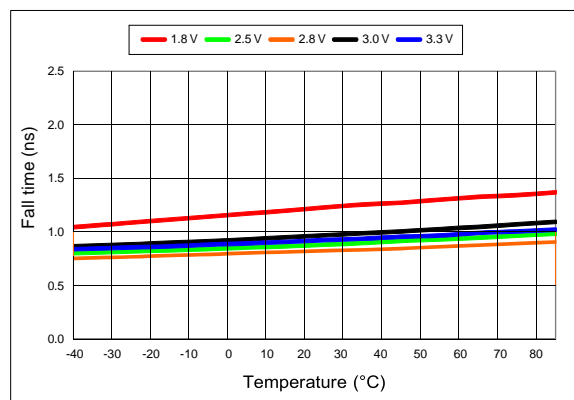
**Figure 10. RMS Period Jitter vs Frequency**



**Figure 11. Duty Cycle vs Frequency**

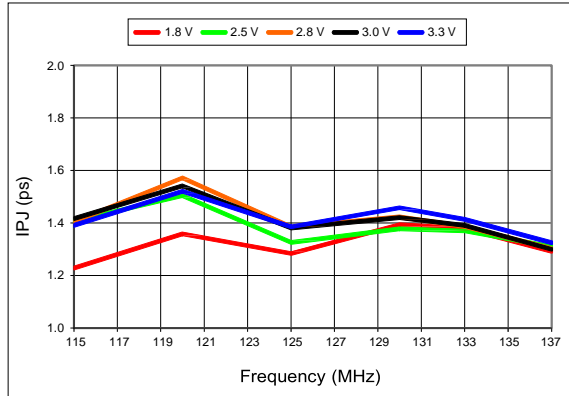


**Figure 12. 20%-80% Rise Time vs Temperature**

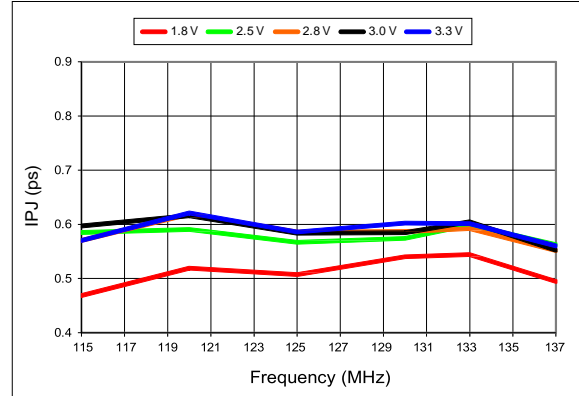


**Figure 13. 20%-80% Fall Time vs Temperature**

**Performance Plots<sup>[8]</sup>**



**Figure 14. RMS Integrated Phase Jitter Random (12 kHz to 20 MHz) vs Frequency<sup>[9]</sup>**



**Figure 15. RMS Integrated Phase Jitter Random (900 kHz to 20 MHz) vs Frequency<sup>[9]</sup>**

**Notes:**

- 8. All plots are measured with 15 pF load at room temperature, unless otherwise stated.
- 9. Phase noise plots are measured with Agilent E5052B signal source analyzer.

## Programmable Drive Strength

The SiT2002 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time.
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the [SiTime Application Notes](#) section.

### Reduction by Slowing Rise/Fall Time

Figure 16 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11<sup>th</sup> clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

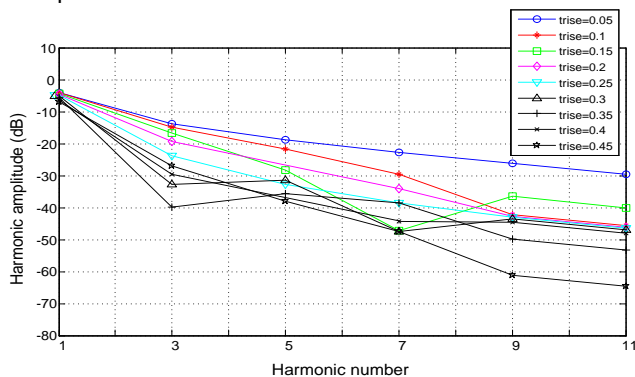


Figure 16. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

### Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to speed up the rise/fall time of the input clock. Some chipsets may also require faster rise/fall time in order to reduce their sensitivity to this type of jitter. Refer to the [Rise/Fall Time Tables \(Table 7 to 11\)](#) to determine the proper drive strength.

### High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3 V SiT2002 device with default drive strength setting, the typical rise/fall time is 1ns for 15 pF output load. The typical rise/fall time slows down to 2.6 ns when the output load increases to 45 pF. One can choose to speed up the rise/fall time to 1.83 ns by then increasing the drive strength setting on the SiT2002.

The SiT2002 can support up to 30 pF maximum capacitive loads with drive strength settings. Refer to the [Rise/Fall Time Tables \(Table 7 to 11\)](#) to determine the proper drive strength for the desired combination of output load vs. rise/fall time.

### SiT2002 Drive Strength Selection

Tables 7 through 11 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the SiT2002 nominal supply voltage (1.8 V, 2.5 V, 2.8 V, 3.0 V, 3.3 V).
2. Select the capacitive load column that matches the application requirement (5 pF to 30 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

### Calculating Maximum Frequency

Based on the rise and fall time data given in [Tables 7 through 11](#), the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature can be determined as follows:

$$\text{Max Frequency} = \frac{1}{5 \times \text{Trf}_{20/80}}$$

where Trf<sub>20/80</sub> is the typical value for 20%-80% rise/fall time.

### Example 1

Calculate f<sub>MAX</sub> for the following condition:

- Vdd = 3.3 V ([Table 11](#))
- Capacitive Load: 30 pF
- Desired Tr/f time = 1.31 ns (rise/fall time part number code = F)

Part number for the above example:

SiT2002BIF12-18E-137.000000



Drive strength code is inserted here. Default setting is “-”

## Rise/Fall Time (20% to 80%) vs C<sub>LOAD</sub> Tables

**Table 7. V<sub>dd</sub> = 1.8 V Rise/Fall Times for Specific C<sub>LOAD</sub>**

Rise/Fall Time Typ (ns)			
Drive Strength \ C <sub>LOAD</sub>	5 pF	15 pF	30 pF
T	0.93	n/a	n/a
E	0.78	n/a	n/a
U	0.70	1.48	n/a
F or "-": default	0.65	1.30	n/a

**Table 8. V<sub>dd</sub> = 2.5 V Rise/Fall Times for Specific C<sub>LOAD</sub>**

Rise/Fall Time Typ (ns)			
Drive Strength \ C <sub>LOAD</sub>	5 pF	15 pF	30 pF
R	1.45	n/a	n/a
B	1.09	n/a	n/a
T	0.62	1.28	n/a
E	0.54	1.00	n/a
U or "-": default	0.43	0.96	n/a
F	0.34	0.88	n/a

**Table 9. V<sub>dd</sub> = 2.8 V Rise/Fall Times for Specific C<sub>LOAD</sub>**

Rise/Fall Time Typ (ns)			
Drive Strength \ C <sub>LOAD</sub>	5 pF	15 pF	30 pF
R	1.29	n/a	n/a
B	0.97	n/a	n/a
T	0.55	1.12	n/a
E	0.44	1.00	n/a
U or "-": default	0.34	0.88	n/a
F	0.29	0.81	1.48

**Table 10. V<sub>dd</sub> = 3.0 V Rise/Fall Times for Specific C<sub>LOAD</sub>**

Rise/Fall Time Typ (ns)			
Drive Strength \ C <sub>LOAD</sub>	5 pF	15 pF	30 pF
R	1.22	n/a	n/a
B	0.89	n/a	n/a
T or "-": default	0.51	1.00	n/a
E	0.38	0.92	n/a
U	0.30	0.83	n/a
F	0.27	0.76	1.39

**Table 11. V<sub>dd</sub> = 3.3 V Rise/Fall Times for Specific C<sub>LOAD</sub>**

Rise/Fall Time Typ (ns)			
Drive Strength \ C <sub>LOAD</sub>	5 pF	15 pF	30 pF
R	1.16	n/a	n/a
B	0.81	n/a	n/a
T or "-": default	0.46	1.00	n/a
E	0.33	0.87	n/a
U	0.28	0.79	1.46
F	0.25	0.72	1.31

**Note:**

- "n/a" in Table 7 to Table 11 indicates that the resulting rise/fall time from the respective combination of the drive strength and output load does not provide rail-to-rail swing and is not available.



### Pin 1 Configuration Options (OE, $\overline{ST}$ , or NC)

Pin 3 of the SiT2002 can be factory-programmed to support three modes: Output Enable (OE), standby ( $\overline{ST}$ ) or No Connect (NC). These modes can also be programmed with the Time Machine using field programmable devices.

#### Output Enable (OE) Mode

In the OE mode, applying logic Low to the OE pin only disables the output driver and puts it in Hi-Z mode. The core of the device continues to operate normally. Power consumption is reduced due to the inactivity of the output. When the OE pin is pulled High, the output is typically enabled in  $<1\mu\text{s}$ .

#### Standby ( $\overline{ST}$ ) Mode

In the  $\overline{ST}$  mode, a device enters into the standby mode when Pin 3 pulled Low. All internal circuits of the device are turned off. The current is reduced to a standby current, typically in the range of a few  $\mu\text{A}$ . When  $\overline{ST}$  is pulled High, the device goes through the “resume” process, which can take up to 5 ms.

#### No Connect (NC) Mode

In the NC mode, the device always operates in its normal mode and outputs the specified frequency regardless of the logic level on pin 3.

Table 12 below summarizes the key relevant parameters in the operation of the device in OE,  $\overline{ST}$ , or NC mode.

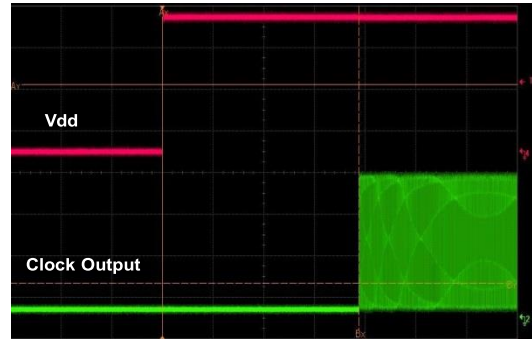
**Table 12. OE vs.  $\overline{ST}$  vs. NC**

	OE	ST	NC
Active current 20 MHz (max, 1.8 V)	5.6 mA	5.6 mA	5.6 mA
OE disable current (max, 1.8 V)	4.1 mA	N/A	N/A
Standby current (typical 1.8 V)	N/A	0.6 $\mu\text{A}$	N/A
OE enable time at 110 MHz (max)	130 ns	N/A	N/A
Resume time from standby (max, all frequency)	N/A	5 ms	N/A
Output driver in OE disable/standby mode	High Z	weak pull-down	N/A

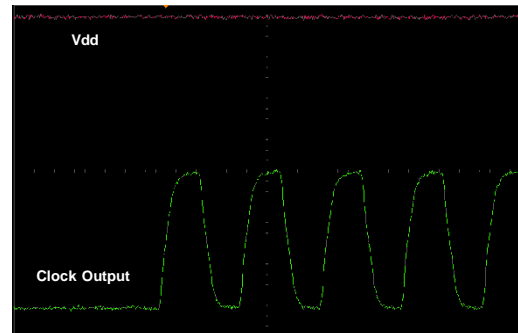
### Output on Startup and Resume

The SiT2002 comes with gated output. Its clock output is accurate to the rated frequency stability within the first pulse from initial device startup or resume from the standby mode.

In addition, the SiT2002 supports “no runt” pulses and “no glitch” output during startup or resume as shown in the waveform captures in Figure 17 and Figure 18.

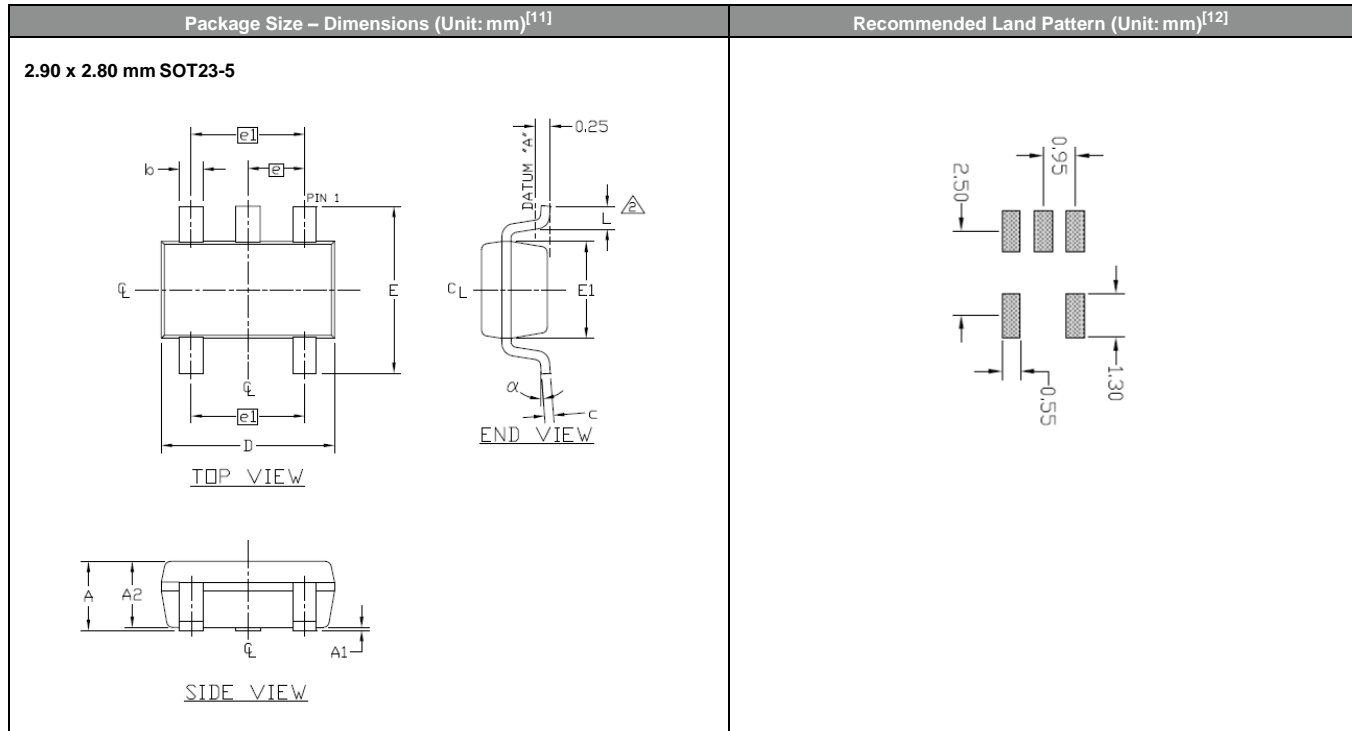


**Figure 17. Startup Waveform vs. Vdd**



**Figure 18. Startup Waveform vs. Vdd (Zoomed-in View of Figure 17)**

### Dimensions and Patterns



**Notes:**

- 11. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
- 12. A capacitor value of 0.1  $\mu$ F between Vdd and GND is required.

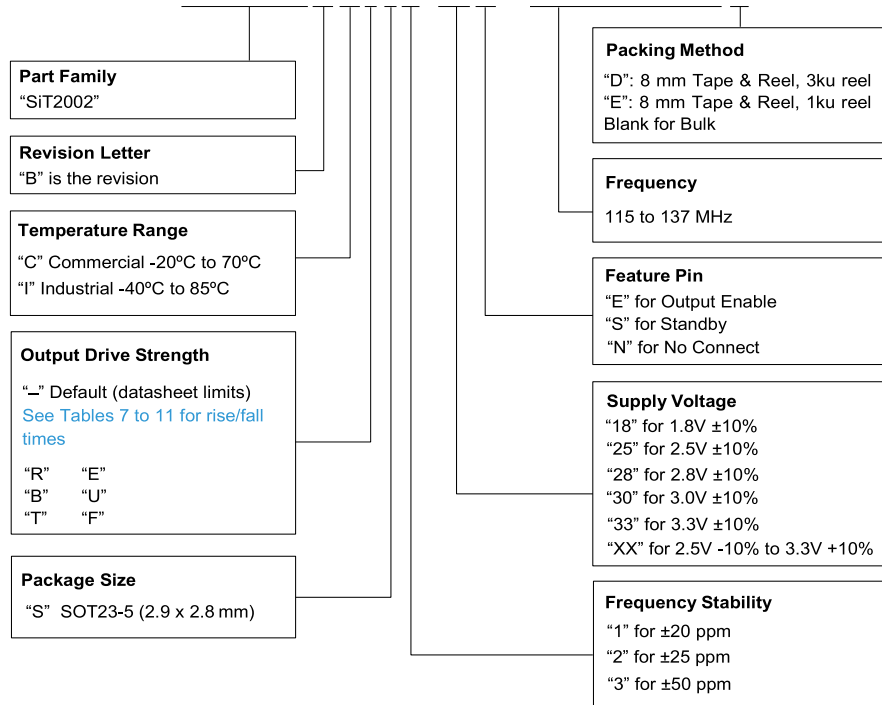
**Table 13. Dimension Table**

Symbol	Min.	Nom.	Max.
A	0.90	1.27	1.45
A1	0.00	0.07	0.15
A2	0.90	1.20	1.30
b	0.30	0.35	0.50
c	0.14	0.15	0.20
D	2.75	2.90	3.05
E	2.60	2.80	3.00
E1	1.45	1.60	1.75
L	0.30	0.38	0.55
L1	0.25 REF		
e	0.95 BSC.		
e1	1.90 BSC.		
$\alpha$	0°	0°	0°

## Ordering Information

The Part No. Guide is for reference only. To customize and build an exact part number, use the [SiTime Part Number Generator](#).

### SiT2002BC-S2-18E - 125.123456 D



**Table 14. Additional Information**

Document	Description	Download Link
Time Machine II	MEMS oscillator programmer	<a href="http://www.sitime.com/support/time-machine-oscillator-programmer">http://www.sitime.com/support/time-machine-oscillator-programmer</a>
Field Programmable Oscillators	Devices that can be programmable in the field by Time Machine II	<a href="http://www.sitime.com/products/field-programmable-oscillators">http://www.sitime.com/products/field-programmable-oscillators</a>
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	<a href="https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products">https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products</a>
Qualification Reports	RoHS report, reliability reports, composition reports	<a href="http://www.sitime.com/support/quality-and-reliability">http://www.sitime.com/support/quality-and-reliability</a>
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	<a href="http://www.sitime.com/support/performance-measurement-report">http://www.sitime.com/support/performance-measurement-report</a>
Termination Techniques	Termination design recommendations	<a href="http://www.sitime.com/support/application-notes">http://www.sitime.com/support/application-notes</a>
Layout Techniques	Layout recommendations	<a href="http://www.sitime.com/support/application-notes">http://www.sitime.com/support/application-notes</a>

**Table 15. Revision History**

Revision	Release Date	Change Summary
1.0	14-May-2015	Final Production Release
1.01	29-Sep-2015	Revised the dimension table
1.02	19-Apr-2018	Changed Clock Generator to SOT23 Oscillator Updated logo and company address, other page layout changes
1.03	1-Jan-2023	Updated company disclaimer, links, references and icons

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# Supplemental Information

The Supplemental Information section is not part of the datasheet and is for informational purposes only.

## Best Reliability

Silicon is inherently more reliable than quartz. Unlike quartz suppliers, SiTime has in-house MEMS and analog CMOS expertise, which allows SiTime to develop the most reliable products. Figure 1 shows a comparison with quartz technology.

### Why is SiTime MEMS Best in Class:

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal™ process, which eliminates foreign particles and improves long term aging and reliability
- World-class MEMS and CMOS design expertise

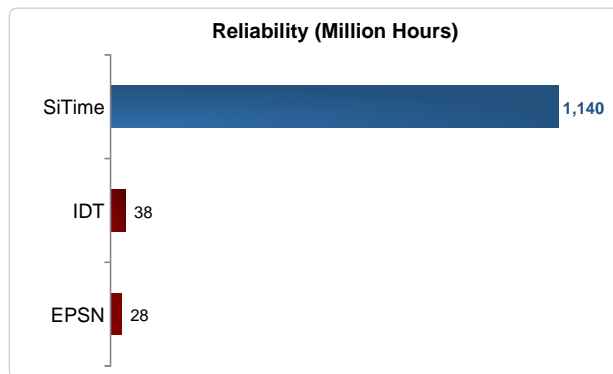


Figure 1. Reliability Comparison<sup>[1]</sup>

## Best Aging

Unlike quartz, MEMS oscillators have excellent long term aging performance which is why every new SiTime product specifies 10-year aging. A comparison is shown in Figure 2.

### Why is SiTime MEMS Best in Class:

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal™ process, which eliminates foreign particles and improves long term aging and reliability
- Inherently better immunity of electrostatically driven MEMS resonator

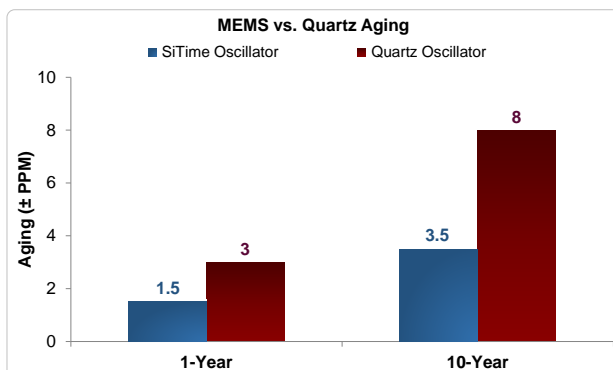


Figure 2. Aging Comparison<sup>[2]</sup>

## Best Electro Magnetic Susceptibility (EMS)

SiTime's oscillators in plastic packages are up to 54 times more immune to external electromagnetic fields than quartz oscillators as shown in Figure 3.

### Why is SiTime MEMS Best in Class:

- Internal differential architecture for best common mode noise rejection
- Electrostatically driven MEMS resonator is more immune to EMS

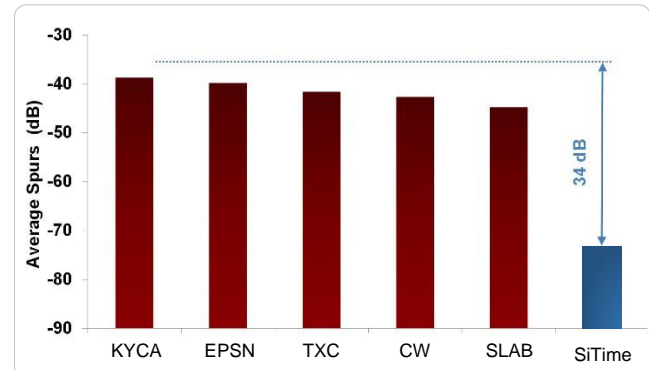


Figure 3. Electro Magnetic Susceptibility (EMS)<sup>[3]</sup>

## Best Power Supply Noise Rejection

SiTime's MEMS oscillators are more resilient against noise on the power supply. A comparison is shown in Figure 4.

### Why is SiTime MEMS Best in Class:

- On-chip regulators and internal differential architecture for common mode noise rejection
- MEMS resonator is paired with advanced analog CMOS IC

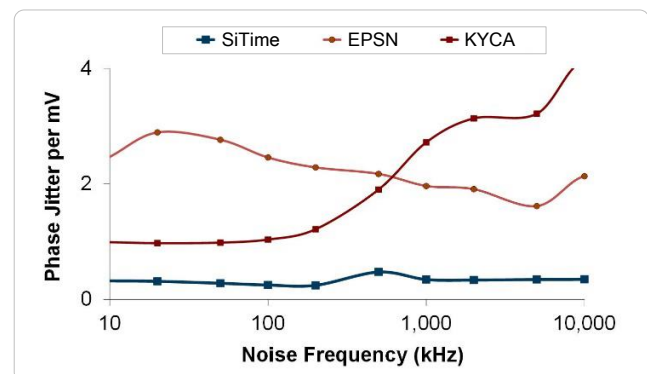


Figure 4. Power Supply Noise Rejection<sup>[4]</sup>

## Best Vibration Robustness

High-vibration environments are all around us. All electronics, from handheld devices to enterprise servers and storage systems are subject to vibration. Figure 5 shows a comparison of vibration robustness.

### Why is SiTime MEMS Best in Class:

- The moving mass of SiTime’s MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

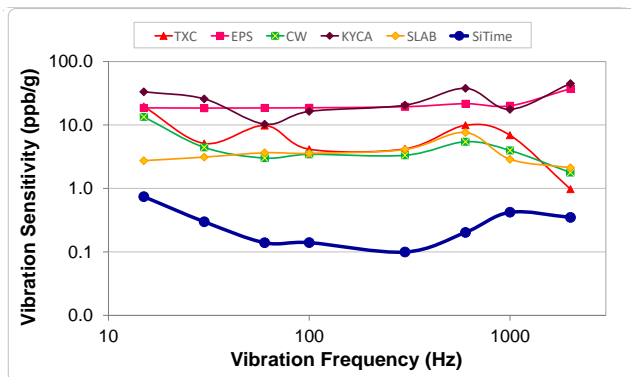


Figure 5. Vibration Robustness<sup>[5]</sup>

### Figure labels:

- TXC = TXC
- Epson = EPSN
- Connor Winfield = CW
- Kyocera = KYCA
- SiLabs = SLAB
- SiTime = EpiSeal MEMS

## Best Shock Robustness

SiTime’s oscillators can withstand at least 50,000 g shock. They all maintain their electrical performance in operation during shock events. A comparison with quartz devices is shown in Figure 6.

### Why is SiTime MEMS Best in Class:

- The moving mass of SiTime’s MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

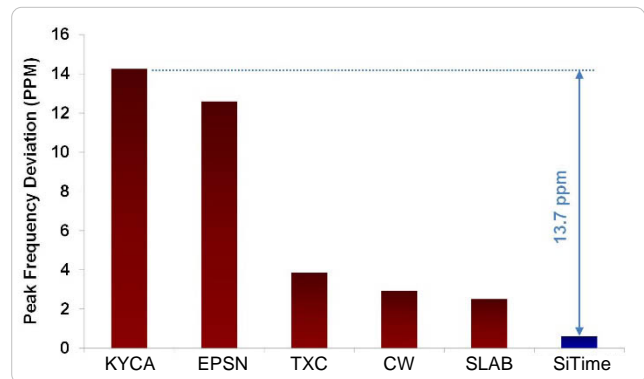


Figure 6. Shock Robustness<sup>[6]</sup>

**Notes:**

1. Data source: Reliability documents of named companies.
2. Data source: SiTime and quartz oscillator devices datasheets.
3. Test conditions for Electro Magnetic Susceptibility (EMS):
  - According to IEC EN61000-4.3 (Electromagnetic compatibility standard)
  - Field strength: 3V/m
  - Radiated signal modulation: AM 1 kHz at 80% depth
  - Carrier frequency scan: 80 MHz – 1 GHz in 1% steps
  - Antenna polarization: Vertical
  - DUT position: Center aligned to antenna

**Devices used in this test:**

Label	Manufacturer	Part Number	Technology
EpiSeal MEMS	SiTime	SIT9120AC-1D2-33E156.250000	MEMS + PLL
EPSN	Epson	EG-2102CA156.2500M-PHPAL3	Quartz, SAW
TXC	TXC	BB-156.250MBE-T	Quartz, 3 <sup>rd</sup> Overtone
CW	Conner Winfield	P123-156.25M	Quartz, 3 <sup>rd</sup> Overtone
KYCA	AVX Kyocera	KC7050T156.250P30E00	Quartz, SAW
SLAB	SilLab	590AB-BDG	Quartz, 3 <sup>rd</sup> Overtone + PLL

4. 50 mV pk-pk Sinusoidal voltage.

**Devices used in this test:**

Label	Manufacturer	Part Number	Technology
EpiSeal MEMS	SiTime	SIT8208AI-33-33E-25.000000	MEMS + PLL
NDK	NDK	NZ2523SB-25.6M	Quartz
KYCA	AVX Kyocera	KC2016B25M0C1GE00	Quartz
EPSN	Epson	SG-310SCF-25M0-MB3	Quartz

5. Devices used in this test:  
same as EMS test stated in Note 3.
6. Test conditions for shock test:
  - MIL-STD-883F Method 2002
  - Condition A: half sine wave shock pulse, 500-g, 1ms
  - Continuous frequency measurement in 100  $\mu$ s gate time for 10 seconds

**Devices used in this test:**

same as EMS test stated in Note 3.

7. Additional data, including setup and detailed results, is available upon request to qualified customer. Please contact [productsupport@sitime.com](mailto:productsupport@sitime.com).