





THE NEXT-GENERATION PROCESSOR TO MEET THE NEEDS OF THE SMART SOCIETY HAS ARRIVED.



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The utilization of intelligent technology is advancing in all aspects of our lives, including electric household appliances, industrial equipment, building management, power grids, and transportation. The cloud-connected "smart society" is coming ever closer to realization. Microcontrollers are now expected to provide powerful capabilities not available previously, such as high-performance and energy-efficient control combined with interoperation with IT networks, support for human-machine interfaces, and more. To meet the demands of this new age, Renesas has drawn on its unmatched expertise in microcontrollers to create the RZ family of embedded processors. The lineup of these "next-generation processors that are as easy to use as conventional microcontrollers" to meet different customer requirements.

The Zenith of the Renesas micro

As embedded processors to help build the next generation of advanced products, the RZ family offers features not available elsewhere and brings new value to customer applications.

RZ/V Series



64-bit Cortex®-A CPU, up to 1GHz Low-power Embedded AI for Vision-AI Application

RZ/G Series



32/64-bit Cortex®-A CPU, up to 1.5Hz 3D Graphics for HMI Application

RZ/A Series



32-bit Cortex®-A CPU, up to 528MHz 10MB Embedded RAM for HMI Application

RZ/T Series



32-bit Cortex®-R CPU, up to 600MHz Real-time Control Multi-protocol Encoder I/F for AC Servo, Actuator, Inverter

RZ/N Series



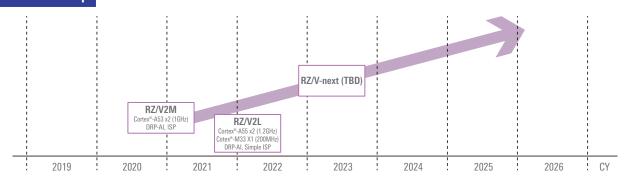
32-bit Cortex®-A/M CPU, up to 500MHz Multi-protocol Industrial Network for PLC, Remote IO, Gateway

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RZ/V Series

RZ/V Series Roadmap



RZ/V Series Features

- Al Accelerator "DRP-Al" achieves high-speed Al inference and low power consumption
- 4K (2160p30) video codec and high-performance image signal processor (ISP) (RZ/V2M)
- Provides image signal processor (Simple ISP) function with DRP library (RZ/V2L)
- Equipped with a 3D Graphics Engine for fast image rendering (RZ/V2L)
- Adopts Civil Infrastructure Platform (CIP) Linux kernel that can be supported for more than 10 years
- * DRP: Dynamically Reconfigurable Processor



RZ/V Series Application







Surveillance camera



Retail



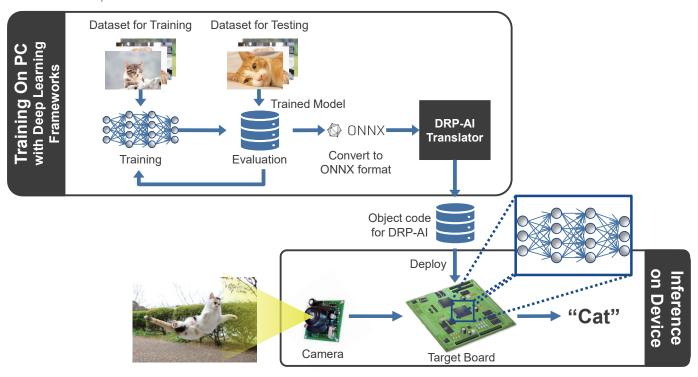
Logistics



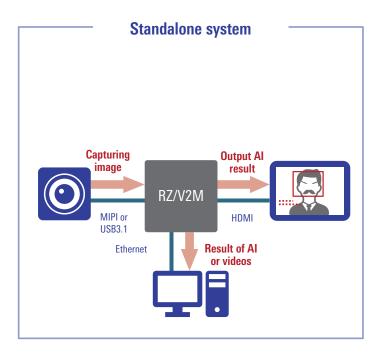
Image inspection

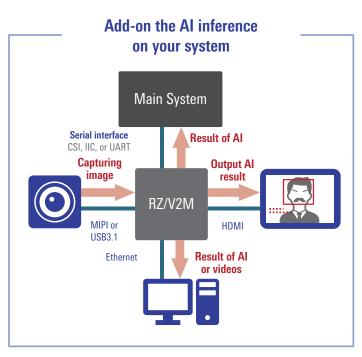
Al Development Flow

- Open frameworks can be used for learning
- Converts from industry standard ONNX Format to executable with DRP-AI Translator



Use Case







RZ/V2M Group

CPU

■ 2× Cortex-A53 (up to 1.0GHz)

Vision and AI

- Al Accelerator; DRP-Al at 1.0 TOPS/W class
- Image Signal Processor (ISP) of multi-stream available
- Camera Interface; 2× MIPI CSI-2
- Face and Human Detection Engine

Video and Graphics

- H.265/H.264 Multi Codec
- JPEG Codec Engine
- 2D Graphics Engine

Display Interface

- MIPI-DSI (4-lane)
- HDMI 1.4a

Audio Interface

■ Serial Sound Interface × 1ch

Communication Interface

- SD Host × 2ch
- PCI-Express 2.0 (1-lane) × 1ch
- Gigabit Ethernet × 1ch
- USB3.1 Gen1 Host/Function × 1ch
- I^2C Bus × 4ch
- SCI × 6ch
- UART × 2ch

Memory Interface

- NAND Flash Interface ONFI1.0 × 1ch
- eMMC 4.5.1 × 1ch
- 32-bit LPDDR4-3200 × 1ch

Security

■ Hardware Security Engine

RZ/V2L Group

CPU

- 2× Cortex-A55 or 1× Cortex-A55 (up to 1.2GHz)
- 1× Cortex-M33 (up to 200MHz)

Vision and AI

- Al Accelerator; DRP-Al
 - * Image Signal Processor (Simple ISP) Function is provided as DRP Library
- Camera Interface; 1× MIPI CSI-2 / 1× Digital Parallel

Video and Graphics

- H.264 Codec
- 3D Graphics Engine

Display Interface

- MIPI-DSI (4-lane)
- Digital Parallel

Audio Interface

Serial Sound Interface × 4ch

Communication Interface

- Gigabit Ethernet × 2ch
- USB2.0 Host × 1ch
- USB2.0 Host/Function × 1ch
- I^2C Bus × 4ch
- SCI × 2ch
- UART × 5ch

Memory Interface

- SPI Multi I/O (8bit DDR) × 1ch
- SDHI (UHS-I) / eMMC × 1ch
- 16-bit DDR3L-1333/DDR4-1600 × 1ch Security
- Hardware Security Engine (Option)

RZ/V2M block diagram

System	Cl	PU	Peripheral I/F
ARM debugger (CoreSight)	Arm® Cortex®-A53: 1GHz	Arm® Cortex®-A53: 1GHz	SDI (2ch)
DMAC (16ch)	L1 I\$: 32KB L1 D\$: 32KB	L1 I\$: 32KB L1 D\$: 32KB	USB3.1 (1ch)
Power control	NEON FPU	NEON FPU	(Host/Peripheral)
	L2\$: 5	512KB	PCIe Gen2 (2Lane)
Timers			Gbit Ethernet MAC (1ch)
Timer (32ch)	RAMA 200KB	RAMB 1MB	I2C (4ch)
PWM (16ch)	NAIVIA ZUUND	NAIVID IIVID	CSI (6ch)
WDT (2ch)	Sensing and Analyzing		UART (2ch)
Image Sensor I/F	Al-accelera	tor (DRP-AI)	GPI0
MIPI CSI-2 v1.2	General Processing Accelerator	Multi-target detection (Face, Person's body)	Motor Controller
(4Lanes, 2ch)	Accelerator	(race, reison's body)	Environment Sensor I/F
Display I/F	Video and	l Graphics	
HDMI v1.4a TX (1ch)	Camera ISP	2D Graphics engine	External Memory I/F
	H.264/265 Multi Codec	JPEG Codec	LPDDR4 (32-bit)
Audio I/F			eMMC (1ch)
I2S (1ch)	Sec	urity	
	Trusted	Secure IP	Analog
			ADC (20ch,12bit)
			Temperature sensor (2ch)

RZ/V2L block diagram

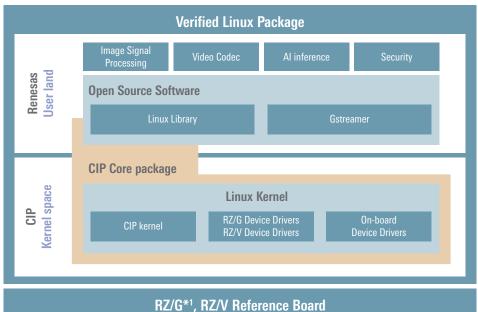
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System	CF	טי		Peripheral I/F
ARM debugger (CoreSight)	Arm® Cortex®-A55: 1.2GHz Arm®	® Cortex®-A55: 1.2GHz	Arm®	SDHI (UHS-I, 1ch)
DMAC (16ch)	L1 I\$: 32KB L1 D\$: 32KB L1 I	φ. JZND LI Dφ. JZND	ortex®	USB2.0 (Host, 1ch)
Power control	NEON FPU N	FUN II FPU III	-M33 00MHz	USB2.0 (Host/Peripheral, 1ch)
Timers	L3\$: 256KB w		70111112	Gbit Ethernet MAC (2ch)
32-bit Timer (1ch)	Mem	nries		I2C (4ch)
16-bit Timer (8ch)	RAM 128I			SCI 8/9-bit (2ch)
PWM (8ch)				SCIF(UART) (5ch)
WDT (3ch)	Sensing and	, 0		RSPI (3ch)
WDT (36H)	Al-accelerator (DRP-AI)		CAN-FD (2ch)	
Image Sensor I/F	Video and Graphics		GPI0	
MIPI CSI-2 (4Lanes, 1ch)	Image Scaling Unit (5M pixel)	3D GPU (Mali™-G3	31)	E / 1 M 1/E
Parallel (HD-30fps, 1ch)	H.264 Enc/Dec (1920	× 1080pixel, 30fps)		External Memory I/F
Display I/F				DDR3L/DDR4-1600 (16-bit)
	Security	(Option)		SPI Multi I/O (8-bit DDR, 1ch)
MIPI DSI-2 (4Lanes, 1ch)	Secure Boot	Device Unique ID)	SDHI (UHS-I) / eMMC (1ch)
Parallel (WXGA-60fps, 1ch)	Crypto Engine	JTAG Disable		Analan
Audio I/F	TRNG	OTP 4K-bit		Analog 12-bit ADC (8ch)
SSI (I2S, 4ch)				
SRC (1ch)				Thermal Sensor (1ch)
(/				

Super Long Term Software Support

Renesas RZ/G2 and RZ/V2 microprocessors are the only embedded MPUs that meet the long-term support demands for industrial and infrastructure equipment manufacturers through the 10+ year support offered by the Super Long Term Support (SLTS) kernel maintained by the Civil Infrastructure Platform (CIP). The CIP SLTS Linux kernel supports countermeasures against vulnerability to security attacks with a longterm maintenance period of 10 years or more. This reduces Linux maintenance costs and simplifies adoption of reliable industrial-grade Linux.

Verified Linux Package(VLP) Reduces Cost and Simplifies Design

The "Verified Linux Package (VLP)" for the RZ/G and RZ/V series is a combination of the Civil Infrastructure Platform (CIP) Core Package and the basic software (Linux BSP, multimedia, graphics, security, etc.) for IoT devices. This packaged software is verified by Renesas and is available. With VLPs, you can start developing applications guickly while minimizing Linux maintenance resources.



Multimedia

- H.264 Codec (up to 1080p)
- H.265 Codec (up to 2160p)
- 2D graphics

Al Inference

DRP-AI

CIP SLTS Kernel

- Civil Infrastructure Platform project
- 10+ years super long term support Reliability/Security/Real-time

Development Environment for Al

- DRP-Al Translator Converts ONNX* format into object code for DRP-AI.
- * ONNX: Open Neural Network Exchange



DRP-AI Translator









Trained model

DRP-AI **Object Code**

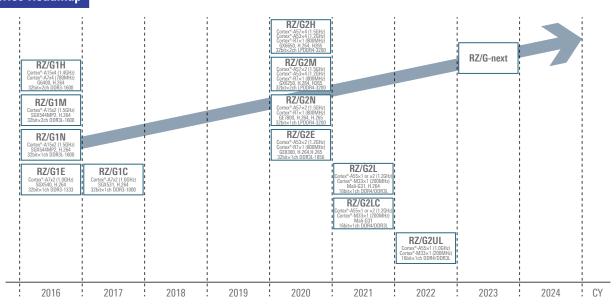
RZ/V2M **Evaluation Board**

^{*1:} RZ/G Reference Board is used for Kernel development as a software development platform for CIP projects.



RZ/G Series

RZ/G Series Roadmap



RZ/G2 Platform Highlights

- High Performance
 - 64-bit Arm Cortex-A cores, plus powerful 3D graphics engine and video engine capable of supporting up to 4K UHD, to offer the highest performance
- Wide Coverage
 - Entry-level RZ/G2L Group 3 products equipped with Cortex-A55 with improved processing performance have been newly added to the RZ/G2 lineup
- High Reliability
 - Built-in Error Correction Code (ECC) for internal and external memory, which is essential for high-reliability mission critical systems
- Super Long Term Support (SLTS)
 - Applying Civil Infrastructure Platform (CIP) Linux, the Linux kernel will be provided with over 10 years of support
- Verified Linux Package
- Renesas verifies and provides a Linux package that combines CIP and Linux basic software. Minimize your Linux maintenance resources

RZ/G2 Group Specification 1

Items	RZ/G2H	RZ/G2M	RZ/G2N	RZ/G2E
CPU (Arm® Cortex®-A)	4× Cortex®-A57@1.5GHz 4× Cortex®-A53@1.2GHz L1,L2 Parity/ECC	2× Cortex®-A57@1.5GHz 4× Cortex®-A53@1.2GHz L1,L2 Parity/ECC	2× Cortex®-A57@1.5GHz L1,L2 Parity/ECC	2× Cortex®-A53@1.2GHz L1,L2 Parity/ECC
CPU (Arm® Cortex®-R)	1× Cortex®-R7@800MHz L1,TCM w/ECC	1× Cortex®-R7@800MHz L1,TCM w/ECC	1× Cortex®-R7@800MHz L1,TCM w/ECC	1× Cortex®-R7@800MHz L1,TCM w/ECC
DRAM I/F	32-bit ×2ch LPDDR4(3200) w/ECC	32-bit ×2ch LPDDR4(3200) w/ECC	32-bit ×1ch LPDDR4(3200) w/ECC	32-bit ×1ch DDR3L(1856) w/ECC
Video in	2×MIPI-CSI2, 2×Digital (RGB/YCbCr) up to 8 input image can be captured	2×MIPI-CSI2, 2×Digital (RGB/YCbCr) up to 8 input image can be captured	2×MIPI-CSI2, 2×Digital (RGB/YCbCr) up to 8 input image can be captured	1×MIPI-CSI2, 1×Digital(RGB/YCbCr) up to 2 input image can be captured
Video Codec	Support up to 4k resolutions Decoding: H.265, Encoding and Decoding: H.264	Support up to 4k resolutions Decoding: H.265, Encoding and Decoding: H.264	Support up to 4k resolutions Decoding: H.265, Encoding and Decoding: H.264	Support up to FHD resolutions Decoding: H.265, Encoding and Decoding: H.264
3D GFX	PowerVR GX6650@600MHz	PowerVR GX6250@600MHz	PowerVR GE7800@600MHz	PowerVR GE8300@600MHz
Display out	1×HDMI, 1×LVDS, 1×Digital RGB	1×HDMI, 1×LVDS, 1×Digital RGB	1×HDMI, 1×LVDS, 1×Digital RGB	2×LVDS or 1×LVDS, 1×Digital RGB
USB	USB2.0×2ch (1H, 1H/F/OTG) USB3.0/2.0×1ch (DRD)	USB2.0×2ch (1H, 1H/F/OTG) USB3.0/2.0×1ch (DRD)	USB2.0×2ch (1H, 1H/F/OTG) USB3.0/2.0×1ch (DRD)	USB2.0×1ch (H/F) USB3.0/2.0×1ch (DRD)
Gbit Ether	1ch	1ch	1ch	1ch
CAN	2ch (support CAN-FD)	2ch (support CAN-FD)	2ch (support CAN-FD)	2ch (support CAN-FD)
PCle	2ch (Rev2.0 1Lane) one of the 2ch is shared with SATA	2ch (Rev2.0 1Lane)	2ch (Rev2.0 1Lane) one of the 2ch is shared with SATA	1ch (Rev2.0 1Lane)
SATA	1ch (Pin Shared)	No	1ch (Pin Shared)	No
Package	1022pin FCBGA, 29mm×29mm 0.8mm ball pitch	1022pin FCBGA, 29mm×29mm 0.8mm ball pitch	1022pin FCBGA, 29mm×29mm 0.8mm ball pitch	552pin FCBGA, 21mm×21mm 0.8mm ball pitch

RZ/G2 Group Specification 2

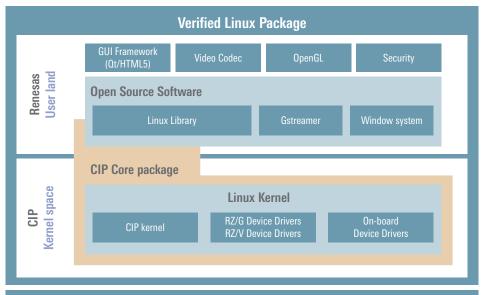
Items	RZ/G2L	RZ/G2LC	RZ/G2UL (Type2) Pin compatible with RZ/G2LC	RZ/G2UL (Type1) Full function
CPU (Arm® Cortex®-A)	1× or 2× Cortex®-A55@1.2GHz L1,L3 Parity/ECC	1× or 2× Cortex®-A55@1.2GHz L1,L3 Parity/ECC	1× Cortex®-A55@1.0GHz L1,L3 Parity/ECC	1× Cortex®-A55@1.0GHz L1,L3 Parity/ECC
CPU (Arm® Cortex®-M)	1× Cortex®-M33@200MHz	1× Cortex®-M33@200MHz	1× Cortex®-M33@200MHz	1× Cortex®-M33@200MHz
DRAM I/F	16-bit ×1ch DDR4-1600/DDR3L-1333 w/ECC	16-bit ×1ch DDR4-1600/DDR3L-1333 w/ECC	16-bit ×1ch DDR4-1600/DDR3L-1333 w/ECC	16-bit ×1ch DDR4-1600/DDR3L-1333 w/ECC
Video in	1×MIPI CSI-2 or 1×Digital Parallel input	1×MIPI CSI-2	1×MIPI CSI-2	1×MIPI CSI-2
Video Codec	Support up to Full HD @30fps resolutions Encoding and Decoding: H.264	_	_	_
3D GFX	Arm Mali-G31 GPU @500MHz	Arm Mali-G31 GPU @500MHz	_	_
Display out	1×MIPI DSI or 1×Digital Parallel output	1×MIPI DSI	_	1×Digital Parallel output
USB	USB2.0×2ch (1Host, 1Host/Function/OTG)	USB2.0×2ch (1Host, 1Host/Function/OTG)	USB2.0×2ch (1Host, 1Host/Function/OTG)	USB2.0×2ch (1Host, 1Host/Function/OTG)
Gbit Ether	2ch	1ch	1ch	2ch
CAN	2ch (support CAN-FD)	2ch (support CAN-FD)	2ch (support CAN-FD)	2ch (support CAN-FD)
12-bit ADC	8ch	_	-	2ch
Package	551pin LFBGA, 21mm×21mm 0.8mm ball pitch 456pin LFBGA, 15mm×15mm 0.5mm ball pitch	361pin LFBGA, 13mm×13mm 0.5mm ball pitch	361pin LFBGA, 13mm×13mm 0.5mm ball pitch	361pin LFBGA, 13mm×13mm 0.5mm ball pitch
		Pin Con	npatible	,

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GUI Framework

Multimedia

■ H.264 Codec

■ H.265 Decoder 3D graphics

Secure Middle Ware Encrypted kernel boot Security communication

Secure storage

 Ot application framework ■ HTML5 application framework

- CIP SLTS Kernel Civil Infrastructure Platform project
- 10+ years super long term support Reliability/Security/Real-time

RZ/G*1, RZ/V Reference Board

^{*1:} RZ/G Reference Board is used for Kernel development as a software development platform for CIP projects.



Flexible Development Kits

RZ/G2 development kits support the industry standard 96Boards specification and SMARC specification to enable evaluation and speed development with wide variety of mezzanine boards and existing carrier boards. Renesas provides circuit schematics, component BOMs, and board layout data to make it easy to spin your own custom hardware.

■ RZ/G2H,G2M,G2N Development Kit (96Boards format compatible)



- Main Memory: 4 GB DDR4
- QSPI NOR FLASH 64 MByte
- I²C EEPROM 512 Byte
- External Storage: micro SD × 1
- Connectivity: USB 2.0 × 2ch, USB 3.0 × 1ch, GbE × 1
- HDMI out / LVDS out or MIPI DSI out
- Wi-Fi + BT

■ RZ/G2E Development Kit (96Boards format compatible)



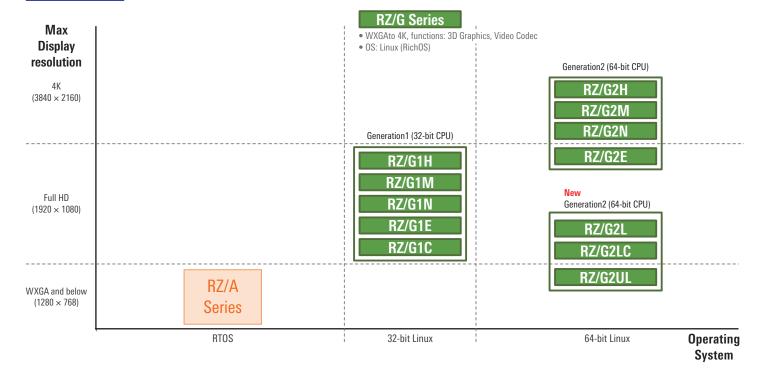
- Main Memory: 2 GB DDR3L
- QSPI NOR FLASH 64 MByte
- I²C EEPROM 512 Byte
- External Storage: micro SD × 1
- Connectivity: USB 2.0 × 2ch, USB 3.0 × 1ch, GbE × 1
- HDMI out / LVDS out or MIPI DSI out
- Wi-Fi + BT

■ RZ/G2L SMARC v2.1 Module board + Carrier Board



- Module board (Dimension: 82mm x 50mm)
 - Processor: RZ/G2L / RZ/G2LC / RZ/G2UL
 - Main Memory: 2GB DDR4 (1GB ×2)
 - QSPI NOR FLASH: 64MB
 - eMMC Memory: 64GB
 - External Storage: micro SD ×1
 - A/D Converter Interface ×6
 - JTAG connector
- Carrier board (Dimension: 160mm × 100mm)
 - Gigabit Ethernet ×2
 - USB2.0 \times 2ch (OTG \times 1ch, Host \times 1ch)
 - MIPI CSI-2 Camera connector (can connect to Google Coral Camera)
 - Micro HDMI (output) connector
 - CAN-FD ×2
 - External Storage: micro SD $\times 1$
 - Audio Line in ×1
 - Audio Line out $\times 1$
 - PMOD ×2
 - USB-Type C for Power Input

HMI Solutions



RZ/G2H (R8A774Ex)

CPU core

- Arm® Cortex®-A57, quad-core Max. operating frequency: 1.5GHz
- Arm® Cortex®-A53, quad-core Max. operating frequency: 1.2GHz
- Arm® Cortex®-R7, single-core Max. operating frequency: 800MHz
- Cache memory (Cortex®-A57)
- L1 instruction cache: 48KB
- L1 data cache: 32KB L2 cache: 2MB

Cache memory (Cortex®-A53)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L2 cache: 512KB
- Cache memory (Cortex®-R7)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- I-TCM: 32KB
- D-TCM: 32KB

External memory

- Ability to connect LPDDR4-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 2 channels External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 8/16 bits
- PCI Express 2.0 : 1 Lane × 2 channels (one of PHY is shared with Serial ATA) 3D graphics
- PowerVR[™] GX6650

Video functions

- Video display interface × 3 channels (1 channel: HDMI(option), 1 channel: LVDS, 1 channel: RGB888)
- Video input interface × 4 channels (2 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))

- Video codec module: VCP4 × 1 channel
- IP converter module
- Video image processing functions (color conversion, image enlargement/reduction, filtering)

Audio functions

- Sampling rate converter × 10 channels
- Serial sound interface × 10 channels Storage interfaces
- USB 3.0 DRD × 1 channel
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1channel)
- SD host interface × 4 channels
- Multimedia card interface × 2 channels
- Serial ATA interface × 1 channel Other peripheral functions
- 32-bit timer × 15 channels
- PWM timer × 7 channels
- I^2C bus interface × 7 channels
- Serial communication interface (SCIF) × 6 channels
- Quad serial peripheral interface (QSPI) × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.1Qav, and IEEE 1722)
- Controller area network (CAN) $interface \times 2 \ channels$
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- On-chip debug function

R7/G2H (R8A774Fx) block diagram

nz/dzii (noA//4L	A) block diagram		
System	СРИ		Connectivity
System controller	4 × Cortex®-A57 1.5GHz 4 × Cortex®-A53 1.3	2GHz 1 × Cortex ^o -R7 800MHz	2 × PCle2.0 (1Lane)
System RAM: 384KB	L1 I\$ 48KB L1 I\$ 32KI		SATA (Rev.3.2) (shared)
Thermal Sensor	L1 D\$ 32KB L1 D\$ 32K		USB3.0/2.0 (DRD)
JTAG Debug	NEON/VFPv4 NEON/VFP		4 × USB2.0 (2H, 2H/F/OTG)
(Coresight)	L2 cache: 2MB with ECC L2 cache: 512KB with	h ECC 1-TCM 32KB, D-TCM 32KB with ECC	Ethernet AVB (1Gbps)
Timers	3D Graphi	CS	2 × CAN2.0B
26 × 32-bit Timer	PowerVR GX		6 × UART, 5 × H-UART
15 × 32-bit Interval	2D/3D tile based	600MHz	$4 \times SPI$ $7 \times I^2C$; $1 \times DVFS$ ctrl
WDT	Video Cod	ec	7 × 1 6, 1 × DVI 3 CIII
7 × PWM out	Up to 4K resol	lution	Memory I/F
Audio IPs	(2 channel	s)	32-bit × 2ch LPDDR4-3200 (ECC)
Audio router w/10 ASRC,	Video IP		access cache
mixer, 10 I ² S (6ch TDM),	3 × Display out 1 × Digital out, 1 × LVDS	Video Signal Processor	16-bit ExtBus/SRAM
90ch Audio DMA	1 × HDMI 2 ×	Fine Display Processor	1 × QSPI (4/8-bit selectable)
Secure IP	8 × Video in		or 1 × Hyperflash
Crypto engine	2 × MIPI-CSI2 (1 × 4L, 1 × 2L)		4 × SDIO (SDR104)
(AES, DES, Hash, RSA, TRNG)	2 × Digital		2 × eMMC (5.0, HS400)

FC-BGA: 29 × 29mm² 1022-pins, 0.8mm pitch



RZ/G2M (R8A774Ax)

CPU core

- Arm® Cortex®-A57, quad-core Max. operating frequency: 1.5GHz
- Arm® Cortex®-A53, quad-core Max. operating frequency: 1.2GHz
- Arm® Cortex®-R7, single-core Max. operating frequency: 800MHz

Cache memory (Cortex®-A57)

- L1 instruction cache: 48KB
- L1 data cache: 32KB
- L2 cache: 2MB

Cache memory (Cortex®-A53)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L2 cache: 512KB

Cache memory (Cortex®-R7)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- I-TCM: 32KB
- D-TCM: 32KB

External memory

- Ability to connect LPDDR4-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 2 channels External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 8/16 bits
- PCI Express 2.0 : 1 Lane \times 2 channels (one of PHY is shared with Serial ATA)
- 3D graphics ■ PowerVR[™] GX6250

Video functions

- Video display interface × 3 channels (1 channel: HDMI(option), 1 channel: LVDS, 1 channel: RGB888)
- Video input interface × 4 channels (2 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))

- Video codec module: VCP4 × 1 channel
- IP converter module
- Video image processing functions (color conversion, image enlargement/ reduction, filtering)

Audio functions

- Sampling rate converter × 10 channels
- Serial sound interface × 10 channels Storage interfaces
- USB 3.0 DRD × 1 channel
- USB 2.0×2 channels (Host only 1 channel/Host-Function 1channel)
- SD host interface \times 4 channels
- Multimedia card interface × 2 channels Other peripheral functions
- 32-bit timer × 15 channels
- PWM timer × 7 channels
- I²C bus interface × 7 channels
- Serial communication interface (SCIF) × 6 channels
- Quad serial peripheral interface (QSPI) × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.10av, and IEEE 1722, GMII/MII interface, PHY device connection
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.10av, and IEEE 1722)
- Controller area network (CAN) interface × 2 channels
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- On-chip debug function

RZ/G2M (R8A774Ax) block diagram

System	CPU		
System controller	2 × Cortex®-A57 1.5GHz 4 × Cortex®-A53 1.2GHz 1 × Cortex®-R7 800MHz		
System RAM: 384KB	L1 I\$ 48KB L1 I\$ 32KB L1 I\$ 32KB		
Thermal Sensor	L1 D\$ 32KB L1 D\$ 32KB L1 D\$ 32KB		
JTAG Debug	NEON/VFPv4 NEON/VFPv4 VFPv3-D16		
(Coresight)	L2 cache: 2MB with ECC L2 cache: 512KB with ECC I-TCM 32KB, D-TCM 32KB with ECC		
Timers	3D Graphics		
00 00 11 70	B 1/B 0//0050		

26 × 32-bit Timer 15 × 32-bit Interval WDT Video Codec 7 × PWM out

Audio IPs Audio router w/10 ASRC, mixer, 10 I2S (6ch TDM). 90ch Audio DMA

Secure IP Crypto engine (AES, DES, Hash, RSA, TRNG) 2D/3D tile based 600MHz

Up to 4K resolution (2 channels) Video IP

3 × Display Out × Digital out, 1 × LVDS 1 × HDMI 2 × Fine Display Processor 8 × Video in 2 × MIPI-CSI2 (1 × 4L, 1 × 2L) 2 × Digital

FC-BGA: 29 × 29mm² 1022-pins, 0.8mm pitch

Connectivity
2 × PCle2.0 (1Lane)
USB3.0/2.0 (DRD)
2 × USB2.0 (1H, 1H/F/0TG)
Ethernet AVB (1Gbps)
2 × CAN2.0B
6 × UART, 5 × H-UART
4 × SPI
7 ∨ I2C· 1 ∨ DVFS ctrl

Memory I/F
32-bit × 2ch LPDDR4-3200 (ECC) access cache
Raw NAND (8/16-bit, ONFI 1.x, ECC 1-8-bits)
16-bit ExtBus/SRAM
$1 \times QSPI$ (4/8-bit selectable) or 1 × Hyperflash
4 × SDIO (SDR104)
2 × eMMC (5.0, HS400)

RZ/G2N (R8A774Bx)

CPU core

- Arm® Cortex®-A57, quad-core Max. operating frequency: 1.5GHz
- Arm® Cortex®-R7, single-core Max. operating frequency: 800MHz

Cache memory (Cortex®-A57)

- L1 instruction cache: 48KB L1 data cache: 32KB
- L2 cache: 2MB

Cache memory (Cortex®-R7)

- L1 instruction cache: 32KB
- L1 data cache: 32KB ■ I-TCM: 32KB
- D-TCM: 32KB

External memory

- Ability to connect LPDDR4-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 1 channel External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 8/16 bits
- PCI Express 2.0: 1 Lane × 2 channels (one of PHY is shared with Serial ATA)

3D graphics

■ PowerVR[™] GE7800

Video functions

- Video display interface × 3 channels (1 channel: HDMI(option), 1 channel: LVDS, 1 channel: RGB888)
- Video input interface × 4 channels (2 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))

- Video codec module: VCP4 × 1 channel
- IP converter module
- Video image processing functions (color conversion, image enlargement/ reduction, filtering)

Audio functions

- Sampling rate converter × 10 channels
- Serial sound interface × 10 channels Storage interfaces
- USB 3.0 DRD × 1 channel
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1channel)
- SD host interface x 4 channels
- Multimedia card interface × 2 channels
- Serial ATA interface × 1 channel Other peripheral functions
- 32-bit timer × 15 channels
- PWM timer × 7 channels
- I²C bus interface × 7 channels
- Serial communication interface (SCIF) × 6 channels
- Quad serial peripheral interface (QSPI) × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.10av, and IEEE 1722)
- Controller area network (CAN) interface × 2 channels
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- On-chip debug function

■ RZ/G2N (R8A774Bx) block diagram

Secure IP

Crypto engine

(AES, DES, Hash, RSA, TRNG)

System	CI	PU	Connectivity
System controller	2 × Cortex®-A57 1.5GHz	1 × Cortex®-R7 800MHz	2 × PCle2.0 (1Lan
System RAM: 384KB	L1 I\$ 48KB	L1 I\$ 32KB	SATA (Rev.3.2) (sha
Thermal Sensor	L1 D\$ 32KB	L1 D\$ 32KB	USB3.0/2.0 (DRD
JTAG Debug	NEON/VFPv4	VFPv3-D16	2 × USB2.0 (1H, 1H/F
(Coresight)	L2 cache: 1MB with ECC	I-TCM 32KB, D-TCM 32KB with ECC	Ethernet AVB (1Gb
Timers	3D Gr	aphics	2 × CAN2.0B
26 × 32-bit Timer	PowerVF	R GE7800	6 × UART, 5 × H-U

EO A OE DICTIMO	2D/3D tile based 600MHz			
15 × 32-bit Interval				
WDT	Video	Codec		
7 × PWM out	Up to 4K resolution (2 channels)		· ·	
Audio IPs				
Audio router w/10 ASRC,	Vide	eo IP		
mixer, 10 I2S (6ch TDM),	3 × Display out	2 × Video Signal Processor		
90ch Audio DMA	1 × Digital out, 1 × LVDS 1 × HDMI	1 × Fine Display Processor		

8 × Video in 2 × MIPI-CSI2 (1 × 4L, 1 × 2L) 2 × Digital FC-BGA: $29 \times 29 \text{mm}^2$ 1022-pins, 0.8 mm pitch

Ш	2 × PCle2.0 (1Lane)
П	SATA (Rev.3.2) (shared)
Ш	USB3.0/2.0 (DRD)
Ш	2 × USB2.0 (1H, 1H/F/OTG)
Ц	Ethernet AVB (1Gbps)
ı	2 × CAN2.0B
	$6 \times \text{UART}$, $5 \times \text{H-UART}$ $4 \times \text{SPI}$ $7 \times \text{I}^2\text{C}$; $1 \times \text{DVFS ctrl}$
н	
	Momory I/E

Memory I/F
32-bit × 1ch LPDDR4-3200 (ECC) access cache
Raw NAND (8/16-bit, ONFI 1.x, ECC 1-8-bits)
16-bit ExtBus/SRAM
1 × QSPI (4/8-bit selectable) or 1 × Hyperflash
4 × SDIO (SDR104)
2 × eMMC (5.0, HS400)

RZ/G2E (R8A774C0)

CPU core

- Arm® Cortex®-A53, quad-core Max. operating frequency: 1.2GHz
- Arm® Cortex®-R7, single-core Max. operating frequency: 800MHz

Cache memory (Cortex®-A53)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L2 cache: 256KB
- Cache memory (Cortex®-R7)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- I-TCM: 32KB
- D-TCM: 32KB

External memory

- Ability to connect DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 1channel External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 8/16 bits
- PCI Express 2.0 : 1 Lane × 1 channel 3D graphics
- PowerVR[™] GE8300
- Video functions
- Video display interface × 2 channels (2 channels: LVDS, 1 channel: RGB888)
- Video input interface × 3 channels (1 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))

■ Video codec module: VCP4 × 1 channel

- IP converter module
- Video image processing functions (color conversion, image enlargement/ reduction, filtering)

Audio functions

- Sampling rate converter × 10 channels
- Serial sound interface × 10 channels Storage interfaces
- USB 3.0 DRD × 1 channel
- USB 2.0 × 1 channel (Host-Function 1channel)
- SD host interface × 3 channels
- Multimedia card interface × 1 channel Other peripheral functions
- 32-bit timer × 15 channels
- PWM timer × 7 channels
- I²C bus interface × 8 channels
- Serial communication interface (SCIF) × 6 channels
- Quad serial peripheral interface (QSPI) × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.10av, and IEEE 1722)
- Controller area network (CAN) interface × 2 channels
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- On-chip debug function

RZ/G2E (R8A774C0) block diagram

Crypto engine

(AES, DES, Hash, RSA, TRNG)

RZ/GZE (NOA/7460) DIOCK Glayfalli			
System	СРИ		Connectivity
System controller	2 × Cortex®-A53 1.2GHz	1 × Cortex®-R7 800MHz	1 × PCle2.0 (1Lane)
System RAM: 128KB	L1 I\$ 32KB	L1 I\$ 32KB	
Thermal Sensor	L1 D\$ 32KB	L1 D\$ 32KB	USB3.0/2.0 (DRD)
JTAG Debug	NEON/VFPv4	VFPv3-D16	USB2.0 (1H/F)
(Coresight)	L2 cache: 256KB with ECC	I-TCM 32KB, D-TCM 32KB with ECC	Ethernet AVB (1Gbps)
Timers	3D Graphics		2 × CAN2.0B
26 × 32-bit Timer	PowerVR GE8300		6 × UART, 5 × H-UART
15 × 32-bit Interval	2D/3D tile based 600MHz		4 × SPI
WDT	Video Codec		8 × I ² C; 1 × DVFS ctrl
7 × PWM out			Memory I/F
Audio IPs	Up to FHD resolution		32-bit DDR3L-1856 (ECC)
Audio router w/10 ASRC,	Video IP		access cache
mixer, 10 I ² S (6ch TDM), 45ch Audio DMA	2 × Display out: (2 × LVDS or 1 × LVDS + 1 × DRGB)	2 × Video Signal Processor 1 × Fine Display Processor	Raw NAND (8-bit, ONFI 1.x, ECC 1-8-bits)
Secure IP	2 × Video in		16-hit EvtRus/SRAM

2 × Video in × MIPI-CSI2 (1 × 2L)

1 × Digital

FC-BGA: 21 × 21mm² 552-pins, 0.8mm pitch

Memory I/F
32-bit DDR3L-1856 (ECC) access cache
Raw NAND (8-bit, ONFI 1.x, ECC 1-8-bits)
16-bit ExtBus/SRAM
$1 \times QSPI$ (4/8-bit selectable) or $1 \times Hyperflash$
3 × SDIO (SDR104)
oMMC (5.0. HS400)

RZ/G2L(R9A07G044Lxx)

CPU core

- Arm® Cortex®-A55, dual-core or single-core Max. operating frequency: 1.2GHz
- Arm® Cortex®-M33, single-core Max. operating frequency: 200MHz

Cache memory (Cortex®-A55)

- L1 instruction cache: 32KB
- L1 data cache: 32KB ■ L3 cache: 256KB
- External memory

Ability to connect DDR4-SDRAM / DDR3L-SDRAM via DDR dedicated bus

- Data bus width: 16 bits × 1 channel 3D graphics
- Arm Mali[™]-G31 GPU

Video functions

- Video display interface: MIPI DSI × 1 channel or Digital parallel output \times 1 channel
- Video input interface: MIPI CSI-2 \times 1 channel or Digital parallel input × 1 channel
- Video codec module: VCPL4 \times 1 channel
- Video image processing functions (Resizer and Color Space / Color Format Conversion)

Audio functions

- Sampling rate converter × 1 channel
- Serial sound interface × 4 channels Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1channel)
- SD host interface × 2 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

Other peripheral functions

- 32-bit timer × 1 channel
- 16-bit timer × 8 channels
- PWM timer × 8 channels
- I²C hus interface × 4 channels
- Serial communication interface with FIFO (SCIF) × 5 channels
- Serial communication interface (SCI) × 2 channels
- SPI Multi I/O Bus Controller× 1 channel (8bit Double data rate)
- Serial Peripheral Interface (RSPI) ×
- Gigabit Ethernet controller × 2 channels
- Controller area network (CAN) interface × 2 channels (support CAN FD)
- 12-bit A/D converter × 8 channels
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

RZ/G2L(R9A07G044Lxx) block diagram

System	CI	PU	Interfaces
Arm Debugger (Coresight)	Cortex®-A55 1.2GHz Cortex®-A55 NEON/VFP NEON	55 [#] 1.2GHz	DDR4/DDR3L (In line ECC) 16-bit × 1.6/1.3Gbps
Arm TrustZone	I-L1\$: 32KB w/Parity D-L1\$: 32KB w/ECC D-L1\$: 32K		1 × SPI Multi I/O (8-bit DDR)
16ch DMAC		OKB Cortex®-M33	2 × SDHI (UHS-I)/MMC
Interrupt Controller		@200MHz	Z X 3DIII (0113-1//WIVIC
PLL/SSCG	L3\$(Shared) : 256KB v	w/ECC	1 × USB2.0 Host
Standby (Sleep/Software/Module)	Memory RAM 128KB w/FCC		1 × USB2.0 Host / Function
Timers 1 × 32-bit MTU3*	Video & Graphics		2 × 100/1000Mbps Ether MAC*
	3D GPU	Camera In	
8 × 16-bit MTU3*	Arm Mali-G31	(MIPI CSI-2 4lane, Parallel*)	2 × I2C, 2 × I2C*
8 × 32-bit PWM*		Display Out	2 × SCI 8/9-bit*
3 × WDT*	H.264 Enc/Dec	(MIPI DSI 4lane, Parallel*)	5 × SCIF (UART)*
Analog	1920 × 1080 @30fps Image Scaling Unit		3 × RSPI*
8 × 12-bit ADC	Security (Option)		2 × CAN*
	Secure Boot	Device Unique ID	GPIO*
	Crypto Engine	JTAG Disable	Audio
	TRNG	OTP 4Kbit	4 × SSI (I ² S)*
	(#) Single Core version is 1CPU.		1 × SRC
			*Shared



RZ/G2LC(R9A07G044Cxx)

CPU core

- Arm® Cortex®-A55, dual-core or single-core Max. operating frequency: 1.2GHz
- Arm® Cortex®-M33, single-core Max. operating frequency: 200MHz

Cache memory (Cortex®-A55)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L3 cache: 256KB
- External memory
- Ability to connect DDR4-SDRAM / DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 16 bits × 1 channel 3D graphics
- Arm Mali[™]-G31 GPU

Video functions

- Video display interface: MIPI DSI x 1 channel
- Video input interface: MIPI CSI-2 × 1 channel
- Video image processing functions (Resizer and Color Space / Color Format Conversion)

Audio functions

- Sampling rate converter × 1 channel
- Serial sound interface × 2 channels Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1channel)
- SD host interface × 2 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

Other peripheral functions

- 32-bit timer × 1 channel
- 16-bit timer × 5 channels
- PWM timer × 4 channels
- I²C bus interface × 4 channels
- Serial communication interface with FIFO (SCIF) × 3 channels
- Serial communication interface (SCI) × 2 channels
- SPI Multi I/O Bus Controller× 1 channel (4bit Double data rate)
- Serial Peripheral Interface (RSPI) × 3channels
- Gigabit Ethernet controller × 1 channel
- Controller area network (CAN) interface × 2 channels (support CAN FD)
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

RZ/G2LC(R9A07G044Cxx) block diagram

		J	
System	CF	PU	Interfaces
Arm Debugger (Coresight)	Cortex®-A55 1.2GHz Cortex®-A5		DDR4/DDR3L (In line ECC) 16-bit × 1.6/1.3Gbps
Arm TrustZone	I-L1\$: 32KB w/Parity D-L1\$: 32KB w/ECC D-L1\$: 32KB		1 × SPI Multi I/O (4-bit DDR)
16ch DMAC Interrupt Controller	L2\$: 0KB L2\$:	0 . 0 1400	2 × SDHI (UHS-I)/MMC
PLL/SSCG	L3\$(Shared) : 256KB v		1 × USB2.0 Host
Standby (Sleep/Software/Module)	Memory RAM 128KB w/ECC		1 × USB2.0 Host / Function
Timers 1 × 32-bit MTU3*	Video & Graphics		1 × 100/1000Mbps Ether MAC*
5 × 16-bit MTU3*	3D GPU Arm Mali-G31	Camera In (MIPI CSI-2 4lane)	2 × I2C, 2 × I2C*
4 × 32-bit PWM*		Display Out	2 × SCI 8/9-bit*
3 × WDT*	Image Scaling Unit	(MIPI DSI 4lane)	3 × SCIF (UART)*
			3 × RSPI*
	Security (Option) Secure Boot Device Unique ID		2 × CAN*
			GPIO*
	Crypto Engine	JTAG Disable	Audio
	TRNG	OTP 4Kbit	2 × SSI (I ² S)*
	(#) Single Core version is 1CPU.		1 × SRC

RZ/G2UL(R9A07G043Uxx)

CPII core

- Arm® Cortex®-A55, single-core Max. operating frequency: 1.0GHz
- Arm® Cortex®-M33, single-core Max. operating frequency: 200MHz Cache memory (Cortex®-A55)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L3 cache: 256KB

External memory

- Ability to connect DDR4-SDRAM / DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 16 bits × 1 channel Video functions
- Video display interface: Digital parallel output \times 1 channel
- Video input interface: MIPI CSI-2 × 1 channel
- Video image processing functions (Resizer and Color Space / Color Format Conversion)

Audio functions

- Sampling rate converter × 1 channel
- Serial sound interface × 4 channels Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1channel)
- SD host interface × 2 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

Other peripheral functions

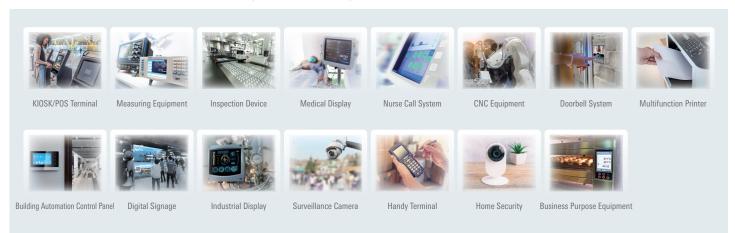
- 16-bit timer × 8 channels
- I^2C bus interface \times 4 channels
- Serial communication interface with FIFO (SCIF) × 5 channels
- Serial communication interface (SCI) × 2 channels
- SPI Multi I/O Bus Controller× 1 channel
- (4bit Double data rate) Serial Peripheral Interface (RSPI) ×
- 3channels ■ Gigabit Ethernet controller × 2 channels
- Controller area network (CAN) interface × 2 channels (support CAN FD)
- 12-bit A/D converter × 2 channels
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

RZ/G2UL(R9A07G043Uxx) block diagram

,	,	0	
System	CF	บ	Interfaces
Arm Debugger (Coresight)	Cortex®-A55 1.0GI	-lz	DDR4/DDR3L (In line ECC) 16-bit × 1.6/1.3Gbps
Arm TrustZone	I-L1\$: 32KB w/Par D-L1\$: 32KB w/E0	CC	1 × SPI Multi I/0 (4-bit DDR)
Interrupt Controller	L2\$: 0KB	Cortex®-M33 @200MHz	SDHI (UHS-I)/MMC
PLL/SSCG	L3\$: 256KB w/EC		1 × USB2.0 Host
Standby (Sleep/Software/Module)	Memory RAM 128KB w/ECC		1 × USB2.0 Host / Function
Timers	Video &	Graphics	2 × 100/1000Mbps Ether MAC*(#)
8 × 16-bit MTU3*(#)	Image Sc	2 × I2C, 2 × I2C*	
	Display Out (Parallel-IF*)(#)		2 × SCI 8/9-bit*
2 × WDT*	Camera In (MIPI CSI-2 4lane)		5 × SCIF (UART)*(#)
Analog			3 × RSPI*
2 × 12-bit ADC(#)	Security (Option)		2 × CAN*
	Secure Boot	Device Unique ID	GPIO*
	Crypto Engine	JTAG Disable	Audio
	TRNG	OTP 1Kbit	4 × SSI (I ² S)*(#)
(#) There are 2 types in RZ/G2UL.	[Type-2] RZ/G2LC pin		1 × SRC
[Type-1] Full function version - This block diagram is Type-1.	 No support: Display out, Parallel-IF 1×Ether MAC, 3×SCIF, 3×SSI 		*Shared

RZ/G Series Application

The HMI can be made more expressive by making full use of the 3D graphics and video capabilities.



RZ/G Linux Platform Solutions from Partner Companies

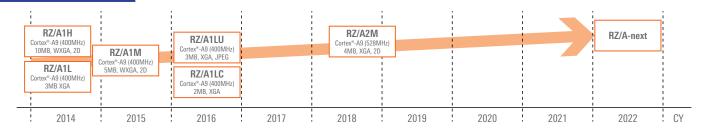
Visit the webpage below for the latest information on RZ/G Linux Platform development tools, including solutions from partner companies. https://www.renesas.com/products/microcontrollers-microprocessors/rz/softtools.html#rzg





RZ/A Series

RZ/A Series Roadmap



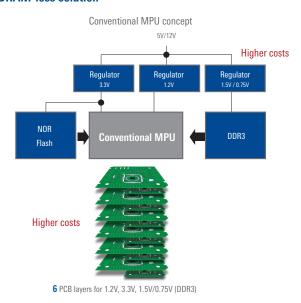
RZ/A Series Application

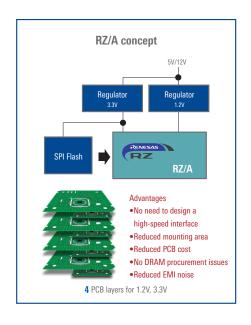


RZ/A Series Features

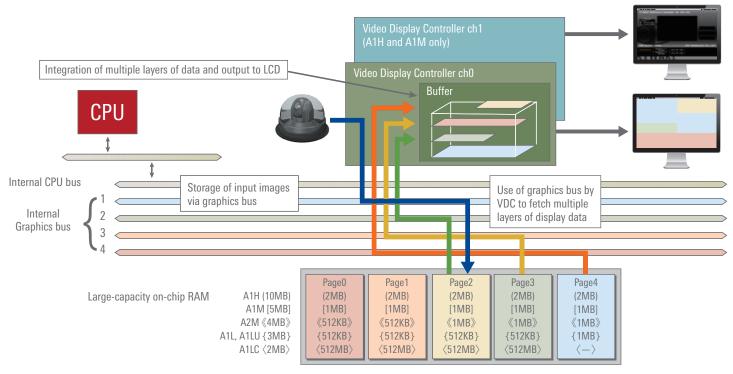
- Large-capacity on-chip RAM: 10MB
- Graphics display and camera input capabilities on a single chip
- Rich peripheral functions and software
- Large-capacity on-chip RAM: 10MB

DRAM-less solution



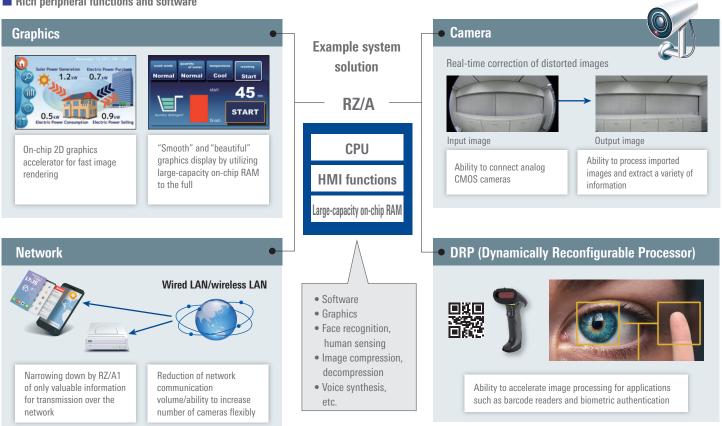


■ Graphics display and camera input capabilities on a single chip



The bus configuration with independent buses for images and hardware-based superimposition processing make it easy to create graphical applications.



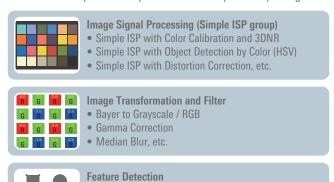


With ample peripheral functions and software, a single chip can cover a wide range of fields, including display, camera input, communication, and audio functions.



DRP Library

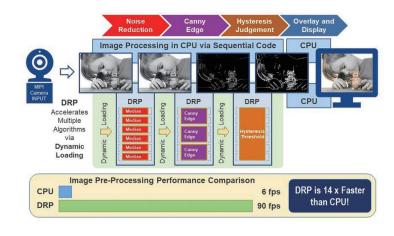
- The RZ/A2M's DRP* can process applications such as image processing several to dozens of times faster than software processing that relies on the CPU, resulting in a faster system.
- A wide variety of DRP libraries are available, and users do not need to code the DRP itself by calling it from user programs using the DRP driver.
- The functions processed by the DRP can be dynamically changed from the user program, allowing multiple different processes to be used in combination.



• Canny Edge Detection

• Find Contours, etc.

• Harris' Corner Detection



RZ/A2M Group

CPU (Arm® Cortex®-A9)

- Operating frequency: 528MHz
- Single-precision/double-precision FPU
- Arm® NEON™

On-chip memory

■ 4MB

Main graphics and camera input functions

- Video display controller (VDC6): 1 channel LCD output: Max. WXGA Screen superimposition: 3 layers Video input: Max. XGA
- CMOS camera input (CEU): 1 channel
- MIPI-CSI2 interface: 1 channel
- Distortion compensation unit (IMR): 1 channel
- 2D graphics engine: 1 channel
- Sprite engine: 1 channel
- JPEG coding engine: 1 channel

Main memory interface functions

- NOR flash, SDRAM, NAND flash
- Serial flash: 1-bit/4-bit/8-bit: 1 channel, 8-bit: 1 channel (ability to run stored programs directly)
- SD/MMC host interface: 2 channels

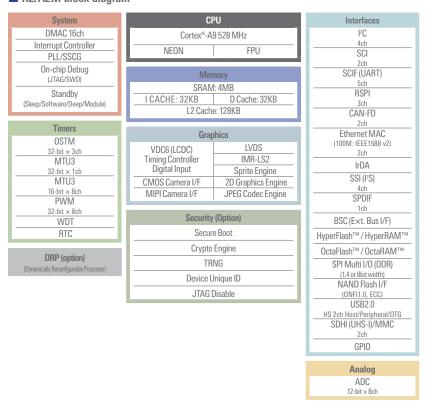
Main communication functions

- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 2 channels
- SCIF: 5 channels
- I²C: 4 channels
- SSI: 4 channels
- RSPI: 3 channels
- CAN-FD: 2 channels

Optional functions

- DRP (Dynamically Reconfigurable Processor)
- Package
- 176-LFBGA (13mm×13mm, 0.8mm pitch)
- 256-LFBGA (11mm×11mm, 0.5mm pitch)
- 272-FBGA (17mm×17mm, 0.8mm pitch)
- **324-FBGA** (19mm×19mm, 0.8mm pitch)

RZ/A2M block diagram



RZ/A1H Group and RZ/A1M Group (Pin Compatible)

CPU (Arm® Cortex®-A9)

- Operating frequency: 400MHz
- Single-precision/double-precision FPU
- Arm® NEON™

On-chip memory

- RZ/A1H: 10MB
- RZ/A1M: 5MB

Main graphics and camera input functions

Video display controller (VDC5): 2 channels LCD output: Max. WXGA

Screen superimposition: 4 layers

Video input: Max. XGA (CVBS analog input supported)

- CMOS camera input (CEU): 1 channel
- PAL/NTSC decoder (DVDEC): 2 channels
- Distortion compensation unit (IMR): 1 channel
- Open VG accelerator: 1 channel
- JPEG coding engine: 1 channel

Main memory interface functions

- NOR flash, SDRAM, NAND flash
- QSPI serial flash: 2 channels (ability to run stored programs directly)
- SD host interface: 2 channels
- MMC host interface: 1 channel

Main communication functions

- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1channel
- SCIF: 8 channels
- I²C: 4 channels
- SSI: 6 channels
- RSPI: 5 channels
- Ethernet AVB: 1 channel
- CAN: 5 channels

Package

- 256-LFBGA (11mm × 11mm, 0.5mm pitch)
- 256-LFQFP (28mm × 28mm, 0.4mm pitch)
- 324-FBGA (19mm × 19mm, 0.8mm pitch)

RZ/A1H,and RZ/A1M block diagram

Memory			
SRAM			
A1H: 10MB/A1M: 5MB			
SRAM L2 Cache			
128 KB			
Cache			
32 KB + 32 KB			
Cache			

System
DMAC 16ch
Interrupt Controller
Clock Generation with SSCG
JTAG Debug
Customer Unique ID*

Audio
SCUX 4ch ASRC
CDROM DEC
Sound Generator
Analog
ADC
12-bit × 8ch

Graphics
Video Display Controller
2ch
OpenVG 1.1
Enhanced eng.
PAL/NTSC
dec. 2ch
CMOS Camera I/F
1ch
Fish Eye Correction
2ch
JPEG Engine
1ch

CPU

Cortex®-A9 400MHz

Timers

MTU2 16-bit × 5ch WDT

8-bit × 1ch

OS Timer

32-bit × 2ch PWM Timer

Real-Time CLK

Interfaces		
10/100 Ether MAC		
USE	32.0	
HS 2ch H	lost/Func	
NAND	Flash	
1/	F	
External Bus	32-bit ROM,	
SRA	AM,	
SDRAM,	PCMCIA	
SPI I	Multi	
2	ch	
SCIF	RSPI	
8ch	5ch	
I ² C	IEBus	
4ch 1ch		
SSI (I ² S) SPDIF		
6ch 1ch		
SDHI	MMC	
2ch	1ch	
CAN	MOST50	
5ch	1ch	
Smart Card I/F		
2		
IrDA	LIN Master	
1ch	2ch	
Ethernet AVB		

RZ/A1LU Group

CPU (Arm® Cortex®-A9)

- Operating frequency: 400MHz
- Single-precision/double-precision FPU
- Arm® NEON™

On-chip memory

■ 3MB

Main graphics and camera input functions

 LCD controller (VDC5): 1 channel LCD output: Max. WXGA Screen superimposition: 3 layers Video input: Max. XGA

- CMOS camera input (CEU): 1 channel
- JPEG coding engine: 1 channel

Main memory interface functions

- NOR flash, SDRAM
- QSPI serial flash: 1 channel (ability to run stored programs directly)
- SD host interface: 2 channels
- MMC host interface: 1 channel

Main communication functions

- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1channel
- SCIF: 5 channels
- I²C: 4 channels
- SSI: 4 channels
- RSPI: 3 channels
- Ethernet AVB: 1 channel
- CAN: 2 channels

Package

- 176-LFBGA (8mm × 8mm,0.5mm pitch)
- 176-LFQFP (24mm × 24mm,0.5mm pitch)
- 208-LFQFP (28mm × 28mm,0.5mm pitch)

■ RZ/A1LU block diagram

Memory	
SRAM 3MB	Co
SRAML2 Cache	NE
Cache 32 KB + 32 KB	
System	
DMAC 16ch	
Interrupt Controller	
Clock Generation with SSCG	
JTAG Debug	
Customer Unique ID*	Vide
Audio	C
SCUX 4ch ASRC	
Analog	
ADC 12-bit × 8ch	

Cortex®-A9 400MHz			
NEON	FPU		
Tim	iers		
16-bit	MTU2 16-bit × 5ch		
W			
8-bit			
OS Timer			
32-bit × 2ch			
Real-Time CLK			
Graphics			
Video Display Controller 1ch			
CMOS Camera I/F			
1ch			
JPEG Engine			
1ch			

CPU

Int	erfaces		
10/100	10/100 Ether MAC		
	CAN		
	2ch		
U	SB2.0		
HS 2c	h Host/Func		
Externa	al Bus 32-bit		
RON	1, SRAM,		
	M, PCMCIA		
SF	l Multi		
	1ch		
SCIF	RSPI		
5ch	3ch		
	I ² C		
	4ch		
SSI (I ² S)	SPDIF		
4ch	1ch		
SDHI	MMC		
2ch	1ch		
Smart Card I/F			
2ch			
IrDA			
	1ch		
Ethe	rnet AVB		
Ethernet AVB			

* =0ption

^{* =}Option



RZ/A1L, RZ/A1LC Group

CPU (Arm® Cortex®-A9)

- Operating frequency: 400MHz
- Single-precision/double-precision FPU
 Arm[®] NEON™

On-chip memory

RZ/A1L: 3MB

- RZ/A1LC: 2MB

- Main graphics and camera input functions

 LCD controller (VDC5): 1 channel LCD output: Max. WXGA Screen superimposition: 3 layers Video input: Max. XGA
- CMOS camera input (CEU): 1 channel

Main memory interface functions

- NOR flash, SDRAM, NAND flash
- QSPI serial flash: 1 channel (ability to run stored programs directly)
- SD host interface: 2 channels
- MMC host interface: 1 channel

Main communication functions

- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1 channel
- SCIF: 5 channels
- I²C: 4 channels
- SSI: 4 channels
- RSPI: 3 channels
- CAN: 2 channels

Package

- 176-LFBGA (8mm × 8mm,0.5mm pitch)
- 176-LFQFP (24mm × 24mm,0.5mm pitch)
- 208-LFQFP (28mm × 28mm,0.5mm pitch)
- 233-FBGA (15mm × 15mm, 0.8mm pitch)

■ RZ/A1L, RZ/A1LC block diagram

Memory	
SRAM	I
A1L: 3 MB/A1LC: 2 MB	
SRAM L2 Cache	
128 KB	
Cache	ı
32 KB + 32 KB	

System		
DMAC 16ch		
Interrupt Controller		
Clock Generation with SSCG		
JTAG Debug		

	Audio			
	SCUX 4ch ASRC			
	CDROM DEC*			
Analog				

ADC	
12-bit × 8ch	

CPU Cortex®-A9 400MHz NEON

Timers		
MTU2		
16-bit × 5ch		
WDT		
8-bit × 1ch		
OS Timer		
32-bit × 2ch		
Real-Time CLK		

Graphics		
Video Display Controller		
1ch		
CMOS Camera I/F		
1ch		

Interfaces			
	10/100 Ether MAC		
		32.0	
	HS 2ch F	lost/Func	
	External E	Bus 32-bit	
	ROM,	SRAM,	
	SDRAM,	PCMCIA	
	SPI Multi		
	1ch		
	SCIF	RSPI	
	5ch	3ch	
	I ² C	IEBus*	
	4ch 1ch		
	SSI (I ² S)	SPDIF	
	4ch	1ch	
	SDHI	MMC	
	2ch	1ch	
	CAN	MOST50*	
	2ch	1ch	
	Smart (Card I/F	
	20	ch	
	IrDA	LIN Master*	
	1ch	1ch	

^{*} RZ/A1L Group specification only.

RZ/A Series: Development Environments (Integrated Development Environments)

	arm	OFFICIENTS SYSTEMS	E SOL	RENESAS
Development environments	• DS-5	• IAR Embedded Workbench® for Arm®	• eBinder	• e² studio*3 e² studio e² studio
Compilers	• Arm CC*1	• IAR C/C++ compiler*2	• Arm CC*1	• GNU tool*4
ICEs	DSTREAM™ ULINKpro™ ULINKproD™ ULINK2™	I-jet [™] /I-jet Trace [™] for Arm Cortex®-A/R/M JTAGjet-Trace	PARTNER-Jet2 from Kyoto Microcomputer Co., Ltd. adviceLUNAII from DTS INSIGHT Corporation	 J-Link LITE from Segger J-Link series from Segger*5
	SKEE ULINA PL		200 COM	

^{*1.} Arm CC is included in DS-5 Starter Kit for RZ/A and RZ/T, which is available free of charge, and in the popularly priced DS-5 RZ/A Edition. There is also a free evaluation version that provides full functionality but is limited to 30 days of use. Contact a DS-5 sales appear for details

- *2. A free evaluation license is available provided the 30-day time-limited evaluation or the permanent 32KB size-limited evaluation (www.iar.com/EWARM)
- *3. Eclipse-based development environment from Renesas (https://www.renesas.com/e2studio)
- *4. GNU TOOLS & SUPPORT Website (https://gcc-renesas.com)
- *5. Renesas does not handle ICEs from Segger. Contact a sales agent for details.

RZ/A Series: Development Tools (Debuggers, ICEs)

	Kyoto Microcomputer Co., Ltd.	Our insight, your value	Computex*
Debuggers	• PARTNER-Jet2		• CSIDE version 7
ICEs		adviceLUNA II	PALMICE 4 PALMICE 4
Supported compilers	 exeGCC from Kyoto Microcomputer GNU tool*¹ Arm CC*² IAR C/C++ compiler,*³ etc. 	• Arm CC*2 • GNU tool,*1 etc.	 Arm CC*² IAR C/C++ compiler*³ GNU tool,*¹ etc.

^{1.} GNU TOOLS & SUPPORT Website (https://gcc-renesas.com)

- *2. Arm CC is included in DS-5. In addition to the popularly priced DS-5 RZ/A and RZ/T editions, a fully functional evaluation version of DS-5 that expires after 30 days is available free of charge. Contact your DS-5 dealer for details.
- *3. Two versions of the software are available for download free of charge. One limits the code size to 32KB and can be used with no time limitation. The other has no limit on code size and expires after 30 days. (www.iar.com/EWARM)

RZ/A Series: Solutions from Partner Companies

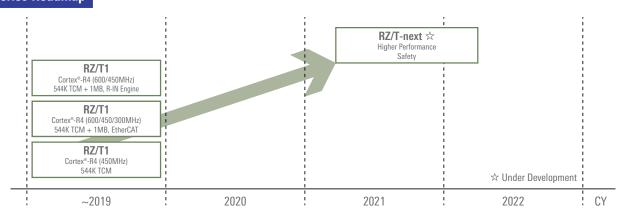
Visit the webpage below for the latest information on RZ/A Series development tools, including solutions from partner companies. https://www.renesas.com/products/microcontrollers-microprocessors/rz/softtools.html#rza





RZ/T Series

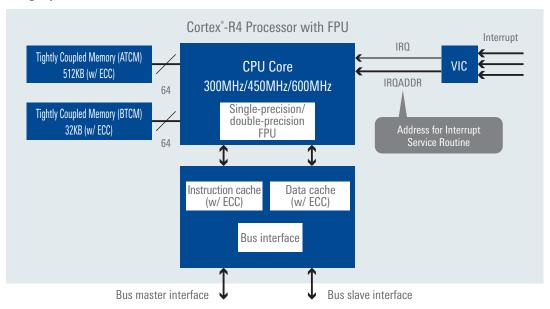
RZ/T Series Roadmap



RZ/T Series Features

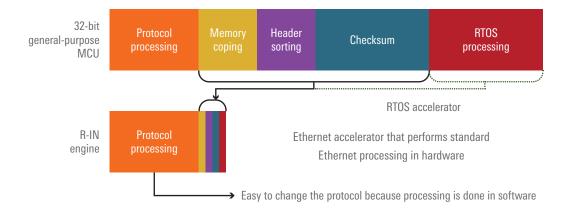
- High-performance, high-speed real-time control
- R-IN engine
- Integrated peripheral functions

■ High-performance, high-speed real-time control



- High-speed RAM directly connected to the CPU for high-speed processing and dependable real-time responsiveness without caching
- ECC for enhanced reliability
- Vectored Interrupt Controller (VIC) to assure interrupt responsiveness suitable for embedded control

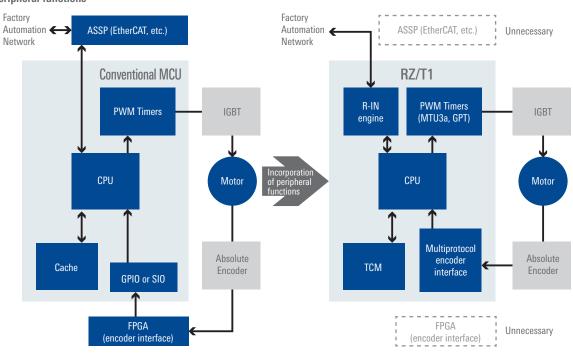
R-IN engine



High-speed, energy-efficient communication Flexible support for multiple protocols

- R-IN engine industrial Ethernet communication accelerator performs standard Ethernet processing in hardware.
- Network processing is up to four times as fast.

■ Integrated peripheral functions



- The encoder interface was external with conventional FPGA or ASIC approaches but is now integrated on-chip.
- This one-chip AC servo solution helps reduce the component count and save space.



RZ/T Series Application

High-speed operation at 300MHz/450MHz/600MHz provides higher performance and improved functionality for industrial equipment such as industrial motors or AC servo drivers. Products incorporating the R-IN engine accelerator for industrial Ethernet communication can also handle a variety of industrial Ethernet processing tasks without sacrificing real-time performance.



RZ/T1 Group

High performance CPU

- Arm® Cortex®-R4 Processor
- Operating frequency: 300MHz/450MHz/600MHz
- High-performance, high-speed real-time control
- Single-precision/double-precision floating-point unit

R-IN engine (option)

- Arm® Cortex®-M3
- Operating frequency: 125MHz
- HW-RTOS accelerator
- R-IN engine instruction memory: 512KB (w/ ECC) + data memory: 512KB (w/ ECC) On-chip memory
- Tightly Coupled Memory: 512KB (w/ ECC) + 32KB (w/ ECC)
- Extended RAM instruction memory 512KB (w/ ECC) + data memory: 512KB (w/ ECC) (option)

Features

- Industrial Ethernet communication accelerator with multi-protocol support (R-IN engine) (option)
- EtherCAT slave controller (option)
- PWM timer: MTU3a, GPT
- Encoder interface (Nikon A-format™/BiSS-C/EnDat2.2/HIPERFACE DSL®/Tamagawa) (option)

Note: 2ch encoder support depends on the combination of the selected protocol.

- High Speed USB
- Secure boot (option)
- Safety functions
 - ECC memory
 - CRC (32-bit)
 - Independent WDT: Operating on dedicated on-chip oscillator
- $\Delta\Sigma$ interface
- 100Mbps EtherMAC (with Ethernet switch)
- Ethernet accelerator
- Power supply voltage: 1.2V, 3.3V

Package

- FBGA 320pin (17mm × 17mm, 0.8mm pitch)
- QFP 176pin (20mm × 20mm, 0.4mm pitch)

■ RZ/T1 Group block diagram

СРИ			
Cortex®-R4 Processor with FPU 300MHz/450MHz/600MHz 1.2V (Core), 3.3V (I/O)			
FPU MPU	Debug VIC		
Memory			
ATCM: 512KB with ECC BTCM: 32KB with ECC			
I Cache: 8KB w/ECC	D Cache: 8KB w/ECC		
Extended RAM: 1MB w/ECC (option)			

CPU Cortex®-M3 125MHz 1.2V (Core), 3.3V (I/O) MPU Debug NVIC
iii o sobag
HW-RTOS Accelerator
Memory
Instruction RAM: 512KB with ECC Data RAM: 512KB with ECC

Z X TOOM DIVINO	
JTAG Debug	
Clock Generation Circuit	
Timers	
8 × 16-bit + 1 × 32-bit MTU3a	
6 × 16-bit CMT	
2 × 32-bit CMT2	Τ
4 × 16-bit GPT	
1 × WDT	Τ
1 × iWDT	
12 × 16-bit TPU	
2 × 4gr× 4-bit PPG	
Security	
Secure boot (option)	
JTAG w/ disable function	

System

 $2 \times 16ch DMAC$

FBGA320 (17mm \times 17mm, 0.8mm pitch) QFP176pin (20mm \times 20mm, 0.4mm pitch)

1111011111000
5 × SCIF
$2 \times I^2C$
2 × CAN
1 × EthernetMAC (100Mbps) With switch + IEEE1588
USB 2.0 HS (Host/Func)
GPI0
Δ <u>Σ</u> /F
EtherCAT Slave Controller (option)
Memory Interfaces
4 × SPI
QSPI (Flash I/F)with Direct Access from CPU
SRAM I/F (32-bit bus)
SDRAM I/F (32-bit bus)
Burst ROM I/F (32-bit bus)
Analog
(8 + 16) × 12-bit ADC

Interface Encoder interfaces (option)

Interfaces

RZ/T1 Product Lineup

CPU	Tightly coupled memory	Extended RAM							
600 MHz + R-IN Engine (150MHz)	512KB +32KB	– (1MB for R-IN)						R7S910017	R7S910018
450 MHz + R-IN Engine (150MHz)	512KB +32KB	– (1MB for R-IN)						R7S910015	R7S910016
600 MHz	512KB +32KB	1MB		R7S910007	R7S910013	R7S910027	R7S910028		
450 MHz	512KB	1MB		R7S910006		R7S910025	R7S910026		
430 IVITZ	+32KB	_	R7S910001	R7S910002	R7S910011				
300 MHz	512KB +32KB	-				R7S910035	R7S910036		
	Package		176 QFP	320 BGA	320 BGA	320 BGA	320 BGA	320 BGA	320 BGA
	Encoder I/F			-	Yes	-	Yes	-	Yes
Industrial Ethernet		_ (Standard Ethernet)		EtherCAT		Multi-protocol support			



Utilizing the Arm® Ecosystem

■ Utilizing Renesas' Experience and the Arm® Ecosystem

Customers can benefit from solutions combining Renesas' accumulated experience in the microcontroller industry and the global ecosystem of Arm® partners. Products such as development environments, OS, and middleware are available from partner companies supporting the RZ/T series



RZ/T Series: Development Environments (Integrated Development Environments)

	OLIVITATION SYSTEMS	arm	RENESAS
Development environments	IAR Embedded Workbench® for Arm®	• DS-5	● e² studio*1 e² studio e² studio
Compilers	• IAR C/C++ compiler*2	• Arm CC*3	• GNU tool*4
Other tools	AP4 code generation tool from Renesas is compatible.	AP4 code generation tool from Renesas is compatible.	Code generation function available as a plug-in.
ICEs	I-jet™/I-jet Trace™ for Arm Cortex®-A/R/M JTAGjet-Trace	• DSTREAM™ • ULINKpro™ • ULINKproD™ • ULINK2™	J-Link LITE from Segger J-Link series from Segger*5

^{*1.} Eclipse-based development environment from Renesas (http://renesas.com/e2studio)

RZ/T Series: Development Tools (Debuggers, ICEs)

	Kyoto Microcomputer Co., Ltd.	Our insight, your value	Compute x*
Debuggers	• PARTNER-Jet2	• microVIEW-PLUS	• CSIDE version 7
ICEs		• adviceLUNA II	PALMICE4 PALMICE4 Computer JTAG model Large capacity trace model
Supported compilers	 exeGCC from Kyoto Microcomputer GNU tool*1 Arm CC*2 IAR C/C++ compiler,*3 etc. 	• Arm CC*2 • GNU tool,*1 etc.	 Arm CC*² IAR C/C++ compiler*³ GNU tool,*¹ etc.

^{*1.} GNU TOOLS & SUPPORT Website (https://gcc-renesas.com)

^{*2.} Two versions of the software are available for download free of charge. One limits the code size to 32KB and can be used with no time limitation. The other has no limit on code size and expires after 30 days. (www.iar.com/EWARM)

^{*3.} Arm CC is included in DS-5. In addition to the popularly priced DS-5 RZ/A and RZ/T editions, a fully functional evaluation version of DS-5 that expires after 30 days is available free of charge. Contact your DS-5 dealer for details.

^{*4.} GNU TOOLS & SUPPORT Website (https://gcc-renesas.com)

^{*5.} Renesas does not handle ICEs from Segger. Contact a sales agent for details.

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^{*3.} Two versions of the software are available for download free of charge. One limits the code size to 32KB and can be used with no time limitation. The other has no limit on code size and expires after 30 days. (www.iar.com/EWARM)

e2 studio: Integrated Development Environment Based on Eclipse

e2 studio is an integrated development environment based on the Eclipse open source integrated development environment and CDT plug-ins supporting development in C/C++. The version of e2 studio that is compatible with the RZ/T series provides support for a code generation plug-in.

■ C/C++ perspective: code generation plug-in

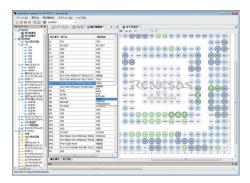
A code generation plug-in is available that enables the user to generate device driver programs for peripheral functions of Renesas microcontrollers (timers, UART, A/D converter, etc.) by entering settings in a graphical user interface. It is possible to specify the processing of multiplexed pins in a pin table and view a pin assignment diagram to confirm the settings.

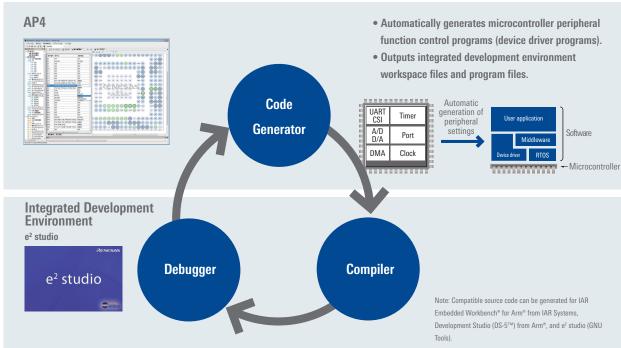


AP4: Code Generation Support Tool

AP4 is a standalone tool that automatically generates peripheral function control programs (device driver programs) based on settings entered by the user. The build tool (compiler) is selectable. This makes it possible to generate peripheral function control program code to match a specific build tool and enables interoperation with integrated development environments. (https://www.renesas.com/ap4)

The version of AP4 that is compatible with the RZ/T series can generate compatible source code for IAR Embedded Workbench® for Arm® from IAR Systems, Development Studio (DS-5™) from Arm®, and e2 studio (GNU Tools).





RZ/T Series: Solutions from Partner Companies

Visit the webpage below for the latest information on RZ/T Series development tools, including solutions from partner companies. https://www.renesas.com/products/microcontrollers-microprocessors/rz/softtools.html#rzt





RZ/T1-Starter-Kit-Plus

https://www.renesas.com/RZT1-Starter-Kit-Plus

- The Renesas Starter Kit+ for RZ/T1 is the perfect starter kit for developers who are new to the RZ/T1.
- The kit includes an LCD display module, J-LINK Lite debugging emulator, and e² studio integrated development environment so you can start evaluating the RZ/T1 immediately after opening the box.
- Ordering number: RTK7910018S01000BE



- RZ/T1 (R7S910018)
- QSPI FlashROM 64Mbyte
- SDRAM 64Mbyte × 2
- NOR Flash 64Mbyte × 2
- Rich interface
- Serial, USB, CAN
- Digilent Pmod I/F (PMOD connector)
- $\Delta \Sigma$ I/F (DSMI connector)
- Ethernet (10/100Base, EtherCAT) I/F etc.
- Audio codec
- Includes Segger's simple debug probe "J-LINK Lite"
- Includes LCD for debugging

RZ/T1 Motion Control Solution Kit

https://www.renesas.com/YDRIVE-IT-RZT1

- RZ/T1 Motion Control Solution Kit is a complete hardware and software solution for the Renesas RZ/T1 MPU. It delivers best-in-class processing power and real-time architecture to run tighter control loops, network connectivity to support deterministic communication, and high-speed encoder interface effectively serving as a connected servo solution on a single chip.
- The kit includes an RZ/T1 CPU card, and a dual channel 3-phase inverter to support dual channel servo motor control with current and position feedback.
- Ordering number: YDRIVE-IT-RZT1



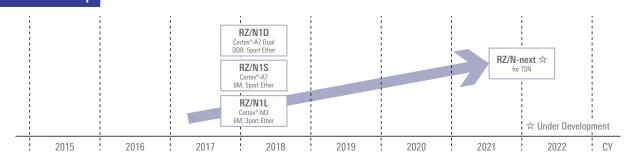
- Package includes all parts needed for motor control evaluation
- Supports safe design and can be used for reference
- Includes multifunction utility tool
- Servo control software is available

MEMO		



RZ/N Series





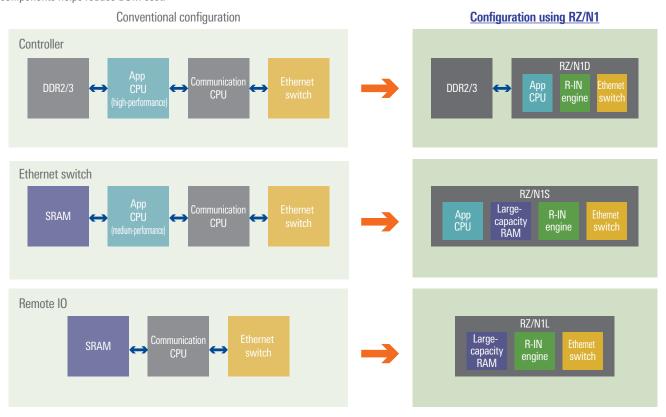
RZ/N Series Features

- 1. Provides optimized microcontrollers for a variety of industrial network applications
- 2. Integrated R-IN engine (accelerator) supporting main industrial Ethernet protocols
- 3. Redundant network configuration reduces network downtime to zero

1. Provides optimized microcontrollers for a variety of industrial network applications

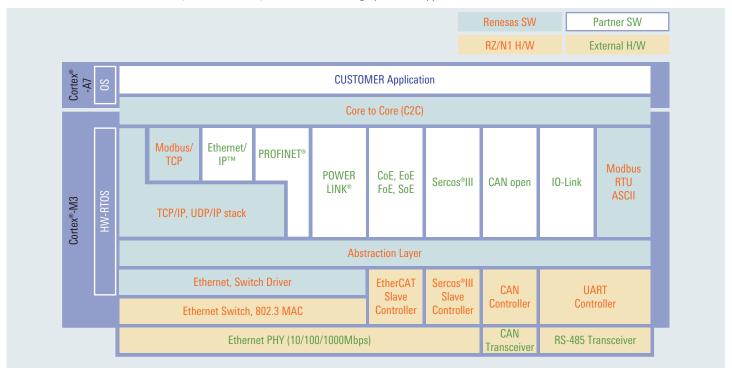
The three CPU types lineup and integrated 5-port gigabit Ethernet switch make it possible to provide the optimal microcontrollers for a wide range of industrial network applications.

- Lineup of three CPU types for excellent hardware scalability: Dual-core Cortex®-A7 (500MHz × 2), single-core Cortex®-A7 (500MHz), and R-IN engine only (125MHz).
- 5-port gigabit Ethernet switch and two independent MAC units support applications such as PLC devices and Ethernet switches. Integration of peripheral components helps reduce BOM cost.



2. Integrated R-IN engine (accelerator) supporting main industrial Ethernet protocols

The R-IN engine accelerator supports a wide range of protocols and enables high-speed processing. It reduces the load on the main CPU (Arm® Cortex®-A7) and contributes to highly efficient application control.



3. Redundant network configuration reduces network downtime to zero

Advanced redundant network configuration support helps eliminate network downtime.

- Redundant network connections: Parallel Redundancy Protocol (PRP)
- Looped network connections: HSR (High-availability Seamless Redundancy), DLR (Device Level Ring), RSTP (Rapid Spawning Trees)

RZ/N Series Application





RZ/N1D Group

CPU core

- Arm® Cortex®-A7 dual-core processor
- Operating frequency: 500MHz

Cache memory

- L1 I-cache: 16KB × 2, D-cache: 16KB × 2
- L2: 256KB

Internal memory

■ 2MB (ECC)

External memory

- DDR2/DDR3 controller
- Quad I/O SPI
- SDIO eMMC
- NAND flash controller

R-IN engine

- Arm® Cortex®-M3
- Operating frequency: 125MHz
- HW-RTOS accelerator
- Ethernet accelerator

Main Ethernet communication functions

- EtherCAT slave controller
- Sercos® III slave controller
- HSR switch (400-pin)
- 5-port Ethernet switch

Other communication functions

- UART × 8 channels
- $I^2C \times 2$ channels
- USB Host/Function × 1 channel, Host 1 channel
- SPI \times 6 channels (master \times 4 channels, slave \times 2 channels)
- CAN

Other functions

- LCD controller
- ADC: 12-bit × 8 channels × 2 units (400-pin)
- ADC: 12-bit × 8 channels × 1 unit (324-pin)
- PWM timer, GPT

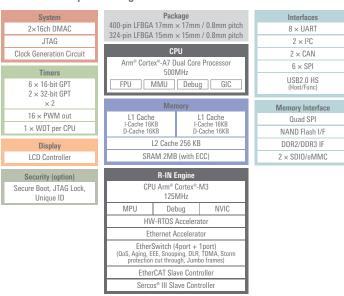
Package

- 400-pin: LFBGA, 17 × 17mm, 0.8mm pin pitch
- 324-pin: LFBGA, 15 × 15mm, 0.8mm pin pitch

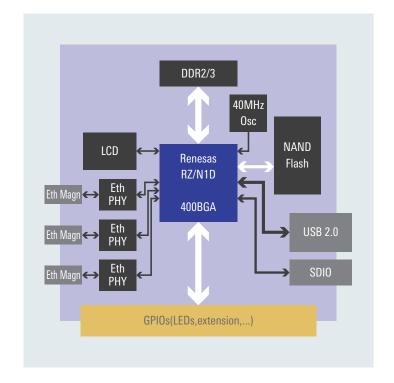
Operating temperature

■ Tj = -40°C to +110°C

■ RZ/N1D Group block diagram



■ Application example: Programmable logic controller block diagram



RZ/N1S Group

CPU core

- Arm® Cortex®-A7 single-core processor
- Operating frequency: 500MHz

Cache memory

- L1 I-cache: 16KB, D-cache: 16KB
- L2: 128KB

Internal memory

- 6MB (ECC)
- External memory
- Quad I/O SPI
- SDIO eMMC
- NAND flash controller

R-IN engine

- Arm® Cortex®-M3
- Operating frequency: 125MHz
- HW-RTOS accelerator
- Ethernet accelerator

Main Ethernet communication functions

- EtherCAT slave controller
- Sercos® III slave controller
- 5-port Ethernet switch

Other communication functions

■ UART × 8 channels

- $I^2C \times 2$ channels
- USB Host/Function × 1 channel, Host 1 channel
- SPI × 6 channels (master × 4 channels, slave × 2 channels)
- CAN

Other functions

- LCD controller
- ADC: 12-bit × 8 channels × 1 unit
- PWM timer, GPT

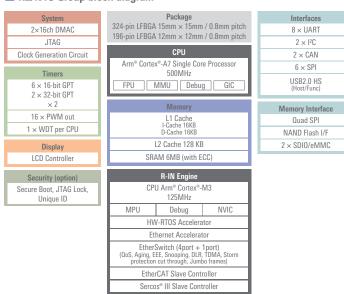
Package

- 324-pin: LFBGA, 15 × 15mm, 0.8mm pin pitch
 196-pin: LFBGA, 12 × 12mm, 0.8mm pin pitch

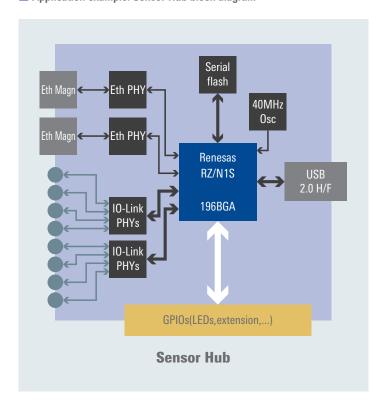
Operating temperature

■ $T_j = -40^{\circ}C \text{ to } +110^{\circ}C$

■ RZ/N1S Group block diagram



Application example: Sensor Hub block diagram





RZ/N1L Group

R-IN engine

- Arm® Cortex®-M3
- Operating frequency: 125MHz
- HW-RTOS accelerator
- Ethernet accelerator

Internal memory

■ 6MB (ECC)

External memory

- Quad I/O SPI
- SDIO eMMC
- NAND flash controller

Main Ethernet communication functions

- EtherCAT slave controller
- Sercos® III slave controller
- GbE Ethernet switch

Other communication functions

- UART × 8 channels
- I²C × 2 channels
- USB Host/Function × 1 channel, Host 1 channel
- SPI \times 6 channels (master \times 4 channels, slave \times 2 channels)
- CAN × 2 channels

Other functions

- LCD controller
- ADC: 12-bit × 8 channels × 1 unit
- PWM timer, GPT

Package

■ 196-pin: LFBGA, 12 × 12mm, 0.8mm pin pitch

Operating temperature $T_j = -40^{\circ}C \text{ to } +110^{\circ}C$

■ RZ/N1L Group block diagram

System	
2×16ch DMAC	196-
JTAG	
Clock Generation Circuit	
Timers	
6 × 16-bit GPT	
2 × 32-bit GPT	
× 2	
16 × PWM out	
1 × WDT per CPU	
	(0

Package 196-pin LFBGA 12mm × 12mm / 0.8mm pitch		
	Memory	
SRA	M 6MB (with E	CC)
	R-IN Engine	
CPL	J Arm® Cortex®- 125MHz	M3
MPU Debug NVIC		
HW-RTOS Accelerator		
Ethernet Accelerator		
EtherSwitch (2port + 1port) (QoS, Aging, EEE, Snooping, DLR, TDMA, Storm protection cut through, Jumbo frames)		
EtherCAT Slave Controller		
Sercos® III Slave Controller		

Interfaces
8 × UART
2 × I ² C
2 × CAN
6 × SPI
USB2.0 HS (Host/Func)
Maman Interfere
Memory Interface
Quad SPI
NAND Flash I/F
1 × SDIO/eMMC

CONNECT IT! ETHERNET RZ/N

https://www.renesas.com/RZN-YConnect-It

- CONNECT IT! ETHERNET RZ/N is the perfect solution kit for developers new to developing with the RZ/N1.
- The kit comes with not only an evaluation board, but also a JTAG emulator and various sample software.
- It is possible to evaluate master communication / slave communication of industrial networks.



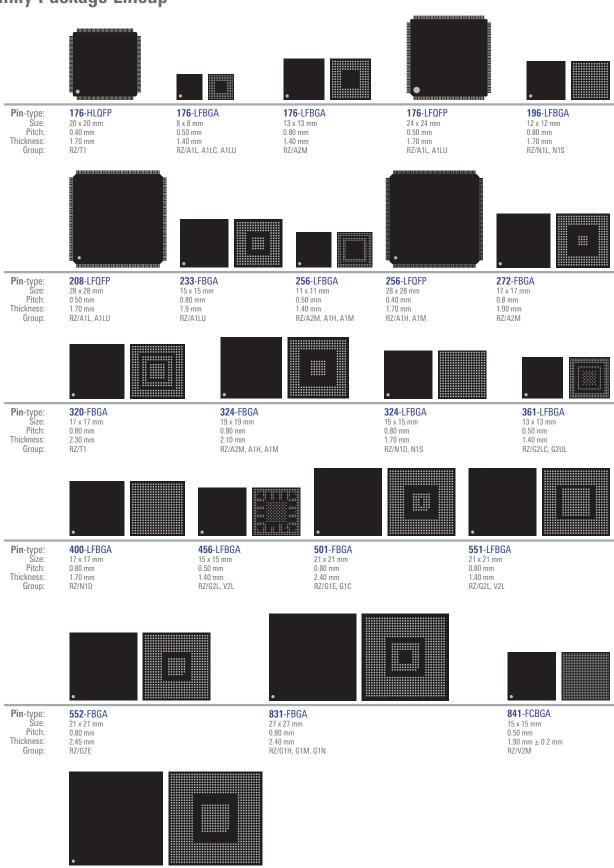
- JTAG emulator
- IAR I-jet Lite (20-pin flat ribbon/USB cable)
- 2 USB cables
- Startup manuals
- Pin setting tool
- RZ/N Solution Kit DVD
 - User's manual
 - OS (Linux, ThreadX®(Evaluation version), HW-RTOS)
 - Software PLC Codesys
 - Protocol stacks

RZ/N Series: Solutions from Renesas Partners

Visit the webpage below for the latest information on RZ/N Series development tools, including solutions from partner companies. https://www.renesas.com/products/microcontrollers-microprocessors/rz/softtools.html#rzn



RZ Family Package Lineup



Pin-type: Size: Pitch: Thickness: Group: **1022-FBGA** 29 x 29 mm 0.80 mm 2.5 mm RZ/G2M, G2N

3.15 mm RZ/G2H



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