

## ISO752xC Low-Power 5 kV<sub>RMS</sub> Dual-Channel Digital Isolators

### 1 Features

- Highest Signaling Rate: 1 Mbps
- Propagation Delay Less Than 20 ns
- Low-Power Consumption
- Wide Ambient Temperature: –40°C to 105°C
- 50 kV/μs Transient Immunity Typical
- Operates From 3.3-V or 5-V Supply and Logic Levels
- 3.3-V and 5.0-V Level Translation
- Safety and Regulatory Approvals
  - 6000 V<sub>PK</sub> Isolation per DIN V VDE V 0884-10 and DIN EN 61010-1
  - 4243 V<sub>RMS</sub> Isolation for 1 Minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1, IEC 61010-1, and IEC 60601-1 End Equipment Standards
  - TUV 5000 V<sub>RMS</sub> Isolation per EN 60950-1 and EN 61010-1
  - CQC Certification per GB4943.1-2011

### 2 Applications

- Opto-Coupler Replacement in:
  - Industrial Field-Buses
    - ProfiBuses
    - ModBuses
    - DeviceNet™ Data Buses
  - Servo Control Interfaces
  - Motor Control
  - Power Supplies
  - Battery Packs

### 3 Description

The ISO7520C and ISO7521C provide galvanic isolation of up to 4243 V<sub>RMS</sub> for 1 minute per UL and 6000 V<sub>PK</sub> per VDE. These devices are also certified to 5000 V<sub>RMS</sub> reinforced insulation per end equipment standards IEC 60950-1, IEC 61010-1, and IEC 60601-1. These digital isolators have two isolated channels with unidirectional (ISO7520C) and bidirectional (ISO7521C) channel configurations. Each isolation channel has a logic input and output buffer separated by a silicon oxide (SiO<sub>2</sub>) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The devices have TTL input thresholds and can operate from 3.3- and 5-V supplies. All inputs are 5-V tolerant when supplied from 3.3-V supplies.

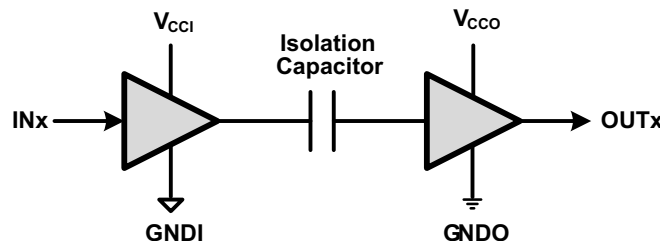
**NOTE:** The ISO7520C and ISO7521C are specified for signaling rates up to 1 Mbps. Due to their fast response time, these devices will also transmit faster data with much shorter pulse widths. Designers must add external filtering to remove spurious signals with input pulse duration < 20 ns, if desired.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7520C	SOIC (16)	10.30 mm × 7.50 mm
ISO7521C		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Schematic



(1) V<sub>CCI</sub> and GNDI are supply and ground connections respectively for the input channels.

(2) V<sub>CCO</sub> and GNDO are supply and ground connections respectively for the output channels.



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2013) to Revision E	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1

Changes from Revision C (November 2011) to Revision D	Page
• Deleted Note 1 from the INSULATION CHARACTERISTICS table .....	12
• Changed the REGULATORY INFORMATION table, TUV column From: Certificate Number: U8V 11 08 77311 006 To: Certificate Number: U8V 1309 77311 010 .....	14

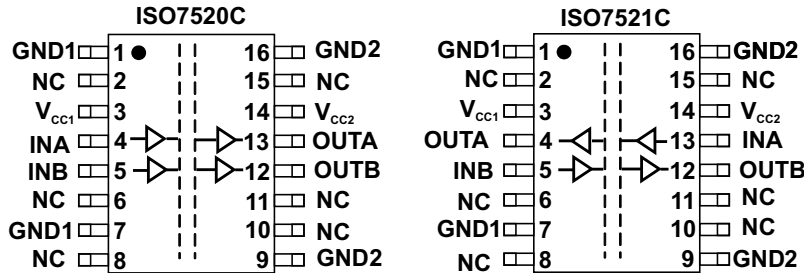
Changes from Revision B (June 2011) to Revision C	Page
• Changed all the devices numbers by adding a 'C' to the end .....	1
• Changed the Safety and Regulatory Approvals Feature .....	1
• Changed the Description section .....	1
• Changed the IEC 60664-1 Ratings Table .....	12
• Changed the INSULATION CHARACTERISTICS table .....	12

<b>Changes from Revision A (September 2010) to Revision B</b>	<b>Page</b>
• Changed 5th Features subbullets.....	1
• Changed the first SWITCHING CHAR table, MAX value, 2nd row from 3.5 to 3.7 and third row from 4 to 4.9.....	8
• Changed the second SWITCHING CHAR table, MAX value, 2nd row from 4 to 5.6 and third row from 5 to 6.3.....	8
• Changed the third SWITCHING CHAR table, MAX value, 3rd row from 5 to 8.5.....	8
• Changed the fourth SWITCHING CHAR table, MAX value, 3rd row from 6 to 6.8.....	9
• Changed REGULATORY INFORMATION table , from: File Number: pending, to: File Number: E181974.....	14

<b>Changes from Original (June 2010) to Revision A</b>	<b>Page</b>
• Added PIN DESCRIPTION table.....	4
• Changed $t_{fs}$ units in Switching Characteristics Table.....	8
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• Changed $t_{fs}$ units in Switching Characteristics Table.....	9
• Deleted $V_{IORM}$ test conditions from INSULATION CHARACTERISTICS table.....	12
• Added $V_{PR}$ parameter and Specifications in INSULATION CHARACTERISTICS table.....	12
• Changed $V_{IOTM}$ row of the INSULATION CHARACTERISTICS tables.....	12
• Changed $V_{ISO}$ Specifications in INSULATION CHARACTERISTICS table.....	12
• Changed Minimum internal gap limit from 0.016 to 0.014 mm.....	12

## 5 Pin Configuration and Functions

DW Package  
16-Pin SOIC  
Top View



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	ISO7520C	ISO7521C		
GND1	1, 7	1, 7	—	Ground connection for $V_{CC1}$
GND2	9, 16	9, 16	—	Ground connection for $V_{CC2}$
INA	4	13	I	Input, channel A
INB	5	5	I	Input, channel B
NC	2, 6, 8, 10, 11, 15	2, 6, 8, 10, 11, 15	—	No internal connection
OUTA	13	4	O	Output, channel A
OUTB	12	12	O	Output, channel B
$V_{CC1}$	3	3	—	Power supply, $V_{CC1}$
$V_{CC2}$	14	14	—	Power supply, $V_{CC2}$

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC1}, V_{CC2}$	Supply voltage <sup>(2)</sup>	-0.5	6	V
$V_I$	Voltage at INx, OUTx	-0.5	$V_{CC} + 0.5$ <sup>(3)</sup>	V
$I_O$	Output Current	-15	15	mA
$T_J$	Maximum junction temperature		150	°C
$T_{stg}$	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.
- (3) Maximum voltage must not exceed 6 V.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000
		Machine model (MM)	±200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC1</sub> , V <sub>CC2</sub>	Supply voltage - 3.3-V Operation	3.15	3.3	3.45	V
	Supply voltage - 5-V Operation	4.75	5	5.25	
I <sub>OH</sub>	High-level output current	-4			mA
I <sub>OL</sub>	Low-level output current			4	mA
V <sub>IH</sub>	High-level output voltage	2		5.25	V
V <sub>IL</sub>	Low-level output voltage	0		0.8	V
T <sub>A</sub>	Ambient temperature	-40		105	°C
T <sub>J</sub> <sup>(1)</sup>	Junction temperature	-40		136	°C
1/t <sub>ui</sub>	Signaling rate	0		1	Mbps
t <sub>ui</sub>	Input pulse duration	1			µs

(1) To maintain the recommended operating conditions for T<sub>J</sub>, see [Thermal Information](#).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ISO7520C, ISO7521C		UNIT
		DW [SOIC]		
		16 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	79.9		°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	44.6		°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	51.2		°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	18.0		°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	42.2		°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## ISO7520C, ISO7521C

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### 6.5 Electrical Characteristics: $V_{CC1}$ and $V_{CC2}$ at $5\text{ V} \pm 5\%$

$V_{CC1}$  and  $V_{CC2}$  at  $5\text{ V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -4\text{ mA}$ ; See <a href="#">Figure 4</a>		$V_{CCO} - 0.8^{(1)}$	4.6		V
		$I_{OH} = -20\text{ }\mu\text{A}$ ; See <a href="#">Figure 4</a>		$V_{CCO} - 0.1$	5		
$V_{OL}$	Low-level output voltage	$I_{OL} = 4\text{ mA}$ ; See <a href="#">Figure 4</a>			0.2	0.4	V
		$I_{OL} = 20\text{ }\mu\text{A}$ ; See <a href="#">Figure 4</a>			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
$I_{IH}$	High-level input current	$I_{Nx}$ at $V_{CCI}^{(2)}$				10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$I_{Nx}$ at $0\text{ V}$		-10			$\mu\text{A}$
CMTI	Common-mode transient immunity	$V_I = V_{CC1}$ or $0\text{ V}$ ; See <a href="#">Figure 6</a>		25	50		$\text{kV}/\mu\text{s}$
<b>SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE-WAVE CLOCK SIGNAL FOR DYNAMIC ICC MEASUREMENT)</b>							
<b>ISO7520C</b>							
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps	$V_I = V_{CC1}$ or $0\text{ V}$ , 15-pF load		0.4	1	mA
$I_{CC2}$	Supply current for $V_{CC2}$	DC to 1 Mbps	$V_I = V_{CC1}$ or $0\text{ V}$ , 15-pF load		3	6	mA
<b>ISO7521C</b>							
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps	$V_I = V_{CC1}$ or $0\text{ V}$ , 15-pF load		2	4	mA
$I_{CC2}$	Supply current for $V_{CC2}$	DC to 1 Mbps	$V_I = V_{CC1}$ or $0\text{ V}$ , 15-pF load		2	4	mA

(1)  $V_{CCO}$  is the supply voltage,  $V_{CC1}$  or  $V_{CC2}$ , for the output channel that is being measured.

(2)  $V_{CCI}$  is the supply voltage,  $V_{CC1}$  or  $V_{CC2}$ , for the input channel that is being measured.

### 6.6 Electrical Characteristics: $V_{CC1}$ at $5\text{ V} \pm 5\%$ , $V_{CC2}$ at $3.3\text{ V} \pm 5\%$

$V_{CC1}$  at  $5\text{ V} \pm 5\%$ ,  $V_{CC2}$  at  $3.3\text{ V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -4\text{ mA}$ ; See <a href="#">Figure 4</a>	ISO7521C (5-V side)	$V_{CCO} - 0.8$	4.6		V
			ISO7520C/7521C(3.3-V side)	$V_{CCO} - 0.4$	3		
		$I_{OH} = -20\text{ }\mu\text{A}$ ; See <a href="#">Figure 4</a>		$V_{CCO} - 0.1$	$V_{CCO}$		
$V_{OL}$	Low-level output voltage	$I_{OL} = 4\text{ mA}$ ; See <a href="#">Figure 4</a>			0.2	0.4	V
		$I_{OL} = 20\text{ }\mu\text{A}$ ; See <a href="#">Figure 4</a>			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
$I_{IH}$	High-level input current	$I_{Nx}$ at $V_{CCI}$				10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$I_{Nx}$ at $0\text{ V}$		-10			$\mu\text{A}$
CMTI	Common-mode transient immunity	$V_I = V_{CC1}$ or $0\text{ V}$ ; See <a href="#">Figure 6</a>		25	40		$\text{kV}/\mu\text{s}$
<b>SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE-WAVE CLOCK SIGNAL FOR DYNAMIC ICC MEASUREMENT)</b>							
<b>ISO7520C</b>							
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps	$V_I = V_{CC1}$ or $0\text{ V}$ , 15-pF load		0.4	1	mA
$I_{CC2}$	Supply current for $V_{CC2}$	DC to 1 Mbps	$V_I = V_{CC1}$ or $0\text{ V}$ , 15-pF load		2	4.5	mA
<b>ISO7521C</b>							
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps	$V_I = V_{CC1}$ or $0\text{ V}$ , 15-pF load		2	4	mA
$I_{CC2}$	Supply current for $V_{CC2}$	DC to 1 Mbps	$V_I = V_{CC1}$ or $0\text{ V}$ , 15-pF load		1.5	3.5	mA

## 6.7 Electrical Characteristics: $V_{CC1}$ at 3.3 V $\pm$ 5%, $V_{CC2}$ at 5 V $\pm$ 5%

 $V_{CC1}$  at 3.3 V  $\pm$  5%,  $V_{CC2}$  at 5 V  $\pm$  5%,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -4\text{ mA}$ ; See <a href="#">Figure 4</a>	ISO7520C/7521C (5-V side)	$V_{CCO} - 0.8$	4.6		V
			ISO7521C (3.3-V side)	$V_{CCO} - 0.4$	3		
		$I_{OH} = -20\ \mu\text{A}$ ; See <a href="#">Figure 4</a>	$V_{CCO} - 0.1$	$V_{CCO}$			
$V_{OL}$	Low-level output voltage	$I_{OL} = 4\text{ mA}$ ; See <a href="#">Figure 4</a>			0.2	0.4	V
		$I_{OL} = 20\ \mu\text{A}$ ; See <a href="#">Figure 4</a>			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
$I_{IH}$	High-level input current	$I_{Nx}$ at $V_{CCI}$				10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$I_{Nx}$ at 0 V		-10			$\mu\text{A}$
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$ or 0 V; See <a href="#">Figure 6</a>		25	40		kV/ $\mu\text{s}$
<b>SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE-WAVE CLOCK SIGNAL FOR DYNAMIC ICC MEASUREMENT)</b>							
<b>ISO7520C</b>							
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps	$V_I = V_{CCI}$ or 0 V, 15-pF load		0.2	0.7	mA
$I_{CC2}$	Supply current for $V_{CC2}$	DC to 1 Mbps	$V_I = V_{CCI}$ or 0 V, 15-pF load		3	6	mA
<b>ISO7521C</b>							
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps	$V_I = V_{CCI}$ or 0 V, 15-pF load		1.5	3.5	mA
$I_{CC2}$	Supply current for $V_{CC2}$	DC to 1 Mbps	$V_I = V_{CCI}$ or 0 V, 15-pF load		2	4	mA

## 6.8 Electrical Characteristics: $V_{CC1}$ and $V_{CC2}$ at 3.3 V $\pm$ 5%

 $V_{CC1}$  and  $V_{CC2}$  at 3.3 V  $\pm$  5%,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -4\text{ mA}$ ; See <a href="#">Figure 4</a>		$V_{CCO} - 0.4$	3		V
		$I_{OH} = -20\ \mu\text{A}$ ; See <a href="#">Figure 4</a>		$V_{CCO} - 0.1$	3.3		
$V_{OL}$	Low-level output voltage	$I_{OL} = 4\text{ mA}$ ; See <a href="#">Figure 4</a>			0.2	0.4	V
		$I_{OL} = 20\ \mu\text{A}$ ; See <a href="#">Figure 4</a>			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
$I_{IH}$	High-level input current	$I_{Nx}$ at $V_{CCI}$					$\mu\text{A}$
$I_{IL}$	Low-level input current	$I_{Nx}$ at 0 V		-10			$\mu\text{A}$
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$ or 0 V; See <a href="#">Figure 6</a>		25	40		kV/ $\mu\text{s}$
<b>SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE-WAVE CLOCK SIGNAL FOR DYNAMIC ICC MEASUREMENT)</b>							
<b>ISO7520C</b>							
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps	$V_I = V_{CCI}$ or 0 V, 15-pF load		0.2	0.7	mA
$I_{CC2}$	Supply current for $V_{CC2}$	DC to 1 Mbps	$V_I = V_{CCI}$ or 0 V, 15-pF load		2	4.5	mA
<b>ISO7521C</b>							
$I_{CC1}$	Supply current for $V_{CC1}$	DC to 1 Mbps	$V_I = V_{CCI}$ or 0 V, 15-pF load		1.5	3.5	mA
$I_{CC2}$	Supply current for $V_{CC2}$	DC to 1 Mbps	$V_I = V_{CCI}$ or 0 V, 15-pF load		1.5	3.5	mA

## 6.9 Power Dissipation Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		ISO7520C, ISO7521C		UNIT
		DW [SOIC]		
		16 PINS		
$P_D$	Device power dissipation, $V_{CC1} = V_{CC2} = 5.25\text{ V}$ , $T_J = 150^\circ\text{C}$ , $C_L = 15\text{ pF}$ , Input a 0.5 MHz 50% duty cycle square wave	42		mW

## 6.10 Switching Characteristics: $V_{CC1}$ and $V_{CC2}$ at $5\text{ V} \pm 5\%$

 $V_{CC1}$  and  $V_{CC2}$  at  $5\text{ V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay time	See <a href="#">Figure 4</a>		9	14	ns
PWD <sup>(1)</sup>	Pulse width distortion $ t_{PHL} - t_{PLH} $			0.3	3.7	ns
$t_{sk(pp)}$	Part-to-part skew time				4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time				3.6	ns
$t_r$	Output signal rise time	See <a href="#">Figure 4</a>		1		ns
$t_f$	Output signal fall time			1		ns
$t_{fs}$	Fail-safe output delay time from input power loss	See <a href="#">Figure 5</a>		6		$\mu\text{s}$

(1) Also known as pulse skew.

## 6.11 Switching Characteristics: $V_{CC1}$ at $5\text{ V} \pm 5\%$ , $V_{CC2}$ at $3.3\text{ V} \pm 5\%$

 $V_{CC1}$  at  $5\text{ V} \pm 5\%$ ,  $V_{CC2}$  at  $3.3\text{ V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay time	See <a href="#">Figure 4</a>		10	17	ns
PWD <sup>(1)</sup>	Pulse width distortion $ t_{PHL} - t_{PLH} $			0.5	5.6	ns
$t_{sk(pp)}$	Part-to-part skew time				6.3	ns
$t_{sk(o)}$	Channel-to-channel output skew time				4	ns
$t_r$	Output signal rise time	See <a href="#">Figure 4</a>		2		ns
$t_f$	Output signal fall time			2		ns
$t_{fs}$	Fail-safe output delay time from input power loss	See <a href="#">Figure 5</a>		6		$\mu\text{s}$

(1) Also known as pulse skew.

## 6.12 Switching Characteristics: $V_{CC1}$ at $3.3\text{ V} \pm 5\%$ , $V_{CC2}$ at $5\text{ V} \pm 5\%$

 $V_{CC1}$  at  $3.3\text{ V} \pm 5\%$ ,  $V_{CC2}$  at  $5\text{ V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay time	See <a href="#">Figure 4</a>		10	17	ns
PWD <sup>(1)</sup>	Pulse width distortion $ t_{PHL} - t_{PLH} $			0.5	4	ns
$t_{sk(pp)}$	Part-to-part skew time				8.5	ns
$t_{sk(o)}$	Channel-to-channel output skew time				4	ns
$t_r$	Output signal rise time	See <a href="#">Figure 4</a>		2		ns
$t_f$	Output signal fall time			2		ns
$t_{fs}$	Fail-safe output delay time from input power loss	See <a href="#">Figure 5</a>		6		$\mu\text{s}$

(1) Also known as pulse skew.



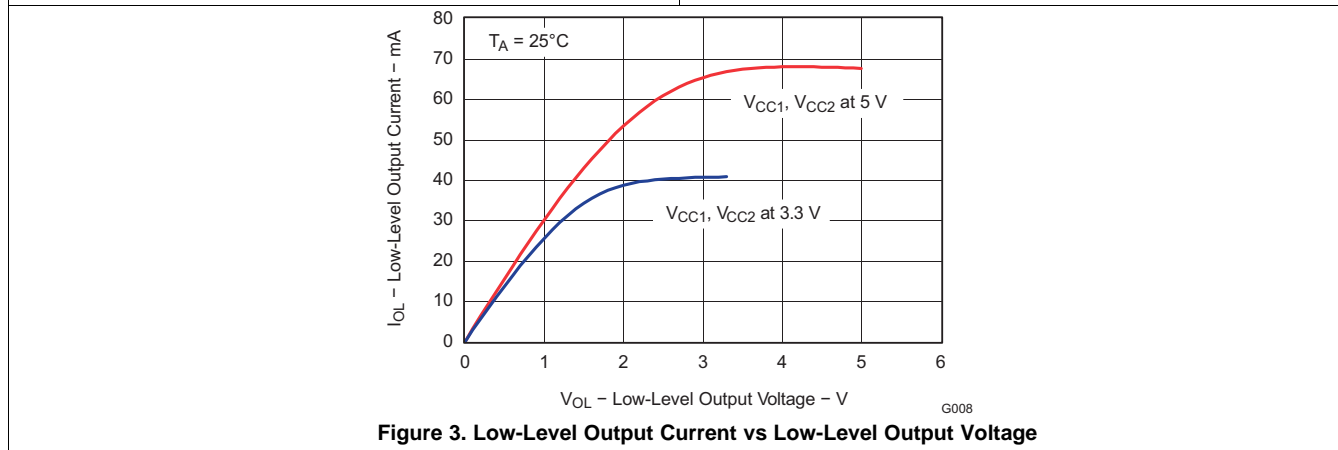
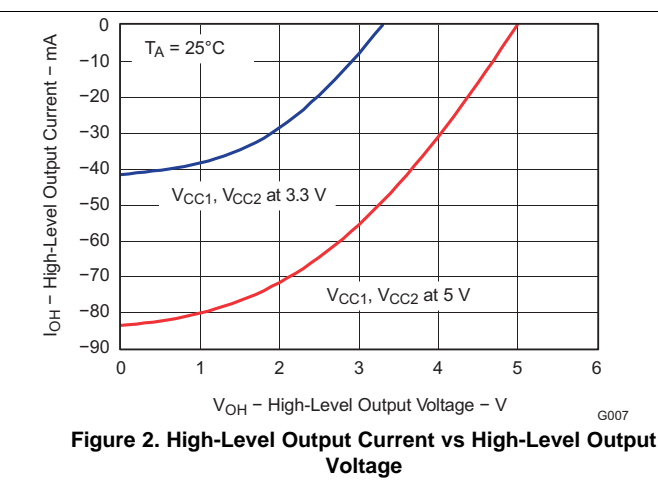
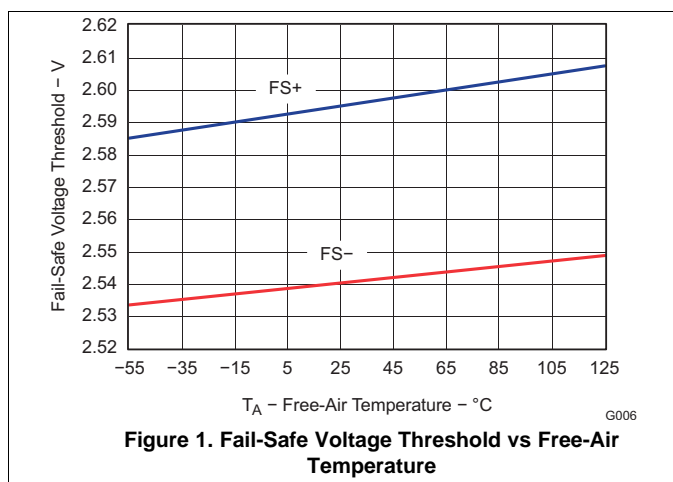
### 6.13 Switching Characteristics: $V_{CC1}$ and $V_{CC2}$ at $3.3\text{ V} \pm 5\%$

$V_{CC1}$  and  $V_{CC2}$  at  $3.3\text{ V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$

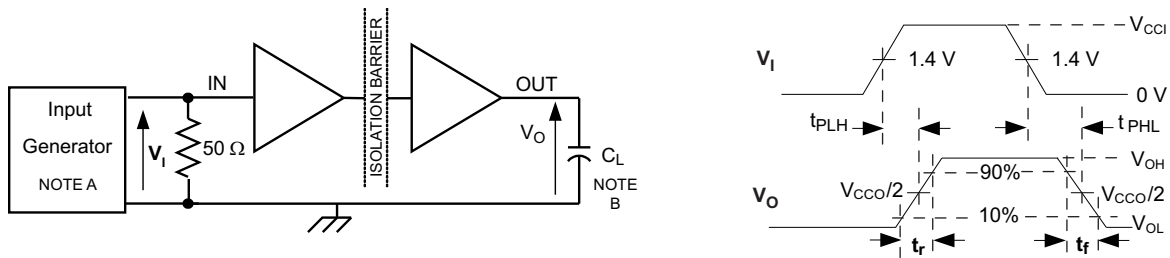
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay time		12	20	ns
PWD <sup>(1)</sup>	Pulse width distortion $ t_{PHL} - t_{PLH} $		1	5	ns
$t_{sk(pp)}$	Part-to-part skew time			6.8	ns
$t_{sk(o)}$	Channel-to-channel output skew time			5.5	ns
$t_r$	Output signal rise time		2		ns
$t_f$	Output signal fall time		2		ns
$t_{fs}$	Fail-safe output delay time from input power loss		6		$\mu\text{s}$

(1) Also known as pulse skew.

### 6.14 Typical Characteristics

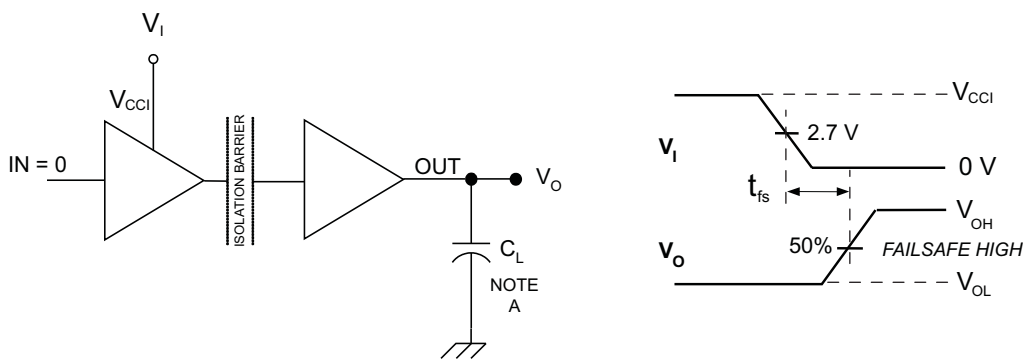


## 7 Parameter Measurement Information



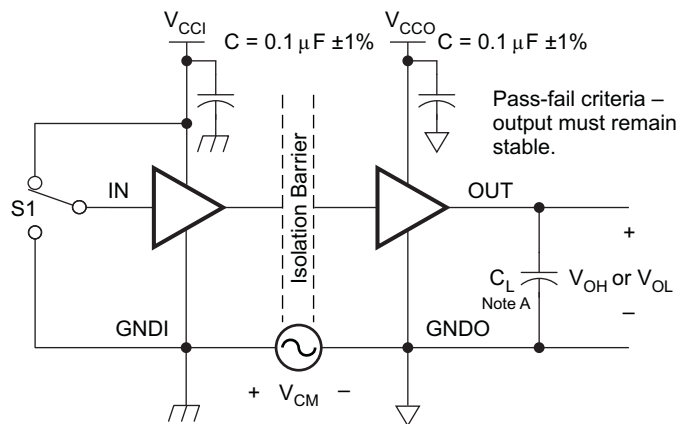
- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50 kHz, 50% duty cycle,  $t_r \leq$  3 ns,  $t_f \leq$  3 ns,  $Z_0 = 50 \Omega$ .
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

**Figure 4. Switching Characteristic Test Circuit and Voltage Waveforms**



- A.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

**Figure 5. Fail-safe Delay Time Test Circuit and Voltage Waveforms**



- A.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

**Figure 6. Common-Mode Transient Immunity Test Circuit**

## 8 Detailed Description

### 8.1 Overview

The isolator in Figure 7 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 1 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single-ended input signal entering the HF-channel is split into a differential signal through the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high- to the low frequency channel. Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

### 8.2 Functional Block Diagram

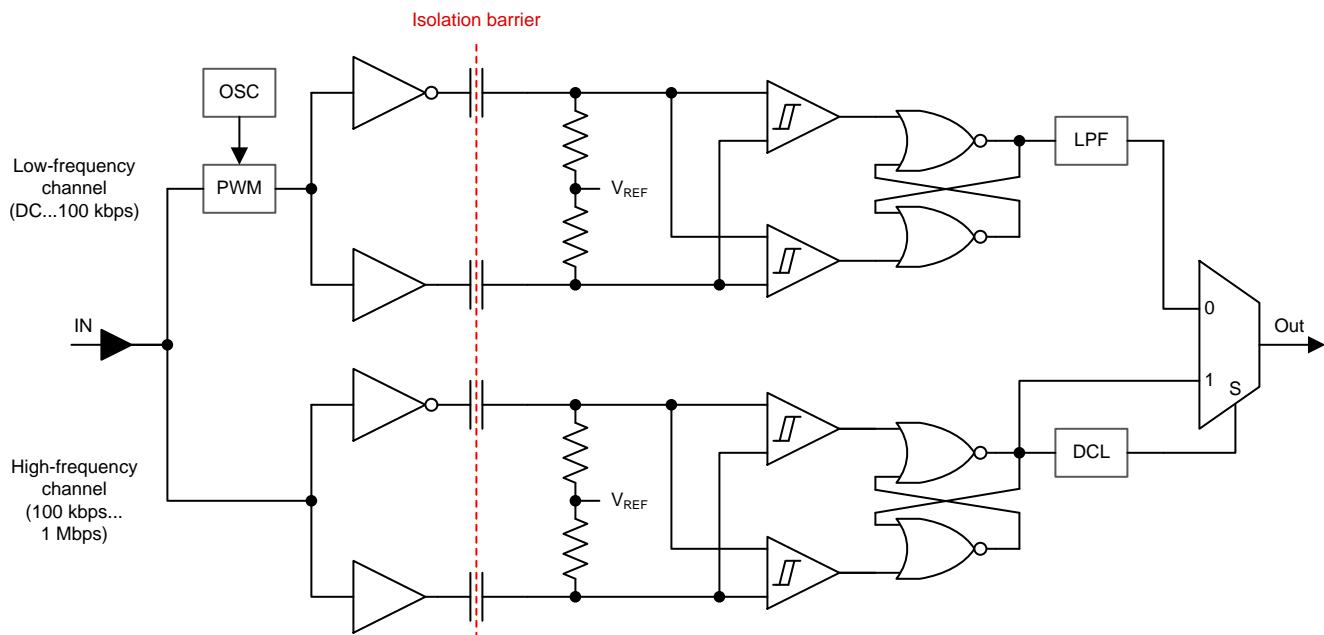


Figure 7. Conceptual Block Diagram of a Digital Capacitive Isolator

## 8.3 Feature Description

### 8.3.1 Insulation Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
$V_{IORM}$	Maximum repetitive peak isolation voltage		1414	$V_{PEAK}$
$V_{PR}$	Input to output test voltage	Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$ , $t = 10$ s, Partial discharge < 5 pC	2262	$V_{PEAK}$
		Method b1, $V_{PR} = V_{IORM} \times 1.875$ , $t = 1$ s (100% Production test) Partial discharge < 5 pC	2651	
		After Input/Output Safety Test Subgroup 2/3, $V_{PR} = V_{IORM} \times 1.2$ , $t = 10$ s, Partial discharge < 5 pC	1697	
$V_{IOTM}$	Maximum Transient Isolation voltage	$t = 60$ sec (qualification)	6000	$V_{PEAK}$
$V_{ISO}$	Withstanding Isolation voltage per UL 1577	$V_{TEST} = V_{ISO} = 4243$ $V_{RMS}$ , $t = 60$ sec (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 5092$ $V_{RMS}$ , $t = 1$ sec (100% production)	4243	$V_{RMS}$
$R_S$	Isolation resistance	$V_{IO} = 500$ V at $T_S = 150^\circ\text{C}$	$>10^9$	$\Omega$
	Pollution degree		2	

### 8.3.2 IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic Isolation Group	Material Group	II
Installation Classification	Rated mains voltages $\leq 150$ Vrms	I - IV
	Rated mains voltages $\leq 600$ Vrms	I - III
	Rated mains voltages $\leq 1000$ Vrms	I - II

### 8.3.3 Package Insulation and Safety-Related Specifications

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	8.34			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	8.1			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN EN 60112 (VDE 0303-11); IEC 60112	>400			V
	Minimum internal gap (Internal Clearance)	Distance through the insulation	0.014			mm
$R_{IO}$	Isolation resistance, input to output <sup>(1)</sup>	$V_{IO} = 500$ V, $T_A = 25^\circ\text{C}$	$>10^{12}$			$\Omega$
		$V_{IO} = 500$ V, $100^\circ\text{C} \leq T_A \leq T_A \text{ max}$	$>10^{11}$			
$C_{IO}$	Barrier capacitance input to output <sup>(1)</sup>	$V_{IO} = 0.4 \sin(2\pi ft)$ , $f = 1$ MHz		2		pF
$C_I$	Input capacitance to ground <sup>(2)</sup>	$V_I = V_{CC}/2 + 0.4 \sin(2\pi ft)$ , $f = 1$ MHz, $V_{CC} = 5$ V		2		pF

(1) All pins on each side of the barrier tied together creating a 2-terminal device.

(2) Measured from input pin to ground.

**NOTE**

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit-board (PCB) do not reduce this distance.

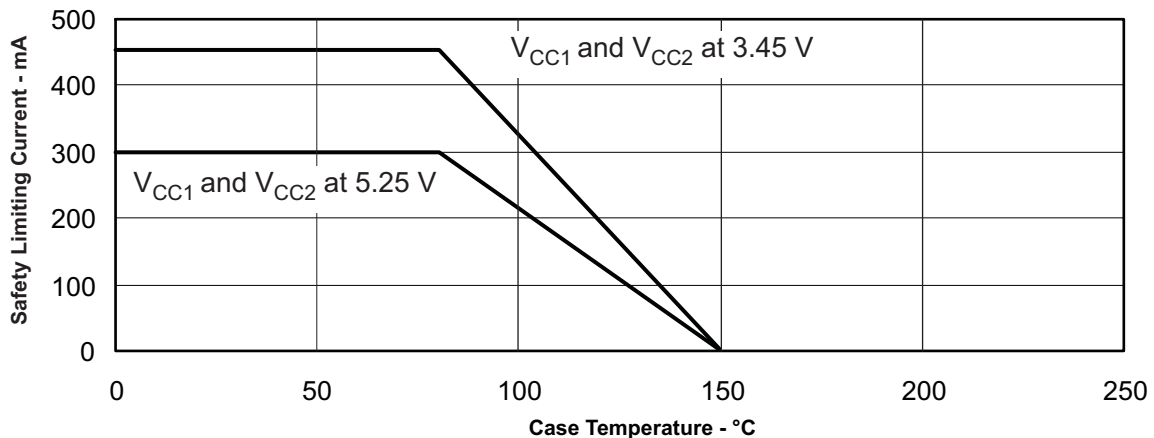
Creepage and clearance on a PCB become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

**8.3.4 Safety Limiting Values**

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current-limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Is	Safety input, output, or supply current	$\theta_{JA} = 79.9^{\circ}\text{C}/\text{W}$ , $V_I = 5.25\text{ V}$ , $T_J = 150^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$			298	mA
		$\theta_{JA} = 79.9^{\circ}\text{C}/\text{W}$ , $V_I = 3.45\text{ V}$ , $T_J = 150^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$			453	
Ts	Maximum Case Temperature				150	$^{\circ}\text{C}$

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the [Thermal Information](#) table is that of a device installed on a High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.



**Figure 8. DW-16  $R_{\theta JC}$  Thermal Derating Curve for VDE**

### 8.3.5 Regulatory Information

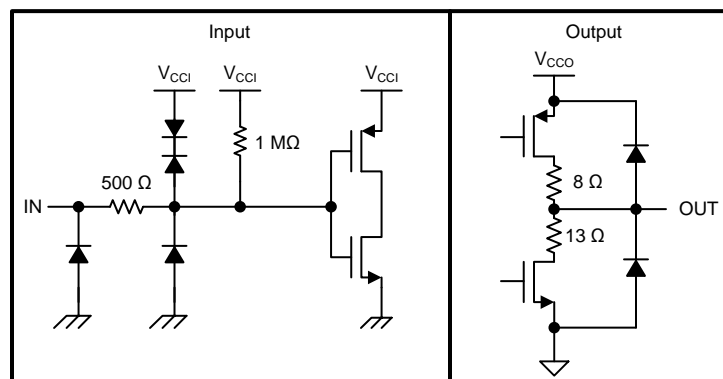
VDE	TUV	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07	Certified according to EN 60950-1 and EN 61010-1	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1, IEC 61010-1, and IEC 60601-1	Recognized under 1577 Component Recognition Program	Certified according to GB 4943.1-2011
Basic Insulation Maximum Transient Isolation voltage, 6000 V <sub>PK</sub> Maximum Repetitive Peak Isolation Voltage, 1414 V <sub>PK</sub>	5000 V <sub>RMS</sub> Isolation Rating; Reinforced Insulation, 400 V <sub>RMS</sub> maximum working voltage; Basic Insulation, 600 V <sub>RMS</sub> maximum working voltage	5000 V <sub>RMS</sub> Isolation Rating; Reinforced insulation per CSA 60950-1-07+A1 and IEC 60950-1 2nd Ed.+A1, 380 V <sub>RMS</sub> max working voltage; Reinforced insulation per CSA 61010-1-04 and IEC 61010-1 2nd Ed, 300 V <sub>RMS</sub> max working voltage; 2 Means of Patient Protection at 125 V <sub>RMS</sub> per IEC 60601-1 (3rd Ed.)	Single Protection, 4243 V <sub>RMS</sub> Withstanding Isolation Voltage	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V <sub>RMS</sub> maximum working voltage
Certificate Number: 40016131	Certificate Number: U8V 1309 77311 010	Master Contract Number: 220991	File Number: E181974	Certificate Number: CQC14001109542

### 8.4 Device Functional Modes

**Table 1. Device Function Table**

V <sub>CCI</sub> <sup>(1)</sup>	V <sub>CCO</sub> <sup>(1)</sup>	INPUT (INA, INB) <sup>(1)</sup>	OUTPUT (OUTA, OUTB) <sup>(1)</sup>
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H
X	PD	X	Undetermined

(1) V<sub>CCI</sub> = Input-side V<sub>CC</sub>; V<sub>CCO</sub> = Output-side V<sub>CC</sub>; PU = Powered Up (V<sub>CC</sub> ≥ 3.15 V); PD = Powered Down (V<sub>CC</sub> ≤ 2.1 V); X = Irrelevant; H = High Level; L = Low Level


**Figure 9. Equivalent Input and Output Schematic Diagrams**

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The ISO7520C and ISO7521C are high-performance, dual-channel digital isolators with a 5-kV<sub>RMS</sub> isolation voltage. The isolator uses single-ended TTL-logic switching technology. The supply voltage range is from 3.15 V to 5.25 V for both supplies, V<sub>CC1</sub> and V<sub>CC2</sub>. When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended TTL digital signal lines. The isolator is typically placed between the data controller (that is,  $\mu$ C or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

### 9.2 Typical Application

The ISO7521C can be used with Texas Instruments' mixed signal micro-controller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4- to 20-mA current loop.

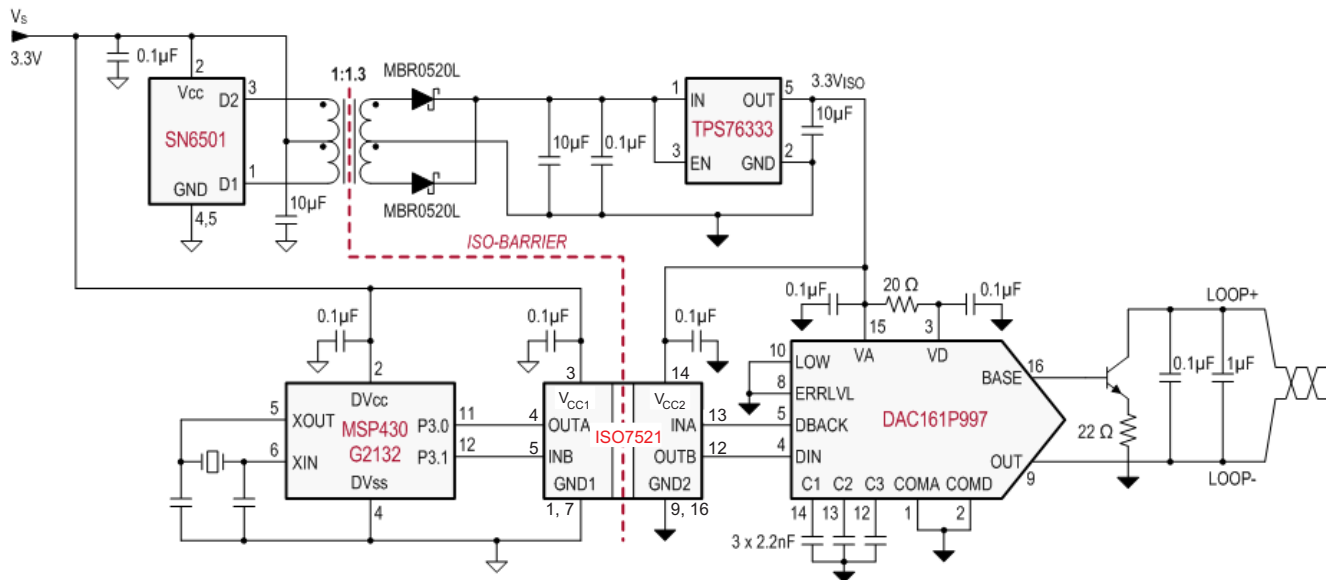


Figure 10. Isolated 4-20 mA Current Loop

#### 9.2.1 Design Requirements

For the ISO7521C, use the parameters shown in [Table 2](#).

Table 2. ISO752xC Design Parameters

PARAMETER	VALUE
Supply voltage	3.15 V to 5.25 V
Decoupling capacitor between V <sub>CC1</sub> and GND1	0.1 $\mu$ F
Decoupling capacitor from V <sub>CC2</sub> and GND2	0.1 $\mu$ F

### 9.2.2 Detailed Design Procedure

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, the ISO7521C only needs two external bypass capacitors to operate.

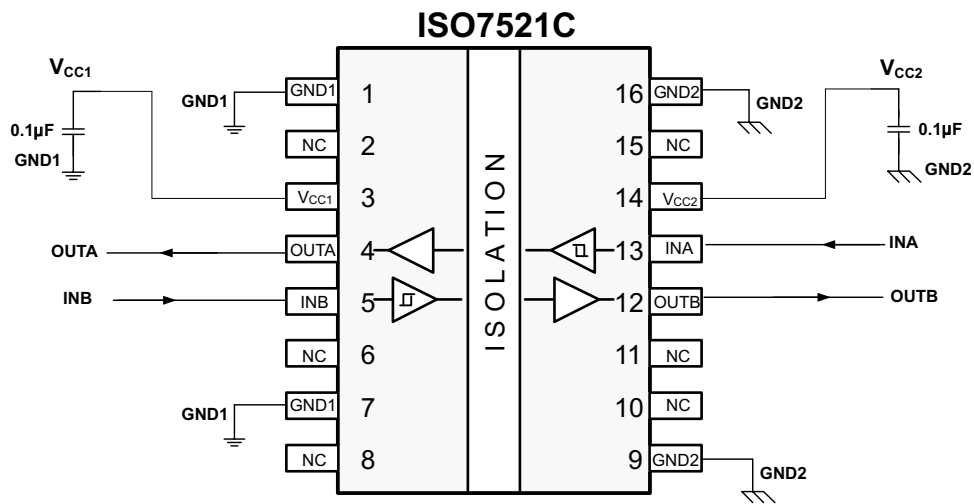


Figure 11. Typical ISO7521C Circuit Hook-up

### 9.2.3 Application Curve

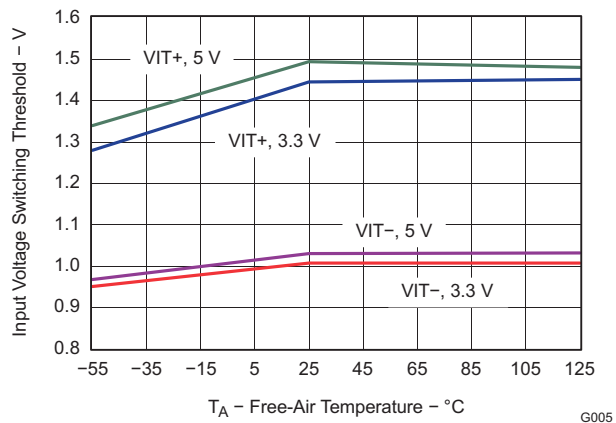


Figure 12. Input Voltage Switching Threshold vs Free-Air Temperature



## 10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, TI recommends placing a 0.1- $\mu\text{F}$  bypass capacitor at the input and output supply pins ( $V_{CC1}$  and  $V_{CC2}$ ). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in the SN6501 data sheet ([SLLSEA0](#)).

## 11 Layout

### 11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 13](#)). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

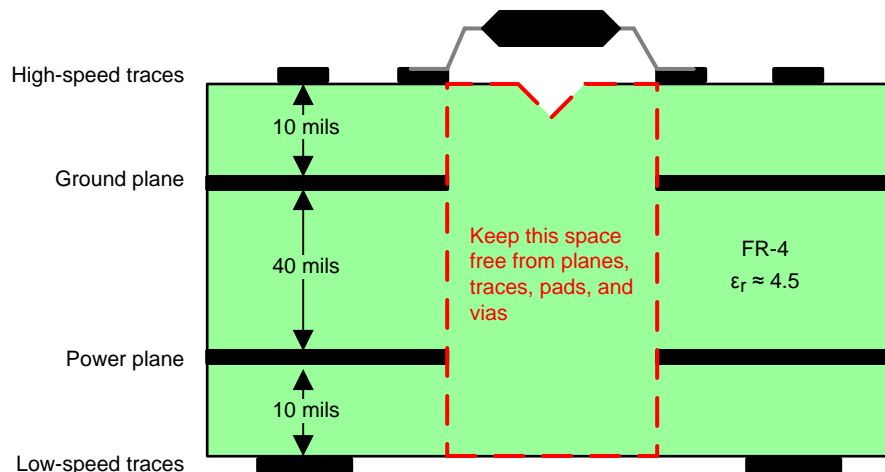
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in<sup>2</sup>.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power/ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly. For detailed layout recommendations, see *Application Note Digital Isolator Design Guide* ([SLLA284](#)).

#### 11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over less expensive alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability characteristics.

### 11.2 Layout Example



**Figure 13. Layout Recommendation**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

*Application Note Digital Isolator Design Guide* ([SLLA284](#))

*Isolation Glossary* ([SLLA353](#))

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 3. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7520C	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
ISO7521C	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.

DeviceNet is a trademark of Open DeviceNet Vendor Association.

All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7520CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7520CDW	<a href="#">Samples</a>
ISO7520CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7520CDW	<a href="#">Samples</a>
ISO7521CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7521CDW	<a href="#">Samples</a>
ISO7521CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	ISO7521CDW	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7520CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7521CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7520CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7521CDWR	SOIC	DW	16	2000	350.0	350.0	43.0

## GENERIC PACKAGE VIEW

**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A



# DW0016B

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



# EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

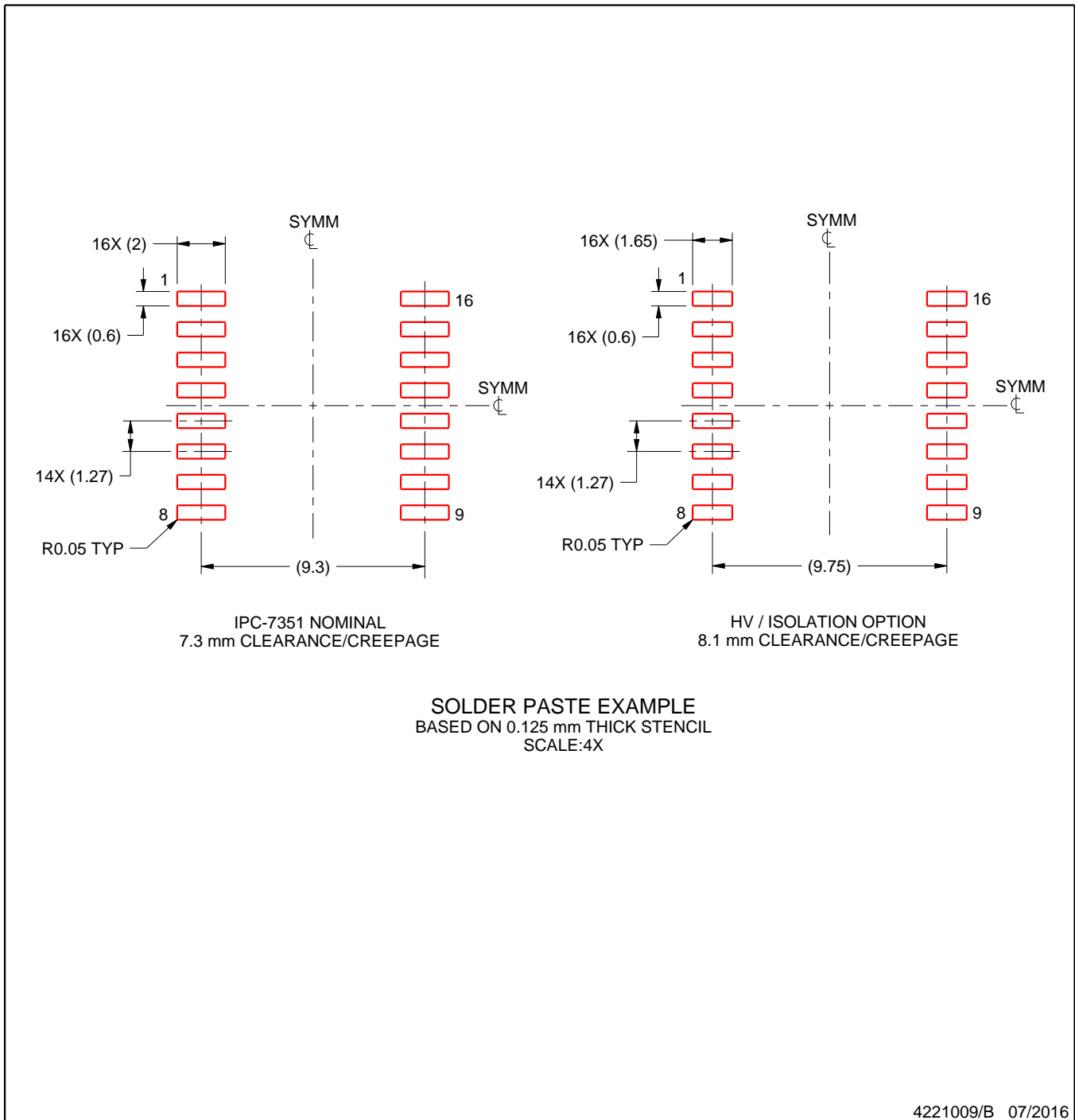
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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