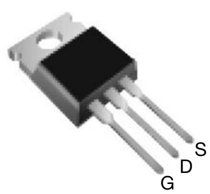
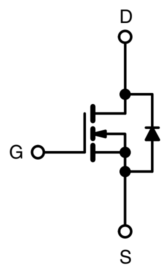
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	400	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	1.0
Q_g (Max.) (nC)	22	
Q_{gs} (nC)	5.8	
Q_{gd} (nC)	9.3	
Configuration	Single	

TO-220AB





N-Channel MOSFET

FEATURES

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss Specified
- Compliant to RoHS Directive 2002/95/EC

Pb Available

RoHS* COMPLIANT

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

TYPICAL SMPS TOPOLOGIES

- Single Transistor Flyback Xfmr. Reset
- Single Transistor Forward Xfmr. Reset (Both US Line Input Only)

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF730APbF
	SiHF730A-E3
SnPb	IRF730A
	SiHF730A

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

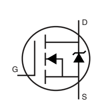
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	400	V
Gate-Source Voltage			V_{GS}	± 30	V
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	5.5	A
		T_C = 100 °C		3.5	
Pulsed Drain Current[a]			I_{DM}	22	
Linear Derating Factor				0.6	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	290	mJ
Repetitive Avalanche Current[a]			I_{AR}	5.5	A
Repetitive Avalanche Energy[a]			E_{AR}	7.4	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	74	W
Peak Diode Recovery dV/dt[c]			dV/dt	4.6	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting T_J = 25 °C, L = 19 mH, R_g = 25 Ω, I_{AS} = 5.5 A (see fig. 12).
c. $I_{SD} \leq$ 5.5 A, dI/dt ≤ 90 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.70	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Ambient	R_{thJA}	-	62	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		400	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.5	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		2.0	-	4.5	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V		-	-	25	μA
		V_{DS} = 320 V, V_{GS} = 0 V, T_J = 125 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 3.3 A[b]	-	-	1.0	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 3.3 A		3.1	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	600	-	pF
Output Capacitance	C_{oss}			-	103	-	
Reverse Transfer Capacitance	C_{rss}			-	4.0	-	
Output Capacitance	C_{oss}	V_{GS} = 0 V	V_{DS} = 1.0 V, f = 1.0 MHz	-	890	-	
			V_{DS} = 320 V, f = 1.0 MHz	-	30	-	
Effective Output Capacitance	C_{oss} eff.		V_{DS} = 0 V to 320 V[c]	-	45	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 3.5 A, V_{DS} = 320 V see fig. 6 and 13[b]	-	-	22	nC
Gate-Source Charge	Q_{gs}			-	-	5.8	
Gate-Drain Charge	Q_{gd}			-	-	9.3	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 200 V, I_D = 3.5 A, R_g = 12 Ω, R_D = 57 Ω, see fig. 10[b]		-	10	-	ns
Rise Time	t_r			-	22	-	
Turn-Off Delay Time	$t_{d(off)}$			-	20	-	
Fall Time	t_f			-	16	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	5.5	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	22	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 5.5 A, V_{GS} = 0 V[b]		-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 3.5 A, dI/dt = 100 A/μs[b]		-	370	550	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	1.6	2.4	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

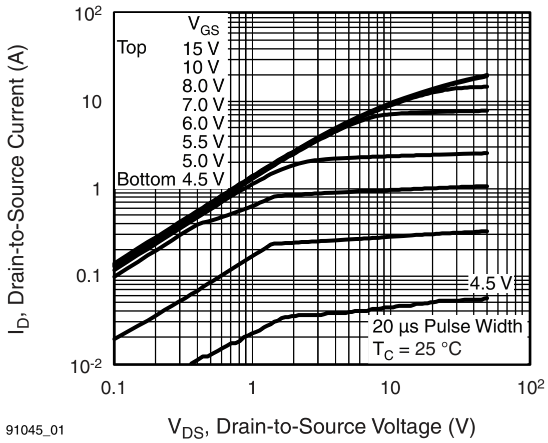


Fig. 1 - Typical Output Characteristics

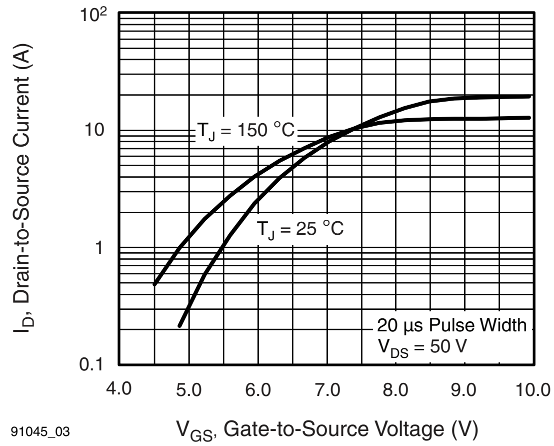


Fig. 3 - Typical Transfer Characteristics

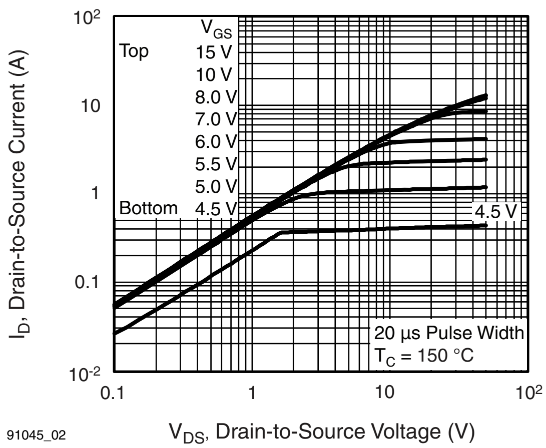


Fig. 2 - Typical Output Characteristics

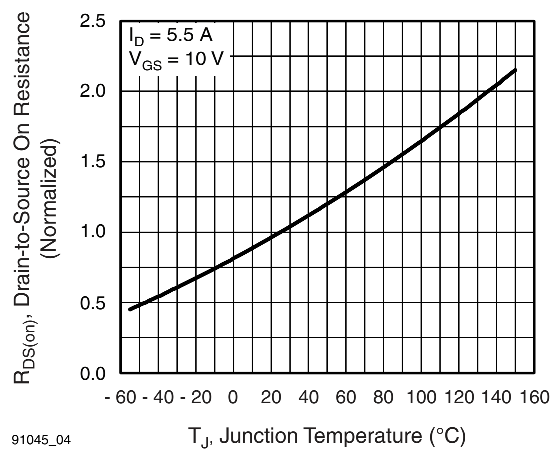


Fig. 4 - Normalized On-Resistance vs. Temperature

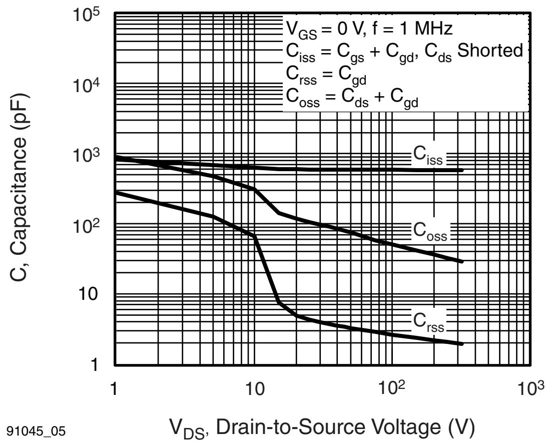


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

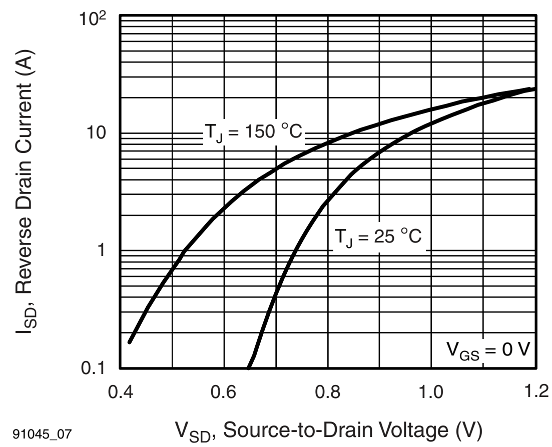


Fig. 7 - Typical Source-Drain Diode Forward Voltage

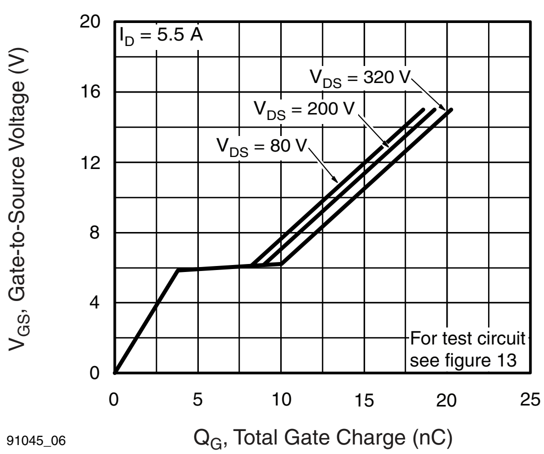


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

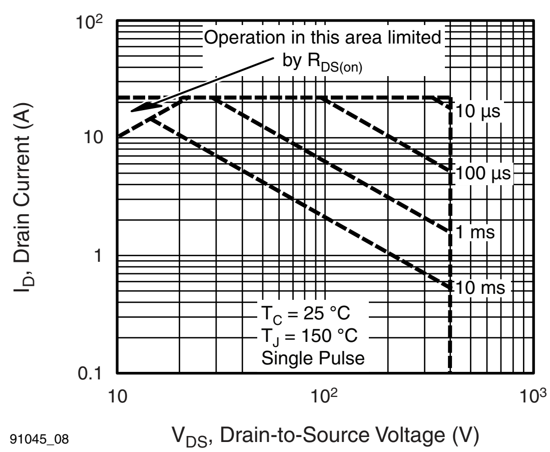


Fig. 8 - Maximum Safe Operating Area

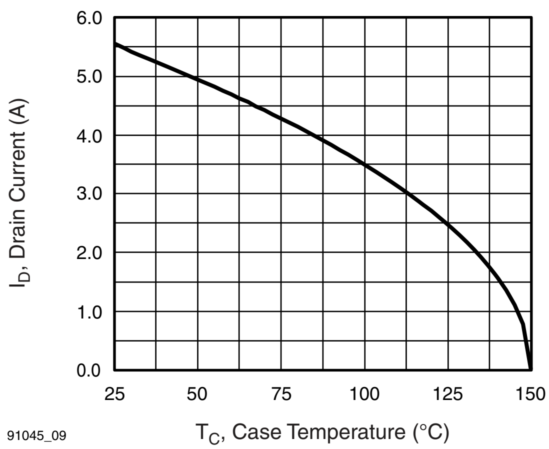


Fig. 9 - Maximum Drain Current vs. Case Temperature

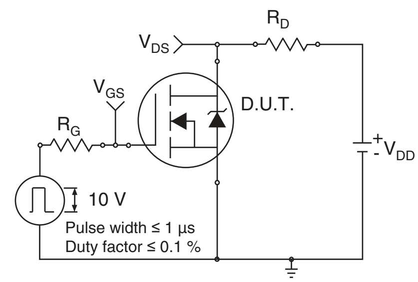


Fig. 10a - Switching Time Test Circuit

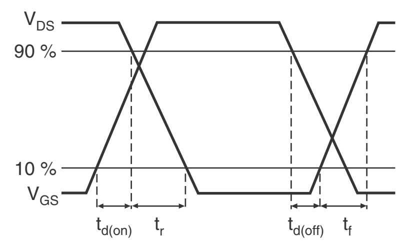


Fig. 10b - Switching Time Waveforms

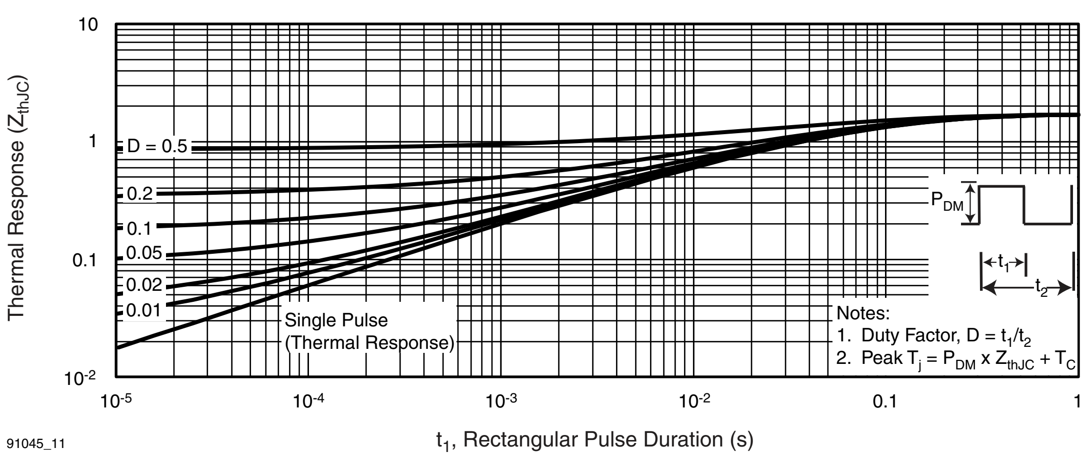


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

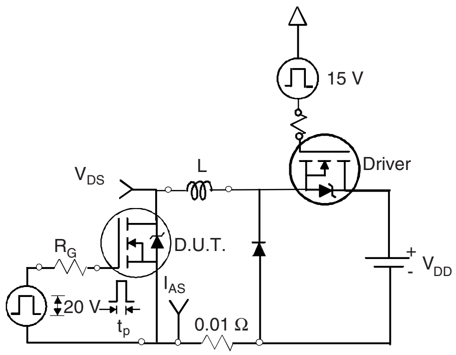


Fig. 12a - Unclamped Inductive Test Circuit

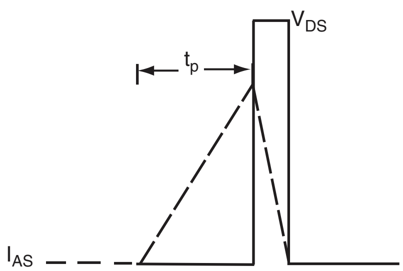


Fig. 12b - Unclamped Inductive Waveforms

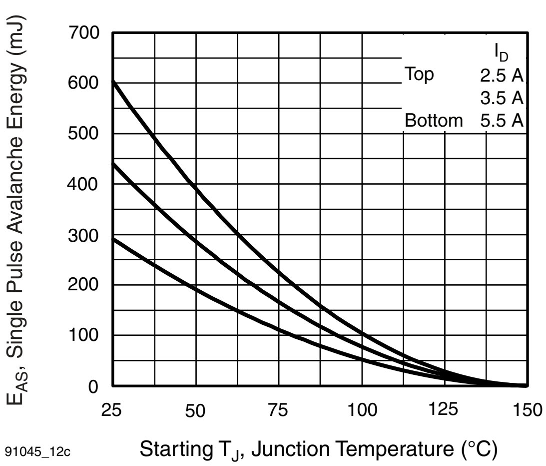


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

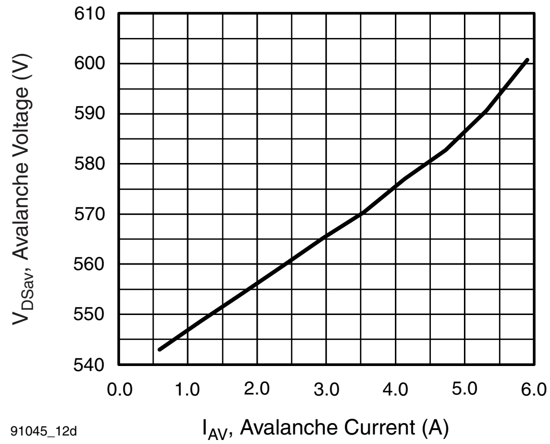


Fig. 12d - Typical Drain Source Voltage vs. Avalanche Current

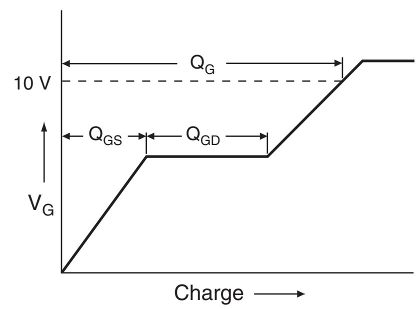


Fig. 13a - Basic Gate Charge Waveform

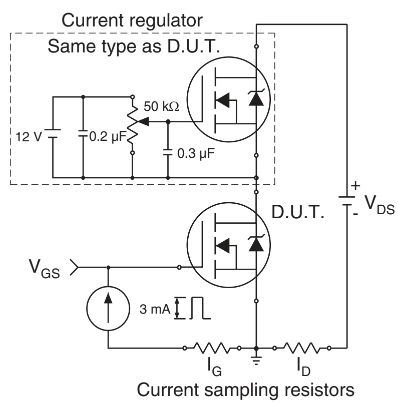
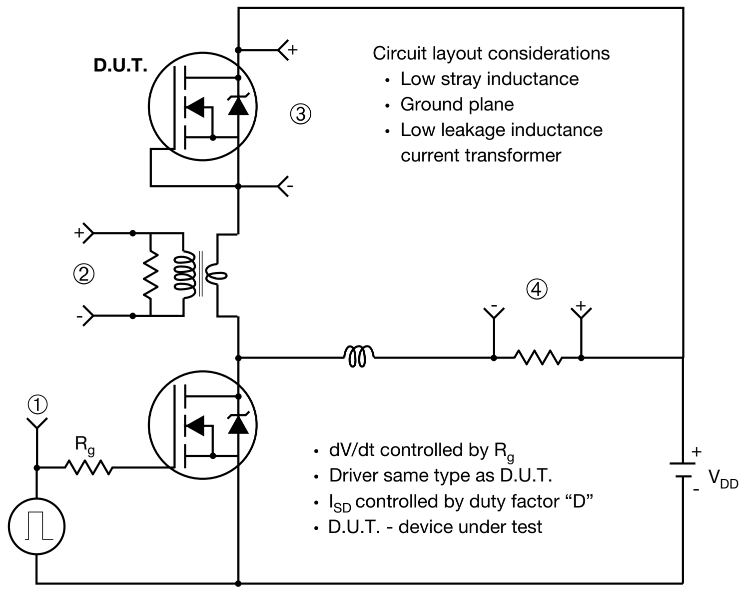
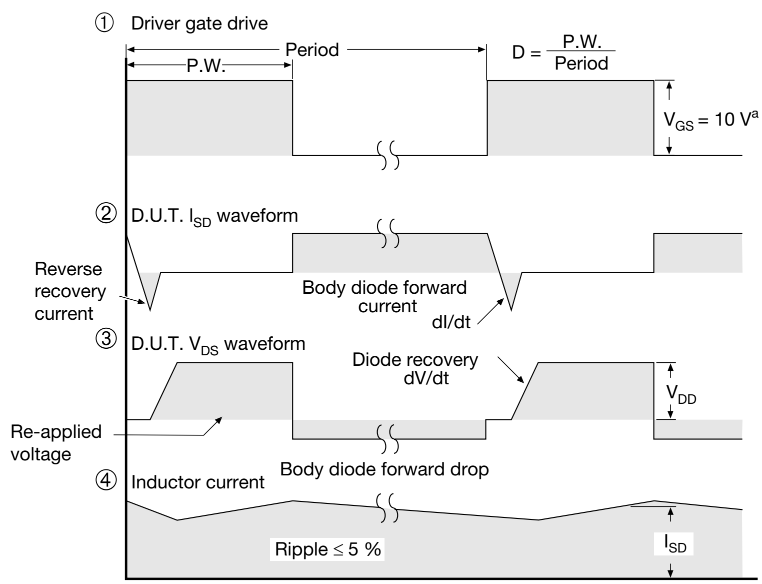


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





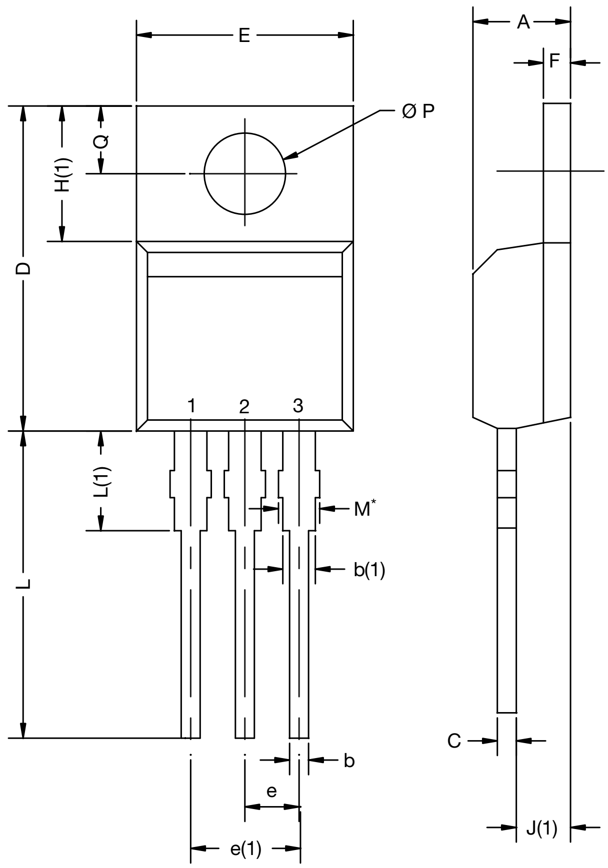
Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91045.

TO-220-1



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<tr><th>MIN.</th><th>MAX.</th><th>MIN.</th><th>MAX.</th></tr>
<tr><td>A</td><td>4.24</td><td>4.65</td><td>0.167</td><td>0.183</td></tr>
<tr><td>b</td><td>0.69</td><td>1.02</td><td>0.027</td><td>0.040</td></tr>
<tr><td>b(1)</td><td>1.14</td><td>1.78</td><td>0.045</td><td>0.070</td></tr>
<tr><td>c</td><td>0.36</td><td>0.61</td><td>0.014</td><td>0.024</td></tr>
<tr><td>D</td><td>14.33</td><td>15.85</td><td>0.564</td><td>0.624</td></tr>
<tr><td>E</td><td>9.96</td><td>10.52</td><td>0.392</td><td>0.414</td></tr>
<tr><td>e</td><td>2.41</td><td>2.67</td><td>0.095</td><td>0.105</td></tr>
<tr><td>e(1)</td><td>4.88</td><td>5.28</td><td>0.192</td><td>0.208</td></tr>
<tr><td>F</td><td>1.14</td><td>1.40</td><td>0.045</td><td>0.055</td></tr>
<tr><td>H(1)</td><td>6.10</td><td>6.71</td><td>0.240</td><td>0.264</td></tr>
<tr><td>J(1)</td><td>2.41</td><td>2.92</td><td>0.095</td><td>0.115</td></tr>
<tr><td>L</td><td>13.36</td><td>14.40</td><td>0.526</td><td>0.567</td></tr>
<tr><td>L(1)</td><td>3.33</td><td>4.04</td><td>0.131</td><td>0.159</td></tr>
<tr><td>Ø P</td><td>3.53</td><td>3.94</td><td>0.139</td><td>0.155</td></tr>
<tr><td>Q</td><td>2.54</td><td>3.00</td><td>0.100</td><td>0.118</td></tr>
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DWG: 6031</td></tr>
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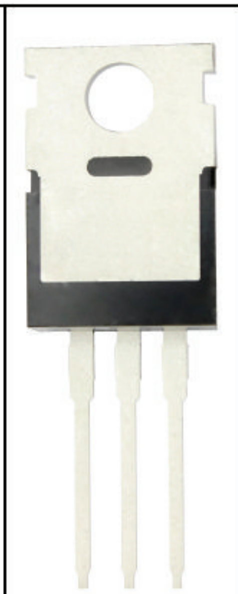
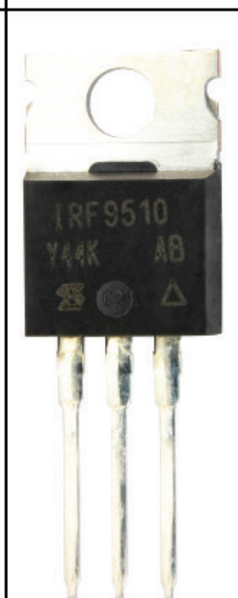
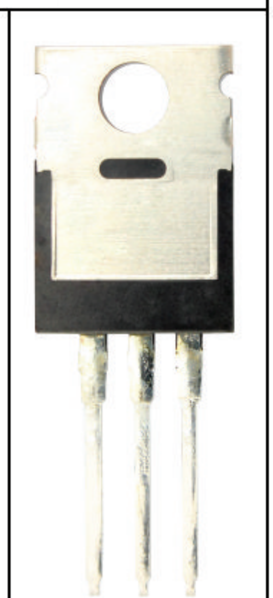
Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

<table>
<tr><th colspan="4">Package Picture</th></tr>
<tr><th colspan="2">ASE</th><th colspan="2">Xi'an</th></tr>
<tr><td></td><td></td><td></td><td></td></tr>
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For technical questions, contact: hvm@vishay.com

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