

### Product introduction

SN74LVC1G00 is a 2-input NAND integrated circuit, which can realize the mathematical logic operation of  $Y = \overline{A+B}$  and  $Y = \overline{A*B}$ . Advanced CMOS process design is adopted, which has the working characteristics of low power consumption and high output driving capability. The chip can work normally when the power supply voltage VCC is between 1.65V and 5.5V V. And 74LVC1G00 has a variety of small package shapes, It can be widely used in high-end precision instruments, miniaturized low-power handheld devices, artificial intelligence and other fields.

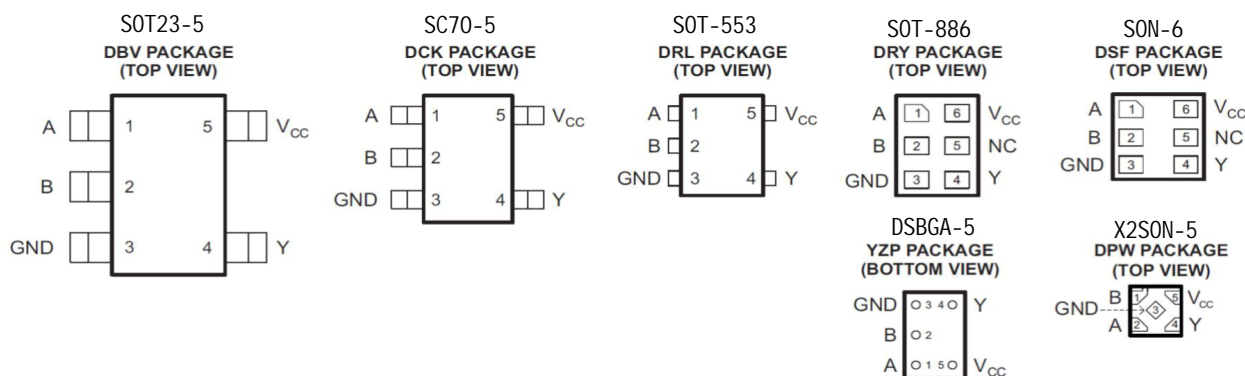
### Product features

- Low input current: 0.1uA typical
- Low static power consumption: 0.1uA typical
- High output drive: VCC=4.5V, more than 32MA
- Wide working voltage range: 1.65V to 5.5V
- Package form: DBV/DCK/DRL/YZP/ DRY/DSF/ DPW

### product usage

- Portable audio interface
- digital television
- Wireless headphones, smart watches, etc.
- Blu-ray player and home theater
- Solid state drive
- Smart wearable devices

### Package form and pin function definition



NAME	PIN			DESCRIPTION
	DBV, DCK, DRL, YZP	DRY, DSF	DPW	
A	1	1	2	Input
B	2	2	1	Input
GND	3	3	3	Ground
Y	4	4	4	Output
V <sub>CC</sub>	5	6	5	Power pin
NC		5		Not connected

Note: NC null pin, no connecting wire inside.

■ Limit parameter

parameter	symbol	limit value	unit
operating voltage	V <sub>CC</sub>	6.5	V
input	V <sub>IN</sub>	-0.5~6.5	V
Output voltage (1)	V <sub>OUT</sub>	-0.5~6.5	V
Single pin output current	I <sub>OUT</sub>	25	mA
Or Vcc current.	I <sub>CC</sub>	50	mA
Storage temperature	T <sub>S</sub>	-65-150	°C
Pin welding temperature	T <sub>W</sub>	260, 10s	°C
Working temperature	T <sub>A</sub>	-40-105	°C

Note: 1. In the power-off state of VCC=0V, the limit voltage that the output can bear,

2. Limit parameter refers to the limit value that can't be exceeded under any conditions. If it exceeds this limit value, it may cause physical damage such as product deterioration; At the same time, the chip can't work normally when it is close to the limit parameters.

■ Principle logic diagram



■ truth table

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

■ working conditions

project	symbol	test condition	minimum value	typical value	maximum	unit
operating voltage	VC	-	1.65	-	5.5	V
Input high level voltage	VHI	VC =1.65V~1.95V	0.65* VC	-	-	V
		VC =2.3V~2.7V	1.7V	-	-	
		VC =3V~5.5V	0.7* VC	-	-	
Low-Level Input Voltage	VIL	VC =1.65V~1.95V	-	-	0.35* VC	V
		VC =2.3V~2.7V	-	-	0.7	
		VC =3V~5.5V	-	-	0.3* VC	
input voltage	VI	-	0	-	5.5	V
Output voltage	VO	-	0	-	VC	V
High level output current	IOH	VC =1.65V	-	-	-4	mA
		VC =2.3V	-	-	-8	
		VC =3V	-	-	-16	
		VC =4.5V	-	-	-32	
Low level output current	IOL	VC =1.65V	-	-	4	mA
		VC =2.3V	-	-	8	
		VC =3V	-	-	16	
		VC =4.5V	-	-	32	

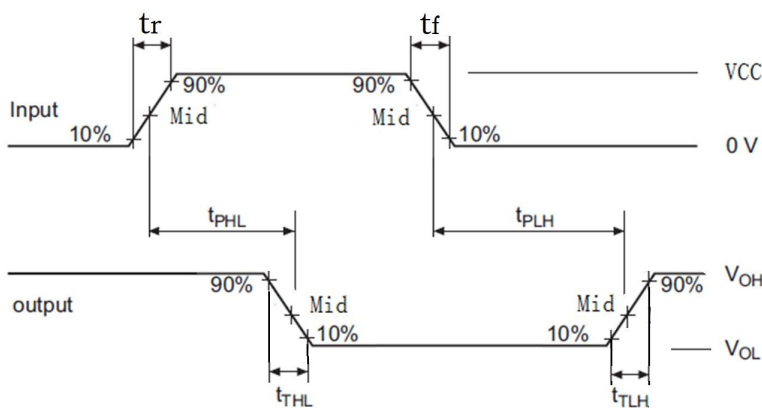
■ Electrical characteristics

Electrical characteristics of DC:  $T_a=25^{\circ}\text{C}$

project	symbol	test condition	minimum value	typical value	maximum value	unit	
High level load voltage	$V_{OH}$	$I_{OH} = -100\mu\text{A}$	1.65V	1.64	5.5	V	
		$I_{OH} = -4\text{ mA}$	1.65V	1.47	-		
		$I_{OH} = -8\text{ mA}$	2.3V	2.15	-		
		$I_{OH} = -16\text{ mA}$	3V	2.73	-		
		$I_{OH} = -32\text{ mA}$	4.5V	4.0	-		
Low level load voltage	$V_{OL}$	$I_{OH} = 100\mu\text{A}$	1.65V~5.5V	0.01	-	V	
		$I_{OH} = 4\text{ mA}$	1.65V	0.11	-		
		$I_{OH} = 8\text{ mA}$	2.3V	0.11	-		
		$I_{OH} = 16\text{ mA}$	3V	0.2	-		
		$I_{OH} = 32\text{ mA}$	4.5V	0.35	-		
incoming current	$I_I$	A	$V_I = 5.5\text{V}$ 或 $\text{GND}$	0~5.5V	0.01	$\pm 5$	uA
		B		0.01	$\pm 5$		
Turn-off current	$I_{OFF}$	$V_I$	$V_I = 5.5\text{V}$	0	0.01	$\pm 10$	uA
		$V_O$	$V_O = 5.5\text{V}$	0	0.01	$\pm 10$	
operational current	$I_{CC}$	$V_I = 5.5\text{V}, I_O = 0$	1.65V~5.5V	0.01	10	uA	
		$V_I = \text{GND}, I_O = 0$		0.01	10		
Working current variation value	$\Delta I_{CC}$	A= $V_{CC} - 0.6\text{V}$ B= $V_{CC}$ 或 $\text{GND}$	3V~5.5V	25	-	uA	
		B= $V_{CC} - 0.6\text{V}$ A= $V_{CC}$ 或 $\text{GND}$		25	-		uA

Ac electrical characteristics:  $T_a=25^{\circ}\text{C}$   $V(298)=5.0\text{V}$ ,  $t_r = \leq 20\text{ns}$ . See test method.

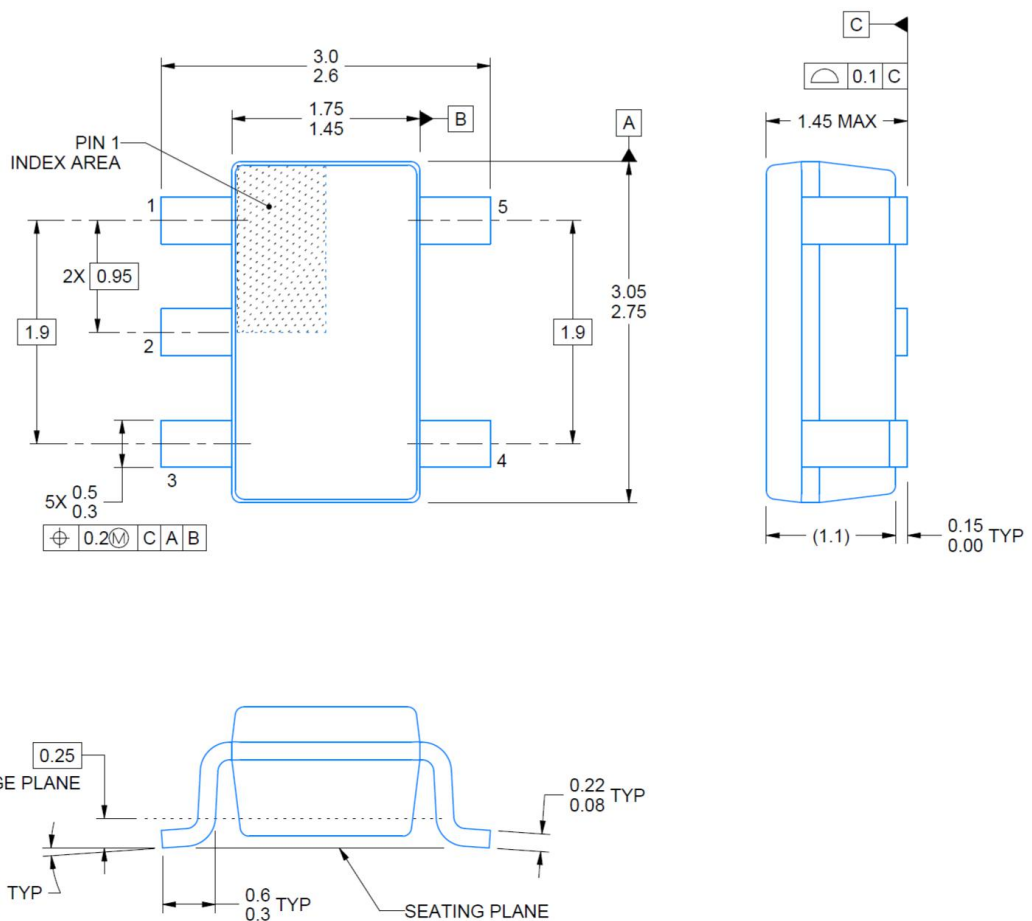
project	symbol	test condition	minimum value	typical value	maximum	unit
Maximum transmission delay time a, B to Y		$C = 15\text{pF}$	-	10	-	ns
		$C = 15\text{pF}$	-	10	-	ns



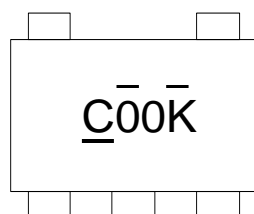
- Note: 1. CL capacitor is external chip capacitor (0603), which is connected close to the output pin, and the capacitor ground is close to the chip GND;  
 2. Input: port input level,  $f=500\text{kHz}$ ,  $D=50\%$ ;  $t_r=t_f \leq 20\text{ns}$ ;  
 3. Output: Y-terminal output test.

■ Encapsulated information

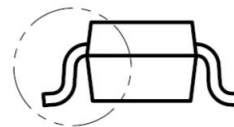
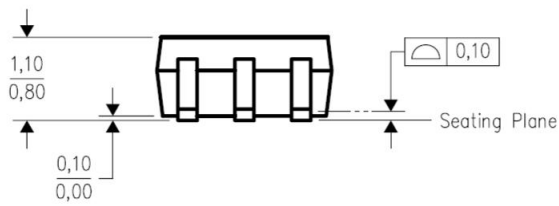
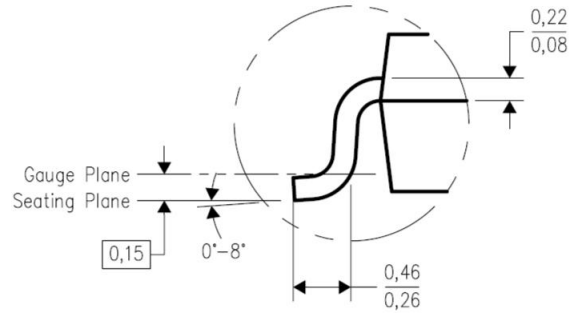
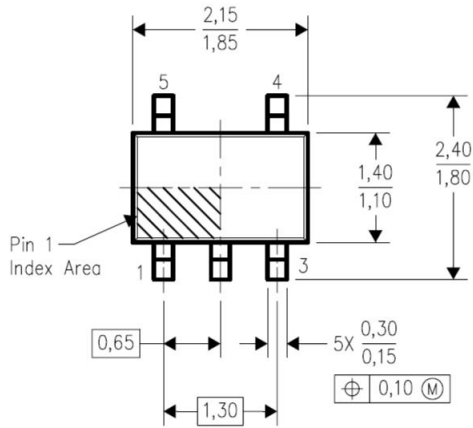
DBV (SOT23-5)



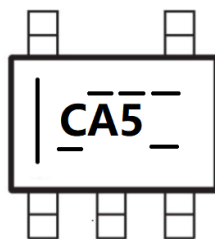
■ Marking



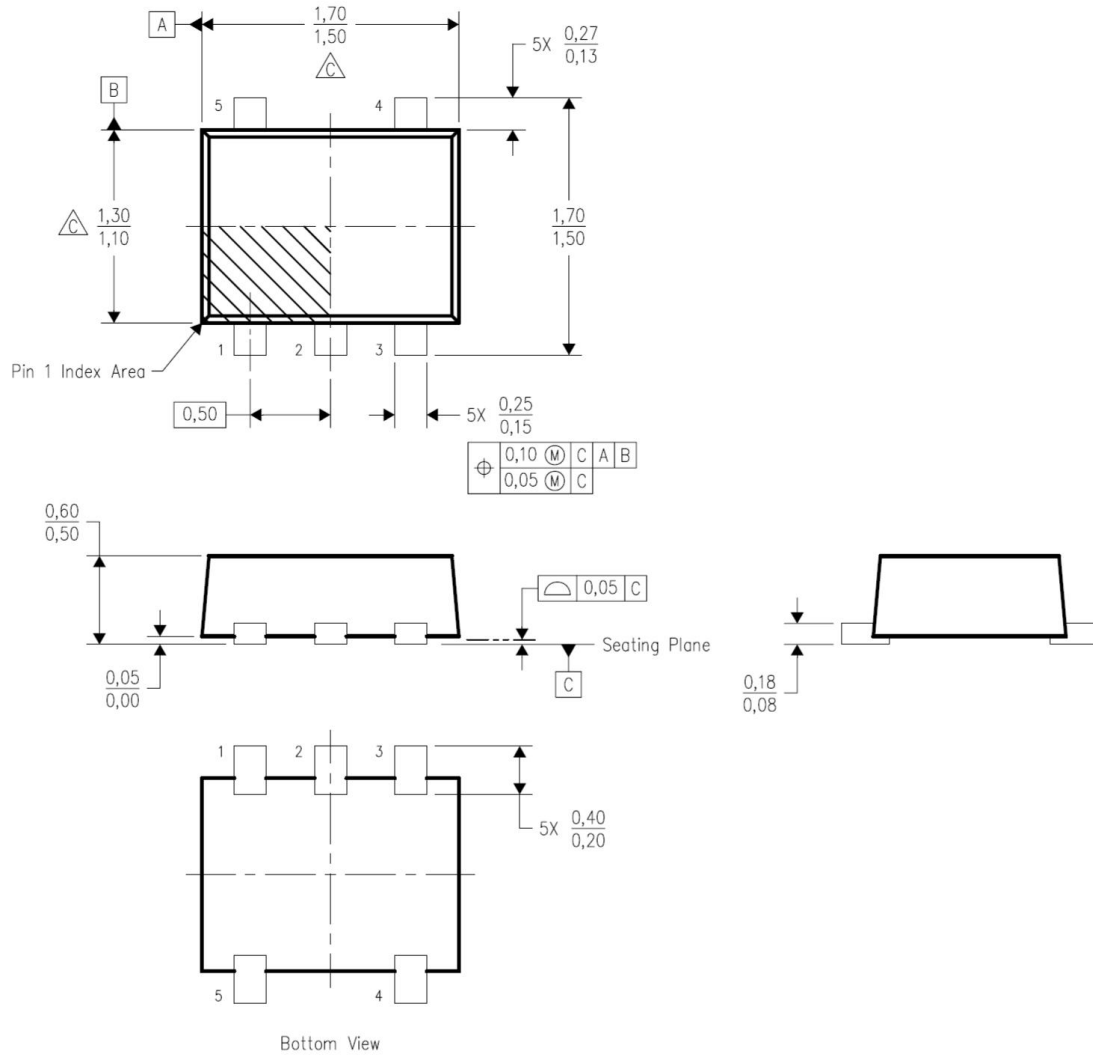
DCK (SC70-5)



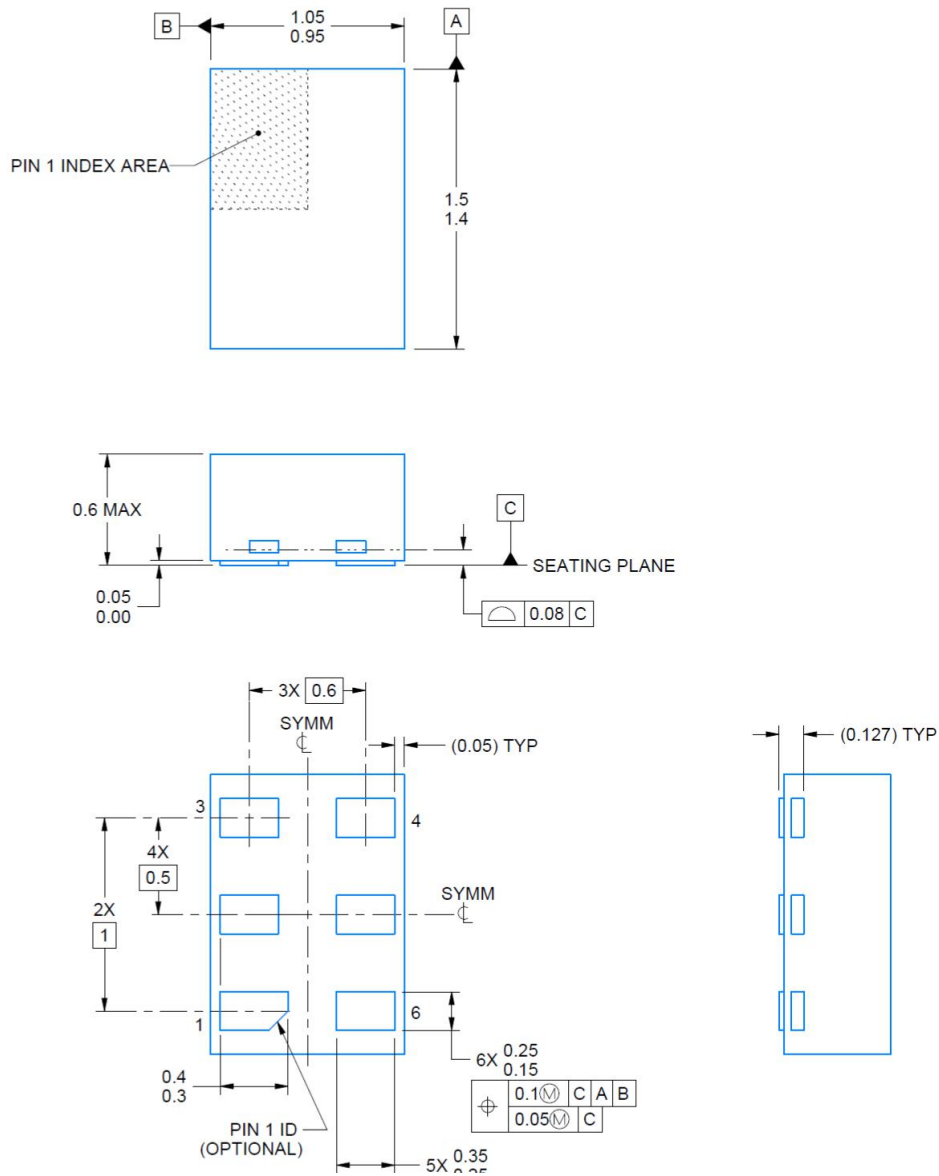
■ Marking



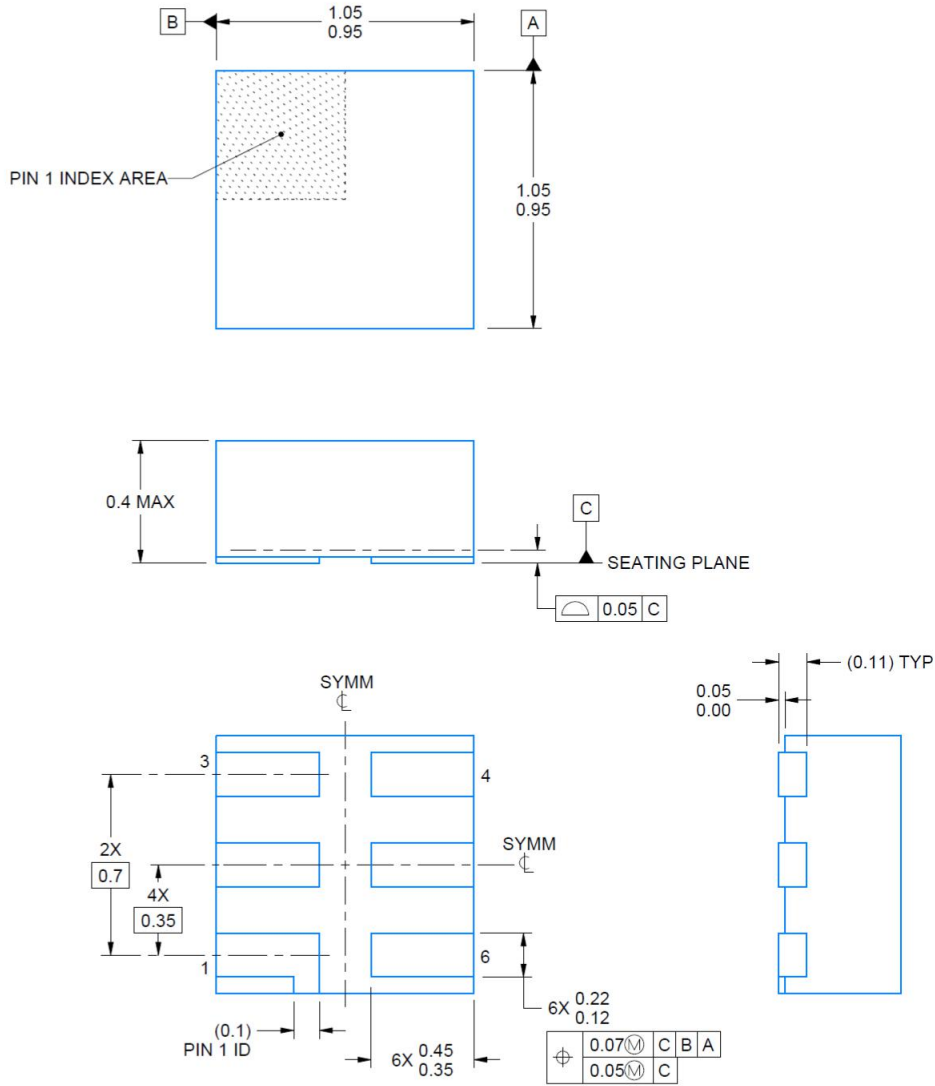
DRL (SOT-553)



DRY (SOT-886)

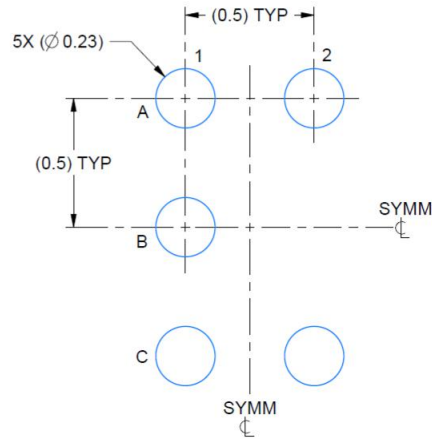


DSF (SON-6)

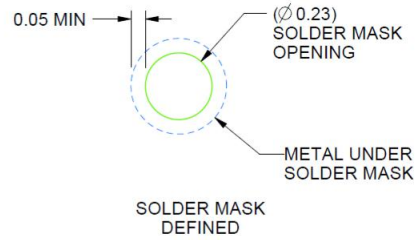
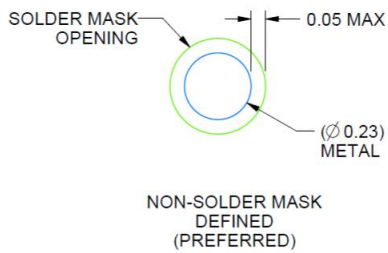




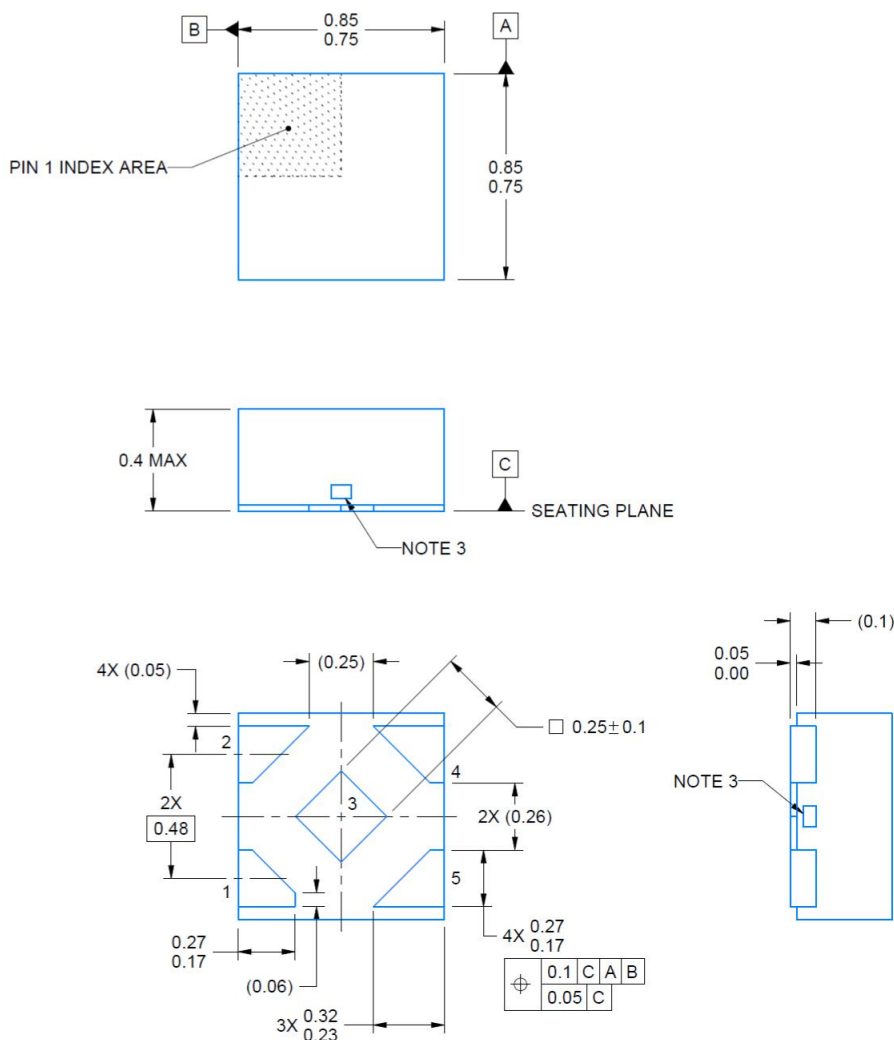
YZP (DSBGA-5)



LAND PATTERN EXAMPLE  
SCALE:40X



DPW (X2SON-5)



Ordering information

Order code	Package	Baseqty	Deliverymode
SN74LVC1G00DBVR	SOT23-5	3000	Tape and reel
SN74LVC1G00DCKR	SC70-5	3000	Tape and reel
SN74LVC1G00DSFR	SON-6	5000	Tape and reel
SN74LVC1G00DRYR	SOT-886	5000	Tape and reel
SN74LVC1G00YZPR	DSBGA-5	3000	Tape and reel
SN74LVC1G00DPWR	X2SON-5	3000	Tape and reel
SN74LVC1G00DRLR	SOT-553	4000	Tape and reel