

# Dual, Low Power INSTRUMENTATION AMPLIFIER

## FEATURES

- **LOW OFFSET VOLTAGE:** 50µV max
- **LOW DRIFT:** 0.5µV/°C max
- **LOW INPUT BIAS CURRENT:** 5nA max
- **HIGH CMR:** 120dB min
- **INPUTS PROTECTED TO ±40V**
- **WIDE SUPPLY RANGE:** ±2.25V to ±18V
- **LOW QUIESCENT CURRENT:** 700µA / IA
- **16-PIN PLASTIC DIP, SOL-16**

## APPLICATIONS

- **SENSOR AMPLIFIER**  
THERMOCOUPLE, RTD, BRIDGE
- **MEDICAL INSTRUMENTATION**
- **MULTIPLE-CHANNEL SYSTEMS**
- **BATTERY OPERATED EQUIPMENT**

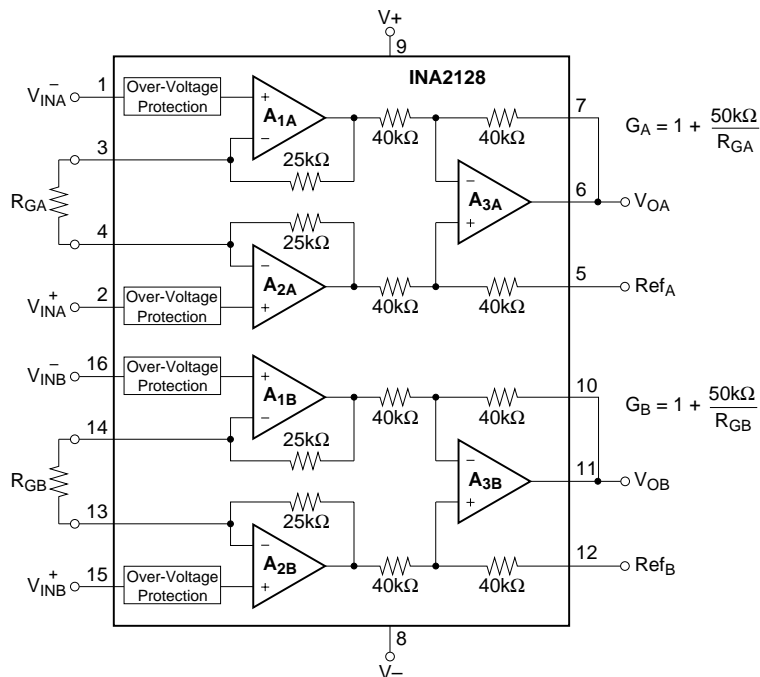
## DESCRIPTION

The INA2128 is a dual, low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA2128 is laser-trimmed for very low offset voltage (50µV), drift (0.5µV/°C) and high common-mode rejection (120dB at G ≥ 100). It operates with power supplies as low as ±2.25V, and quiescent current is only 700µA per IA—ideal for battery-operated and multiple-channel systems.

The INA2128 is available in SOL-16 packages, specified for the –40°C to +85°C temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

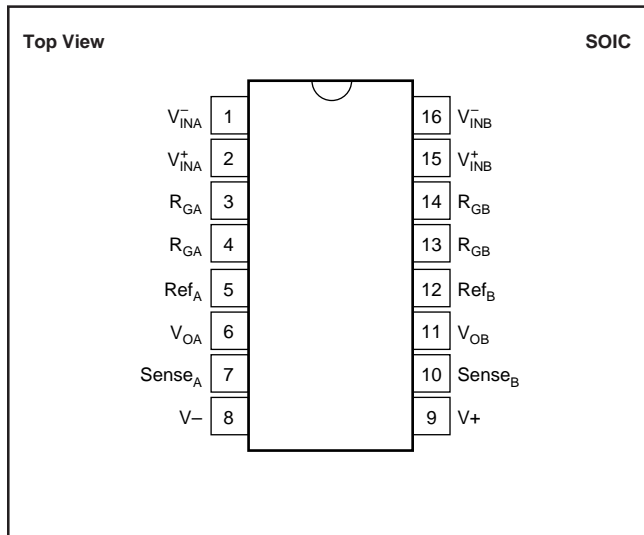
All trademarks are the property of their respective owners.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage .....	±18V
Analog Input Voltage Range .....	±40V
Output Short-Circuit (to ground) .....	Continuous
Operating Temperature .....	-40°C to +125°C
Storage Temperature .....	-55°C to +125°C
Junction Temperature .....	+150°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

## PIN CONFIGURATION



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	TEMPERATURE RANGE
INA2128UA	SOIC-16	DW	-40°C to +85°C
INA2128U	SOIC-16	DW	-40°C to +85°C

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

# ELECTRICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

PARAMETER	CONDITIONS	INA2128U			INA2128UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUT</b>								
Offset Voltage, RTI								
Initial	$T_A = +25^\circ\text{C}$		$\pm 10 \pm 100/\text{G}$	$\pm 50 \pm 500/\text{G}$		$\pm 25 \pm 100/\text{G}$	$\pm 125 \pm 1000/\text{G}$	$\mu\text{V}$
vs Temperature	$T_A = T_{\text{MIN}}$ to $T_{\text{MAX}}$		$\pm 0.2 \pm 2/\text{G}$	$\pm 0.5 \pm 20/\text{G}$		$\pm 0.2 \pm 5/\text{G}$	$\pm 1 \pm 20/\text{G}$	$\mu\text{V}/^\circ\text{C}$
vs Power Supply	$V_S = \pm 2.25\text{V}$ to $\pm 18\text{V}$		$\pm 0.2 \pm 20/\text{G}$	$\pm 1 \pm 100/\text{G}$		*	$\pm 2 \pm 200/\text{G}$	$\mu\text{V}/\text{V}$
Long-Term Stability			$\pm 0.1 \pm 3/\text{G}$			*		$\mu\text{V}/\text{mo}$
Impedance, Differential			$10^{10} \parallel 2$			*		$\Omega \parallel \text{pF}$
Common-Mode			$10^{11} \parallel 9$			*		$\Omega \parallel \text{pF}$
Common-Mode Voltage Range <sup>(1)</sup>	$V_O = 0\text{V}$	$(V+) - 2$ $(V-) + 2$	$(V+) - 1.4$ $(V-) + 1.7$		*	*		V
Safe Input Voltage				$\pm 40$			*	V
Common-Mode Rejection	$V_{\text{CM}} = \pm 13\text{V}$ , $\Delta R_S = 1\text{k}\Omega$						*	V
	$G=1$	80	86		73	*		dB
	$G=10$	100	106		93	*		dB
	$G=100$	120	125		110	*		dB
	$G=1000$	120	130		110	*		dB
<b>BIAS CURRENT</b>								
vs Temperature			$\pm 2$	$\pm 5$		*	$\pm 10$	nA
Offset Current			$\pm 30$			*		$\text{pA}/^\circ\text{C}$
vs Temperature			$\pm 1$	$\pm 5$		*	$\pm 10$	nA
			$\pm 30$			*		$\text{pA}/^\circ\text{C}$
<b>NOISE VOLTAGE, RTI</b>	$G = 1000$ , $R_S = 0\Omega$							
f = 10Hz			10			*		$\text{nV}/\sqrt{\text{Hz}}$
f = 100Hz			8			*		$\text{nV}/\sqrt{\text{Hz}}$
f = 1kHz			8			*		$\text{nV}/\sqrt{\text{Hz}}$
$f_B = 0.1\text{Hz}$ to 10Hz			0.2			*		$\mu\text{V}_{\text{PP}}$
Noise Current								
f=10Hz			0.9			*		$\text{pA}/\sqrt{\text{Hz}}$
f=1kHz			0.3			*		$\text{pA}/\sqrt{\text{Hz}}$
$f_B = 0.1\text{Hz}$ to 10Hz			30			*		$\text{pA}_{\text{PP}}$
<b>GAIN</b>								
Gain Equation			$1 + (50\text{k}\Omega/R_G)$	10000	*	*	*	V/V
Range of Gain		1						V/V
Gain Error	$G=1$		$\pm 0.01$	$\pm 0.024$		*	$\pm 0.1$	%
	$G=10$		$\pm 0.02$	$\pm 0.4$		*	$\pm 0.5$	%
	$G=100$		$\pm 0.05$	$\pm 0.5$		*	$\pm 0.7$	%
	$G=1000$		$\pm 0.5$	$\pm 1$		*	$\pm 2$	%
Gain vs Temperature <sup>(2)</sup>	$G=1$		$\pm 1$	$\pm 10$		*	*	$\text{ppm}/^\circ\text{C}$
50k $\Omega$ Resistance <sup>(2, 3)</sup>			$\pm 25$	$\pm 100$		*	*	$\text{ppm}/^\circ\text{C}$
Nonlinearity	$V_O = \pm 13.6\text{V}$ , $G=1$		$\pm 0.0001$	$\pm 0.001$		*	$\pm 0.002$	% of FSR
	$G=10$		$\pm 0.0003$	$\pm 0.002$		*	$\pm 0.004$	% of FSR
	$G=100$		$\pm 0.0005$	$\pm 0.002$		*	$\pm 0.004$	% of FSR
	$G=1000$		$\pm 0.001$	(Note 4)		*	*	% of FSR
<b>OUTPUT</b>								
Voltage: Positive	$R_L = 10\text{k}\Omega$	$(V+) - 1.4$	$(V+) - 0.9$		*	*		V
Negative	$R_L = 10\text{k}\Omega$	$(V-) + 1.4$	$(V-) + 0.8$		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			+6/-15			*		mA
<b>FREQUENCY RESPONSE</b>								
Bandwidth, -3dB	$G=1$		1.3			*		MHz
	$G=10$		700			*		kHz
	$G=100$		200			*		kHz
	$G=1000$		20			*		kHz
Slew Rate	$V_O = \pm 10\text{V}$ , $G=10$		4			*		V/ $\mu\text{s}$
Settling Time, 0.01%	$G=1$		7			*		$\mu\text{s}$
	$G=10$		7			*		$\mu\text{s}$
	$G=100$		9			*		$\mu\text{s}$
	$G=1000$		80			*		$\mu\text{s}$
Overload Recovery	50% Overdrive		4			*		$\mu\text{s}$
<b>POWER SUPPLY</b>								
Voltage Range		$\pm 2.25$	$\pm 15$	$\pm 18$	*	*	*	V
Current, Total	$V_{\text{IN}} = 0\text{V}$		$\pm 1.4$	$\pm 1.5$		*	*	mA
<b>TEMPERATURE RANGE</b>								
Specification		-40		85	*		*	$^\circ\text{C}$
Operating		-40		125	*		*	$^\circ\text{C}$
$\theta_{\text{JA}}$			80			*		$^\circ\text{C}/\text{W}$

\* Specification same as INA2128P, U.

NOTE: (1) Input common-mode range varies with output voltage—see Electrical Characteristics.

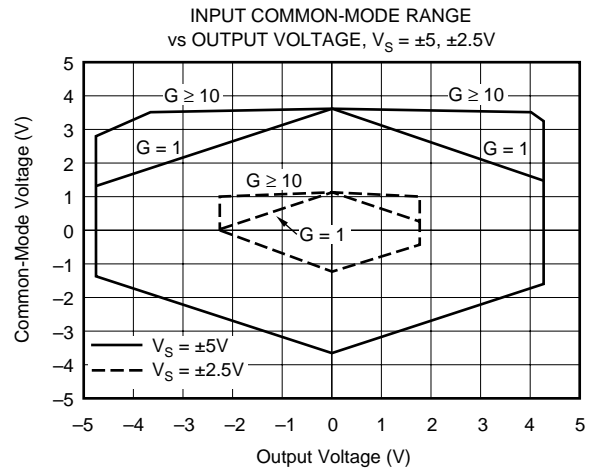
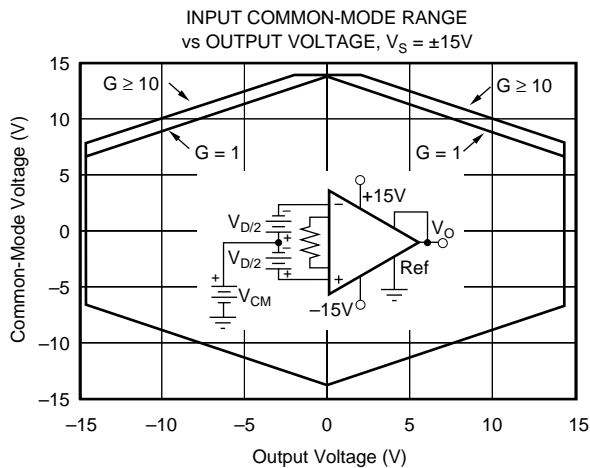
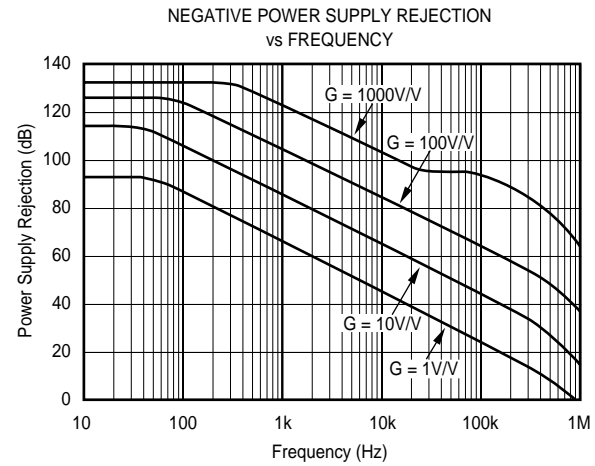
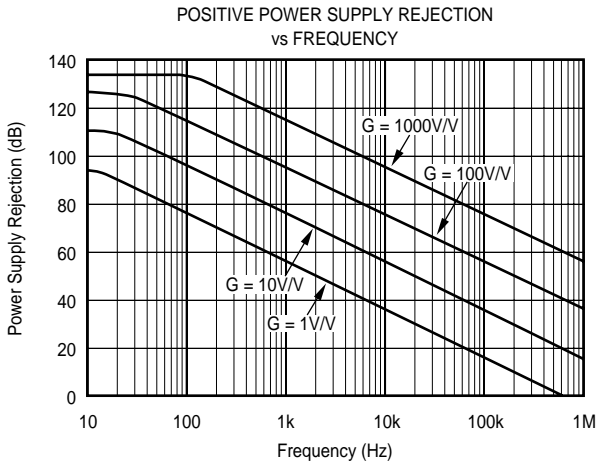
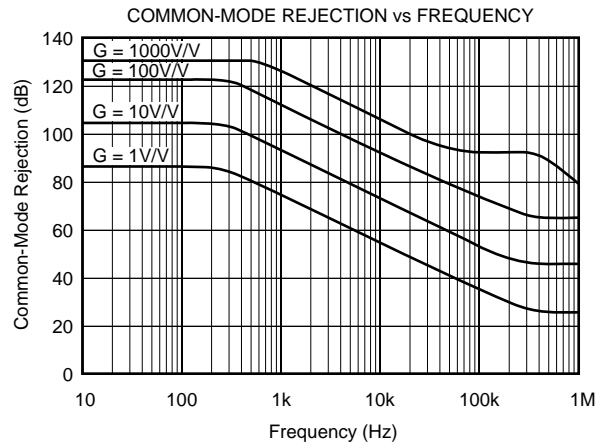
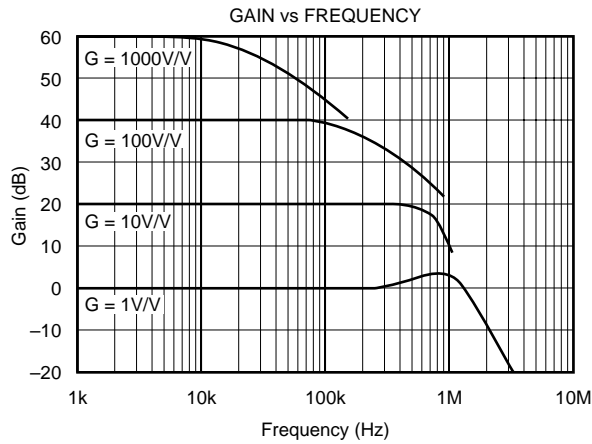
(2) Ensured by wafer test.

(3) Temperature coefficient of the 50k $\Omega$  term in the gain equation.

(4) Nonlinearity measurements in  $G = 1000$  are dominated by noise. Typical nonlinearity is  $\pm 0.001\%$ .

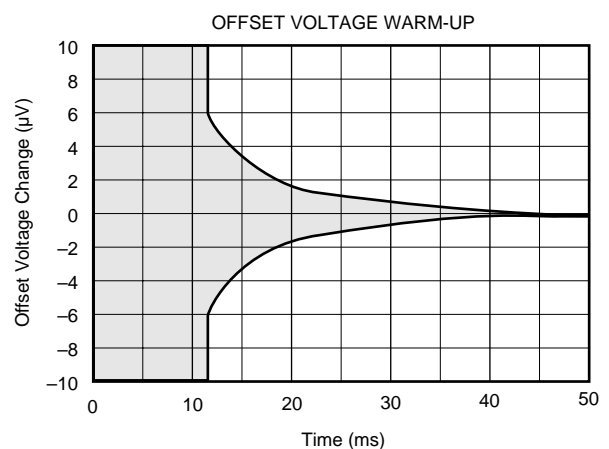
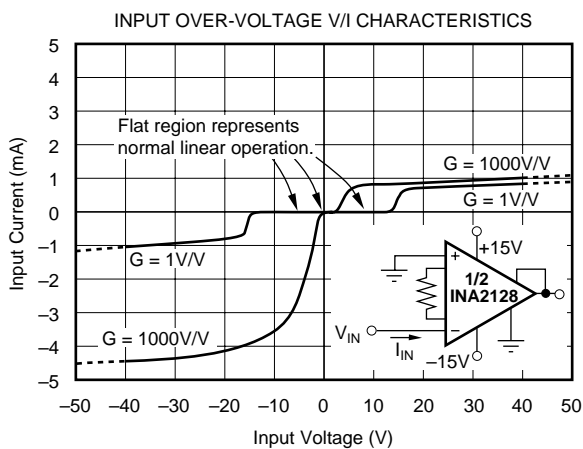
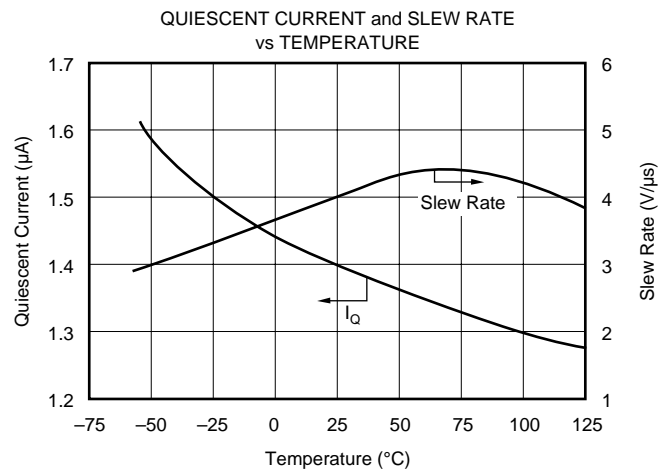
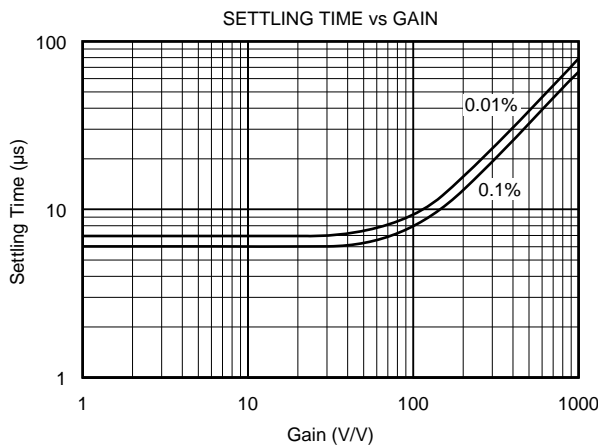
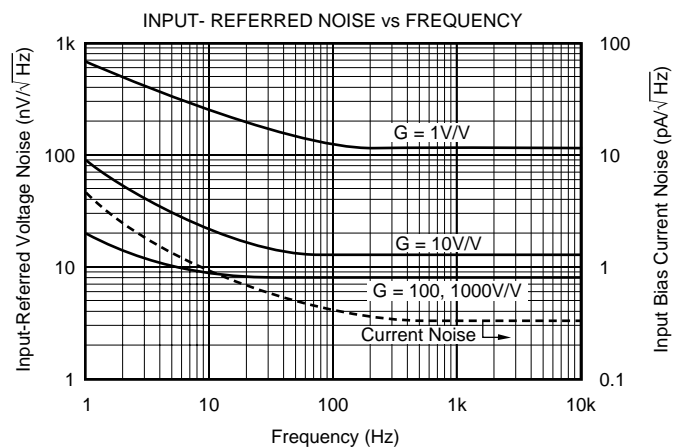
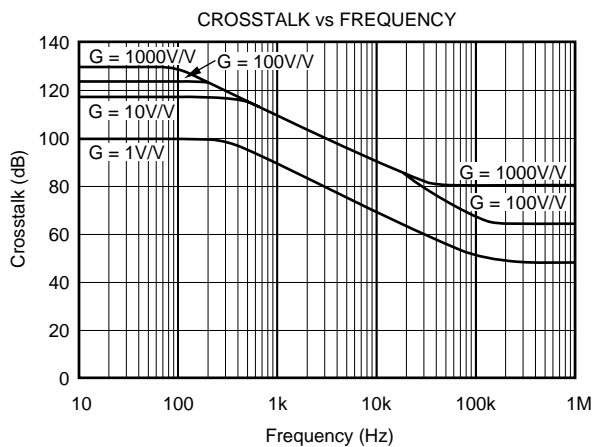
# TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS (Continued)

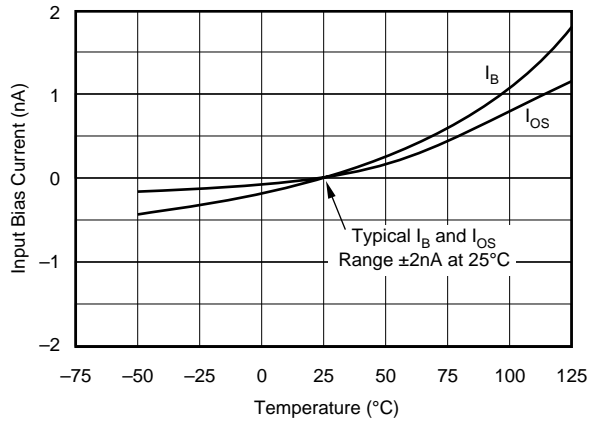
At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.



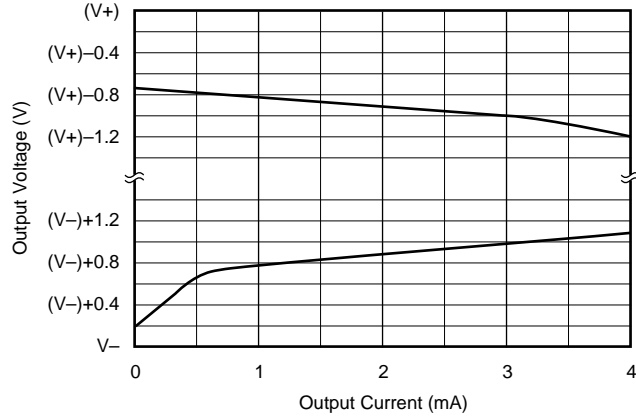
# TYPICAL CHARACTERISTICS (Continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.

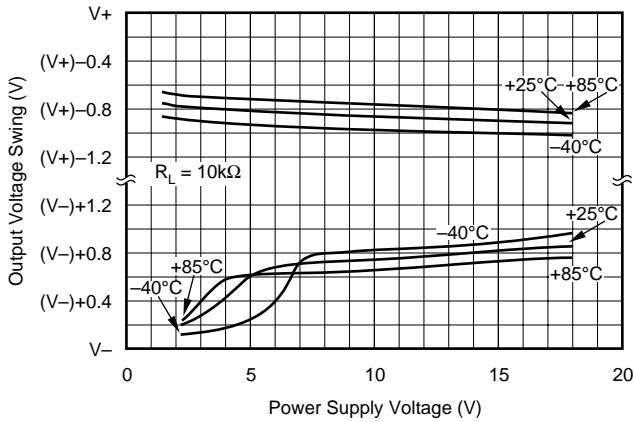
INPUT BIAS CURRENT vs TEMPERATURE



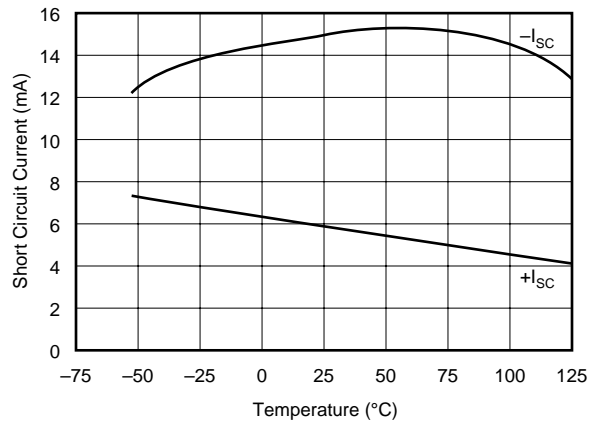
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



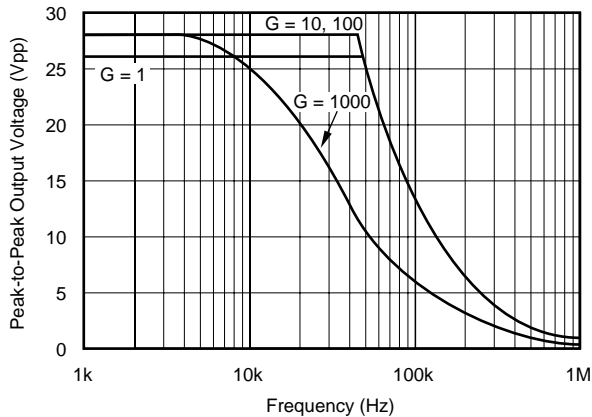
OUTPUT VOLTAGE SWING vs POWER SUPPLY VOLTAGE



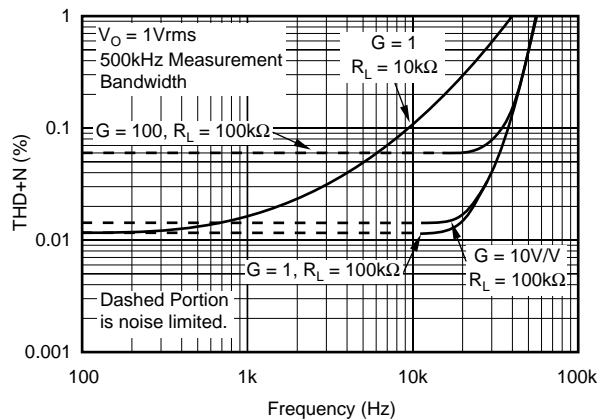
SHORT-CIRCUIT OUTPUT CURRENT vs TEMPERATURE



MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



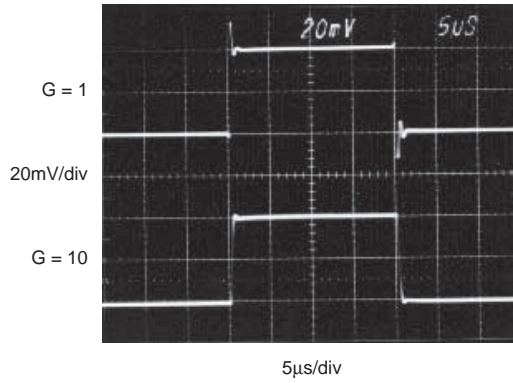
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



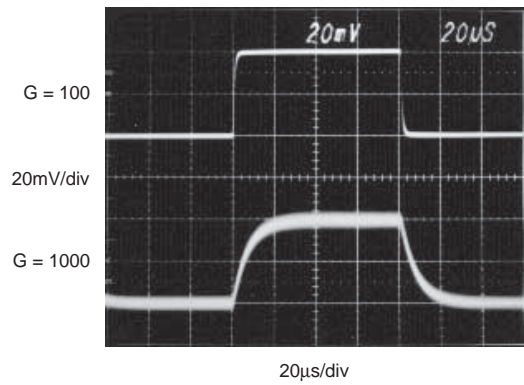
# TYPICAL CHARACTERISTICS (Continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.

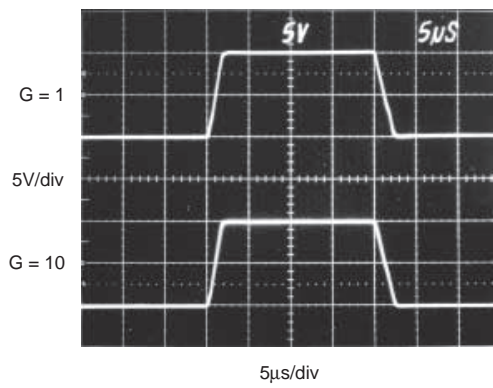
SMALL-SIGNAL STEP RESPONSE  
( $G = 1, 10$ )



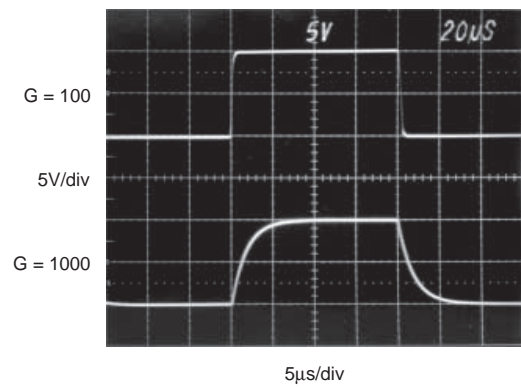
SMALL-SIGNAL STEP RESPONSE  
( $G = 100, 1000$ )



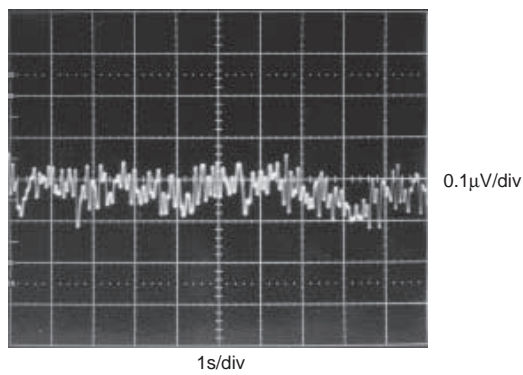
LARGE-SIGNAL STEP RESPONSE  
( $G = 1, 10$ )



LARGE-SIGNAL STEP RESPONSE  
( $G = 100, 1000$ )



VOLTAGE NOISE 0.1Hz to 10Hz  
INPUT-REFERRED,  $G \geq 100$



# APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA2128. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminals (Ref<sub>A</sub> and Ref<sub>B</sub>) which are normally grounded. These must be low-impedance connections to assure good common-mode rejection. A resistance of 8Ω in series with a Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

The INA2128 has separate output sense feedback connections, Sense<sub>A</sub> and Sense<sub>B</sub>. These must be connected to their respective output terminals for proper operation. The output sense connection can be used to sense the output voltage directly at the load for best accuracy.

## SETTING THE GAIN

Gain of the INA2128 is set by connecting a single external resistor, R<sub>G</sub>, connected as shown:

$$G = 1 + \frac{50k\Omega}{R_G} \quad (1)$$

Commonly-used gains and resistor values are shown in Figure 1.

The 50kΩ term in Equation 1 comes from the sum of the two

internal feedback resistors, A<sub>1</sub> and A<sub>2</sub>. These on-chip metal film resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA2128.

The stability and temperature drift of the external gain setting resistor, R<sub>G</sub>, also affects gain. R<sub>G</sub>'s contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error in gains of approximately 100 or greater.

## DYNAMIC PERFORMANCE

The typical performance curve “Gain vs Frequency” shows that despite its low quiescent current, the INA2128 achieves wide bandwidth, even at high gain. This is due to its current-feedback topology. Settling time also remains excellent at high gain—see “Settling Time vs Gain.”

## NOISE PERFORMANCE

The INA2128 provides very low noise in most applications. Low frequency noise is approximately 0.2μV<sub>PP</sub> measured from 0.1 to 10Hz (G ≥ 100). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

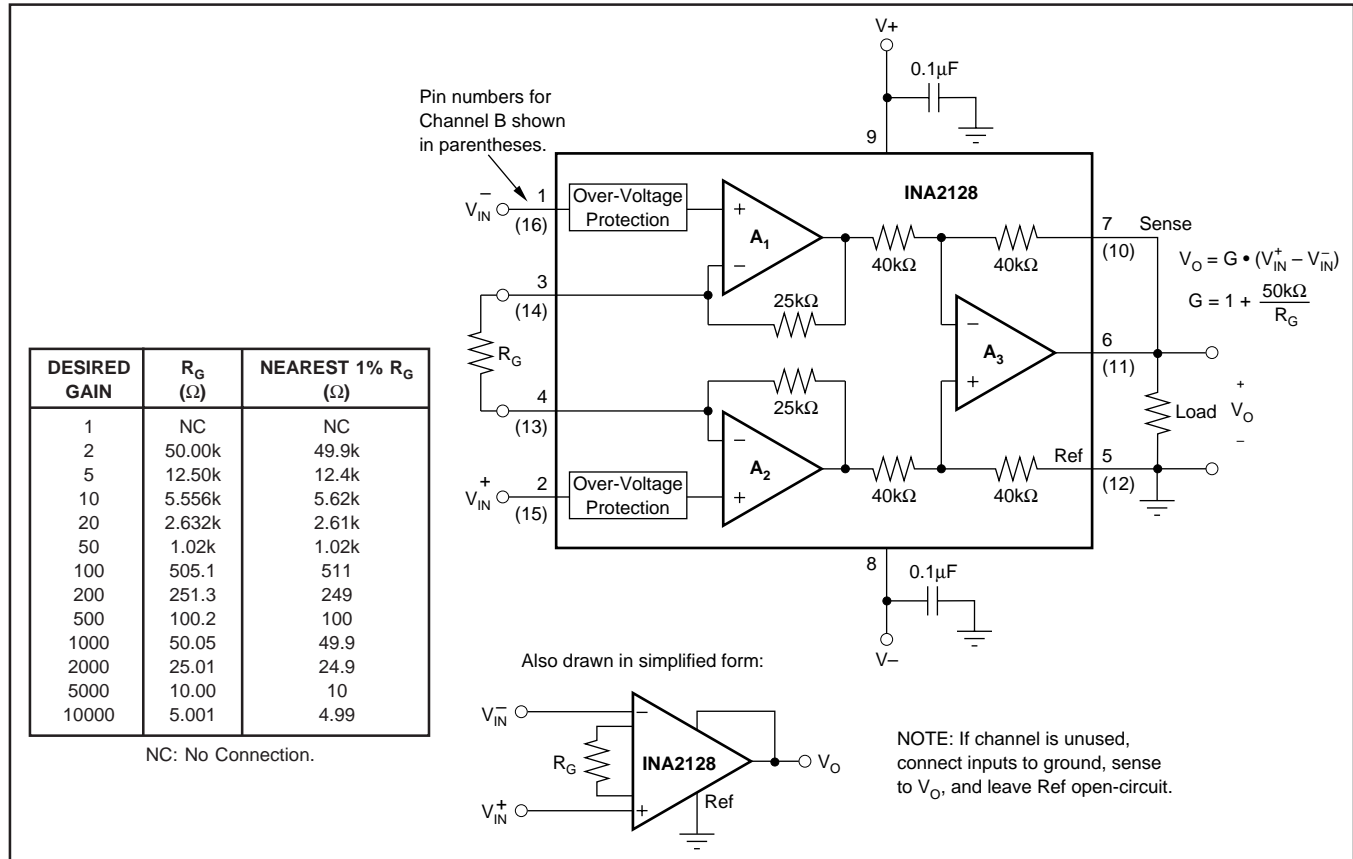


FIGURE 1. Basic Connections.



## OFFSET TRIMMING

The INA2128 is laser-trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

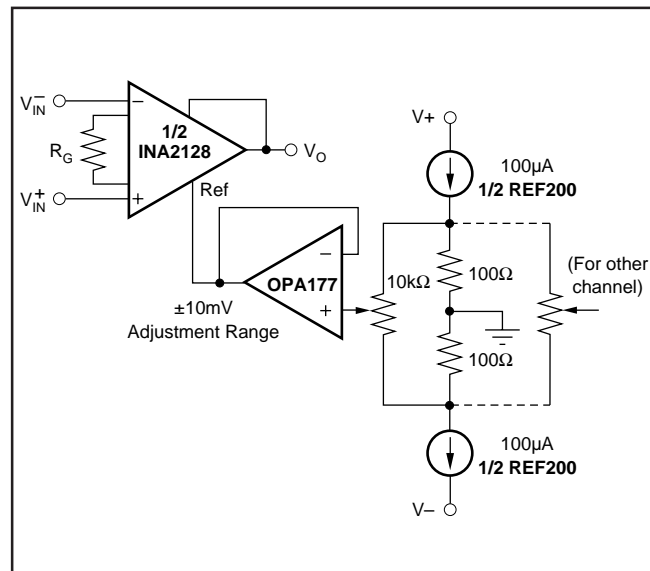


FIGURE 2. Optional Trimming of Output Offset Voltage.

## INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA2128 is extremely high—approximately  $10^{10}\Omega$ . However, a path must be provided for the input bias current of both inputs. This input bias current is approximately  $\pm 2\text{nA}$ . High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range of the INA2128 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

## INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA2128 is from approximately 1.4V below the positive supply voltage to 1.7V above the negative supply. As a differential input voltage causes the output voltage increase, however, the linear input range will be limited by the output

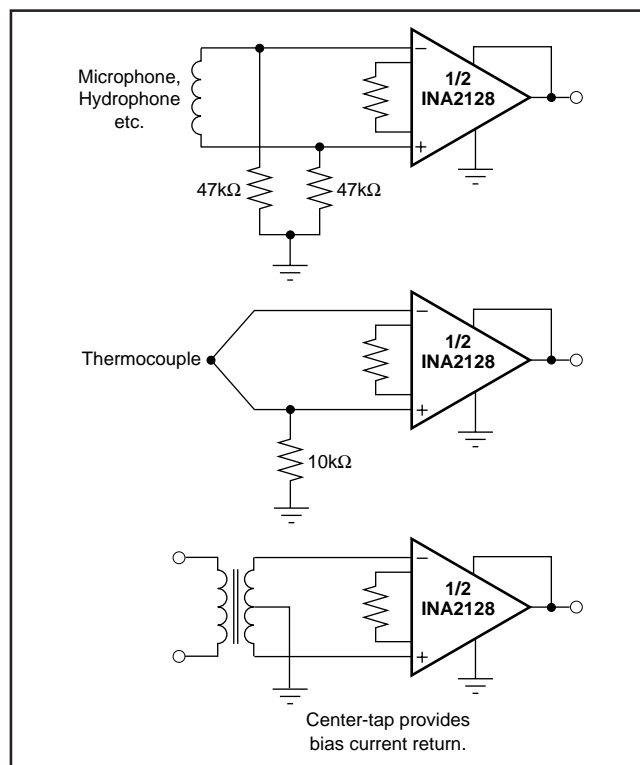


FIGURE 3. Providing an Input Common-Mode Current Path.

voltage swing of amplifiers  $A_1$  and  $A_2$ . So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves “Input Common-Mode Range vs Output Voltage.”

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA2128 will be near 0V even though both inputs are overloaded.

## LOW VOLTAGE OPERATION

The INA2128 can be operated on power supplies as low as  $\pm 2.25\text{V}$ . Performance remains excellent with power supplies ranging from  $\pm 2.25\text{V}$  to  $\pm 18\text{V}$ . Most parameters vary only slightly throughout this supply voltage range—see typical performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, “Input Common-Mode Range vs Output Voltage,” show the range of linear operation for  $\pm 15\text{V}$ ,  $\pm 5\text{V}$ , and  $\pm 2.5\text{V}$  supplies.

## INPUT PROTECTION

The inputs of the INA2128 are individually protected for voltages up to  $\pm 40\text{V}$ . For example, a condition of  $-40\text{V}$  on one input and  $+40\text{V}$  on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately  $1.5\text{mA}$  to  $5\text{mA}$ . The typical performance curve “Input Bias Current vs Common-Mode Input Voltage” shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

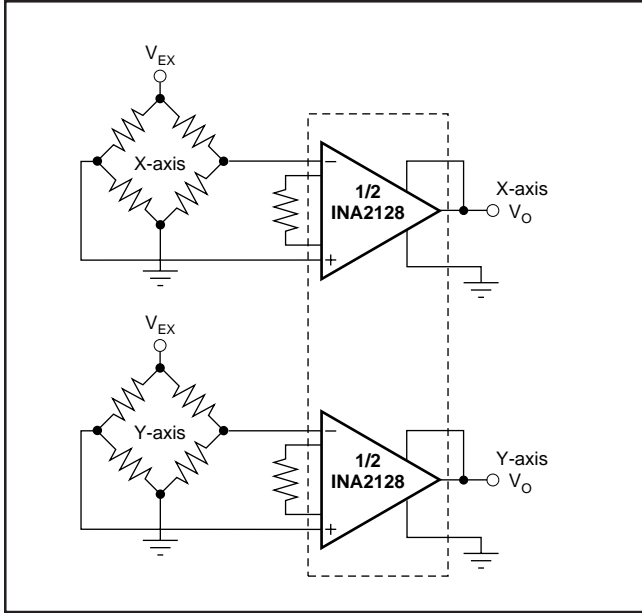


FIGURE 4. Two-Axis Bridge Amplifier.

## CHANNEL CROSSTALK

The two channels of the INA2128 are completely independent, including all bias circuitry. At DC and low frequency there is virtually no signal coupling between channels. Crosstalk increases with frequency and is dependent on circuit gain, source impedance and signal characteristics.

As source impedance increases, careful circuit layout will help achieve lowest channel crosstalk. Most crosstalk is produced by capacitive coupling of signals from one channel to the input section of the other channel. To minimize coupling, separate the input traces as far as practical from any signals associated with the opposite channel. A grounded guard trace surrounding the inputs helps reduce stray coupling between channels. Run the differential inputs of each channel parallel to each other or directly adjacent on top and bottom side of a circuit board. Stray coupling then tends to produce a common-mode signal which is rejected by the IA's input.

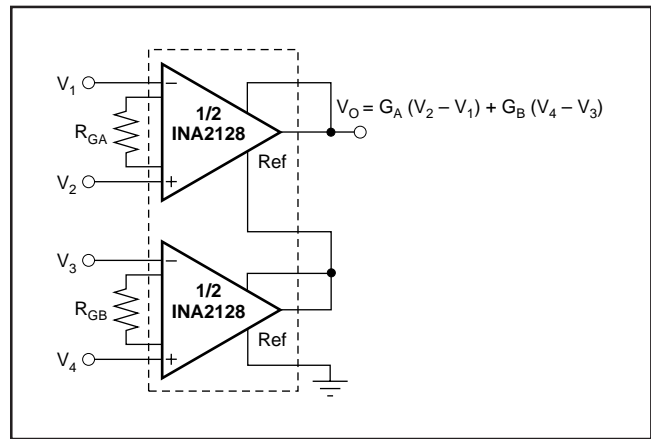


FIGURE 5. Sum of Differences Amplifier.

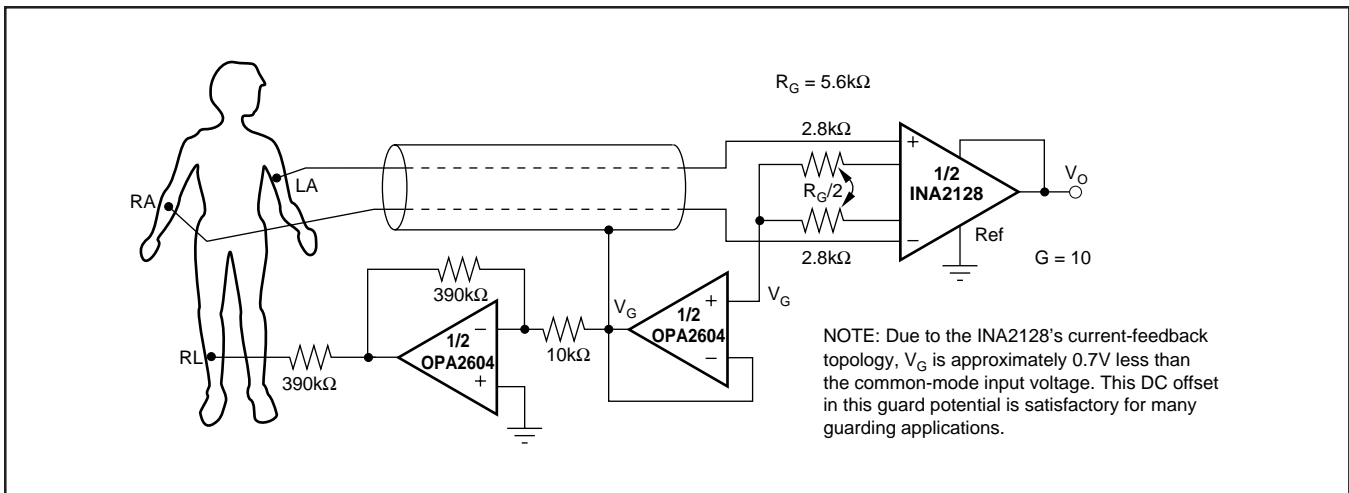


FIGURE 6. ECG Amplifier With Right-Leg Drive.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA2128U	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	INA2128U	<a href="#">Samples</a>
INA2128U/1K	ACTIVE	SOIC	DW	16	1000	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR		INA2128U	<a href="#">Samples</a>
INA2128U/1KE4	ACTIVE	SOIC	DW	16	1000	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR		INA2128U	<a href="#">Samples</a>
INA2128UA	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR		INA2128U A	<a href="#">Samples</a>
INA2128UA/1K	ACTIVE	SOIC	DW	16	1000	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR		INA2128U A	<a href="#">Samples</a>
INA2128UA/1KG4	ACTIVE	SOIC	DW	16	1000	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR		INA2128U A	<a href="#">Samples</a>
INA2128UG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	INA2128U	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA2128U/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
INA2128UA/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA2128U/1K	SOIC	DW	16	1000	367.0	367.0	38.0
INA2128UA/1K	SOIC	DW	16	1000	367.0	367.0	38.0

## GENERIC PACKAGE VIEW

**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A



DW0016A

# PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



# EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated