

# High-Speed 10 MBit/s Logic Gate Optocouplers

## Single-Channel: 6N137, HCPL2601, HCPL2611 Dual-Channel: HCPL2630, HCPL2631

### Description

The 6N137, HCPL2601, HCPL2611 single-channel and HCPL2630, HCPL2631 dual-channel optocouplers consist of a 850 nm AlGaAs LED, optically coupled to a very high speed integrated photo-detector logic gate with a strobable output. This output features an open collector, thereby permitting wired OR outputs. The coupled parameters are guaranteed over the temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . A maximum input signal of 5 mA will provide a minimum output sink current of 13 mA (fan out of 8).

An internal noise shield provides superior common mode rejection of typically 10 kV/ $\mu\text{s}$ . The HCPL2601 and HCPL2631 has a minimum CMR of 5 kV/ $\mu\text{s}$ . The HCPL2611 has a minimum CMR of 10 kV/ $\mu\text{s}$ .

### Features

- Very High Speed – 10 MBit/s
- Superior CMR – 10 kV/ $\mu\text{s}$
- Double working voltage – 480 V
- Fan-out of 8 Over  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Logic Gate Output
- Storable Output
- Wired OR–open Collector
- U.L. Recognized (File # E90700)

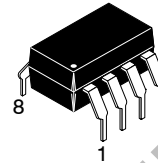
### Applications

- Ground Loop Elimination
- LSTTL to TTL, LSTTL or 5–volt CMOS
- Line Receiver, Data Transmission
- Data Multiplexing
- Switching Power Supplies
- Pulse Transformer Replacement
- Computer–peripheral Interface

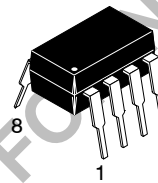


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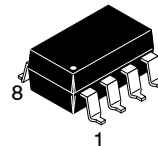
[www.onsemi.com](http://www.onsemi.com)



PDIP8 6.6x3.81, 2.54P  
CASE 646BW

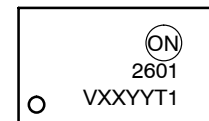


PDIP8 9.655x6.6, 2.54P  
CASE 646CQ



PDIP8 GW  
CASE 709AC

### MARKING DIAGRAM

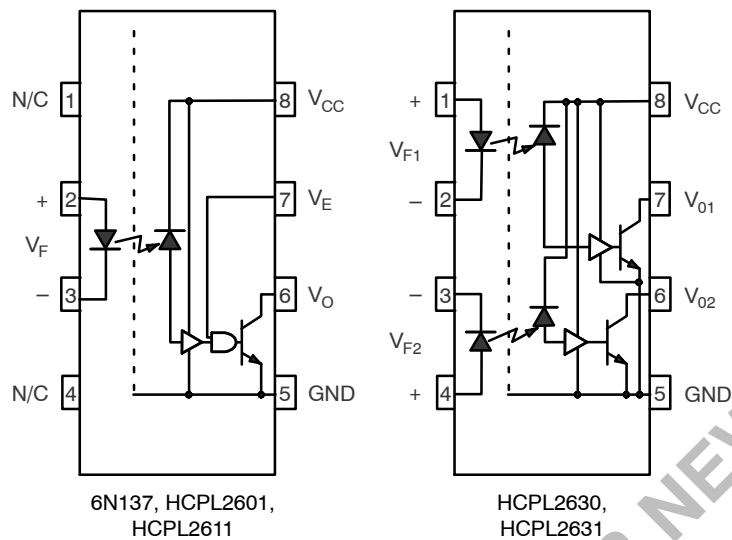


|      |  |
|------|--|
| 2601 | = Device Number  |
| V    | = VDE mark (Note: Only Appears on Parts Ordered with VDE Option – See Order Entry Table) |
| XX   | = Two-Digit Year Code, e.g., '03'  |
| YY   | = Two-Digit Work Week, Ranging from '01' to '53'   |
| T1   | = Assembly Package Code  |

### ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

SCHEMATICS



A 0.1  $\mu$ F bypass capacitor must be connected between pins 8 and 5 (Note 1).

Figure 1. Schematics

TRUTH TABLE (Positive Logic)

| Input | Enable | Output |
|-------|--------|--------|
| H     | H      | L      |
| L     | H      | H      |
| H     | L      | H      |
| L     | L      | H      |
| H     | NC     | L      |
| L     | NC     | H      |

# Single-Channel: 6N137, HCPL2601, HCPL2611 Dual-Channel: HCPL2630, HCPL2631

## ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)

| Symbol           | Parameter  | Value        | Unit |
|------------------|--|--------------|------|
| T <sub>STG</sub> | Storage Temperature                                | -55 to +125  | °C   |
| T <sub>OPR</sub> | Operating Temperature                              | -40 to +85   | °C   |
| T <sub>SOL</sub> | Lead Solder Temperature (for Wave Soldering Only)* | 260 for 10 s | °C   |

## EMITTER

|                |  |                             |     |    |
|----------------|--|-----------------------------|-----|----|
| I <sub>F</sub> | DC/Average Forward Input Current                                       | Single Channel              | 50  | mA |
|                |  | Dual Channel (Each Channel) | 30  |    |
| V <sub>E</sub> | Enable Input Voltage Not to Exceed V <sub>CC</sub> by More than 500 mV | Single Channel              | 5.5 | V  |
| V <sub>R</sub> | Reverse Input Voltage  | Each Channel                | 5.0 | V  |
| P <sub>I</sub> | Power Dissipation  | Single Channel              | 100 | mW |
|                |  | Dual Channel (Each Channel) | 45  |    |

## DETECTOR

|                                   |                                    |                             |     |    |
|-----------------------------------|------------------------------------|-----------------------------|-----|----|
| V <sub>CC</sub><br>(1 Minute Max) | Supply Voltage                     |                             | 7.0 | V  |
| I <sub>O</sub>                    | Output Current                     | Single Channel              | 25  | mA |
|                                   |                                    | Dual Channel (Each Channel) | 50  |    |
| V <sub>O</sub>                    | Output Voltage                     | Each Channel                | 7.0 | V  |
| P <sub>O</sub>                    | Collector Output Power Dissipation | Single Channel              | 85  | mW |
|                                   |                                    | Dual Channel (Each Channel) | 60  |    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

\*For peak soldering reflow, please refer to the [Reflow Profile](#) on page 9.

## RECOMMENDED OPERATING CONDITIONS

| Symbol          | Parameter                  | Min  | Max             | Unit |
|-----------------|----------------------------|------|-----------------|------|
| I <sub>FL</sub> | Input Current, Low Level   | 0    | 250             | μA   |
| I <sub>FH</sub> | Input Current, High Level  | *6.3 | 15              | mA   |
| V <sub>CC</sub> | Supply Voltage, Output     | 4.5  | 5.5             | V    |
| V <sub>EL</sub> | Enable Voltage, Low Level  | 0    | 0.8             | V    |
| V <sub>EH</sub> | Enable Voltage, High Level | 2.0  | V <sub>CC</sub> | V    |
| T <sub>A</sub>  | Low Level Supply Current   | -40  | +85             | °C   |
| N               | Fan Out (TTL Load)         | -    | 8               |      |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

\*6.3 mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0 mA or less.

# Single-Channel: 6N137, HCPL2601, HCPL2611 Dual-Channel: HCPL2630, HCPL2631

## ELECTRICAL CHARACTERISTICS ( $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------|-----------|-----------------|-----|-----|-----|------|
|--------|-----------|-----------------|-----|-----|-----|------|

### INDIVIDUAL COMPONENT CHARACTERISTICS

| EMITTER                   |                                     |  |   |     |      |      |                      |
|---------------------------|-------------------------------------|--|---|-----|------|------|----------------------|
| $V_F$                     | Input Forward Voltage               | $I_F = 10\text{ mA}$   |   | –   | –    | 1.8  | V                    |
|                           |                                     |  | $T_A = 25^\circ\text{C}$                    | –   | 1.4  | 1.75 |                      |
| $B_{VR}$                  | Input Reverse Breakdown Voltage     | $I_R = 10\text{ }\mu\text{A}$                                  |   | 5.0 | –    | –    | V                    |
| $C_{IN}$                  | Input Capacitance                   | $V_F = 0, f = 1\text{ MHz}$                                    |   | –   | 60   | –    | pF                   |
| $\Delta V_F / \Delta T_A$ | Input Diode Temperature Coefficient | $I_F = 10\text{ mA}$   |   | –   | –1.4 | –    | mV/ $^\circ\text{C}$ |
| DETECTOR                  |                                     |  |   |     |      |      |                      |
| $I_{CCH}$                 | High Level Supply Current           | $V_{CC} = 5.5\text{ V}, I_F = 0\text{ mA}, V_E = 0.5\text{ V}$ | Single Channel                              | –   | 7    | 10   | mA                   |
|                           |                                     |  | Dual Channel                                | –   | 10   | 15   |                      |
| $I_{CCL}$                 | Low Level Supply Current            | Single Channel   | $V_{CC} = 5.5\text{ V}, I_F = 10\text{ mA}$ | –   | 9    | 13   | mA                   |
|                           |                                     | Dual Channel   | $V_E = 0.5\text{ V}$                        | –   | 14   | 21   |                      |
| $I_{EL}$                  | Low Level Enable Current            | $V_{CC} = 5.5\text{ V}, V_E = 0.5\text{ V}$                    |   | –   | –0.8 | –1.6 | mA                   |
| $I_{EH}$                  | High Level Enable Current           | $V_{CC} = 5.5\text{ V}, V_E = 2.0\text{ V}$                    |   | –   | –0.6 | –1.6 | mA                   |
| $V_{EH}$                  | High Level Enable Voltage           | $V_{CC} = 5.5\text{ V}, I_F = 10\text{ mA}$                    |   | 2.0 | –    | –    | V                    |
| $V_{EL}$                  | Low Level Enable Voltage            | $V_{CC} = 5.5\text{ V}, I_F = 10\text{ mA}$ (Note 3)           |   | –   | –    | 0.8  | V                    |

### SWITCHING CHARACTERISTICS ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ , $V_{CC} = 5\text{ V}$ , $I_F = 7.5\text{ mA}$ unless otherwise specified)

|                       |   |   |                          |        |        |     |                  |
|-----------------------|---|---|--------------------------|--------|--------|-----|------------------|
| $T_{PLH}$             | Propagation Delay Time to Output HIGH Level           | $R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$ (Note 4) (Figure 13)  | $T_A = 25^\circ\text{C}$ | 20     | 45     | 75  | ns               |
|                       |   |   |                          | –      | –      | 100 |                  |
| $T_{PHL}$             | Propagation Delay Time to Output LOW Level            | $T_A = 25^\circ\text{C}$ (Note 5)   |                          | 25     | 45     | 75  | ns               |
|                       |   | $R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$ (Figure 13)   |                          | –      | –      | 100 |                  |
| $ T_{PHL} - T_{PLH} $ | Pulse Width Distortion                                | $R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$ (Figure 13)   |                          | –      | 3      | 35  | ns               |
| $t_r$                 | Output Rise Time (10–90%)                             | $R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$ (Note 6) (Figure 13)  |                          | –      | 50     | –   | ns               |
| $t_f$                 | Output Rise Time (90–10%)                             | $R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$ (Note 7) (Figure 13)  |                          | –      | 12     | –   | ns               |
| $t_{ELH}$             | Enable Propagation Delay Time to Output HIGH Level    | $I_F = 7.5\text{ mA}, V_{EH} = 3.5\text{ V}, R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$ (Note 8) (Figure 14)  |                          | –      | 20     | –   | ns               |
| $t_{EHL}$             | Enable Propagation Delay Time to Output LOW Level     | $I_F = 7.5\text{ mA}, V_{EH} = 3.5\text{ V}, R_L = 350\text{ }\Omega, C_L = 15\text{ pF}$ (Note 9) (Figure 14)  |                          | –      | 20     | –   | ns               |
| $ CM_H $              | Common Mode Transient Immunity (at Output HIGH Level) | $T_A = 25^\circ\text{C},  V_{CM}  = 50\text{ V}$ (Peak), $I_F = 0\text{ mA}, V_{OH}(\text{Min.}) = 2.0\text{ V}, R_L = 350\text{ }\Omega$ (Note 10) (Figure 15) | 6N137, HCPL2630          | –      | 10,000 | –   | V/ $\mu\text{s}$ |
|                       |   |   | HCPL2601, HCPL2631       | 5000   | 10,000 | –   |                  |
|                       |   | $ V_{CM}  = 400\text{ V}$   | HCPL2611                 | 10,000 | 15,000 | –   | V/ $\mu\text{s}$ |
| $ CM_L $              | Common Mode Transient Immunity (at Output LOW Level)  | $R_L = 350\text{ }\Omega, I_F = 7.5\text{ mA}, V_{OL}(\text{Max.}) = 0.8\text{ V}, T_A = 25^\circ\text{C}$ (Note 11) (Figure 15)                                | 6N137, HCPL2630          | –      | 10,000 | –   | V/ $\mu\text{s}$ |
|                       |   |   | HCPL2601, HCPL2631       | 5000   | 10,000 | –   |                  |
|                       |   | $ V_{CM}  = 400\text{ V}$   | HCPL2611                 | 10,000 | 15,000 | –   |                  |

### TRANSFER CHARACTERISTICS ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise specified)

|          |                           |  |   |     |     |               |
|----------|---------------------------|--|---|-----|-----|---------------|
| $I_{OH}$ | HIGH Level Output Current | $V_{CC} = 5.5\text{ V}, V_O = 5.5\text{ V}, I_F = 250\text{ }\mu\text{A}, V_E = 2.0\text{ V}$ (Note 2) | – | –   | 100 | $\mu\text{A}$ |
| $V_{OL}$ | LOW Level Output Current  | $V_{CC} = 5.5\text{ V}, I_F = 5\text{ mA}, V_E = 2.0\text{ V}, I_{CL} = 13\text{ mA}$ (Note 2)         | – | .35 | 0.6 | V             |
| $I_{FT}$ | Input Threshold Current   | $V_{CC} = 5.5\text{ V}, V_O = 0.6\text{ V}, V_E = 2.0\text{ V}, I_{OL} = 13\text{ mA}$                 | – | 3   | 5   | mA            |

# Single-Channel: 6N137, HCPL2601, HCPL2611 Dual-Channel: HCPL2630, HCPL2631

## ELECTRICAL CHARACTERISTICS ( $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ unless otherwise specified) (continued)

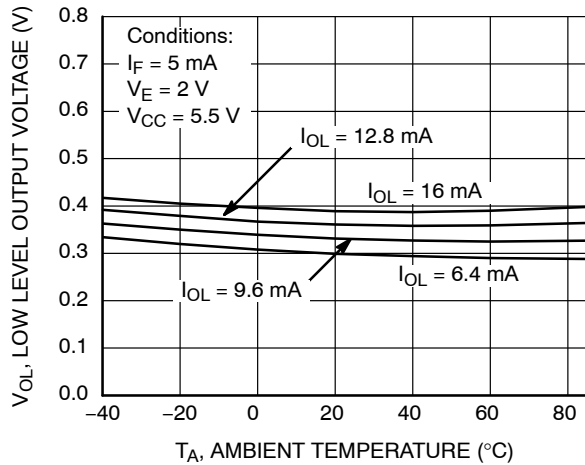
| Symbol  | Parameter                               | Test Conditions   | Min  | Typ       | Max  | Unit          |
|---|---|---|------|-----------|------|---------------|
| <b>ISOLATION CHARACTERISTICS</b> ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise specified) |   |   |      |           |      |               |
| $I_{I-O}$   | Input-Output Insulation Leakage Current | Relative Humidity = 45%, $T_A = 25^\circ\text{C}$ , $t = 5$ s, $V_{I-O} = 3000$ VDC (Note 12) | –    | –         | 1.0* | $\mu\text{A}$ |
| $V_{ISO}$   | Withstand Insulation Test Voltage       | RH < 50%, $T_A = 25^\circ\text{C}$ , $I_{I-O} \leq 2$ $\mu\text{A}$ , $t = 1$ min. (Note 12)  | 2500 | –         | –    | $V_{RMS}$     |
| $R_{I-O}$   | Resistance (Input to Output)            | $V_{I-O} = 500$ V (Note 12)   | –    | $10^{12}$ | –    | $\Omega$      |
| $C_{I-O}$   | Capacitance (Input to Output)           | $f = 1$ MHz (Note 12)   | –    | 0.6       | –    | pF            |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

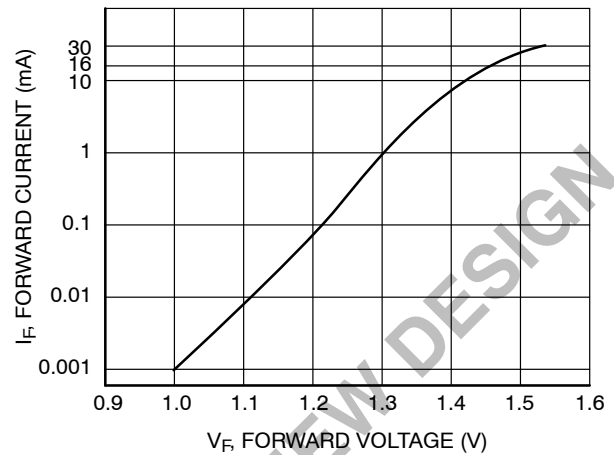
\*All Typicals at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$

1. The  $V_{CC}$  supply to each optoisolator must be bypassed by a 0.1  $\mu\text{F}$  capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package  $V_{CC}$  and GND pins of each device.
2. Each channel.
3. Enable Input – No pull up resistor required as the device has an internal pull up resistor.
4.  $t_{PLH}$  – Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
5.  $t_{PHL}$  – Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
6.  $t_r$  – Rise time is measured from the 10% to the 90% levels on the LOW to HIGH transition of the output pulse.
7.  $t_f$  – Fall time is measured from the 90% to the 10% levels on the HIGH to LOW transition of the output pulse.
8.  $t_{ELH}$  – Enable input propagation delay is measured from the 1.5 V level on the HIGH to LOW transition of the input voltage pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
9.  $t_{EHL}$  – Enable input propagation delay is measured from the 1.5 V level on the LOW to HIGH transition of the input voltage pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
10.  $CM_H$  – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e.,  $V_{OUT} > 2.0$  V). Measured in volts per microsecond (V/ $\mu\text{s}$ ).
11.  $CM_L$  – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e.,  $V_{OUT} < 0.8$  V). Measured in volts per microsecond (V/ $\mu\text{s}$ ).
12. Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.

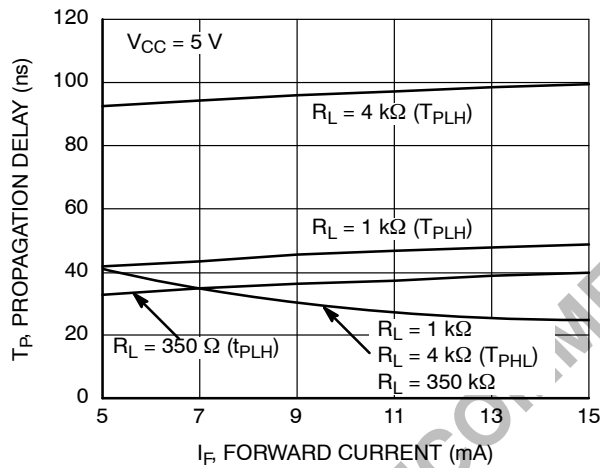
# TYPICAL PERFORMANCE CURVES



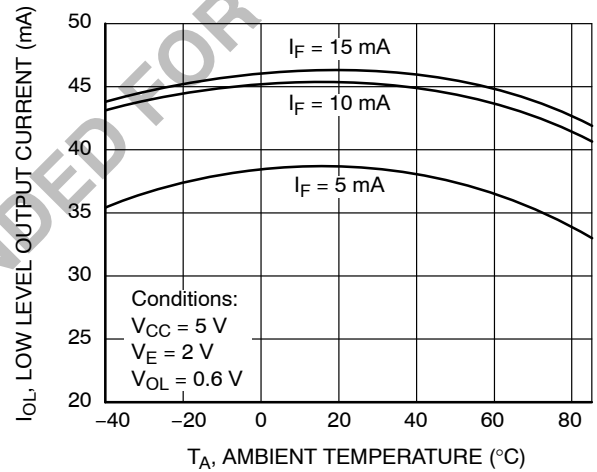
**Figure 2. Low Level Output Voltage vs. Ambient Temperature**



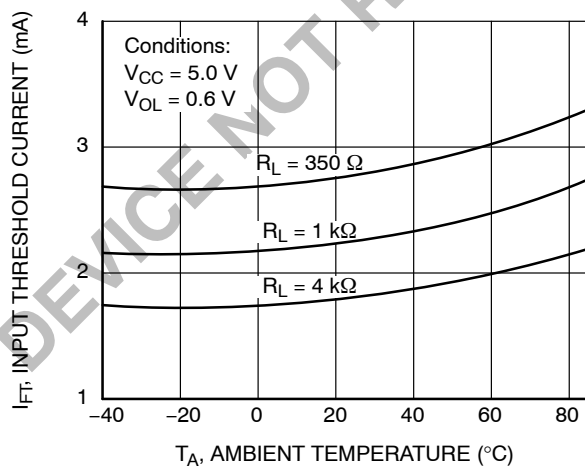
**Figure 3. Input Diode Forward Voltage vs. Forward Current**



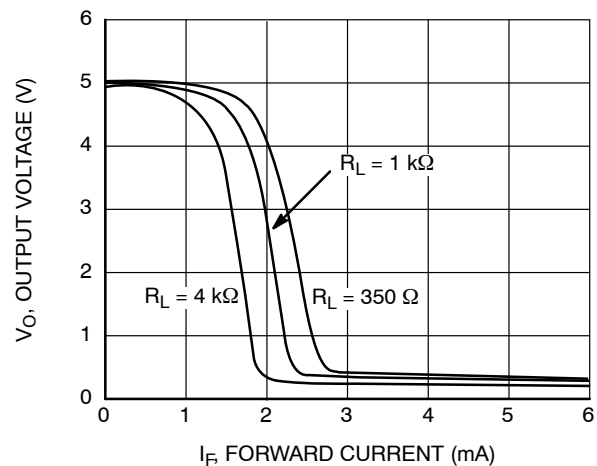
**Figure 4. Switching Time vs. Forward Current**



**Figure 5. Low Level Output vs. Ambient Temperature**



**Figure 6. Input Threshold Current vs. Ambient Temperature**



**Figure 7. Output Voltage vs. Input Forward Current**

TYPICAL PERFORMANCE CURVES (Continued)

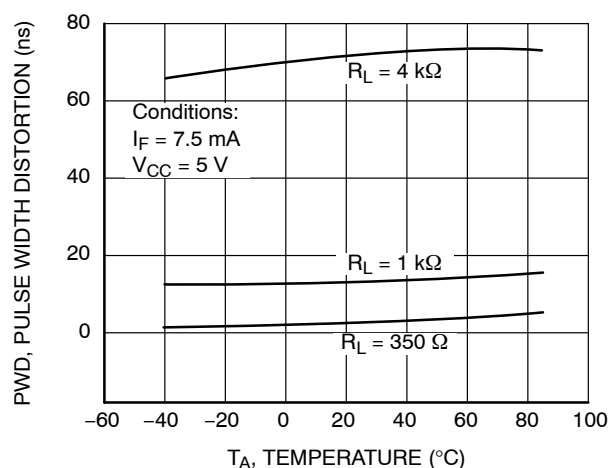


Figure 8. Pulse Width Distortion vs. Temperature

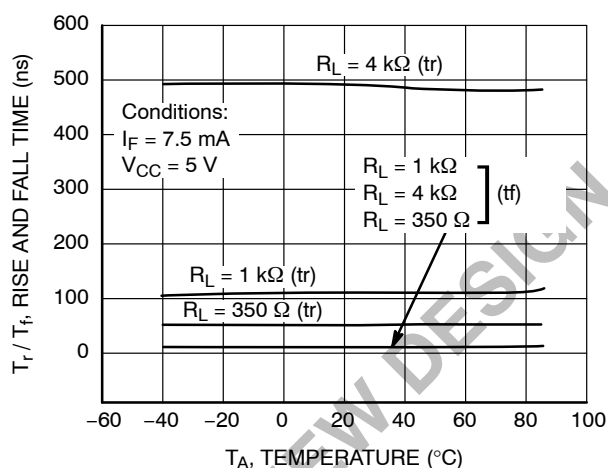


Figure 9. Rise and Fall Time vs. Temperature

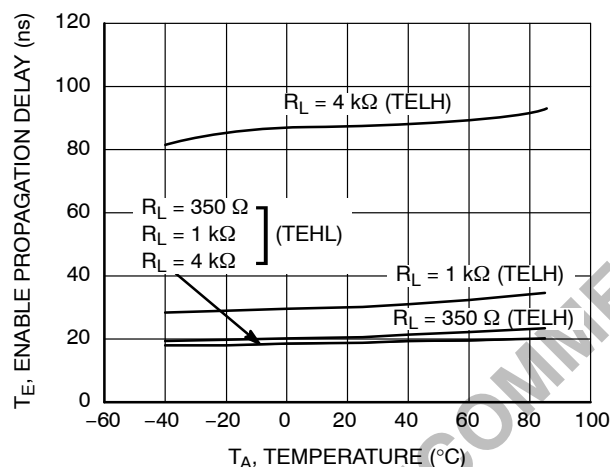


Figure 10. Enable Propagation Delay vs. Temperature

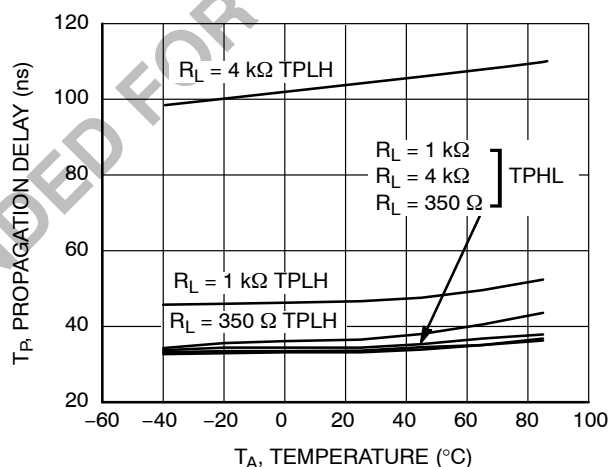


Figure 11. Switching Time vs. Temperature

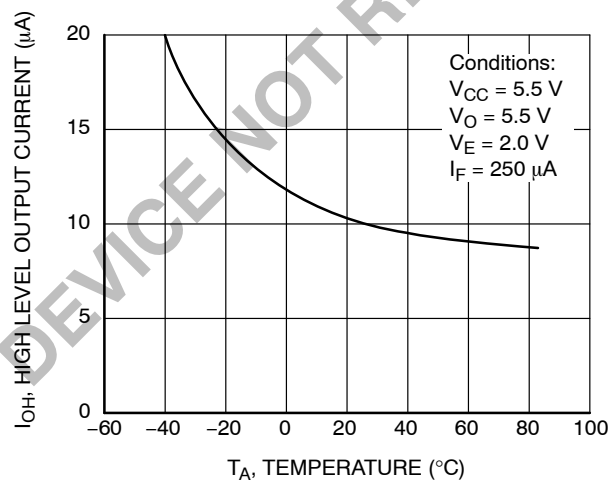


Figure 12. High Level Output Current vs. Temperature

## TEST CIRCUITS

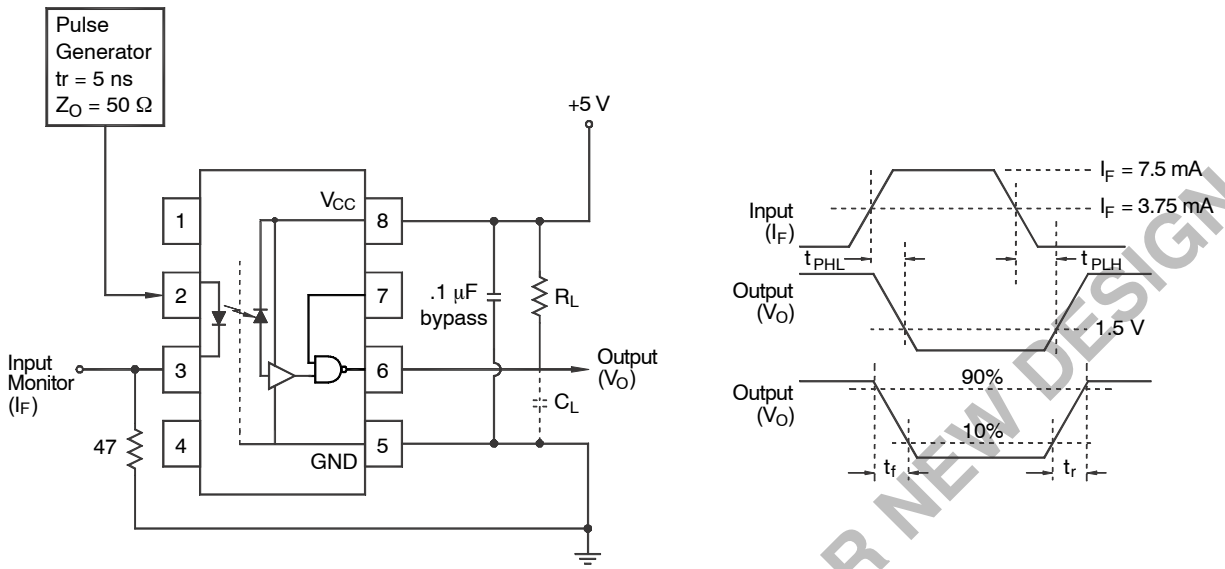


Figure 13. Test Circuit and Waveforms for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$  and  $t_f$

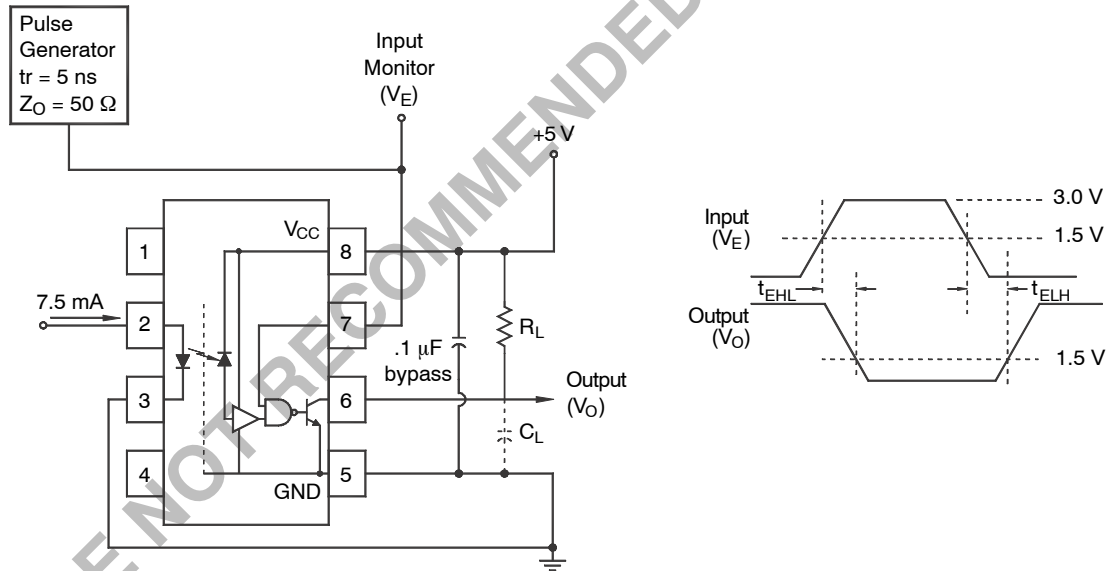


Figure 14. Test Circuit  $t_{EHL}$  and  $t_{ELH}$



# TEST CIRCUITS (Continued)

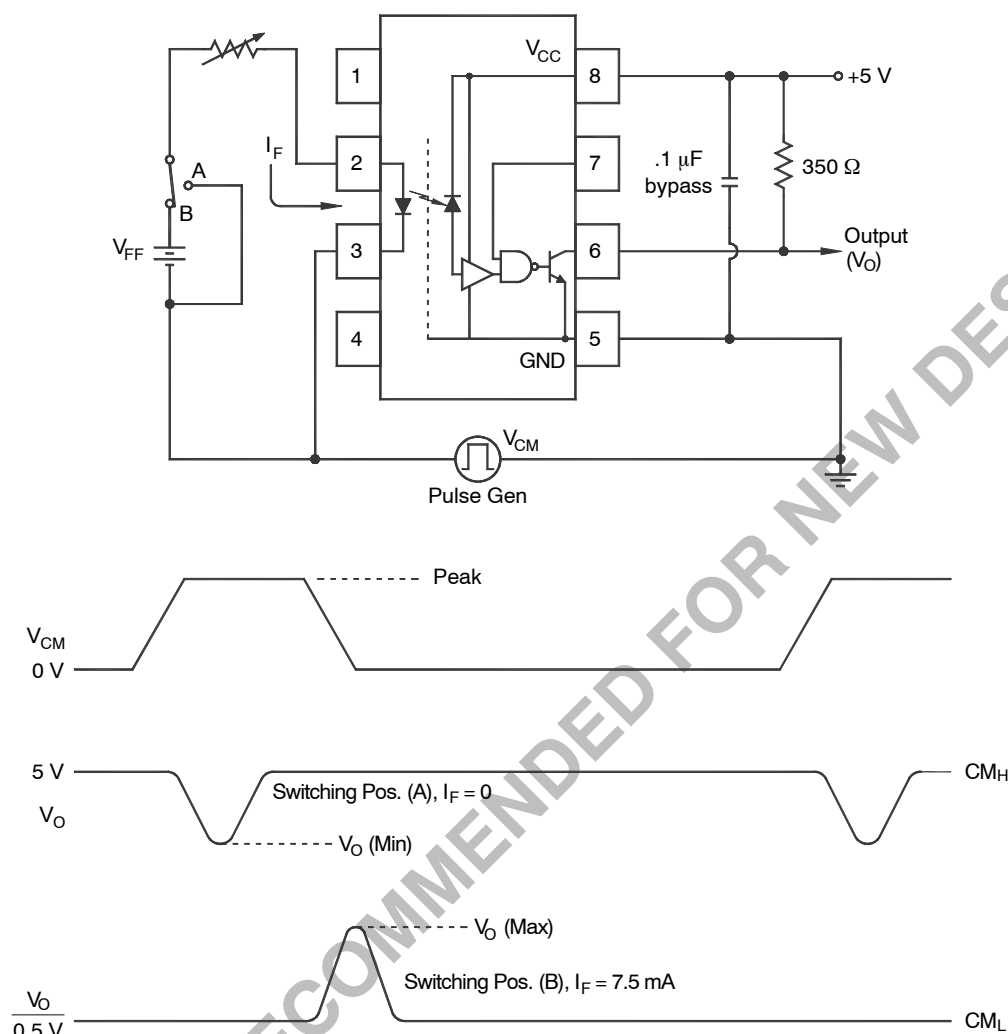
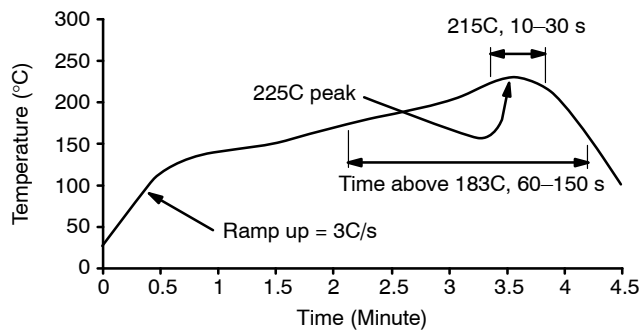


Figure 15. Test Circuit Common Mode Transient Immunity

## REFLOW PROFILE



- Peak reflow temperature: 225C (package surface temperature)
- Time of temperature higher than 183C for 60–150 seconds
- One time soldering reflow is recommended

Figure 16. Reflow Profile

#### ORDERING INFORMATION

| Option | Example Part Number | Description†  |
|--------|---------------------|---|
| S      | 6N137S              | PDIP8 GW, CASE 709AC<br>Surface Mount Lead Bend                 |
| SD     | 6N137SD             | PDIP8 GW, CASE 709AC<br>Surface Mount; Tape and Reel            |
| W      | 6N137W              | PDIP8 6.6x3.81, 2.54P, CASE 646BW<br>0.4" Lead Spacing          |
| V      | 6N137V              | PDIP8 9.655x6.6, 2.54P, CASE 646CQ<br>VDE0884                   |
| WV     | 6N137WV             | PDIP8 6.6x3.81, 2.54P, CASE 646BW<br>VDE0884; 0.4" Lead Spacing |
| SV     | 6N137SV             | PDIP8 GW, CASE 709AC<br>VDE0884; Surface Mount                  |
| SDV    | 6N137SDV            | PDIP8 GW, CASE 709AC<br>VDE0884; Surface Mount; Tape and Reel   |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DEVICE NOT RECOMMENDED FOR NEW DESIGN

# MECHANICAL CASE OUTLINE

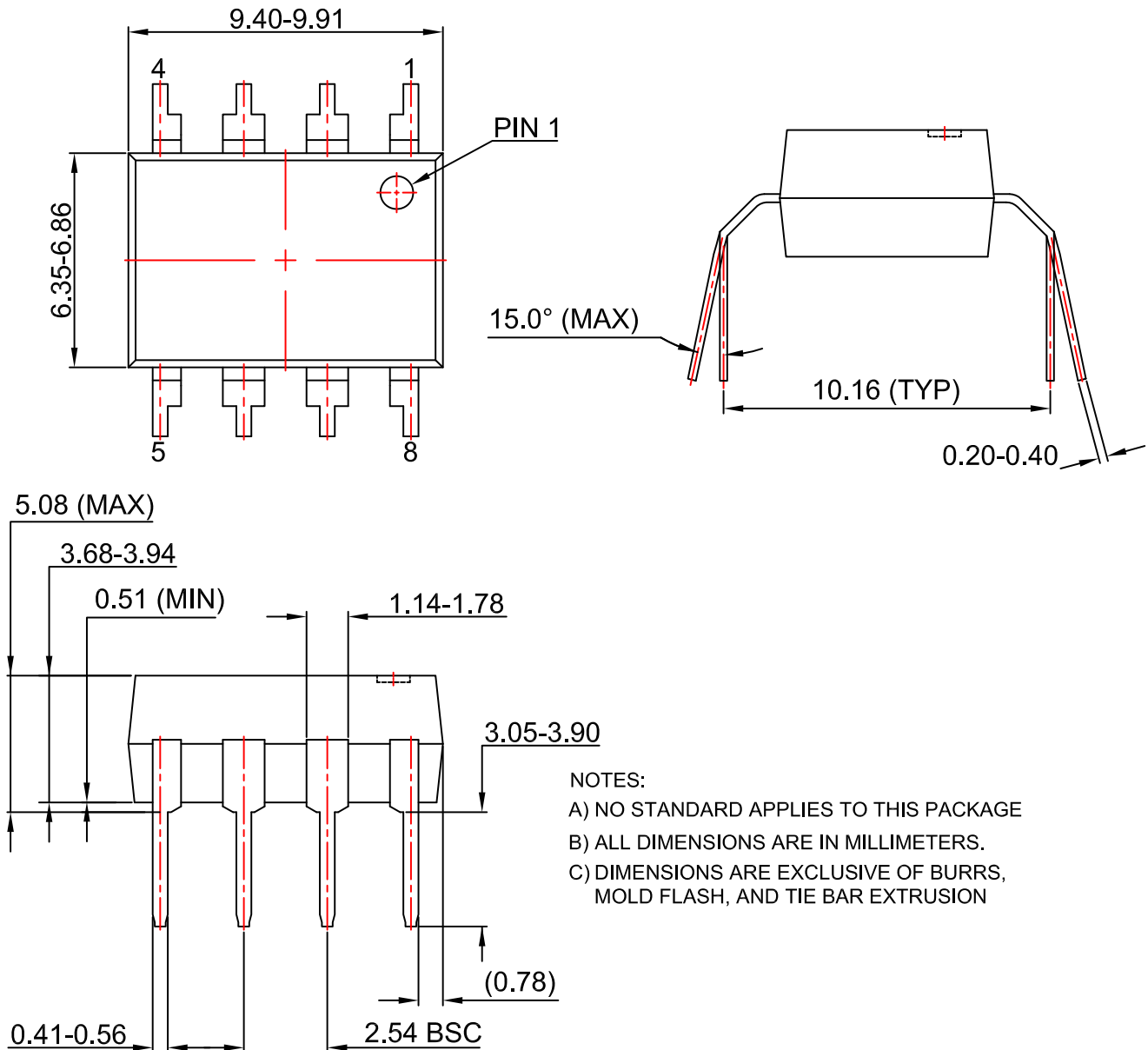
## PACKAGE DIMENSIONS

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PDIP8 6.6x3.81, 2.54P  
CASE 646BW  
ISSUE O

DATE 31 JUL 2016



|                  |                       |   |
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| DESCRIPTION:     | PDIP8 6.6X3.81, 2.54P | PAGE 1 OF 1   |

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# MECHANICAL CASE OUTLINE

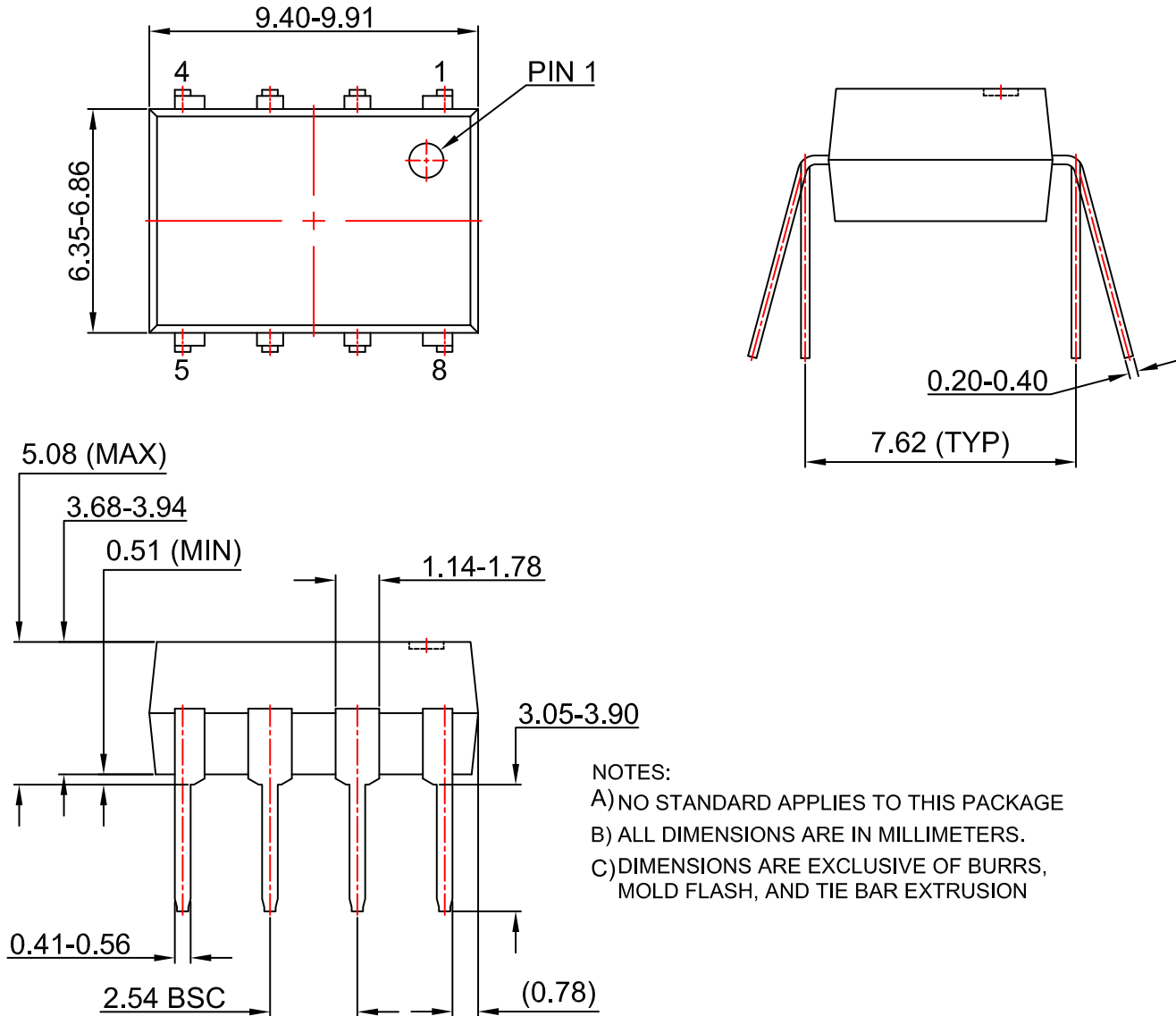
## PACKAGE DIMENSIONS

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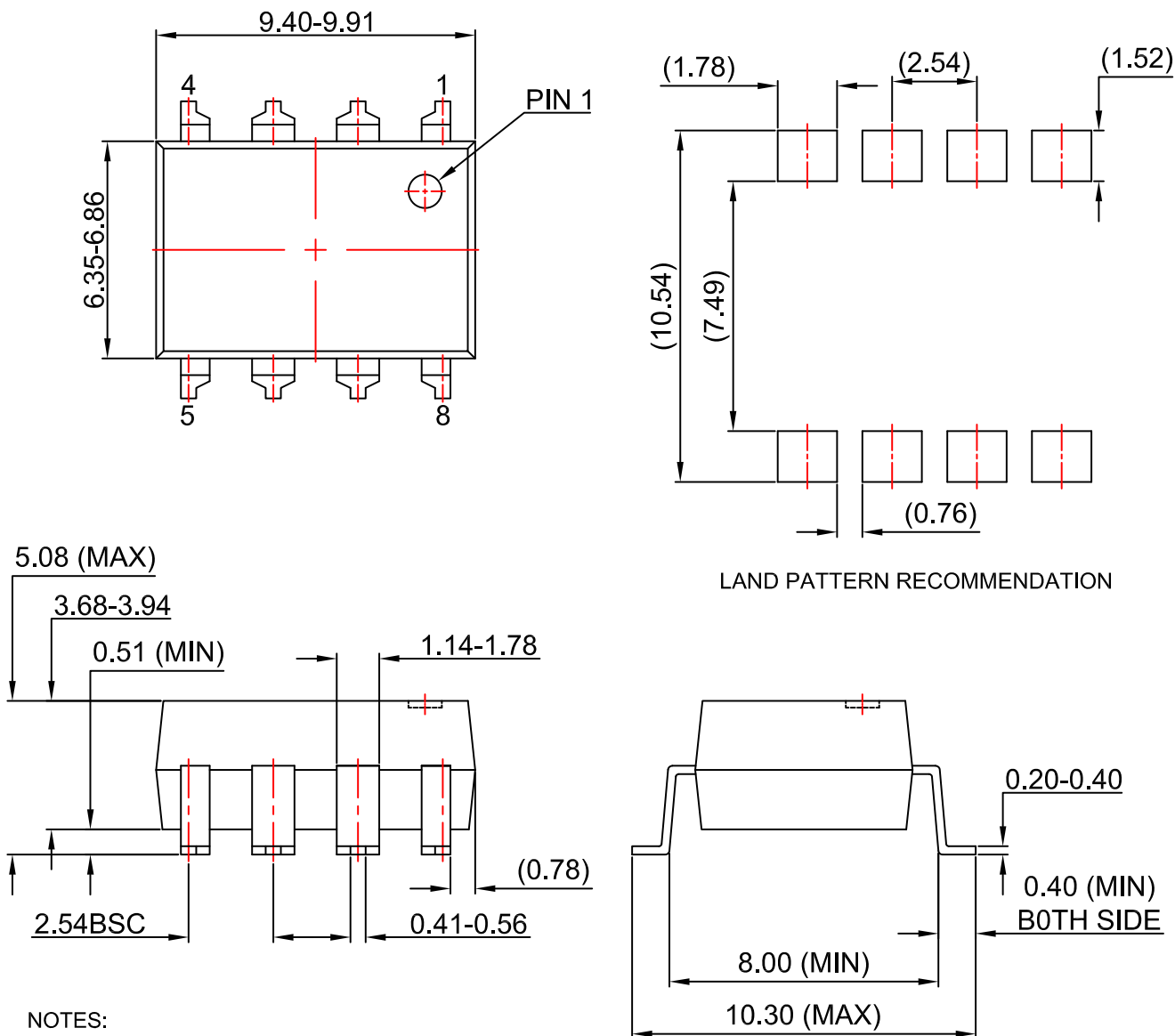


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