Integer-N Clock Translator for Wireline Communications

AD9550

FEATURES

- Converts preset standard input frequencies to standard output frequencies
- Input frequencies from 8 kHz to 200 MHz
- Output frequencies up to 810 MHz LVPECL and LVDS (200 MHz CMOS)
- Preset pin-programmable frequency translation ratios
- On-chip VCO
- Single-ended CMOS reference input
- Two output clocks (independently programmable as LVDS, LVPECL, or CMOS)
- Single supply (3.3 V)
- Very low power: <450 mW (under most conditions)
- Small package size (5 mm × 5 mm)
- Exceeds Telcordia GR-253-CORE jitter generation, transfer and tolerance specifications

APPLICATIONS

- Cost effective replacement of high frequency VCXO, OCXO, and SAW resonators
- Flexible frequency translation for wireline applications such as Ethernet, T1/E1, SONET/SDH, GPON, xDSL
- Wireless infrastructure
- Test and measurement (including handheld devices)

BASIC BLOCK DIAGRAM

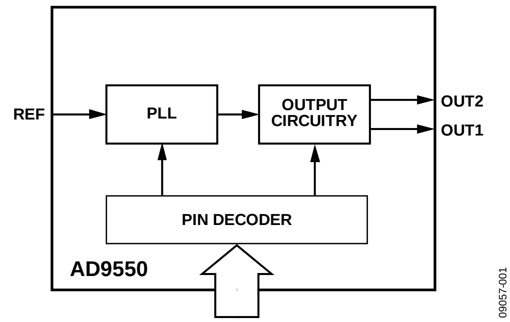

Figure 1.

GENERAL DESCRIPTION

The AD9550 is a phase-locked loop (PLL) based clock translator designed to address the needs of wireline communication and base station applications. The device employs an integer-N PLL to accommodate the applicable frequency translation requirements. It accepts a single-ended input reference signal at the REF input.

The AD9550 is pin programmable, providing a matrix of standard input/output frequency translations from a list of 15 possible input frequencies to a list of 52 possible output frequency pairs (OUT1 and OUT2).

The AD9550 output is compatible with LVPECL, LVDS, or single-ended CMOS logic levels, although the AD9550 is implemented in a strictly CMOS process.

The AD9550 operates over the extended industrial temperature range of −40°C to +85°C.

Rev. 0

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REVISION HISTORY

8/10—Revision 0: Initial Version

SPECIFICATIONS

Minimum (min) and maximum (max) values apply for the full range of supply voltage and operating temperature variations. Typical (typ) values apply for VDD = 3.3 V; T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE	3.135	3.30	3.465	V	Pin 18, Pin 21, and Pin 28
POWER CONSUMPTION					Tested with both output channels active at maximum output frequency; LVPECL and LVDS outputs use a 100 Ω termination between both pins of the output driver
Total Current		162	185	mA	
VDD Current By Pin					
Pin 18		93	106	mA	
Pin 21					
LVDS Configured Output		35	41	mA	
LVPECL Configured Output		36	42	mA	
CMOS Configured Output		29	34	mA	
Pin 28					
LVDS Configured Output		35	41	mA	
LVPECL Configured Output		36	42	mA	
CMOS Configured Output		29	34	mA	
LOGIC INPUT PINS					
Input Characteristics[1]					
Logic 1 Voltage, V_{IH}	1.02			V	For the CMOS inputs, a static Logic 1 results from either a pull-up resistor or no connection
Logic 0 Voltage, V_{IL}			0.64	V	
Logic 1 Current, I_{IH}			3	μA	
Logic 0 Current, I_{IL}			17	μA	
LOGIC OUTPUT PINS					
Output Characteristics					Tested at 1 mA load current
Output Voltage High, V_{OH}	2.7			V	
Output Voltage Low, V_{OL}			0.19	V	
$\overline{\text{RESET}}$ Pin					
Input Characteristics[2]					
Input Voltage High, V_{IH}	1.96			V	
Input Voltage Low, V_{IL}			0.85	V	
Input Current High, I_{INH}		0.3	12.5	μA	
Input Current Low, I_{INL}		31	43	μA	
Minimum Pulse Width Low	150			μs	Tested with an active source driving the $\overline{\text{RESET}}$ pin
REFERENCE CLOCK INPUT CHARACTERISTICS					
CMOS Single-Ended Input					
Input Frequency Range	0.008		200	MHz	
Input High Voltage	1.62			V	
Input Low Voltage			0.52	V	
Input Threshold Voltage		1.0		V	When ac coupling to the input receiver, the user must dc bias the input to 1 V
Input High Current		0.04		μA	
Input Low Current		0.03		μA	
Input Capacitance		3		pF	
Duty Cycle					Pulse width high and pulse width low establish the bounds for duty cycle
Pulse Width Low	2			ns	
Pulse Width High	2			ns	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
×2 Frequency Multiplier			125	MHz	To avoid excessive reference spurs, the ×2 multiplier requires 48% to 52% duty cycle; reference clock input frequencies greater than 125 MHz require the use of the divide-by-5 prescaler
VCO CHARACTERISTICS					
Frequency Range	3350		4050	MHz	
VCO Gain		45		MHz/V	
VCO Tracking Range	±300			ppm	
PLL Lock Time					Using the pin selected frequency settings; lock time is from the rising edge of the RESET pin to the rising edge of the LOCKED pin
Low Bandwidth Setting (170 Hz)					Applies for Pin A3 to Pin A0 = 0001 to 1100, or for Pin A3 to Pin A0 = 1111
13.3 kHz PFD Frequency		214		ms	
16 kHz PFD Frequency		176		ms	
Medium Bandwidth Setting (20 kHz)					Applies for Pin A3 to Pin A0 = 1110 and Pin Y5 to Pin Y0= 111111
1.5625 MHz PFD Frequency		2		ms	
High Bandwidth Setting (75 kHz)					Applies for Pin A3 to Pin A0 = 1101 to 1110
2.64 MHz PFD Frequency		1.50		ms	
4.86 MHz PFD Frequency		0.89		ms	

[1] The A3 to A0 and Y5 to Y0 pins have 100 kΩ internal pull-up resistors. The OM2 to OM0 pins have 40 kΩ pull-up resistors.
[2] The RESET pin has a 100 kΩ internal pull-up resistor.

OUTPUT CHARACTERISTICS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL MODE					
Differential Output Voltage Swing	690	800	890	mV	Output driver static (for dynamic performance see Figure 15)
Common-Mode Output Voltage	VDD – 1.66	VDD – 1.34	VDD – 1.01	V	Output driver static
Frequency Range	0		810	MHz	
Duty Cycle	40		60	%	Up to 805 MHz output frequency
Rise/Fall Time[1] (20% to 80%)		255	305	ps	100 Ω termination between both pins of the output driver
LVDS MODE					
Differential Output Voltage Swing					Output driver static (for dynamic performance see Figure 15)
Balanced, V_{OD}	297		398	mV	Voltage swing between output pins; output driver static
Unbalanced, ΔV_{OD}			8.3	mV	Absolute difference between voltage swing of normal pin and inverted pin; output driver static
Offset Voltage					
Common Mode, V_{OS}	1.17		1.35	V	Output driver static
Common-Mode Difference, ΔV_{OS}			7.3	mV	Voltage difference between output pins; output driver static
Short-Circuit Output Current		17	24	mA	
Frequency Range	0		810	MHz	
Duty Cycle	40		60	%	Up to 805 MHz output frequency
Rise/Fall Time[1] (20% to 80%)		285	355	ps	100 Ω termination between both pins of the output driver

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CMOS MODE					
Output Voltage High, V_{OH}					Output driver static
I_{OH} = 10 mA	2.8			V	
I_{OH} = 1 mA	2.8			V	
Output Voltage Low, V_{OL}					Output driver static
I_{OL} = 10 mA			0.5	V	
I_{OL} = 1 mA			0.3	V	
Frequency Range	0		200	MHz	3.3 V CMOS; output toggle rates in excess of the maximum are possible, but with reduced amplitude (see Figure 14)
Duty Cycle	45		55	%	At maximum output frequency
Rise/Fall Time[1] (20% to 80%)		500	745	ps	3.3 V CMOS; 10 pF load

[1] The listed values are for the slower edge (rise or fall).

JITTER CHARACTERISTICS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					
Output					
12 kHz to 20 MHz					
LVPECL		1.31		ps rms	Input = 122.88 MHz, output = 155.52 MHz
		1.28		ps rms	Input = 19.44 MHz, output = 245.76 MHz
		0.89		ps rms	Input = 25 MHz, output = 125 MHz, Pin A3 to Pin A0 = 1110, Pin Y5 to Pin Y0 = 111111 (see Figure 3)
LVDS Output		1.32		ps rms	Input = 122.88 MHz, output = 155.52 MHz
		1.29		ps rms	Input = 19.44 MHz, output = 245.76 MHz
CMOS Output		1.24		ps rms	Input = 122.88 MHz, output = 155.52 MHz
		1.26		ps rms	Input = 19.44 MHz, output = 245.76 MHz, see Figure 14 regarding CMOS toggle rates above 250 MHz
50 kHz to 80 MHz					Input = 122.88 MHz, output = 155.52 MHz
LVPECL		0.44		ps rms	Input = 122.88 MHz, output = 155.52 MHz
		0.75		ps rms	Input = 19.44 MHz, output = 245.76 MHz
		0.58		ps rms	Input = 25 MHz, output = 125 MHz, Pin A3 to Pin A0 = 1110, Pin Y5 to Pin Y0 = 111111 (see Figure 3)
LVDS		0.45		ps rms	Input = 122.88 MHz, output = 155.52 MHz
		0.76		ps rms	Input = 19.44 MHz, output = 245.76 MHz
CMOS		0.39		ps rms	Input = 122.88 MHz, output = 155.52 MHz
		0.44		ps rms	Input = 19.44 MHz, output = 245.76 MHz, see Figure 14 regarding CMOS toggle rates above 250 MHz
JITTER TRANSFER BANDWIDTH					See the Typical Performance Characteristics section
Bandwidth Setting					
Low		170		Hz	
Medium		20		kHz	
High		75		kHz	
JITTER TRANSFER PEAKING					See the Typical Performance Characteristics section
Bandwidth Setting					
Low		1.3		dB	
Medium		0		dB	
High		0.08		dB	

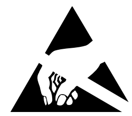
ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage (VDD)	3.6 V
Maximum Digital Input Voltage	−0.5 V to VDD + 0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

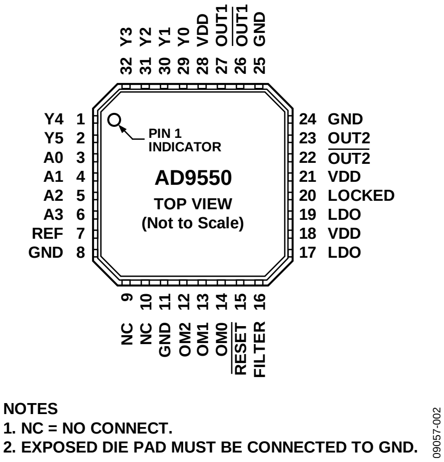


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
29, 30, 31, 32, 1, 2	Y0, Y1, Y2, Y3, Y4, Y5	I	Control Pins. These pins select one of 52 preset output frequency combinations for OUT1 and OUT2. Each pin has an internal 100 kΩ pull-up resistor.
3, 4, 5, 6	A0, A1, A2, A3	I	Control Pins. These pins select one of 15 preset input reference frequencies. Each pin has an internal 100 kΩ pull-up resistor.
7	REF	I	Reference Clock Input. Connect this pin to a single-ended active clock input signal.
8, 11, 24, 25	GND	P	Ground.
9, 10	NC		No Connection. Make no external connection to these pins. Do not connect to GND or VDD.
12, 13, 14	OM2, OM1, OM0	I	Control Pins. These pins select one of eight preset output configurations (see Table 10). Each pin has an internal 40 kΩ pull-up resistor.
15	$\overline{\text{RESET}}$	I	Reset Internal Logic. This is a digital input pin. This pin is active low with a 100 kΩ internal pull-up resistor and resets the internal logic to default states (see the Automatic Power-On Reset section).
16	FILTER	I/O	Loop Filter Node for the PLL. Connect external loop filter components (see Figure 24) from this pin to Pin 17 (LDO).
17, 19	LDO	P/O	LDO Decoupling Pins. Connect a 0.47 µF decoupling capacitor from each of these pins to ground.
18, 21, 28	VDD	P	Power Supply Connection: 3.3 V Supply. Pin 21 supplies the OUT2 driver and Pin 28 supplies the OUT1 driver.
20	LOCKED	O	Locked Status Indicator for the PLL. Active high.
26, 22	$\overline{\text{OUT1}}$, $\overline{\text{OUT2}}$	O	Complementary Square Wave Clocking Outputs.
27, 23	OUT1, OUT2	O	Square Wave Clocking Outputs.
N/A[2]	EP		Exposed Die Pad. The exposed die pad must be connected to GND.

[1] I is input, I/O is input/output, O is output, P is power, and P/O is power/output.
[2] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

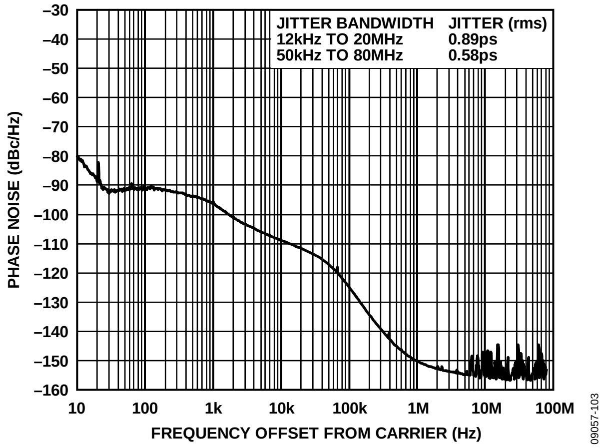


Figure 3. Phase Noise (f_{REF} = 25 MHz, f_{OUT1} = 125 MHz)

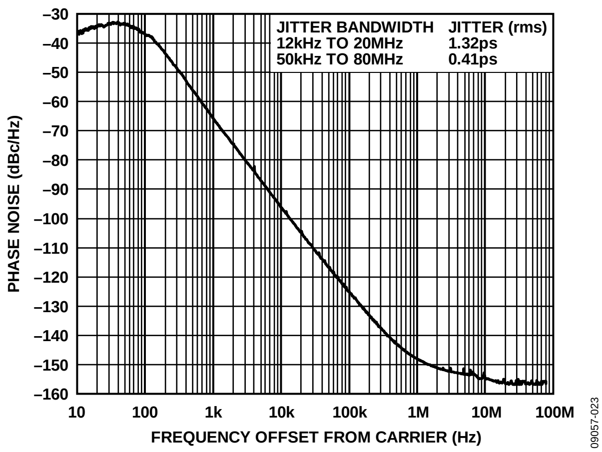


Figure 4. Phase Noise (f_{REF} = 25 MHz, f_{OUT1} = 156.25 MHz)

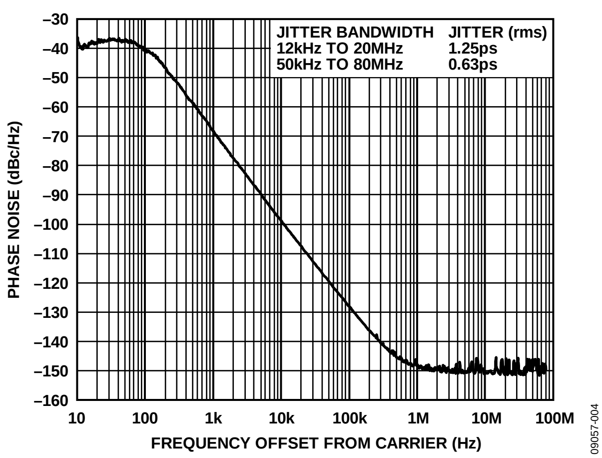


Figure 5. Phase Noise (f_{REF} = 61.44 MHz, f_{OUT1} = 122.88 MHz)

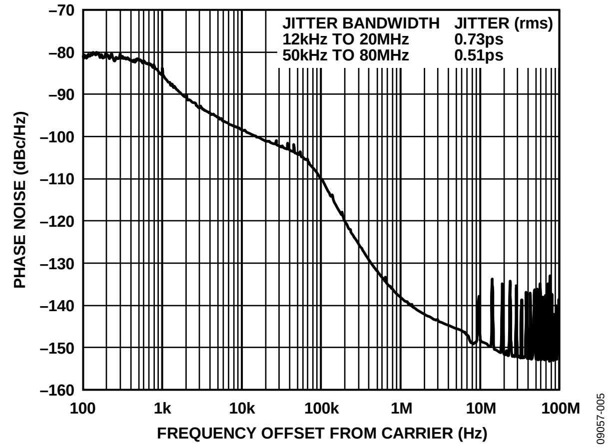


Figure 6. Phase Noise (f_{REF} = 77.76 MHz, f_{OUT1} = 622.08 MHz)

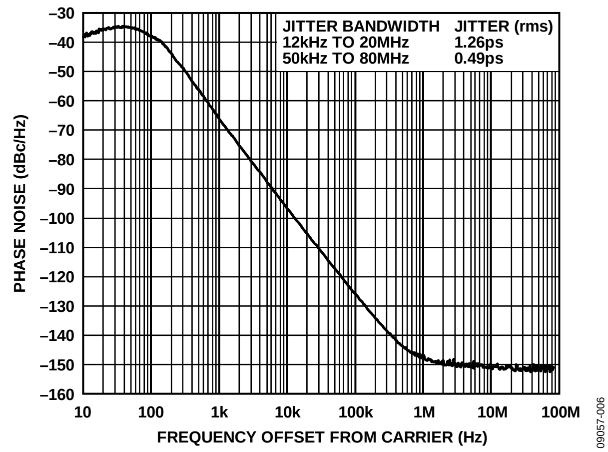


Figure 7. Phase Noise (f_{REF} = 19.44 MHz, f_{OUT1} = 155.52 MHz)

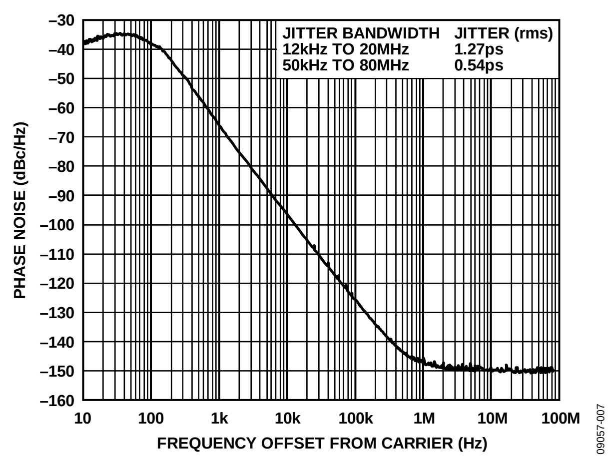


Figure 8. Phase Noise (f_{REF} = 8 kHz, f_{OUT1} = 155.52 MHz)

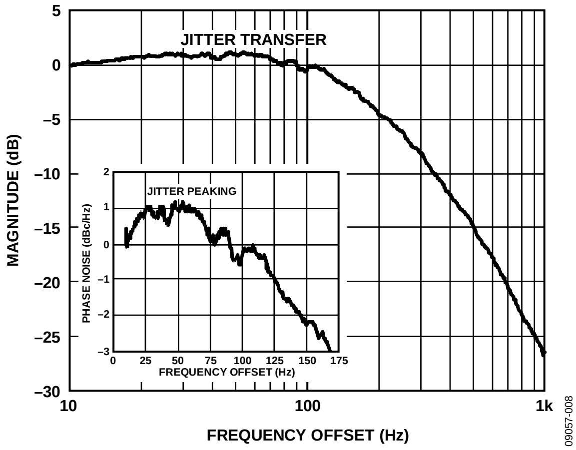


Figure 9. Jitter Transfer, Loop Bandwidth = 170 Hz

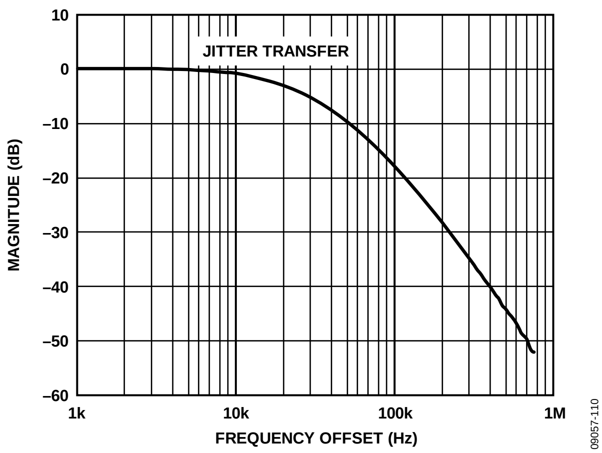


Figure 10. Jitter Transfer, Loop Bandwidth = 20 kHz

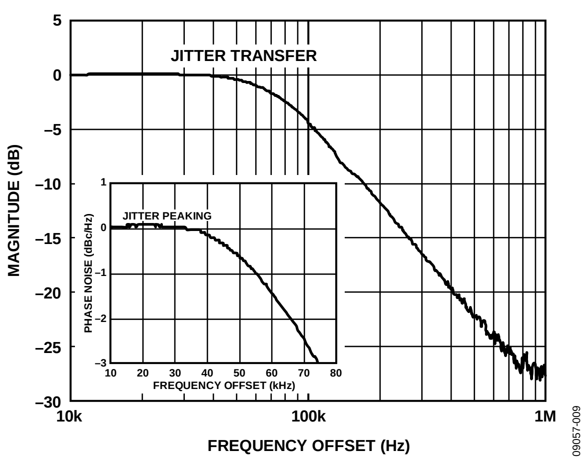


Figure 11. Jitter Transfer, Loop Bandwidth = 75 kHz

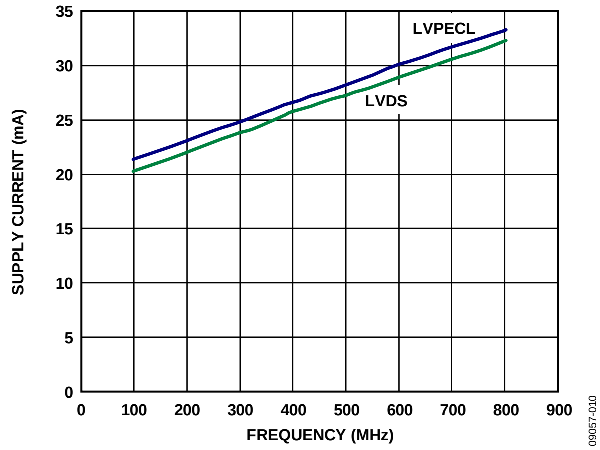


Figure 12. Supply Current vs. Output Frequency, LVPECL and LVDS (10 pF Load)

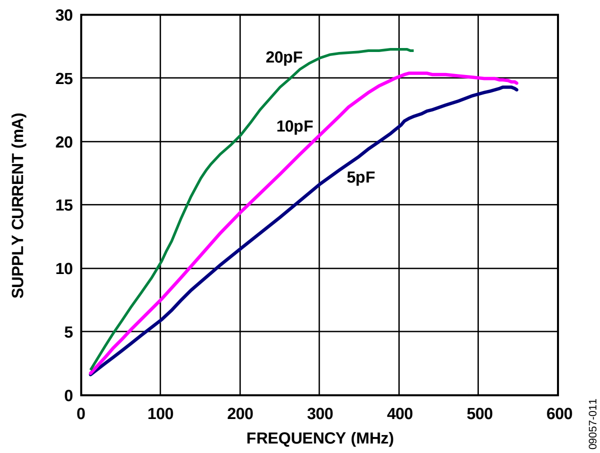


Figure 13. Supply Current vs. Output Frequency, CMOS (10 pF Load)

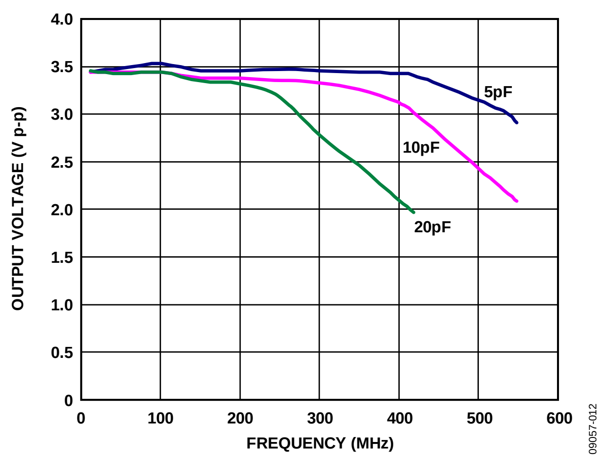


Figure 14. Peak-to-Peak Output Voltage vs. Frequency, CMOS

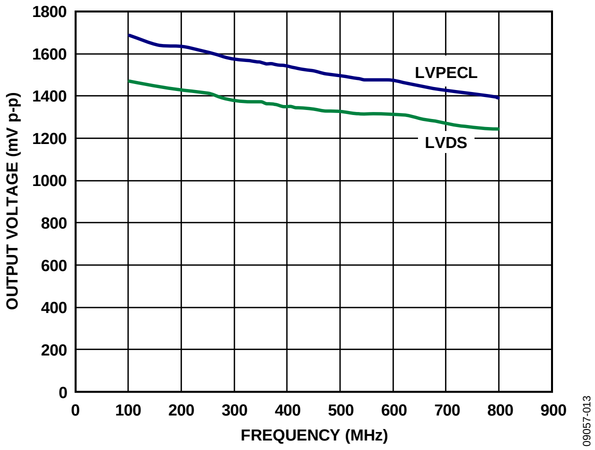


Figure 15. Peak-to-Peak Output Voltage vs. Frequency, LVPECL and LVDS (100 Ω Load)

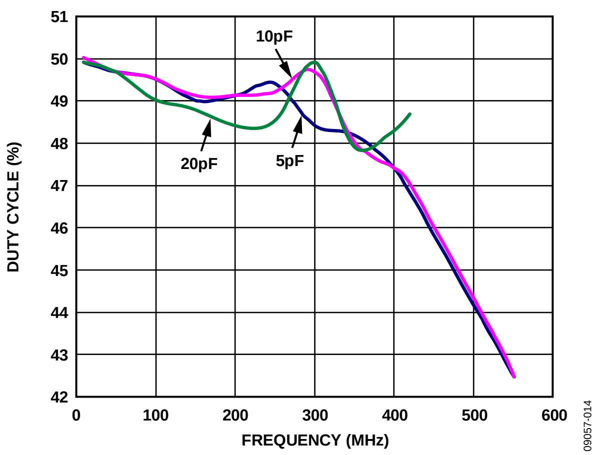


Figure 16. Duty Cycle vs. Output Frequency, CMOS

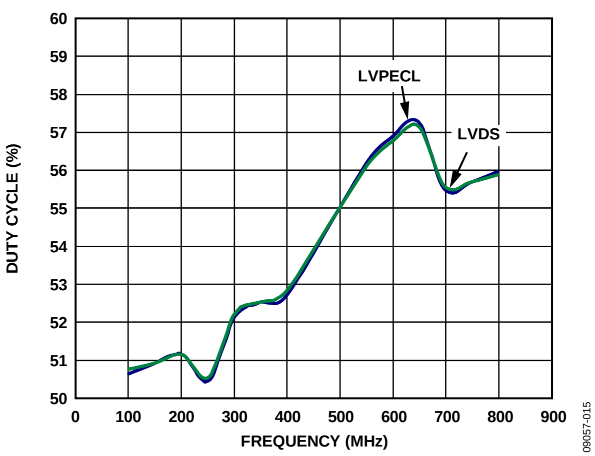


Figure 17. Duty Cycle vs. Output Frequency, LVPECL and LVDS (100 Ω Load)

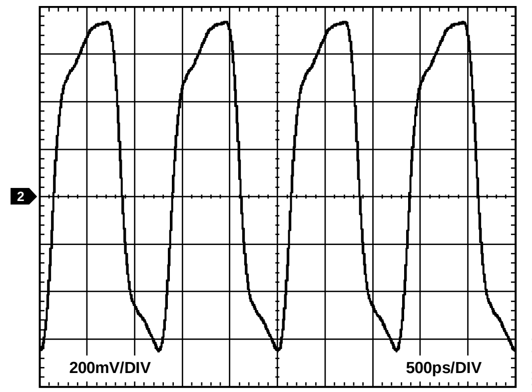


Figure 18. Typical Output Waveform, LVPECL (800 MHz)

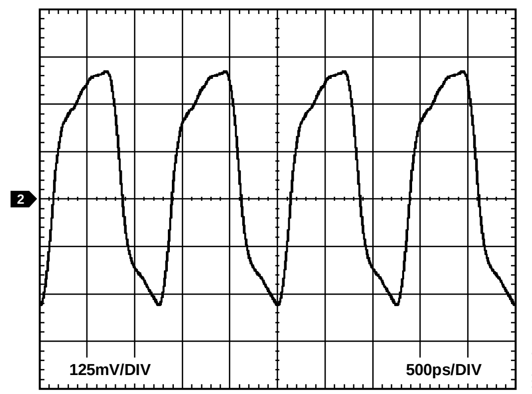


Figure 19. Typical Output Waveform, LVDS (800 MHz, 3.5 mA Drive Current)

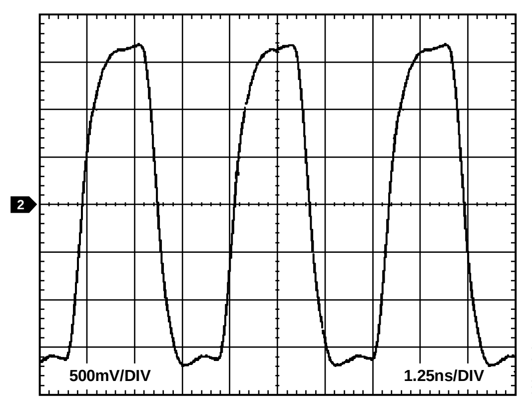


Figure 20. Typical Output Waveform, CMOS (250 MHz, 10 pF Load)

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

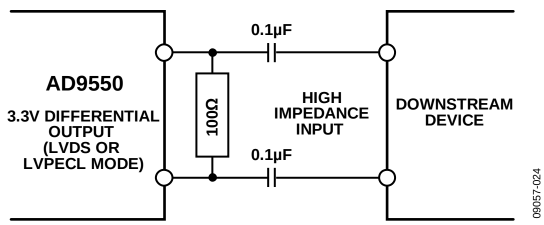


Figure 21. AC-Coupled LVDS or LVPECL Output Driver

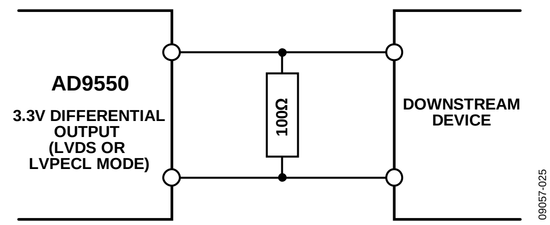


Figure 22. DC-Coupled LVDS or LVPECL Output Driver

THEORY OF OPERATION

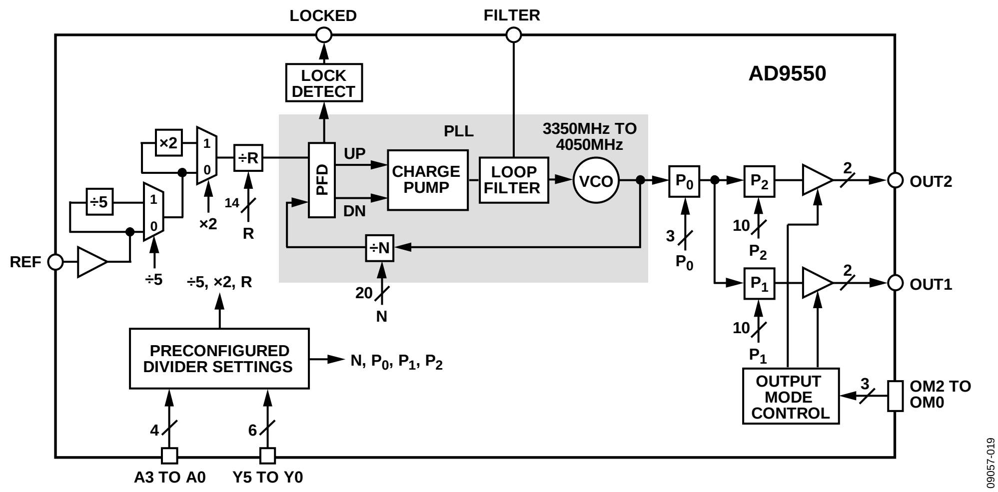


Figure 23. Detailed Block Diagram

OVERVIEW

The AD9550 accepts one input reference clock, REF. The input clock path includes an optional divide-by-5 prescaler, an optional ×2 frequency multiplier, and a 14-bit programmable divider (R). The output of the R divider drives the input to the PLL.

The PLL translates the R-divider output to a frequency within the operating range of the VCO (3.35 GHz to 4.05 GHz) based on the value of the feedback divider (N). The VCO prescaler (P_0) reduces the VCO output frequency by an integer factor from 5 to 11, resulting in an intermediate frequency in the range of 305 MHz to 810 MHz. The 10-bit P_1 and P_2 dividers can further reduce the P_0 output frequency to yield the final output clock frequencies at OUT1 and OUT2, respectively.

Thus, the frequency translation ratio from the reference input to the output depends on the selection of the divide-by-5 prescalers, the ×2 frequency multipliers, the values of the three R dividers, the N divider, and the P_0, P_1, and P_2 dividers. These parameters are set automatically via the preconfigured divider settings per the Ax and Yx pins (see the Preset Frequencies section).

PRESET FREQUENCIES

The frequency selection pins (A3 to A0 and Y5 to Y0) allow the user to hardwire the device for preset input and output frequencies based on the pin logic states (see Figure 23). The pins decode ground or open connections as Logic 0 or Logic 1, respectively.

The A3 to A0 pins allow the user to select one of 15 input reference frequencies as shown in Table 6. The device sets the appropriate divide-by-5 (÷5), multiply-by-2 (×2), and input divider (R) values based on the logic levels applied to the Ax pins.

The divide-by-5, ×2, and R values cause the PLL input frequency to be either 16 kHz or 40/3 kHz. There are two exceptions. The first is for A3 to A0 = 1101, which yields a PLL input frequency of 155.52/59 MHz. The second is for A3 to A0 = 1110, which yields a PLL input frequency of either 1.5625 MHz or 4.86 MHz depending on the Y5 to Y0 pins.

The Y5 to Y0 pins allow the user to select one of 52 output frequency combinations (f_{OUT1} and f_{OUT2}) per Table 7. The device sets the appropriate P_0, P_1, and P_2 settings based on the logic levels applied to the Yx pins. Note, however, that selecting 101101 through 110010 require A3 to A0 = 1101 and selecting 110011 requires A3 to A0 = 1110.

The value (N) of the PLL feedback divider and the control setting for the charge pump current (CP) depend on a combination of both the Ax and Yx pin settings as shown in Table 8.

Table 6. Pin Configured Input Frequency, Ax Pins

A3 to A0	f_{REF} (MHz)	Divide-by-5[1]	×2[1]	R (Decimal)
0000	Not used			
0001	0.008	Bypassed	On	1
0010	1.536	Bypassed	Bypassed	96
0011	2.048	Bypassed	Bypassed	128
0100	16.384	Bypassed	Bypassed	1024
0101	19.44	Bypassed	Bypassed	1215
0110 [2]	25	Bypassed	On	3125
0111	38.88	Bypassed	Bypassed	2430
1000	61.44	Bypassed	Bypassed	3840
1001	77.76	Bypassed	Bypassed	4860
1010	122.88	Bypassed	Bypassed	7680
1011	125	On	On	3125
1100	1.544	Bypassed	On	193
1101[3]	155.52	Bypassed	Bypassed	59
1110[4]	25 or 77.76	Bypassed	Bypassed	16
1111	200/3	Bypassed	Bypassed	5000

[1] For divide-by-5 and ×2 frequency scalers, on indicates active.
[2] Using A3 to A0 = 0110 to yield a 25 MHz to 125 MHz conversion provides a loop bandwidth of 170 Hz. An alternate 25 MHz to 125 MHz conversion uses A3 to A0 = 1110, which provides a loop bandwidth of 20 kHz.
[3] A3 to A0 = 1101 only works with Y5 to Y0 = 101101 through 110010.
[4] A3 to A0 = 1110 only works with Y5 to Y0 = 110011 or 111111.

Table 7. Pin Configured Output Frequency, Yx Pins

Y5 to Y0	f_{VCO} (MHz)	f_{OUT1} (MHz)	f_{OUT2} (MHz)	P_0	P_1	P_2
000000	Not used					
000001	3686.4	245.76	245.76	5	3	3
000010	3686.4	245.76	122.88	5	3	6
000011	3686.4	245.76	61.44	5	3	12
000100	3686.4	245.76	16.384	5	3	45
000101	3686.4	245.76	2.048	5	3	360
000110	3686.4	245.76	1.536	5	3	480
000111	3686.4	122.88	122.88	5	6	6
001000	3686.4	122.88	61.44	5	6	12
001001	3686.4	122.88	16.384	5	6	45
001010	3686.4	122.88	2.048	5	6	360
001011	3686.4	122.88	1.536	5	6	480
001100	3686.4	61.44	61.44	5	12	12
001101	3686.4	61.44	16.384	5	12	45
001110	3686.4	61.44	2.048	5	12	360
001111	3686.4	61.44	1.536	5	12	480
010000	3686.4	16.384	16.384	5	45	45
010001	3686.4	16.384	2.048	5	45	360
010010	3686.4	16.384	1.536	5	45	480
010011	3686.4	2.048	2.048	5	360	360
010100	3686.4	2.048	1.536	5	360	480
010101	3686.4	1.536	1.536	5	480	480
010110	3750	156.25	156.25	6	4	4
010111	3750	156.25	125	6	4	5
011000	3750	156.25	25	6	4	25
011001	3750	125	125	6	5	5
011010	3750	125	25	6	5	25
011011	3750	25	25	6	25	25
011100	3732.48	155.52	155.52	6	4	4

Y5 to Y0	f_{VCO} (MHz)	f_{OUT1} (MHz)	f_{OUT2} (MHz)	P_0	P_1	P_2
011101	3732.48	155.52	77.76	6	4	8
011110	3732.48	155.52	19.44	6	4	32
011111	3732.48	77.76	77.76	6	8	8
100000	3732.48	77.76	19.44	6	8	32
100001	3732.48	19.44	19.44	6	32	32
100010	3686.4	153.6	153.6	6	4	4
100011	3686.4	153.6	122.88	6	4	5
100100	3686.4	153.6	61.44	6	4	10
100101	3686.4	153.6	2.048	6	4	300
100110	3686.4	153.6	1.536	6	4	400
100111	3600	100	100	6	6	6
101000	3600	100	50	6	6	12
101001	3600	100	25	6	6	24
101010	3600	50	50	6	12	12
101011	3600	50	25	6	12	24
101100	3705.6	1.544	1.544	6	400	400
101101	~3985.53	f_O[1]	f_O[1]	6	1	1
101110	~3985.53	f_O[1]	$f_O/2$[1]	6	1	2
101111	~3985.53	f_O[1]	$f_O/4$[1]	6	1	4
110000	~3985.53	$f_O/2$[1]	$f_O/2$[1]	6	2	2
110001	~3985.53	$f_O/2$[1]	$f_O/4$[1]	6	2	4
110010	~3985.53	$f_O/4$[1]	$f_O/4$[1]	6	4	4
110011	3732.48	622.08	622.08	6	1	1
110100 to 111110	Undefined					
111111	3750	125	25	5	6	30

[1] f_O = 39,191.04/59 MHz.

Table 8. Pin Configuration vs. PLL Feedback Divider Value and Charge Pump Value

A3 to A0	Y5 to Y0	N[1]	CP[2]
0001 to 1100	000001 to 010101	230,400	121
	010110 to 011011	234,375	121
	011100 to 100001	233,280	121
	100010 to 100110	230,400	121
	100111 to 101011	225,000	121
	101100	231,600	121
	101101 to 111111	Undefined	
1101	000001 to 101100	Undefined	
	101101 to 110010	1512	255
	110010 to 111111	Undefined	
1110	000001 to 110010	Undefined	
	110011	768	121
	110100 to 111110	Undefined	
	111111	2400	121
1111	000001 to 010101	276,480	145
	010110 to 011011	281,250	145
	011100 to 100001	279,936	145
	100010 to 100110	276,480	145
	100111 to 101011	270,000	145
	101100	277,920	145
	101101 to 111111	Undefined	

[1] PLL feedback divider value (decimal).
[2] Charge pump value (decimal). Multiply by 3.5 μA to yield I_{CP}.

DESCRIPTION OF FUNCTIONAL BLOCKS

Input Frequency Prescaler (Divide-by-5)

The divide-by-5 prescaler provides the option to reduce the input reference frequency by a factor of five. Note that the prescaler physically precedes the ×2 frequency multiplier. This allows the prescaler to bring a high frequency reference clock down to a frequency that is within the range of the ×2 frequency multiplier.

Input ×2 Frequency Multiplier

The ×2 frequency multiplier doubles the frequency at its input, thereby taking advantage of a higher frequency at the input to the PLL. This provides greater separation between the frequency generated by the PLL and the modulation spur associated with frequency at the PLL input.

PLL (PFD, Charge Pump, VCO, Feedback Divider)

The PLL (see Figure 23) consists of a phase/frequency detector (PFD), a partially integrated analog loop filter (see Figure 24), an integrated voltage controlled oscillator (VCO), and a 20-bit programmable feedback divider. The PLL generates a 3.35 GHz to 4.05 GHz clock signal that is phase-locked to the input reference signal, and its frequency is the phase detector frequency (f_{PFD}) multiplied by the feedback divider value.

The PFD of the PLL drives a charge pump that increases, decreases, or holds constant the charge stored on the loop filter capacitors (both internal and external). The stored charge results in a voltage that sets the output frequency of the VCO. The feedback loop of the PLL causes the VCO control voltage to vary in such a way as to phase lock the PFD input signals.

The PLL has a VCO with 128 frequency bands spanning a range of 3350 MHz to 4050 MHz (3700 MHz nominal). However, the actual operating frequency within a particular band depends on the control voltage that appears on the loop filter capacitor.

The control voltage causes the VCO output frequency to vary linearly within the selected band. This frequency variability allows the control loop of the PLL to synchronize the VCO output signal with the reference signal applied to the PFD. Selection of the VCO frequency band (as well as gain adjustment) occurs automatically as part of the automatic VCO calibration process of the device, which initiates at power-up (or reset). VCO calibration centers the dc operating point of the VCO control signal. During VCO calibration, the output drivers provide a static dc signal.

The feedback divider (N-divider) sets the frequency multiplication factor of the PLL in integer steps over a 20-bit range. Note that the N-divider has a lower limit of 32.

Loop Filter

The charge pump in the PFD delivers current to the loop filter (see Figure 24). The components primarily responsible for the bandwidth of the loop filter are external and connect between Pin 16 and Pin 17.

The internal portion of the loop filter has two configurations: one is for low loop bandwidth applications (~170 Hz) and the other is for medium (~20 kHz)/high (~75 kHz) bandwidth applications. The low loop bandwidth condition applies when the feedback divider value (N) is 2^{14} (16,384) or greater. Otherwise, the medium/high loop bandwidth configuration is in effect. The feedback divider value depends on the configuration of the Ax and Yx pins per Table 8.

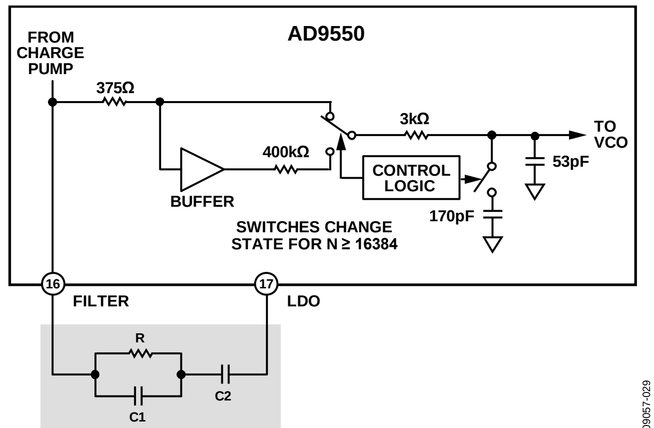


Figure 24. External Loop Filter

The bandwidth of the loop filter primarily depends on three external components (R, C1, and C2). There are two sets of recommended values for these components corresponding to the low and medium/high loop bandwidth configurations (see Table 9).

Table 9. External Loop Filter Components

A3 to A0 Pins	R	C1	C2	Loop Bandwidth
0001 to 1100, and 1111	6.8 kΩ	47 nF	1 μF	0.17 kHz
1110[1]	12 kΩ	51 pF	220 nF	20 kHz
1101 to 1110	12 kΩ	51 pF	220 nF	75 kHz

[1] The 20 kHz loop bandwidth case only applies when the A3 pin to A0 pin = 1110 and the Y5 pin to Y0 pin = 111111.

To achieve the best jitter performance in applications requiring a loop bandwidth of less than 1 kHz, C1 and C2 must have an insulation resistance of at least 500 ΩF.

PLL Locked Indicator

The PLL provides a status indicator that appears at Pin 20 (LOCKED). When the PLL acquires phase lock, the LOCKED pin switches to a Logic 1 state. When the PLL loses lock, however, the LOCKED pin returns to a Logic 0 state.

Output Dividers

The output divider section consists of three dividers: P_0, P_1, and P_2. The P_0 divider (or VCO frequency prescaler) accepts the VCO frequency and reduces it by an integer factor of 5 to 11, thereby reducing the frequency to a range between 305 MHz and 810 MHz.

The output of the P_0 divider independently drives the P_1 divider and the P_2 divider. The P_1 divider establishes the frequency at OUT1 and the P_2 divider establishes the frequency at OUT2. The P_1 and P_2 dividers are each programmable over a range of 1 to 1023, which results in a frequency at OUT1 or OUT2 that is an integer submultiple of the frequency at the output of the P_0 divider.

Output Driver Mode Control

Three mode control pins (OM0, OM1, and OM2) establish the logic family and pin function of the output drivers. The logic families include LVDS, LVPECL, and CMOS (see Table 10).

Table 10. Logic Family Assignment via the OMx Pins

	Logic Family	
Pin OMx	**OUT1**	**OUT2**
000	LVPECL	LVPECL
001	LVPECL	LVDS
010	LVDS	LVPECL
011	LVPECL	CMOS
100	LVDS	LVDS
101	LVDS	CMOS
110	CMOS	LVDS
111	CMOS	CMOS

Because both output drivers support the LVDS and LVPECL logic families, each driver has two pins to handle the differential signals associated with these two logic families. The OUT1 driver uses the OUT1 and $\overline{\text{OUT1}}$ pins, and the OUT2 driver uses the OUT2 and $\overline{\text{OUT2}}$ pins. When the OMx pins select the CMOS logic family, the signal at the $\overline{\text{OUT1}}$ pin is a phase aligned replica of the signal at the OUT1 pin and the signal at the $\overline{\text{OUT2}}$ pin is a phase aligned replica of the signal at the OUT2 pin.

JITTER TOLERANCE

Jitter tolerance is the ability of the AD9550 to maintain lock in the presence of sinusoidal jitter. The AD9550 meets the input jitter tolerance mask per Telcordia GR-253-CORE (see Figure 25). The acceptable jitter tolerance is the region above the mask.

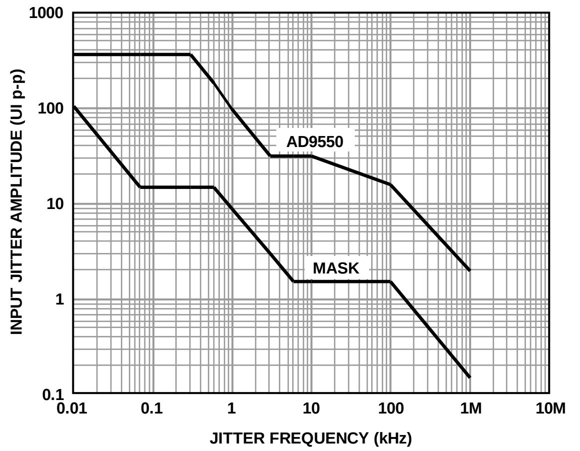


Figure 25. Jitter Tolerance

LOW DROPOUT (LDO) REGULATORS

The AD9550 is powered from a single 3.3 V supply and contains on-chip LDO regulators for each function to eliminate the need for external LDOs. To ensure optimal performance, each LDO output should have a 0.47 µF capacitor connected between its access pin and ground.

AUTOMATIC POWER-ON RESET

The AD9550 has an internal power-on reset circuit (see Figure 26). At power-up, an 800 pF capacitor momentarily holds a Logic 0 at the active low input of the reset circuitry. This ensures that the device is held in a reset state (~250 µs) until the capacitor charges sufficiently via the 100 kΩ pull-up resistor and 200 kΩ series resistor. Note that when using a low impedance source to drive the $\overline{\text{RESET}}$ pin, be sure that the source is either tristate or Logic 0 at power-up; otherwise, the device may not calibrate properly.

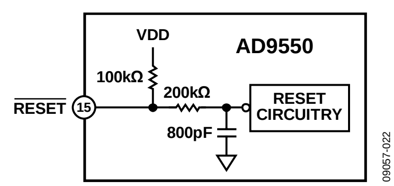


Figure 26. Power-On Reset

Provided an input reference signal is present at the REF pin, the device automatically performs a VCO calibration during power-up. If the input reference signal is not present, VCO calibration fails and the PLL does not lock. As soon as an input reference signal is present, the user must reset the device to initiate the automatic VCO calibration process.

Any change to the preset frequency selection pins requires the user to reset the device. This is necessary to initiate the automatic VCO calibration process.

APPLICATIONS INFORMATION

THERMAL PERFORMANCE

The AD9550 is specified for case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, use an airflow source.

The following equation determines the junction temperature on the application printed circuit board (PCB):

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:
T_J is the junction temperature (°C).
T_{CASE} is the case temperature (°C) measured by the customer at the top center of the package.
Ψ_{JT} is the value indicated in Table 11.
P_D is the power dissipation (see Table 1 for the power consumption parameters).

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J using the following equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations.

Table 11. Thermal Parameters for the 32-Lead LFCSP

Symbol	Description	Value[1]	Unit
θ_{JA}	Junction-to-ambient thermal resistance, 0 m/sec airflow per JEDEC JESD51-2 (still air)	41.6	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 1.0 m/sec airflow per JEDEC JESD51-6 (moving air)	36.4	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 2.5 m/sec airflow per JEDEC JESD51-6 (moving air)	32.6	°C/W
θ_{JB}	Junction-to-board thermal resistance, 0 m/sec airflow per JEDEC JESD51-8 (still air)	24.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter, 0 m/sec airflow per JEDEC JESD51-6 (still air)	22.9	°C/W
θ_{JC}	Junction-to-case thermal resistance	4.8	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter, 0 m/sec airflow per JEDEC JESD51-2 (still air)	0.5	°C/W

[1] Results are from simulations. The PCB is a JEDEC multilayer type. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine whether they are similar to those assumed in these calculations.

OUTLINE DIMENSIONS

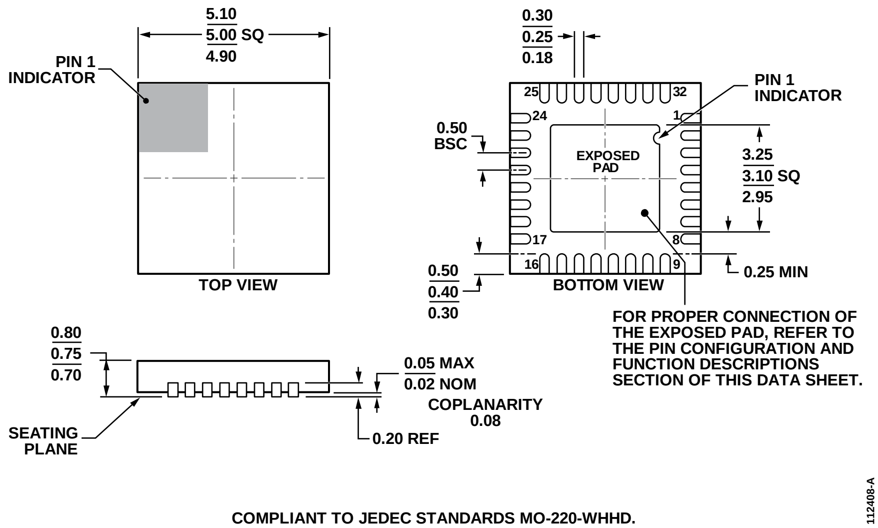


Figure 27. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very, Very Thin Quad
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9550BCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-7
AD9550BCPZ-REEL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-7
AD9550/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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