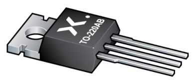

PSMN035-150P

N-channel TrenchMOS SiliconMAX standard level FET

Rev. 04 — 16 November 2009 | Product data sheet

1. Product profile

1.1 General description

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- Switched-mode power supplies

1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	150	V
		T_{mb} = 25 °C; see Figure 1 and 2	-	-	50	
			-	-	-	
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 3	-	-	-	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	V_{GS} = 10 V; V_{DS} = 120 V; T_j = 25 °C; see Figure 13	-	33	45	nC
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 11 and 12	-	30	35	mΩ

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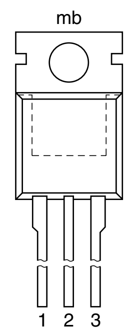
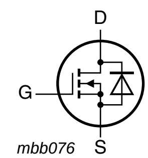
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT78 (TO-220AB)	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

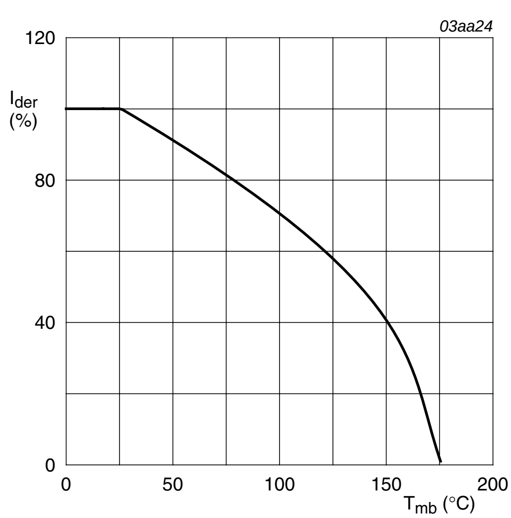
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN035-150P	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

4. Limiting values

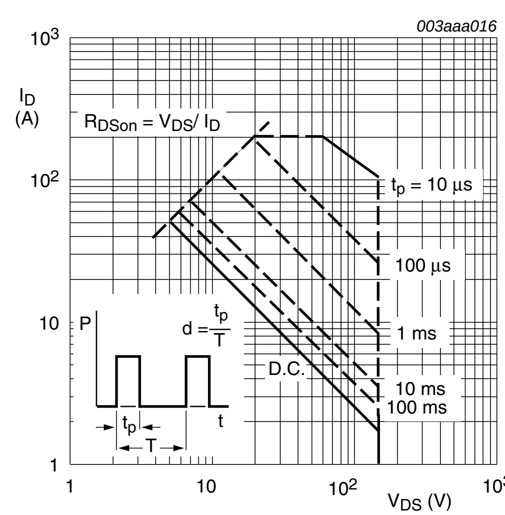
Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	T_j ≥ 25 °C; T_j ≤ 175 °C	-	150	V
V_{DGR}	drain-gate voltage	T_j ≤ 175 °C; T_j ≥ 25 °C; R_{GS} = 20 kΩ	-	150	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	T_{mb} = 100 °C; see Figure 1 and 2	-	36	A
		T_{mb} = 25 °C; see Figure 1 and 2	-	50	A
I_{DM}	peak drain current	t_p ≤ 10 µs; pulsed; T_{mb} = 25 °C; see Figure 2	-	200	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 3	-	250	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	T_{mb} = 25 °C	-	50	A
I_{SM}	peak source current	t_p ≤ 10 µs; pulsed; T_{mb} = 25 °C	-	200	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 47 A; V_{sup} ≤ 50 V; unclamped; t_p = 0.1 ms; R_{GS} = 50 Ω; see Figure 4	-	460	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} ≤ 50 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; unclamped; see Figure 4	-	50	A



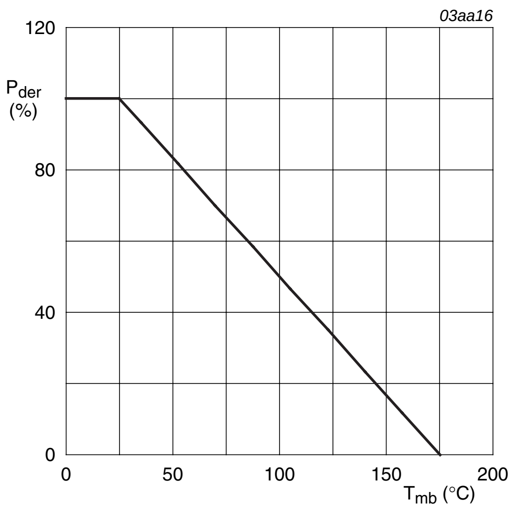
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



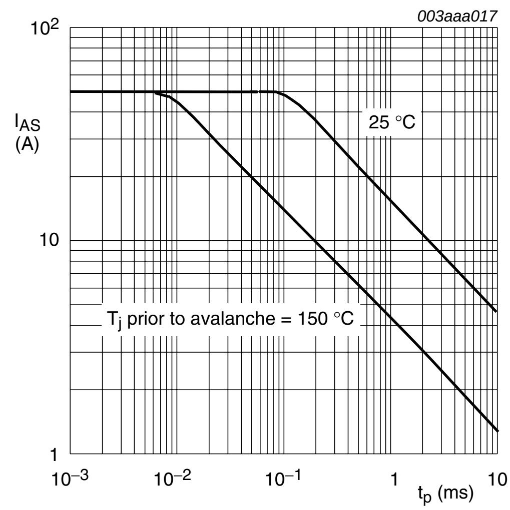
$T_{mb} = 25°C; I_{DM}$ is single pulse

Fig 2. Safe operating area; continuous and peak drain currents as a function of drain-source volt



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 3. Normalized total power dissipation as a function of mounting base temperature



Unclamped inductive load; $V_{DS} \leq 15V$; $R_{GS} = 50\Omega$; $V_{GS} = 10V$

Fig 4. Non-repetitive avalanche ruggedness current as a function of pulse duration

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	0.6	-	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air	-	-	60	K/W

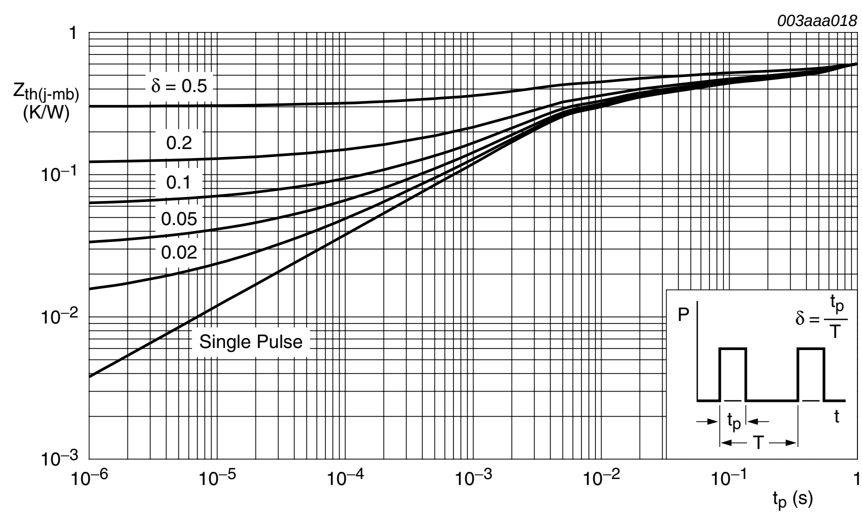
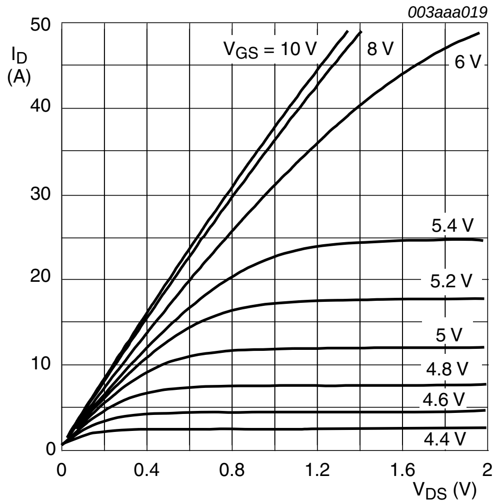


Fig 5. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

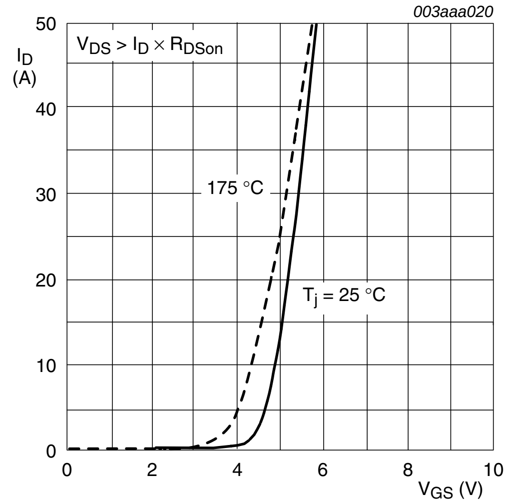
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	150	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 10	1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 10	2	3	4	V
I_{DSS}	drain leakage current	V_{DS} = 150 V; V_{GS} = 0 V; T_j = 25 °C	-	0.05	10	µA
		V_{DS} = 150 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see Figure 11 and 12	-	-	98	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 11 and 12	-	30	35	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 50 A; V_{DS} = 120 V; V_{GS} = 10 V; T_j = 25 °C; see Figure 13	-	79	-	nC
Q_{GS}	gate-source charge		-	17	-	nC
Q_{GD}	gate-drain charge		-	33	45	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 14	-	4720	-	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 13	-	456	-	pF
C_{rss}	reverse transfer capacitance		-	208	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 75 V; R_L = 1.5 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5.6 Ω; T_j = 25 °C	-	25	-	ns
t_r	rise time		-	138	-	ns
$t_{d(off)}$	turn-off delay time		-	79	-	ns
t_f	fall time		-	93	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25 °C	-	118	-	ns
Q_r	recovered charge		-	0.66	-	nC



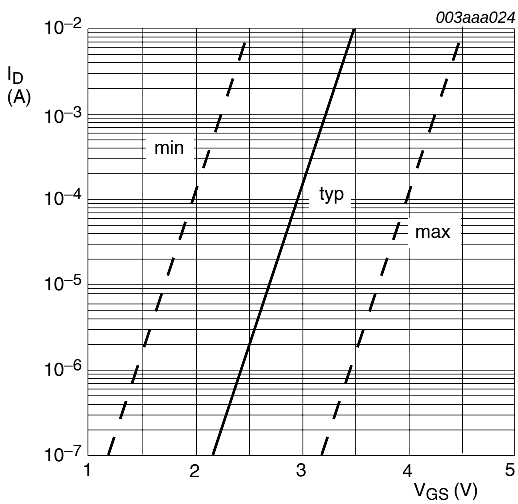
$T_j = 25°C$

Fig 6. **Output characteristics: drain current as a function of drain-source voltage; typical values**



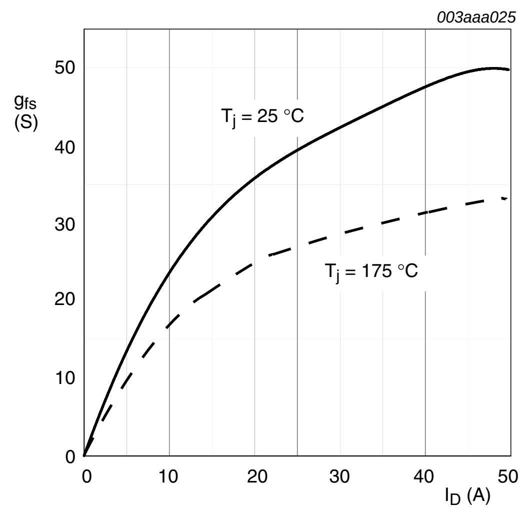
$T_j = 25°C$ and $175°C; V_{DS} > I_D \times R_{DSon}$

Fig 7. **Transfer characteristics: drain current as a function of gate-source voltage; typical values**



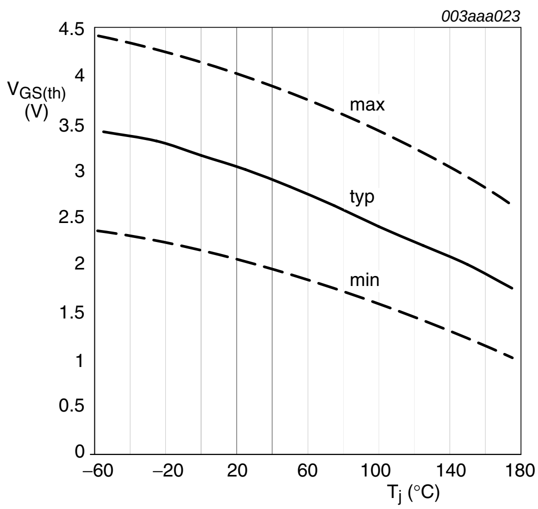
$T_j = 25°C$

Fig 8. **Sub-threshold drain current as a function of gate-source voltage**



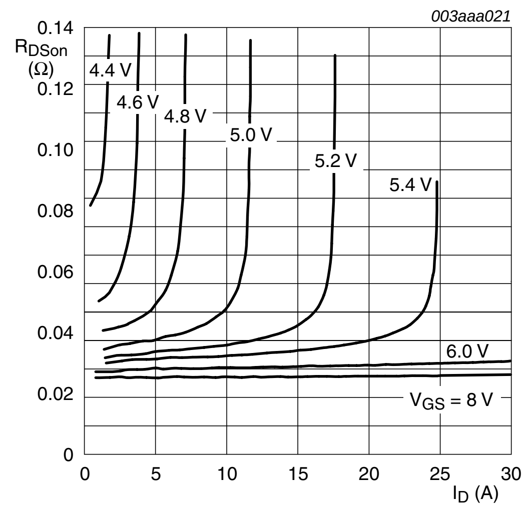
$T_j = 25°C$ and $175°C; V_{DS} > I_D \times R_{DSon}$

Fig 9. **Forward transconductance as a function of drain current; typical values**



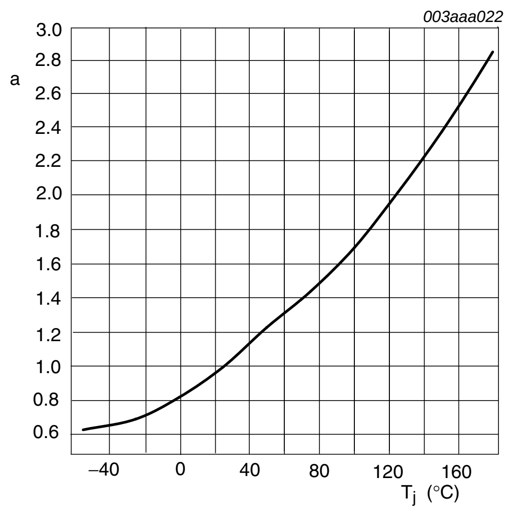
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



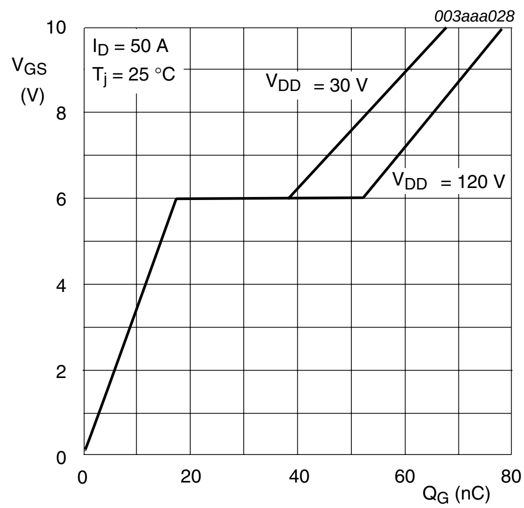
$T_j = 25°C$

Fig 11. Drain-source on-state resistance as a function of drain current; typical values



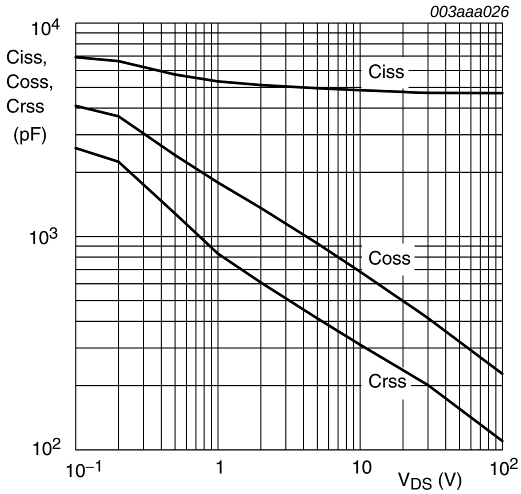
$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



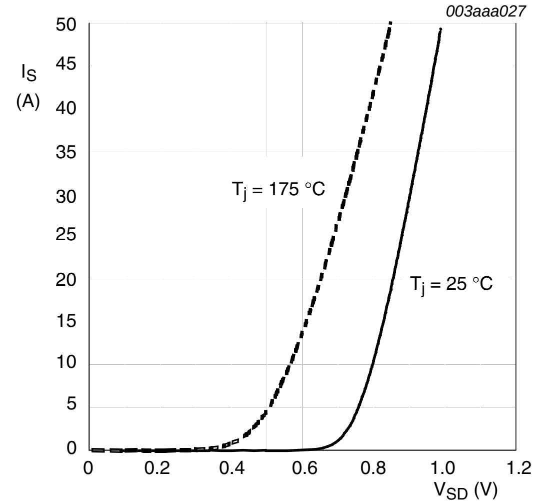
$I_D = 50\ A; T_j = 25\ °C$

Fig 13. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

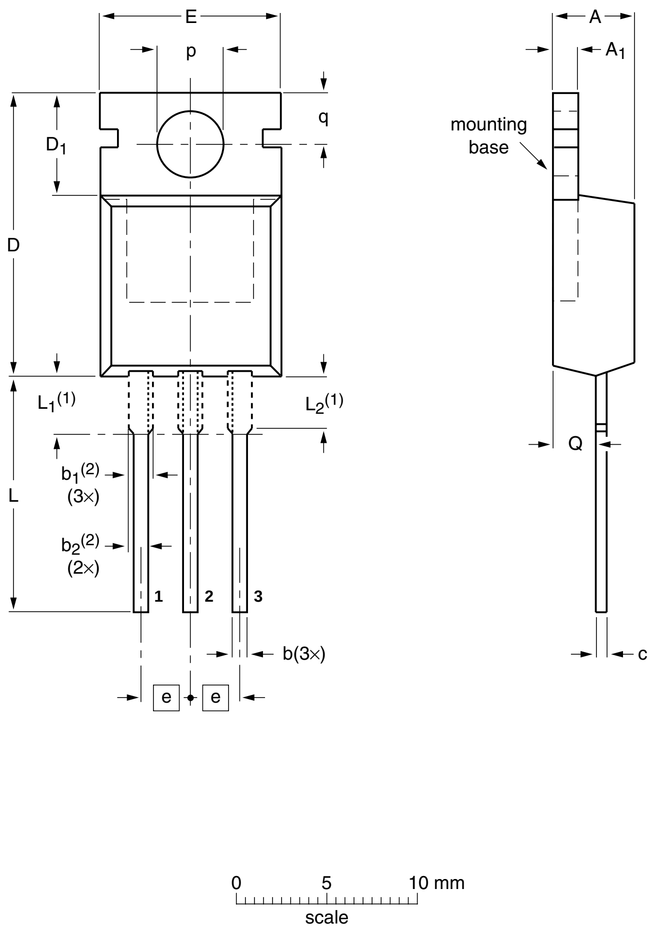


$T_j = 25°C$ and $175°C; V_{GS} = 0V$

Fig 15. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	$b_1^{(2)}$	$b_2^{(2)}$	c	D	D_1	E	e	L	$L_1^{(1)}$	$L_2^{(1)}$ max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

Notes
1. Lead shoulder designs may vary.
2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78		3-lead TO-220AB	SC-46			~~08-04-23~~ 08-06-13

Fig 16. Package outline SOT78 (TO-220AB)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN035-150P_4	20091116	Product data sheet	-	PSMN035-150_SERIES_HG_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number PSMN035-150P separated from data sheet PSMN035-150_SERIES_HG_3.			
PSMN035-150_SERIES_HG_3	20000328	Product specification	-	PSMN035-150_SERIES_2
PSMN035-150_SERIES_2	19990801	Product specification	-	PSMN035-150_SERIES_1
PSMN035-150_SERIES_1	19990201	Objective specification	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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For sales office addresses, please send an email to: salesaddresses@nexperia.com

11. Contents

Date of release: 16 November 2009