



STD65N55F3

N-channel 55V - 6.5mΩ - 80A - DPAK
STripFET™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STD65N55F3	55V	<8.5mΩ	80A	110W

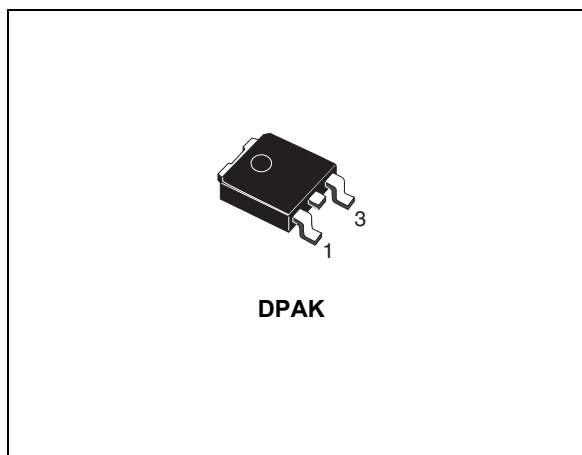
- Standard threshold drive
- 100% avalanche tested

Description

This n-channel enhancement mode Power MOSFET is the latest refinement of STMicroelectronics' unique "Single Feature Size™" strip-based process, which has decreased the critical alignment steps, offering remarkable manufacturing reproducibility. The outcome is a transistor with extremely high packing density for low onresistance, rugged avalanche characteristics and low gate charge.

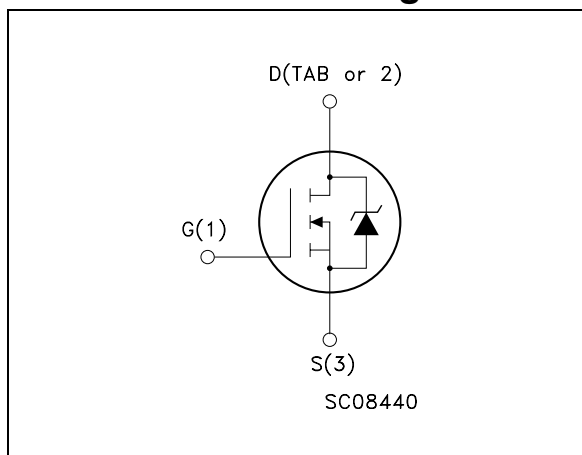
Applications

- Switching application
 - Automotive



DPAK

Internal schematic diagram



Order code

Part number	Marking	Package	Packaging
STD65N55F3	65N55F3	DPAK	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS}=0$)	55	V
V_{GS}	Gate-Source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	80	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	56	A
$I_{DM}^{(1)}$	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	110	W
	Derating factor	0.73	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	11	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	390	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 65\text{A}$, $di/dt \leq 300\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{jmax}$
3. Starting $T_j = 25^\circ\text{C}$, $I_d = 32\text{A}$, $V_{dd} = 25\text{V}$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.36	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	50	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu.

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	$I_D = 250\mu A, V_{GS} = 0$	55			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating}, T_c = 125^{\circ}C$			10 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 200	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 32A$		6.5	8.5	m Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 25V, I_D = 32A$		50		S
C_{iss}	Input capacitance	$V_{DS} = 25V, f = 1MHz, V_{GS} = 0$		2200		pF
C_{oss}	Output capacitance			500		pF
C_{rss}	Reverse transfer capacitance			25		pF
Q_g	Total gate charge	$V_{DD} = 27V, I_D = 65A$		33.5	45	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10V$		12.5		nC
Q_{gd}	Gate-drain charge	(see Figure 15)		9.5		nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 5. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=27V$, $I_D=32A$, $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 14)		20 50		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=27V$, $I_D=32A$, $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 14)		35 11.5		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				80	A
I_{SDM}	Source-drain current (pulsed) ⁽¹⁾				320	A
V_{SD}	Forward on voltage	$I_{SD}=65A$, $V_{GS}=0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD}=65A$, $di/dt=100A/\mu s$, $V_{DD}=25V$, $T_j=150^\circ C$		47		ns
Q_{rr}	Reverse recovery charge	(see Figure 16)		87		nC
I_{RRM}	Reverse recovery current			3.7		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

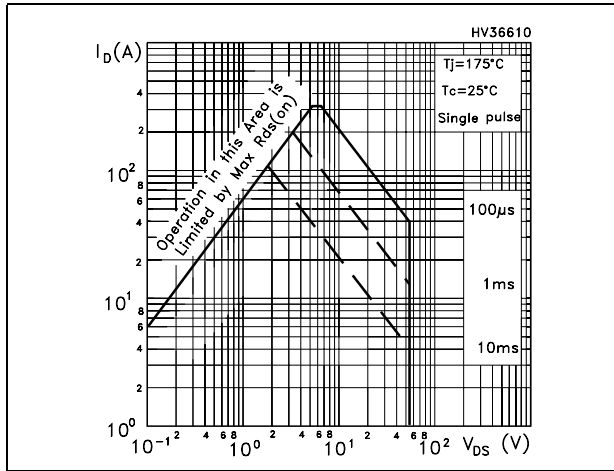


Figure 2. Thermal impedance

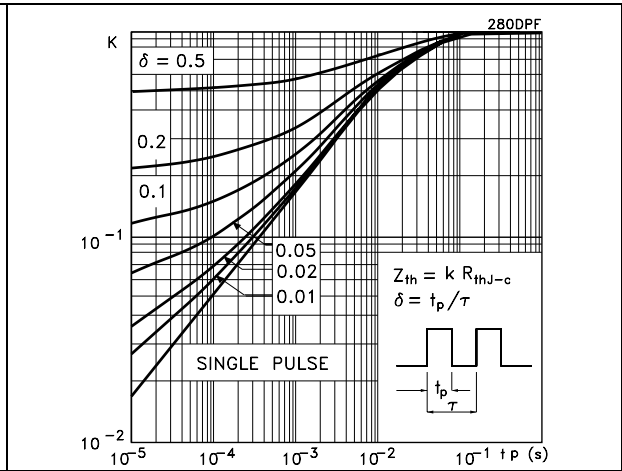


Figure 3. Output characteristics

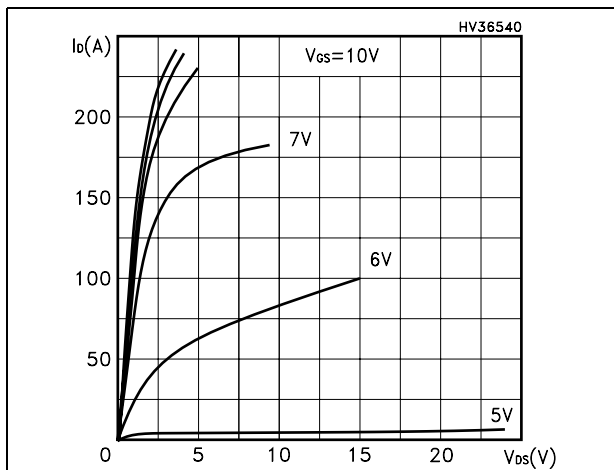


Figure 4. Transfer characteristics

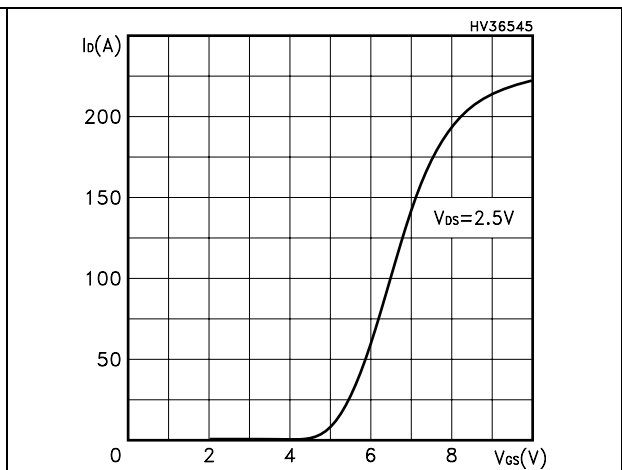


Figure 5. Normalized BV_{DSS} vs temperature

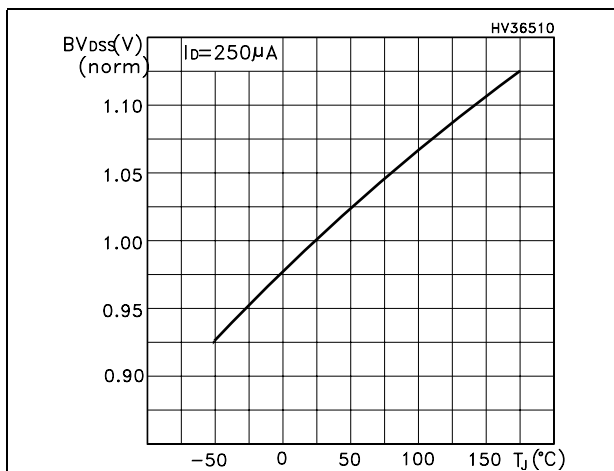


Figure 6. Static drain-source on resistance

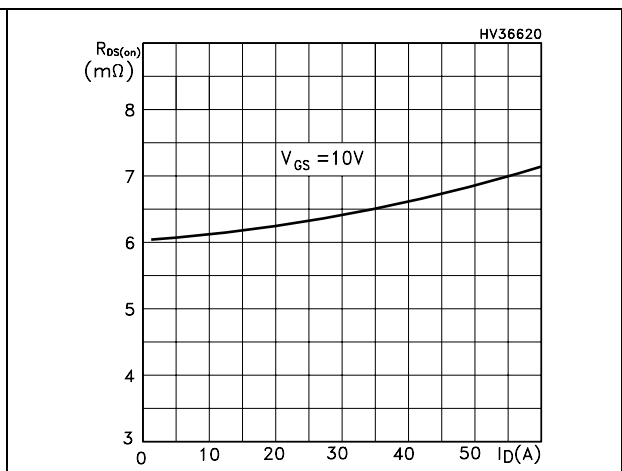


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

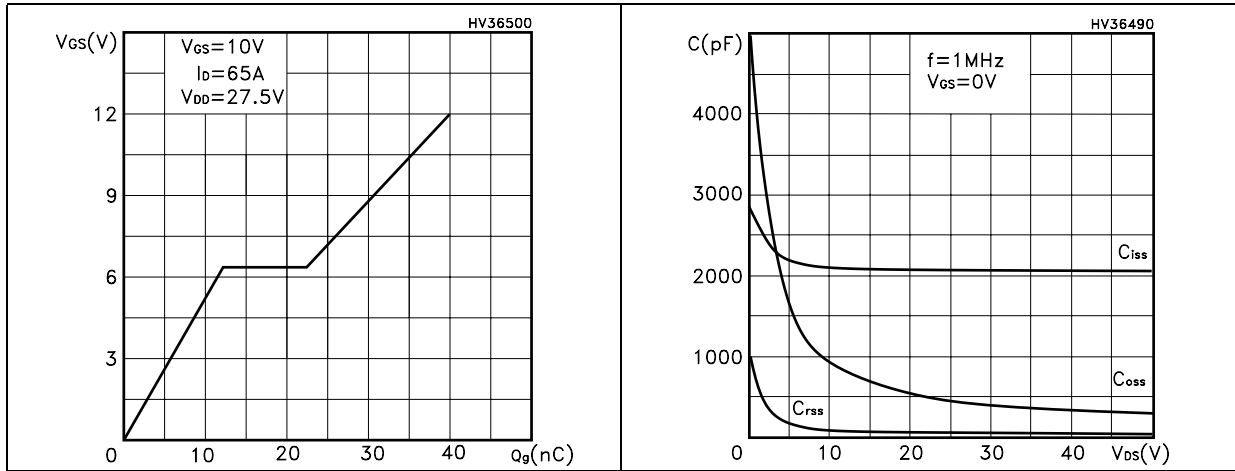


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

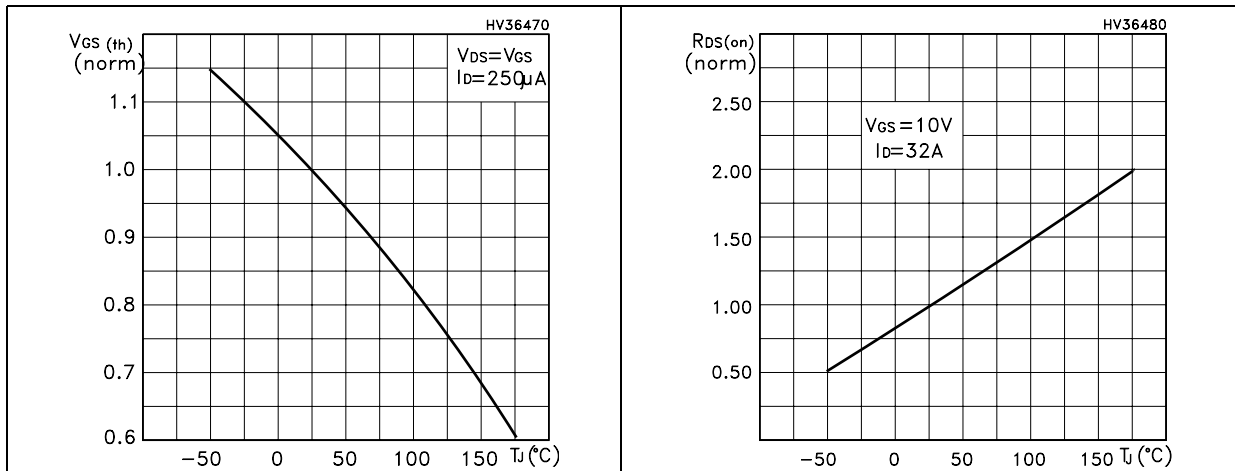
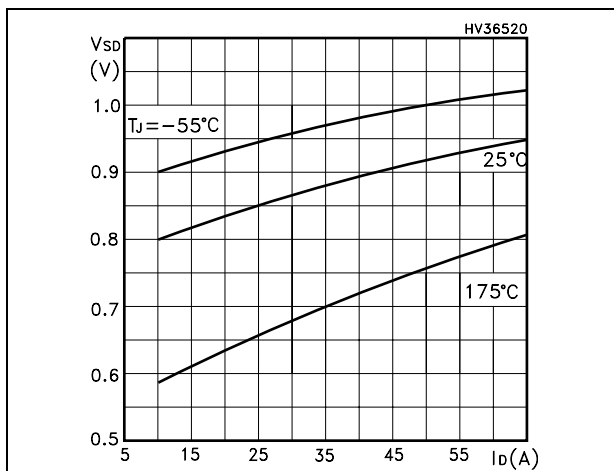


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Unclamped inductive load test circuit

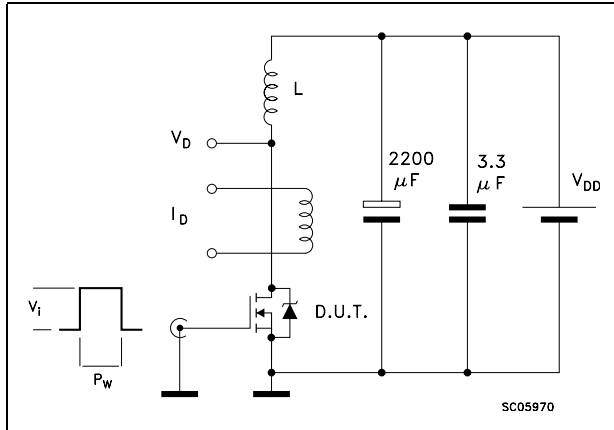


Figure 13. Unclamped inductive waveform

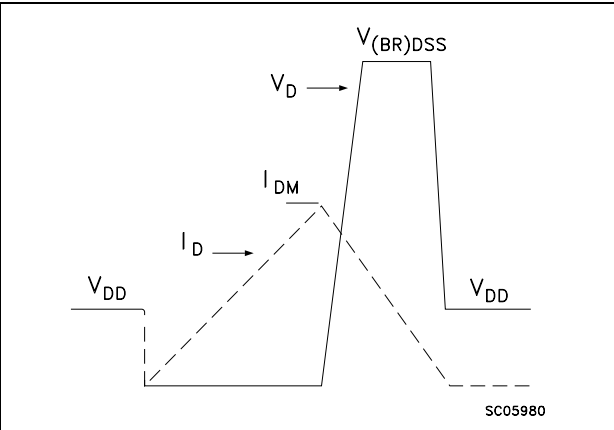


Figure 14. Switching times test circuit for resistive load

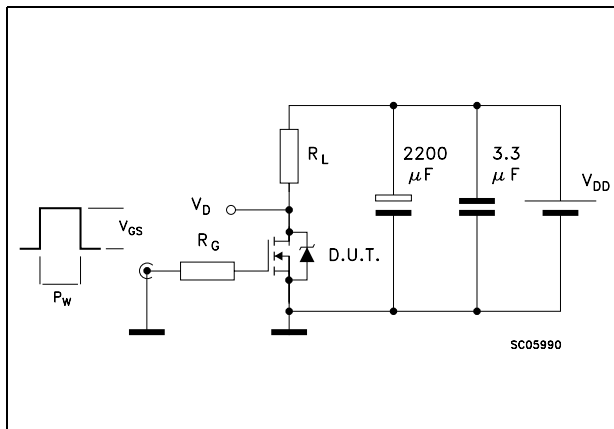


Figure 15. Gate charge test circuit

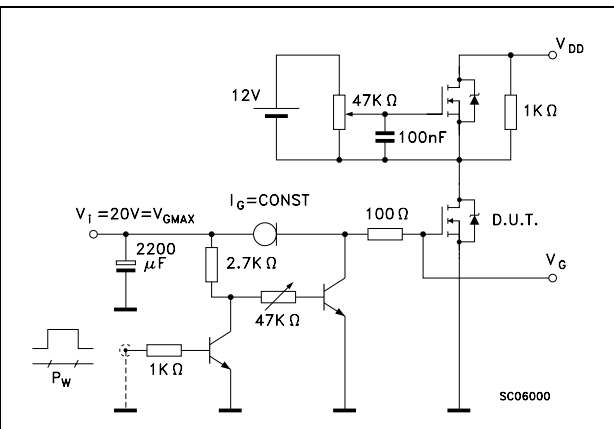


Figure 16. Test circuit for inductive load switching and diode recovery times

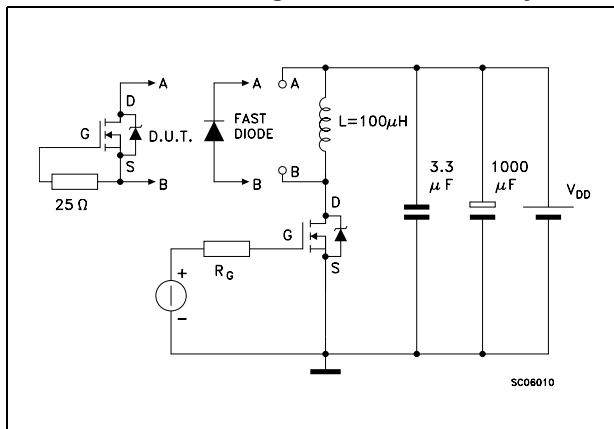
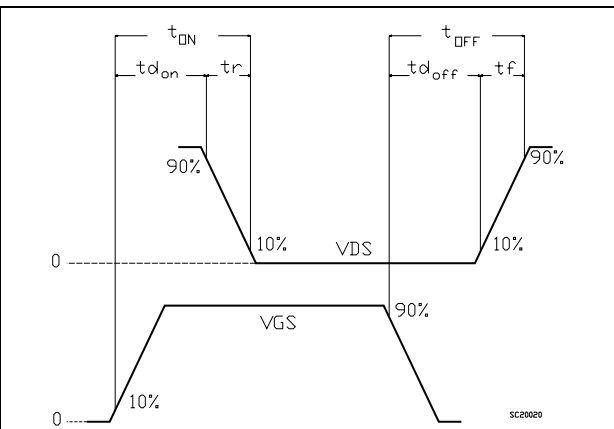


Figure 17. Switching time waveform

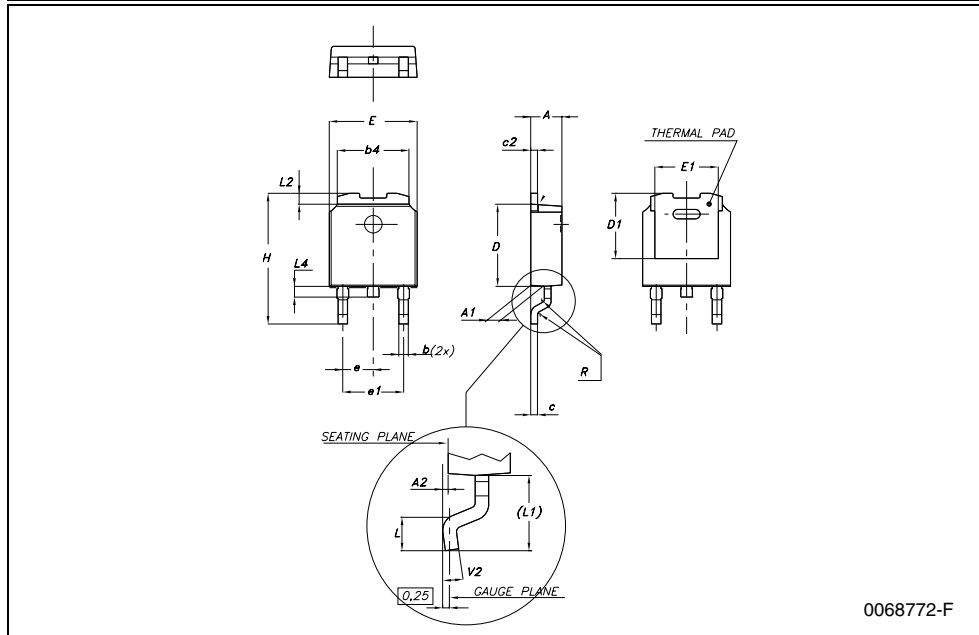


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

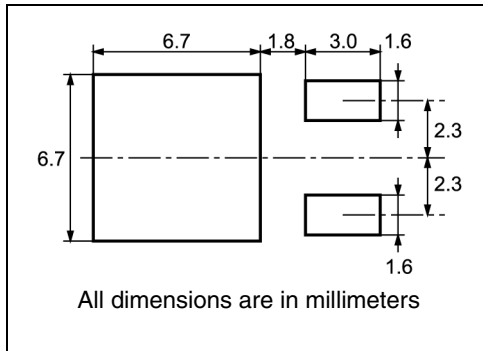
DPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

TOP COVER TAPE

User Direction of Feed

Center line of cavity

Bending radius R min.

FEED DIRECTION

For machine ref. only including draft and radii concentric around B0

10 pitches cumulative tolerance on tape +/- 0.2 mm

6 Revision history

Table 7. Revision history

Date	Revision	Changes
08-Feb-2007	1	First release
22-Feb-2007	2	Description has been changed
11-May-2007	3	Improved current values

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