FAIRCHILD SEMICONDUCTOR TM

June 1999

FDT439N

N-Channel 2.5V Specified Enhancement Mode Field Effect Transistor

General Description

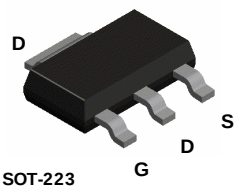
This N-Channel Enhancement mode field effect transistor is produced using Fairchild Semiconductor's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, and provide superior switching performance. These products are well suited to low voltage, low current applications such as notebook computer power management, battery powered circuits, and DC motor control.

Features

- 6.3 A, 30 V. $R_{DS(on)}$ = 0.045 Ω @ V_{GS} = 4.5 V
  $R_{DS(on)}$ = 0.058 Ω @ V_{GS} = 2.5 V
- Fast switching speed.
- High power and current handling capabitlity in a widely used surface mount package.

Applications

- DC/DC converter
- Load switch
- Motor driving



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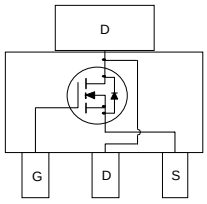

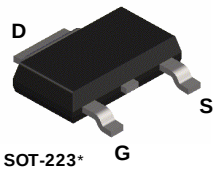

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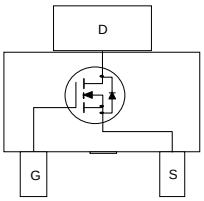


Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		FDT439N	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±8	V
I_D	Drain Current - Continuous	(Note 1a)	6.3	A
	- Pulsed		20	
P_D	Power Dissipation for Single Operation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J, T_{stg}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDT439N	FDT439N	13''	12mm	2500 units

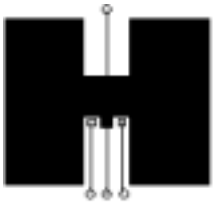
Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		40		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.4	0.67	1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		-2.2		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 6.3 A V_{GS} = 4.5 V, I_D = 6.3 A, T_J=125°C V_{GS} = 2.5 V, I_D = 5.5A		0.038 0.055 0.048	0.045 0.072 0.058	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	10			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 6.3 A		17		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		500		pF
C_{oss}	Output Capacitance			185		pF
C_{rss}	Reverse Transfer Capacitance			43		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		6	12	ns
t_r	Turn-On Rise Time			10	18	ns
$t_{d(off)}$	Turn-Off Delay Time			30	48	ns
t_f	Turn-Off Fall Time			10	18	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 6.3 A, V_{GS} = 4.5 V,		10.7	15	nC
Q_{gs}	Gate-Source Charge			0.9		nC
Q_{gd}	Gate-Drain Charge			3.7		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.5 A (Note 2)		0.8	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 42° C/W when mounted on a 1 in² pad of 2 oz. copper.

b) 95° C/W when mounted on a 0.066 in² pad of 2 oz. copper.

c) 110° C/W when mounted on a minimum mounting pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

Typical Characteristics

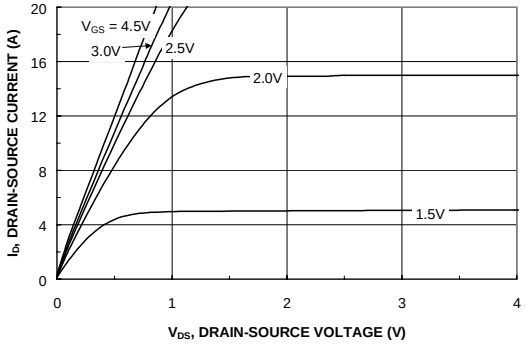


Figure 1. On-Region Characteristics.

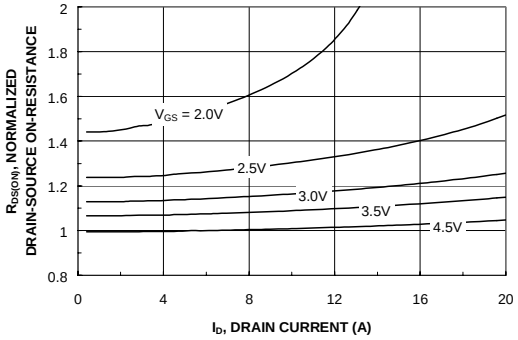


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

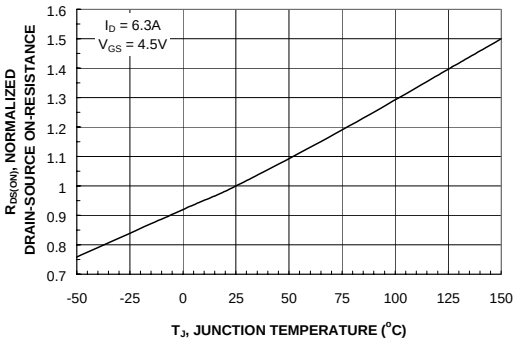


Figure 3. On-Resistance Variation with Temperature.

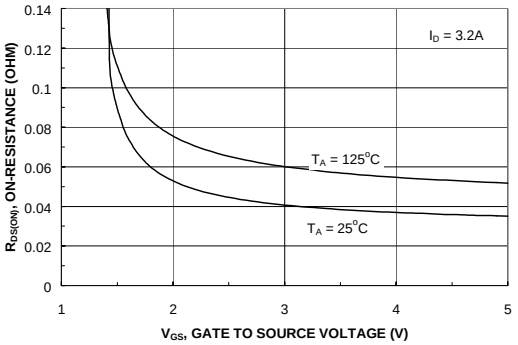


Figure 4. On-Resistance Variation with Gate-To-Source Voltage.

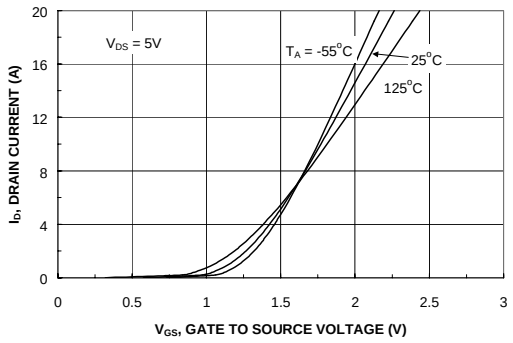


Figure 5. Transfer Characteristics.

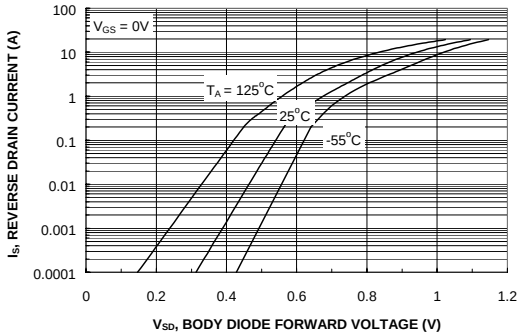


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

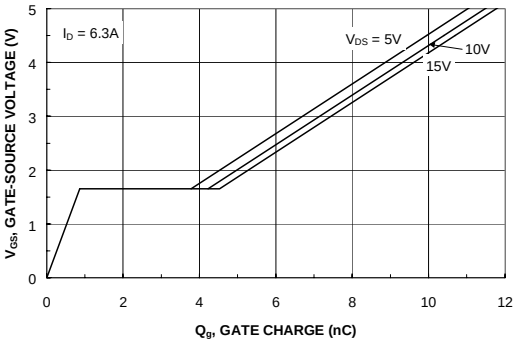


Figure 7. Gate-Charge Characteristics.

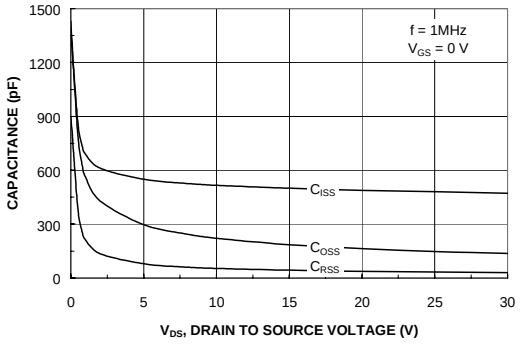


Figure 8. Capacitance Characteristics.

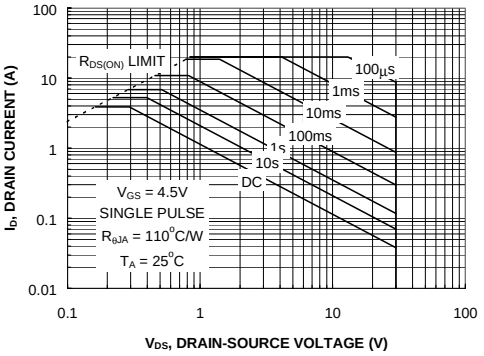


Figure 9. Maximum Safe Operating Area.

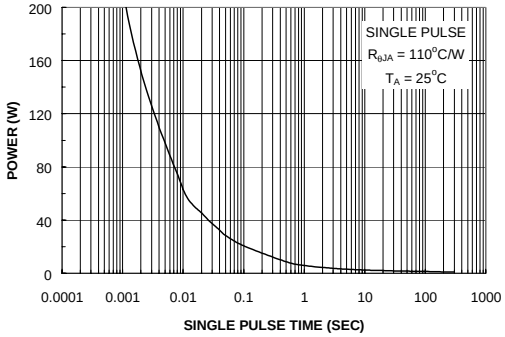


Figure 10. Single Pulse Maximum Power Dissipation.

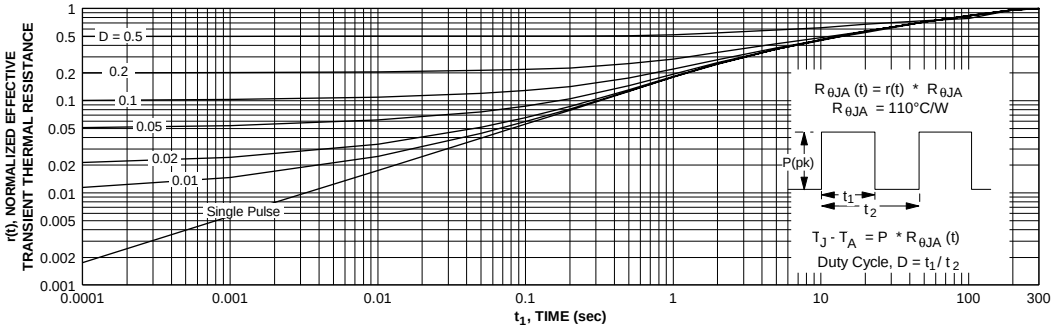


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1.
Transient themal response will change depending on the circuit board design.

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