FPF2283CUCX

28 V / 7 A Rated OVP with Ultra Low On-resistance Switch and Moisture Detection

ON Semiconductor®

Description

FPF2283C is a super OVP with ultra low on−resistance single channel switch controlled by external logic pin or I^2C interface. The device contains an N−MOSFET that can operate over an input voltage range of 2.8 V to 28 V and can support a maximum continuous current of 10 A.

When the input voltage exceeds the over−voltage threshold, the internal FET is turned off immediately to prevent damage to the protected downstream components. When in detection mode, the internal current source and ADC can be used to calculate the resistance on VIN for moisture detection.

FPF2283CUCX is available in a small 20 bumps WLCSP package and operate over the free−air temperature range of −40°C to +85°C.

Features

- Over−voltage Protection Up to +28 V
- Internal Low $R_{DS(on)}$ NMOS Transistors: Typical 7.5 mΩ
- Programmable Over−voltage Lockout (OVLO)
  - ♦ Externally Adjustable via ADJ Pin
  - ♦ Programmable via I^2C Interface
- Active−low Enable Pin for Device
- Super Fast OVLO Response Time: Typical 50 ns
- I^2C Communication with System
- 8−bits ADC for Moisture Detection on VIN
- Short Circuit Protection and Auto−restart
- Over Temperature Protection (Thermal Shutdown)
- +40 V Surge Capability Base on IEC61000−4−5
- System Level ESD Base on IEC61000−4−2
  - ♦ 8 kV Contact Discharge
  - ♦ 15 kV Air Gap Discharge
- Robust ESD Performance
  - ♦ 3.5 kV Human Body Model (HBM)
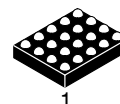 - ♦ 1 kV Charged Device Model (CDM)
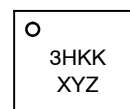
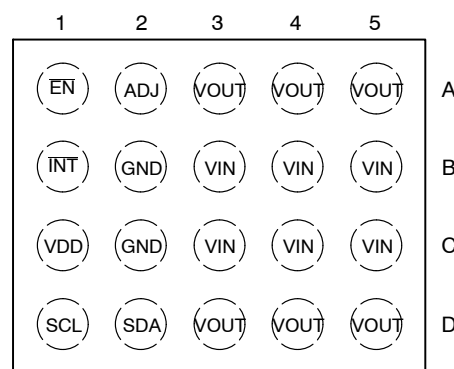## Typical Applications

- Mobile Phones
- PDAs
- GPS

WLCSP20
CU SUFFIX
CASE 567UT

MARKING DIAGRAM

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  ○
    3HKK
    XYZ
```

3H	= Specific Device Code
KK	= 2−digit Lot Run Code
XY	= 2−digit Date Code
Z	= 1−digit Plant Code

PIN CONNECTIONS

	1	2	3	4	5	
A	EN	ADJ	VOUT	VOUT	VOUT	
B	INT	GND	VIN	VIN	VIN	
C	VDD	GND	VIN	VIN	VIN	
D	SCL	SDA	VOUT	VOUT	VOUT	

(Top View)

ORDERING INFORMATION

Device	Package	Shipping[†]
FPF2283CUCX	WLCSP20	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
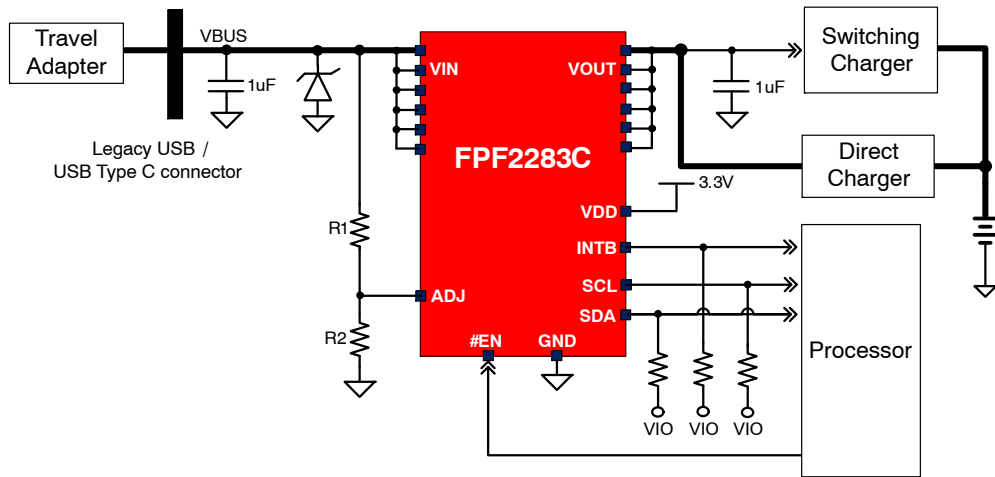
FPF2283CUCX

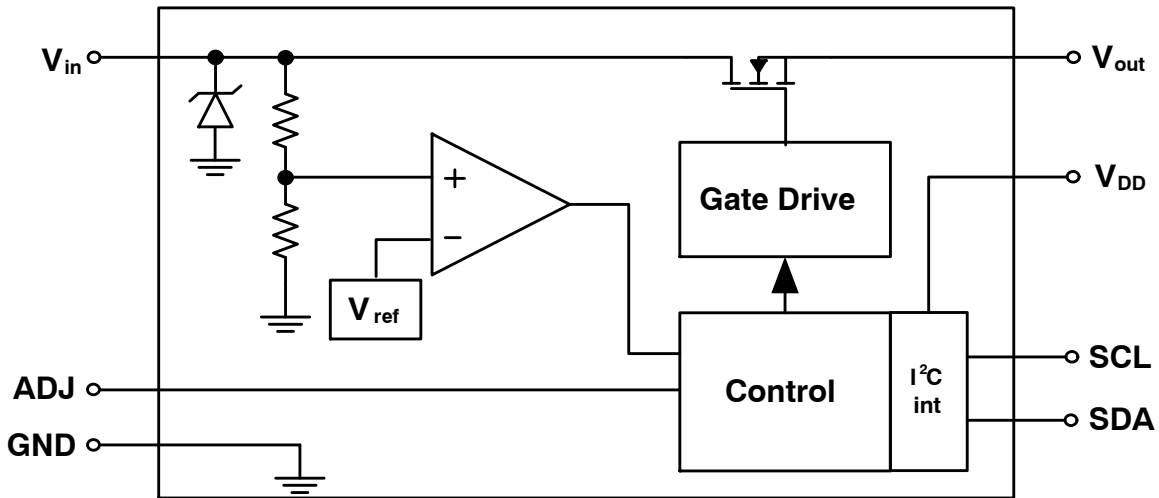Figure 1. Application Schematic – Adjustable Option

Figure 2. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin #	Name	Description
B3, B4, B5, C3, C4, C5	IN	Power Input: Switch Input and Device Supply
A3, A4, A5, D3, D4, D5	OUT	Power Output: Switch Output to Load
B1	INTB	Interrupt: Open−drain output. Pull down to ground when any FLAG register alarms.
A1	ENB	Enable Input: Active LOW.
A2	ADJ	OVLO Input: Over Voltage Lockout Adjustment Input
C1	VDD	Power supply: Supply for ADC and I^{2}C communication during communication
D1	SCL	Serial Clock Input: Be used to synchronize data movement on the I2C serial interface
D2	SDA	Serial Data Input/Output: Input / Output pin for the 2−wire serial interface. Open−drain output and requires an external pull−up resistor.
B2, C2	GND	Ground

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range (Note 1)	V_{in}	−0.3 to 28	V
Output Voltage Range	V_{out}	−0.3 to (V_{in} + 0.3)	V
I/O pin voltage Range	ENB, INTB, SCL, SDA	−0.3 to 6	V
VDD Voltage Range	V_{DD}	−0.3 to 6	V
Adjustable Input Range	ADJ	−0.3 to 28	V
Internal FET continuous current	I_{OUT}	0 to 10	A
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	TSTG	−65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESDHBM	3.5	kV
ESD Capability, Charge Device Model (Note 2)	ESDCDM	1	
IEC 61000−4−2 SYSTEM Level ESD	Contact	8	
	Air Gap	15	
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C
Moisture Sensitivity	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series incorporates ESD protection and is tested by the following methods:
    ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
    ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
    Latch−up Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WLCSP−20 (Note 4) Thermal Resistance, Junction−to−Air (Note 5)	$R_{\theta JA}$	36.5	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
5. Values based on 2S2P JEDEC std. PCB.

Table 4. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Supply Voltage on VIN	V_{in}	2.8	23	V
Supply Voltage on VDD	V_{DD}	3.0	5.5	V
I²C interface	SDA, SCL	1.5	5.5	V
I/O pins	ADJ, INTB, ENB	0	5.5	V
Output Current	I_{out}	0	7	A
VIN Capacitor	C_{in}	0.1		μF
VOUT Capacitor	C_{out}	0.1		μF
Ambient Temperature	T_A	−40	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

#FPF2283CUCX

Table 5. ELECTRICAL CHARACTERISTICS

V_{in} = 2.5 to 23 V, C_{in} = 0.1 μF, C_{out} = 0.1 μF, T_A = −40 to 85°C; For typical values V_{in} = 5.0 V, $I_{in} \le$ 3 A, C_{in} = 0.1 μF, T_A = 25°C, for min/max values T_A = −40°C to 85°C; unless otherwise noted. (Note 6)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
LEAKAGE AND QUIESCENT CURRENTS						
Input Quiescent Current on VIN	V_{IN} = 5 V, ENB = 0 V, 0x01 = 8'h00	I_Q		100		μA
	V_{IN} = 20 V, ENB = 0 V, 0x01 = 8'h00			150		
Input Quiescent Current on VDD	V_{DD} = 3.3 V, ENB = 0 V, 0x01 = 8'hC0, 0x06 = 8'h00, 0x07 = 8'h00 (detection mode, 0 A, single pulse)				100	
	V_{DD} = 3.3 V, ENB = 0 V, VIN = 0V, 0x01 = 8'h00 (charging mode)				30	
VDD Current consumption of ADC	VDD = 3.3 V, ENB = 0 V, 0x01 = 8'hC0, 0x06 = 8'h00, 0x07 = 8'hF0	I_{ADC}			1	mA
Device shutdown current	VIN = 5 V, ENB = 3.3 V, VOUT = 0 V	I_{SHDN}		5	10	μA
ADJ Input Leakage Current	$V_{ADJ} = V_{OVLO\_TH}$	I_{ADJ}	−100		100	nA
INTB and SDA Output leakage	V_{PULL_UP} = 3 V, Interrupt De−asserted	I_{LEAK}			0.5	μA
OVER VOLTAGE AND UNDER VOLTAGE LOCKOUT						
Under−Voltage Rising Trip Level for VIN	V_{IN} rising, T_A = −40 to 85°C	$V_{IN\_UV\_R}$	2.47	2.6	2.8	V
Under−Voltage Falling Trip Level for VIN	V_{IN} falling, T_A = −40 to 85°C	$V_{IN\_UV\_F}$		2.5		V
Under−Voltage Falling Trip Level for VDD	V_{DD} falling, T_A = −40 to 85°C	$V_{DD\_UV\_F}$	2.6	2.8	3.0	V
UVLO Hysteresis for VDD		V_{HYS_VDD}		100		mV
Default Over−Voltage Trip Level	V_{IN} rising, T_A = −40 to 85°C, refer to register table for other value set by I2C	V_{IN_OVLO}	6.6	6.8	7.0	V
OVLO set threshold	V_{ADJ} = 1.1 V to 1.3 V, the voltage of ADJ to trigger OVLO	V_{OVLO_TH}	1.18	1.204	1.22	V
OVLO threshold hysteresis		V_{HYS_OVLO}		2		%
Adjustable OVLO range	OV_MODE = 0, V_{ADJ} > 0.5 V	V_{OV_RNG}	4		23	V
I/O THRESHOLDS						
SCL, SDA and ENB Threshold Voltage						V
Voltage Increasing, Logic High	High	V_{IH}	1.2			
Voltage Decreasing, Logic Low	Low	V_{IL}			0.4	
ADJ Input Threshold Voltage						V
Voltage Increasing, Logic High	High	V_{IH_ADJ}	0.3			
Voltage Decreasing, Logic Low	Low	V_{IL_ADJ}			0.15	
INTB and SDA Output Low Voltage (Note 8)	I_{OUT} = 1 mA, logic Low asserted	V_{OL}			0.4	V
RESISTANCE						
On−resistance of Power FET	V_{IN} = 5 V, I_{OUT} = 500 mA, T_A = 25°C	r_{ON}		7.5		mΩ
Pull−down resistor on ENB		r_{PD}		1000		kΩ
MOISTURE DETECTION						
Current Source for Moisture Detection	Set by register: 04h	I_{SRC}	0.001		10	mA
Settle time for I_{SRC} and ADC (Note 8)		t_{SET}			60	μs
Resolution of ADC		RES	8			Bits
ADC Full Scale Voltage Range	Powered by V_{DD}; $V_{DD} \ge$ 2.1 V	V_{FSV}	0		2.04	V
LSB Voltage of ADC		V_{LSB}		8		mV

6. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
7. Refer to the APPLICATION INFORMATION section.
8. Values based on design and/or characterization.
9. Depends on the capacitance on ADJ pin.

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Table 5. ELECTRICAL CHARACTERISTICS V_{in} = 2.5 to 23 V, C_{in} = 0.1 μF, C_{out} = 0.1 μF, T_A = −40 to 85°C; For typical values
V_{in} = 5.0 V, $I_{in} \leq$ 3 A, C_{in} = 0.1 μF, T_A = 25°C, for min/max values T_A = −40°C to 85°C; unless otherwise noted. (Note 6)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
I²C INTERFACE						
SCL clock frequency	Stand Mode	f_{SCL}		100		kHz
	Fast Mode			400		kHz
	Fast Mode Plus			1000		kHz
Bus Free Time Between STOP and START conditions (Note 8)	Stand Mode	t_{BUF}		4.7		μs
	Fast Mode			1.3		μs
	Fast Mode Plus			0.5		μs
START or Repeated START Hold Time (Note 8)	Stand Mode	$t_{HD;STA}$		4		μs
	Fast Mode			0.6		μs
	Fast Mode Plus			0.26		μs
LOW Period of SCL Clock (Note 8)	Stand Mode	t_{LOW}		4.7		μs
	Fast Mode			1.3		μs
	Fast Mode Plus			0.5		μs
HIGH Period of SCL Clock (Note 8)	Stand Mode	t_{HIGH}		4		μs
	Fast Mode			0.6		μs
	Fast Mode Plus			0.26		μs
Repeated START Setup Time (Note 8)	Stand Mode	$t_{SU;STA}$		4.7		μs
	Fast Mode			0.6		μs
	Fast Mode Plus			0.26		μs
Stop Condition Setup Time (Note 8)	Stand Mode	$t_{SU;STO}$		4		μs
	Fast Mode			0.6		μs
	Fast Mode Plus			0.26		μs
Data Setup Time (Note 8)	Stand Mode	$t_{SU;DAT}$		250		ns
	Fast Mode			100		ns
	Fast Mode Plus			50		ns
Data Hold Time (Note 8)	Stand Mode	$t_{HD;DAT}$	0		3.45	μs
	Fast Mode		0		0.9	μs
	Fast Mode Plus		0		0.45	μs
SCL Rising Time (Note 8)	Stand Mode	t_{RCL}	$20+0.1C_b$		1000	ns
	Fast Mode		$20+0.1C_b$		300	ns
	Fast Mode Plus		$20+0.1C_b$		120	ns
SDA Rising Time (Note 8)	Stand Mode	t_{RDA}	$20+0.1C_b$		1000	ns
	Fast Mode		$20+0.1C_b$		300	ns
	Fast Mode Plus		$20+0.1C_b$		120	ns
SDA Falling Time (Note 8)	Stand Mode	t_{FDA}	$20+0.1C_b$		300	ns
	Fast Mode		$20+0.1C_b$		300	ns
	Fast Mode Plus		$20+0.1C_b$		120	ns
Capacitive Load for SDA and SCL		C_b			400	pF

6. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
7. Refer to the APPLICATION INFORMATION section.
8. Values based on design and/or characterization.
9. Depends on the capacitance on ADJ pin.

Table 5. ELECTRICAL CHARACTERISTICS V_{in} = 2.5 to 23 V, C_{in} = 0.1 μF, C_{out} = 0.1 μF, T_A = −40 to 85°C; For typical values V_{in} = 5.0 V, $I_{in} \le$ 3 A, C_{in} = 0.1 μF, T_A = 25°C, for min/max values T_A = −40°C to 85°C; unless otherwise noted. (Note 6)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
I²C INTERFACE						
Pulse width of spikes which must be sup-pressed by input filter (Note 8)		t_{SP}	0		50	ns
Slave Address	Read			1101100		
	Write					
TIMING						
Hard−short protection auto−restart time	Time from power switch turned off to being turned on	t_{HS_RST}		200		ms
Interrupt maximum duration		t_{INTB}		1000		ms
De−bounce Time of Power FET turned on	Time from 2.5 V < V_{IN} < V_{IN_OVLO} to V_{OUT} = 0.1 x V_{IN}	t_{SW_DEB}		22		ms
Soft−Start Time (Note 8)	Time from de−bounce time finished to Power Switch fully turn on	t_{SS}		15		ms
Switch Turn−On rising Time (Note 8)	V_{IN} = 5 V, R_L = 100 Ω, C_L = 22 μF, V_{OUT} from 0.1 x V_{IN} to 0.9 x V_{IN}	t_R		2		ms
Switch Turn−Off Time (Note 8)	R_L = 10 Ω, C_L = 0 μF, time from V_{IN} > V_{OVLO} to V_{OUT} = 0.9 x V_{IN}					
	Internal OVP level			50		ns
	External OVP level (Note 9)			100		ns
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 8)		T_{SD}	–	130	–	°C
Thermal Shutdown Hysteresis (Note 8)		T_{SH}	–	20	–	°C

6. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
7. Refer to the APPLICATION INFORMATION section.
8. Values based on design and/or characterization.
9. Depends on the capacitance on ADJ pin.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
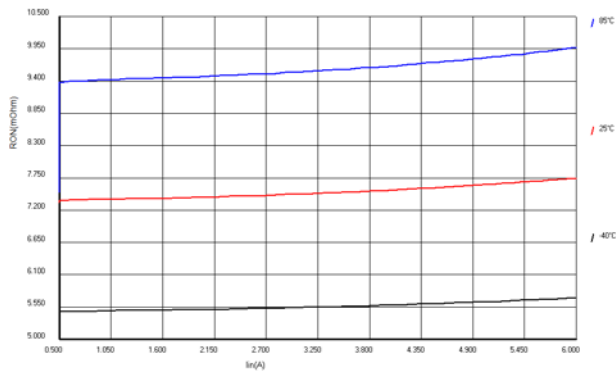
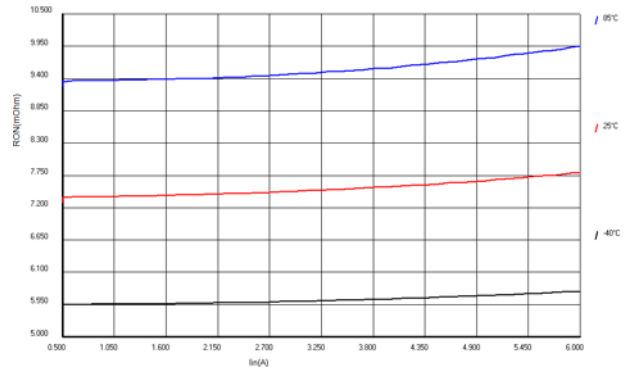# TYPICAL CHARACTERISTICS

Figure 3. ON−resistance @ VIN = 5 V
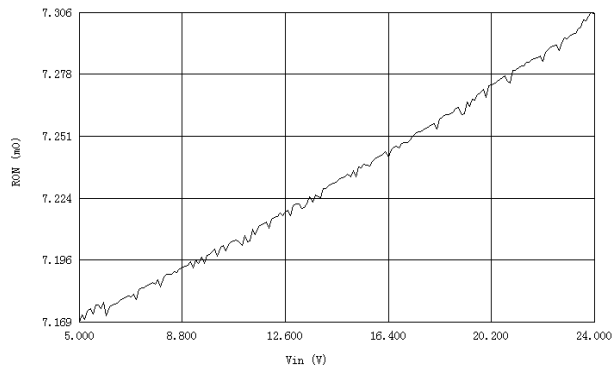

Figure 4. ON−resistance @ VIN = 23 V

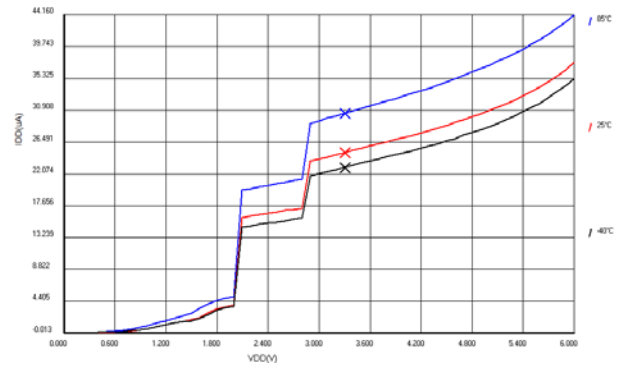**Figure 5. ON−resistance vs. Input Voltage**

Figure 6. Quiescent Current vs. Input Voltage

Function Description

General

FPF2283CUCX is an OVP power switch to protect next stage system which is optimized to lower voltage working condition. The device includes ultra low on−resistance power FET (7 mΩ) and super fast OVP response time (50 ns).

The device integrates moisture detection function to detect the resistance on VIN side. The communication with processor can be done via I^{2}C interface.

Power MOSFET

The FPF2283CUCX integrates an N−type MOSFET with 8 mΩ resistance. The power FET can work under 2.8 V ~ 23 V and up to 7 A DC current capability.

Power Supply

The FPF2283CUCX is supplied by both VIN and VDD. When both VDD and VIN drop below threshold, the entire chip will stop working. When only VDD drops, detection mode will not be working anymore.

Enable Control

The ENB pin is active low control of FPF2283CUCX with 1 MΩ pull down resistor. When ENB is tight to ground or floating, the device is alive and ready to be configured by internal registers. When ENB is HIGH, the device will be turned off entirely including the power switch.

Under Voltage Lockout

FPF2283CUCX power switch will be turned off when the voltage on VIN is lower than the UVLO threshold $V_{IN\_UV\_F}$.

Whenever VIN voltage ramps up to higher than $V_{IN\_UV\_R}$, the register 0x01 will be reset to default value and the power FET will be turned on automatically after t_{DEB} de−bounce time if there is no OV or OT condition.

Over Voltage Lockout

The power FET will be turned off whenever VIN voltage higher than V_{IN_OVLO}. The value of V_{IN_OVLO} can be set by external resistor ladder or by internal registers via I^{2}C communication.

When $V_{ADJ} \leq 0.15$ V or OV_MODE = 1, V_{OVLO} is decided by internal registers. When $V_{ADJ} > 0.3$ V and OV_MODE = 0, the power switch will be turned off once $V_{ADJ} > V_{OVLO\_TH}$. The external resistor ladder can be decided according to the following equation:

$$V_{IN\_OVLO} = V_{OVLO\_TH} \times \left(1 + \frac{R1}{R2}\right) \qquad \text{(eq. 1)}$$

where R1 and R2 are the resistors in Figure 1.

INTB will be triggered to ground when OV event appears. At the meantime, OV_FLG will be set to 1 and latched.

Hard Short Protection

When the VOUT is short to ground, the power switch will be turned off to protect the system and power supply. If hard−short condition keeps, the switch will be turned off and re−try again after t_{HS_RST}.

Thermal Shutdown

When the device is in the switch mode, to protect the device from over temperature, the power switch will be turned off when the junction temperature exceeds T_{SD}. INTB will be triggered to ground. At the meantime, OT_FLG will be set to 1 and latched. The switch will be turned on again when temperature drop below $T_{SD} - T_{SH}$.

Interrupt

The processor recognizes interrupt signals by observing the INTB signal of FPF2283CUCX, which is active LOW and open−drain. Interrupts are masked during VIN or VDD power up. The INTB pin is default floating in preparation for an interrupt.

By default, when the following event occurs, INTB transitions LOW: Over Voltage Lockout, Over Current Protection, Over Temperature Protection, Over TAG of VIN, Detection Timeout, Power Switch turned on, Power applied on VIN.

When the following event occurs, INTB transitions HIGH: Read clear, Interrupt time−out, t_{DET} start, Power down, Hardware disable; ENB pin is pulled.

Moisture detection

FPF2283CUCX provide a Moisture Detection, or called resistance detection, feature to help the system detect any risk on VBUS. The detection can be setup via I^{2}C bus.

The Moisture Detection includes two parts:
  1. A programmable current source which will be applied to VIN;
  2. An 8−bits ADC to detect the voltage on VIN.

While the voltage value is read via I^{2}C, resistance between VIN and GND can be calculated through the formula:

$$R_{VIN} = \frac{V_{VIN}}{I_{SRC}} \qquad \text{(eq. 2)}$$

Where V_{VIN} is a value can be looked up from the value of register 0x08.

The Moisture Detection will be implemented during t_{DET}. t_{DET} is only valid when all the following conditions met:
  1. The register DET_EN is set to 1'b1;
  2. The status is under detecting period according to t_{BLNK} and t_{DET} set by register 05h.

The moisture detection will only be available when external supply VDD is applied. The detection result can be used to decide if there is significant leakage on VBUS or other power line. The programmable current source is convenient for different measurement range and for different input capacitance.

The moisture detection function makes it possible for system to find out the abnormal condition on USB connector

before power source is applied. It provides a safer way than temperature detection to prevent huge leakage burning connector.

I²C interface

FPF2283CUCX allows I²C communication to program the registers. Registers will control the OVP, I_{SRC} and ADC for moisture detection. I²C communication is only valid when VDD supply is higher than 1.5 V. The I²C of

FPF2283CUCX has 3 modes for different speed. Different speed has different power consumption level.

The device has its slave address for I²C communication with fixed length of 7−bits (7'b1101100).

Register Mapping

There are registers integrated in FPF2283CUCX. The registers can be used to control the device or get the status information. Register table is followed:

Address	Description	Default Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x00	ID Register		0	0	0	0	1	0	0	1
0x01	Enable Register	00 h	SW_ENB	DET_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x02	Detection status Register	00 h	PON_STS	TAG_STS	TMO_STS	SW_STS	Reserved	Reserved	Reserved	Reserved
0x03	Switch Flag Register	00 h	Reserved	Reserved	Reserved	Reserved	Reserved	OV_FLG	HS_FLG	OT_FLG
0x04	Interrupt mask register	00 h	PON_MSK	TAG_MSK	TMO_MSK	SW_MSK	Reserved	OV_MSK	HS_MSK	OT_MSK
0x05	Working Mode	30 h	Reserved	RNG2	RNG1	RNG0	OV_MODE	Reserved	OV1	OV0
0x06	Isource to VIN	00 h	Reserved	Reserved	Reserved	Reserved	ISRC3	ISRC2	ISRC1	ISRC0
0x07	Isource Working Time	00 h	TDET3	TDET2	TDET1	TDET0	TBLK3	TBLK2	TBLK1	TBLK0
0x08	Voltage on VIN (0V~2.04V, 8mV LSB)	00 h	VIN7	VIN6	VIN5	VIN4	VIN3	VIN2	VIN1	VIN0
0x09	Set Tag of VIN	FF h	TH_VIN7	TH_VIN6	TH_VIN5	TH_VIN4	TH_VIN3	TH_VIN2	TH_VIN1	TH_VIN0

Identification Register
Address: 00h, Bit [7:0]
Type: Read Only
Description: Vendor ID and Revision ID

Bit Name	Bit #	Value	Description
VID	7:3	5'b00001	Vendor ID for customer recognition
RID	2:0	3'b001	Revision ID

Enable Register
Address: 01h, Bit [7:6]
Default Value: 2'b00
Type: Read / Write
Function: Control the working mode of FPF2283CUCX

Bit Name	Bit #	Value	Description
SW_ENB	7	0 (Default)	Written by processor via I²C or cleared during POR. Turned on the power switch if UV, OV, Hard Short, OT condition cleared and detection not being implemented.
		1	Written by processor via I²C. Power switch OFF.
DET_EN	6	0 (Default)	Written by processor via I²C or cleared during POR. Moisture Detection is not applied until the state of this bit changed. The detection related registers will not be reset.
		1	Written by processor via I²C. Moisture Detection turned on. If VIN voltage is lower than $V_{IN\_UVLO\_F}$, I_{SRC} and ADC will be applied on VIN in t_{DET}, which is defined by register 04h.

NOTE: The status 2'b01 is invalid. Any writing action 2'b01 to these two bits will be looked as invalid writing and not executed.

The register SW_ENB is an active−low control bit for the Switch Mode. Writing SW_ENB to 1 will turn off the power FET in any case, while writing it to 0 will switch the device into Switch Mode. In Switch Mode, the power FET will be turned on if no over stress condition is detected for at least t_{DEB}.

The register DET_EN is an active−high control bit for the Detection Mode. When DET_EN = 0, the moisture detection setup (including I_{SRC} and ADC) will not be implemented. When DET_EN = 1, the device will enter the detection mode. During Detection Mode, current source and ADC will work according to the setup in register 0x06 and 0x07.

Detection Status Register
Address: 02h, Bit [7:0]
Default Value: 3'b000
Type: Read

Bit Name	Bit #	Value	Description
PON_STS	7	0 (Default)	Initialed by POR or set by function defined. Indicate the condition that VIN is lower than $V_{IN\_UVLO\_F}$.
		1	Set by FPF2283CUCX. The voltage on VIN is higher than $V_{IN\_UVLO\_R}$ when ENB is low.
TAG_STS	6	0 (Default)	Initialed by POR or cleared when the value in register 08h is smaller than the value in 09h.
		1	Set by FPF2283CUCX. The value in register 08h is larger than the value in 09h.
TMO_STS	5	0 (Default)	Initialed by POR or cleared when t_{DET} begins. Refer to diagram.
		1	Set by FPF2283CUCX during t_{BLNK}. Refer to diagram.
SW_STS	4	0 (Default)	Initialed by POR or cleared when the power switch is turned off when ENB tight low.
		1	Set by FPF2283CUCX. The power switch is turned on when ENB tight low.

PON_STS is a register bit indicates the power on status. Unless ENB pin is pulled down to ground, a logical '0' means VIN voltage is lower than UVLO threshold, while a logical '1' means VIN voltage is higher than UVLO level. An interrupt will be sent out when VIN rises above UVLO level.

TAG_STS is a "target reached" indicate register for moisture Detection Mode. When the device is in this mode, it will monitor VIN voltage. Once VIN is higher than the threshold level (set by register 0x09) during Detection Mode, TAG_STS will be set to 1 and interrupt signal will be triggered via INTB pin.

TMO_STS is a status register for "time−out" situation. During Detection Mode, it will suggest if the device is in "detection" period or "blank" period. When it is in "detection" period, TMO_STS will be 0. When it is in "blank" period, TMO_STS will be 1. Every time the status is switched from "detection" period to "blank" period, interrupt signal will be sent our via INTB pin. Figure x is a reference timing diagram for that.
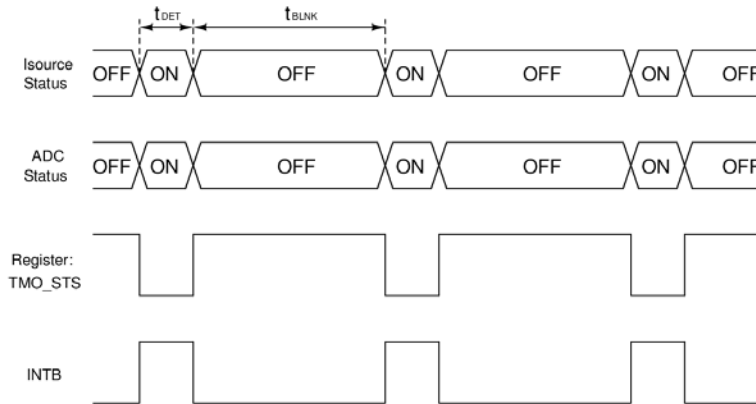
Figure 7. TMO_STS and Related Interrupt

SW_STS is a status register for power switch. It indicates if the power FET is on or off. When the FET is in conducting condition, SW_STS is 1. When the FET is in isolating condition, SW_STS is 0. Every time the power FET is turned on, interrupt signal will be triggered.

Power Switch FLAG Register
Address: 03h, Bit [2:0]
Default Value: 3'b000
Type: Read / Clear

Bit Name	Bit #	Value	Description
OV_FLG	2	0 (Default)	Initialed by POR. Be 0 as long as VIN is lower than V_{OVLO}.
		1	Set and latched by FPF2283CUCX when ENB is logical LOW and VIN is higher than V_{OVLO}.
HS_FLG	1	0 (Default)	Initialed by POR. Be 0 as long as VOUT is high enough.
		1	Set and latched by FPF2283CUCX and kept until this byte been read.
OT_FLG	0	0 (Default)	Initialed by POR. Be 0 as long as the junction temperature is lower than T_{SDN}.
		1	Set and latched by FPF2283CUCX when the junction temperature is higher than T_{SDN}.

OV_FLAG is a flag indicator for over voltage protection. When the device is in Switch Mode, SW_ENB = 0, power switch will be turned off and OV_FLG will be latched to 1 when VIN > V_{OVLO}. Interrupt will also be asserted in this case. V_{OVLO} is decided by the register byte 0x03 and external resistor ladder (Figure 1). The action of reading 0x02 will reset OV_FLG and INTB although they might be triggered again if VIN is still under over voltage stress.

HS_FLG is a flag indicator for hard short circuit protection. When the device is in Switch Mode, SW_ENB = 0, power switch will be turned off and HS_FLG will be latched to 1 and INTB will be asserted, when the VOUT encounters hard−short to ground. The action of reading 0x02 will reset HS_FLG and de−asserted INTB. However, the power switch will keep OFF for t_{HS_RST}. After t_{HS_RST}, the switch will be re−started again. If the short condition still exists, the device will be turned off again.

OT_FLG is a flag indicator for over temperature protection. When the device is in Switch Mode, SW_ENB = 0, power switch will be turned off and OT_FLG will be latched to 1 when the device junction temperature exceed T_{SDN}. The action of reading 0x02 will reset OT_FLG although it might be triggered to 1 again if the temperature is still high.
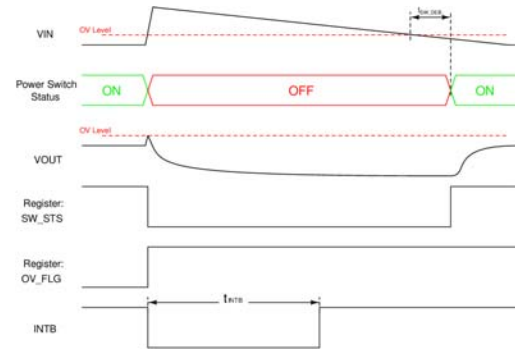
Figure 8. Timing for OVLO Trip Without
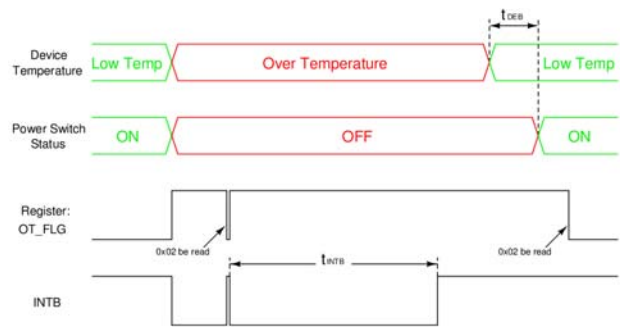
Figure 9. Timing for Power Switch Thermal Shutdown

Mask Register
Address: 04h, Bit [7:0]
Default Value: 8'h00
Type: Write / Read

Bit Name	Bit #	Value	Description
PON_MSK	7	0 (Default)	Initialed by POR or set by function defined. Interrupt responding to PON_STS is normal.
		1	Set by I^{2}C. The interrupt INTB will not be triggered because of PON_STS.
TAG_MSK	6	0 (Default)	Initialed by POR or set by function defined. Interrupt responding to TAG_STS is normal.
		1	Set by I^{2}C. The interrupt INTB will not be triggered because of TAG_STS.
TMO_MSK	5	0 (Default)	Initialed by POR or set by function defined. Interrupt responding to TMO_STS is normal.
		1	Set by I^{2}C. The interrupt INTB will not be triggered because of TMO_STS.
SW_MSK	4	0 (Default)	Initialed by POR or set by function defined. Interrupt responding to SW_STS is normal.
		1	Set by I^{2}C. The interrupt INTB will not be triggered because of SW_STS.
Reserved	3	0 (Default)	Do not use
OV_MSK	2	0 (Default)	Initialed by POR or set by function defined. Interrupt responding to OV_FLG is normal.
		1	Set by I^{2}C. The interrupt INTB will not be triggered because of OV_FLG.
HS_MSK	1	0 (Default)	Initialed by POR or set by function defined. Interrupt responding to HS_FLG is normal.
		1	Set by I^{2}C. The interrupt INTB will not be triggered because of HS_FLG.
OT_MSK	0	0 (Default)	Initialed by POR or set by function defined. Interrupt responding to OT_FLG is normal.
		1	Set by I^{2}C. The interrupt INTB will not be triggered because of OT_FLG.

The mask registers will control the interrupt assert behavior. By default, the 0x04 is all 0. If one bit of it is written to 1, the relevant STS bit or FLG bit will not trigger INTB when they flip to 1. For example, when SW_MSK=0, interrupt will be asserted if SW_STS turns from 0 to 1. However, if SW_MSK=1, interrupt will not be asserted by this process.

Register for OVP Internal Threshold

Address: 05h, Bit [1:0]

Default Value: 2'b00

Type: Read / Write

Function: Define the center of rising trigger level of OVP, see the description followed

OV [1:0]	Data	Internal OVP Threshold
Define the internal Over Voltage Lockout center value	2'b00	6.8 V
	2'b01	11.5 V
	2'b10	17.0 V
	2'b11	23.0 V

Register for OVP Internal Threshold Offset

Address: 05h, Bit [6:4]

Default Value: 3'b011

Type: Read / Write

Function: Define the offset of OVP from center value, see the description followed

RNG [6:4]	Data	Internal OVP offset
Define the OVP offset	3'b000	−600 mV
	3'b001	−400 mV
	3'b010	−200 mV
	3'b011	0 mV
	3'b100	200 mV
	3'b101	400 mV
	3'b110	600 mV
	3'b111	800 mV

When OV_MODE = 0 or V_{ADJ} < 0.15 V, the OVLO level will be decided by external resistor divider (Equation 1). When OV_MODE = 1, the OVLO level will be decided by register 0x05. [OV1:OV0] will decide the OVP level center value and RNG[6:4] will decide the offset value.

For example, when 0x06 = 8'h19 ([OV1:OV0] =2'b01, RNG[6:4]=3'b001, OV_MODE=1), the OVP level of VIN can be calculated as V_{OVLO} = 11.5 V − 0.4 V = 11.1 V.

Register for I$_{SRC}$ Current Value

Address: 06h, Bit [3:0]

Default Value: 4'b0000

Type: Read / Write

Function: Define current source amplitude

ISRC [3:0]	Data	I$_{SRC}$ Value
Define Source Current value	4'b0000	0 μA
	4'b0001	1 μA
	4'b0010	2 μA
	4'b0011	3 μA
	4'b0100	4 μA
	4'b0101	5 μA
	4'b0110	10 μA
	4'b0111	20 μA
	4'b1000	50 μA
	4'b1001	100 μA
	4'b1010	200 μA
	4'b1011	500 μA
	4'b1100	1 mA
	4'b1101	2 mA
	4'b1110	5 mA
	4'b1111	10 mA

The internal current source value can be set via I^{2}C. The register 0x06 can decide it by the above table.

The current source is powered by VDD. It could be used to set the measurement range. In the case that capacitance on VIN is large, a large I$_{SRC}$ could be applied firstly. After the voltage change becomes smoothly, smaller I$_{SRC}$ can be used to save the standby consumption.

Register for I$_{SRC}$ Pulse

Address: 07h, Bit [7:4]

Default Value: 4'b0000

Type: Read / Write

Function: Define t$_{DET}$, see the description followed

TDET [3:0]	Data	I$_{SRC}$ Pulse Width
Define pulse width t$_{DET}$ of the current source applied on VIN	4'b0000	200 μs
	4'b0001	400 μs
	4'b0010	1 ms
	4'b0011	2 ms
	4'b0100	4 ms
	4'b0101	10 ms
	4'b0110	20 ms
	4'b0111	40 ms
	4'b1000	100 ms
	4'b1001	200 ms
	4'b1010	400 ms
	4'b1011	1 s
	4'b1100	2 s
	4'b1101	4 s
	4'b1110	10 s
	4'b1111	Always ON

Register for I$_{SRC}$ Blank Time

Address: 07h, Bit [3:0]

Default Value: 4'b0000

Type: Read / Write

Function: define t$_{BLNK}$, see the description followed

TBLK [3:0]	Data	I$_{SRC}$ Apply Period
Define Period t$_{PD}$ of Detection	4'b0000	Single Pulse
	4'b0001	10 ms
	4'b0010	20 ms
	4'b0011	50 ms
	4'b0100	100 ms
	4'b0101	200 ms
	4'b0110	500 ms
	4'b0111	1 s
	4'b1000	2 s
	4'b1001	3 s
	4'b1010	6 s
	4'b1011	12 s
	4'b1100	30 s
	4'b1101	60 s
	4'b1110	120 s
	4'b1111	300 s

NOTE: It should be noticed, when 0x07 is set to 8'hF0 (conflict as single pulse and always ON), always on mode will be dominating.

The detection mode period will be decided by above table and following diagram:
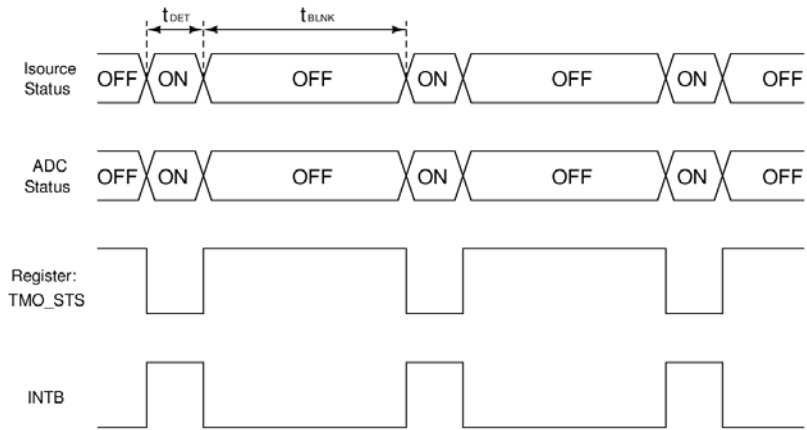
Figure 10. Timing for Detection Period Setup

Register for Detection Target

Address: 09h, Bit [7:0]

Default Value: 8'b00

Type: Read / Write

Function: Define the threshold of moisture detection. This register can be written to a threshold value for 0 V to 2.04 V with 8 mV/step. During detection, once the voltage on VIN exceed the value set by 0x09, the interrupt will be asserted and register TAG_STS (bit[6] of register 0x02) will be set to 1. By doing that, processor will know when the low resistance condition has disappeared before proceed to the next action.
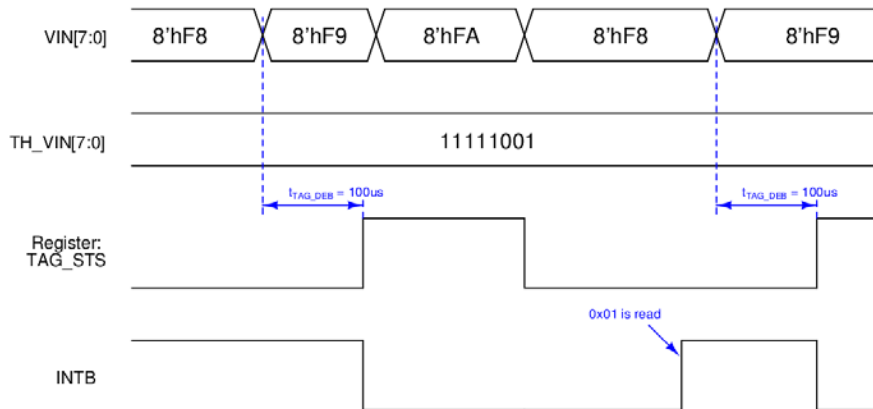
Figure 11. Timing for TAG_STS and Register 0x09 (TAG_DIR = 0)

APPLICATIONS INFORMATION

Overview of I²C

The I²C bus supports bi−directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on. Both the SCL and SDA signals are held at high level whenever communications are not being performed.

The starting and stopping of communications will be controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse.

Starting and Stopping I²C

START condition: SDA level changes from high to low while SCL is at high level

STOP condition: SDA level changes from low to high while SCL is at high level

Repeated START condition (RESTART condition)
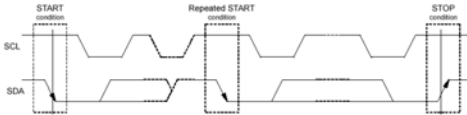
Data Transfer and Acknowledge Responses during I²C Communication

Data transfers are performed in 8−bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition. The address auto increment function operates during both write and read operations.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level. The receiver (receiving side) captures data while the SCL line is at high level.
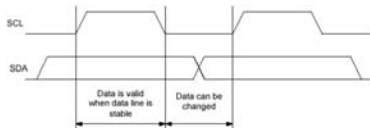
When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8−bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.
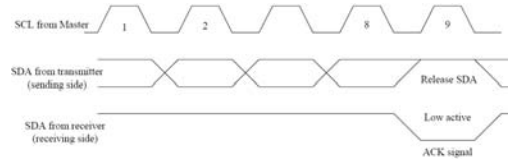
After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, it indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

Slave Address

The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

All communications begin with transmitting the [START condition] + [slave address (+ R/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address. Slave addresses have a fixed length of 7−bits (7'b1101100). See table for the details. An R/W bit is added to each 7−bits slave address during 8−bits transfers.

Operation	Transfer data	Slave Address							R/W bit
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	D9h	1	1	0	1	1	0	0	1 (=Read)
Write	D8h								0 (=Write)

Input Decoupling (C$_{in}$)

A ceramic or tantalum at least 0.1 μF capacitor is recommended and should be connected close to the FPF2283CUCX package. Higher capacitance and lower ESR will improve the overall line and load transient response.

Output Decoupling (C$_{out}$)

The FPF2283CUCX is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The minimum output decoupling value is 0.1 μF and can be augmented to fulfill stringent load transient requirements.

Enable Operation

The enable pin ENB will turn the device on or off without I²C communication. The threshold limits are covered in the

electrical characteristics table in this data sheet. The turn−on/turn−off transient voltage being supplied to the enable pin should exceed a slew rate of 10 mV/μs to ensure correct operation. If the enable function is not to be used then the pin should be connected to Ground.

Thermal Considerations

As power in the FPF2283CUCX increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the FPF2283CUCX has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the FPF2283CUCX can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 3)}$$

Since T_J is not recommended to exceed 125°C, then the FPF2283CUCX soldered on 645 mm^2, 1 oz copper area, the power dissipated by the FPF2283CUCX can be calculated from the following equations:

$$P_D \approx V_{in} \cdot \left(I_Q @ I_{out}\right) + I_{out}^2 \cdot r_{on} \qquad \text{(eq. 4)}$$

Hints

V_{in} and V_{out} printed circuit board traces should be as wide as possible. Place external components, especially the input capacitor and TVS, as close as possible to the FPF2283CUCX, and make traces as short as possible.

PACKAGE DIMENSIONS

WLCSP20 2.2x1.8x0.574
CASE 567UT
ISSUE O

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

BALL A1 INDEX AREA

TOP VIEW

0.05 C

SEATING PLANE

SIDE VIEW

DETAIL A

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	.536	.574	.612
A1	.176	.196	.216
A2	.360	.378	.396
b	.240	.260	.280
D	2.170	2.200	2.230
E	1.770	1.800	1.830
e	0.40 BSC		
x	0.285	0.300	0.315
y	0.285	0.300	0.315

0.005 (M) C A B

Ø b
20X

BOTTOM VIEW

(Ø0.215) Bottom of Cu Pad
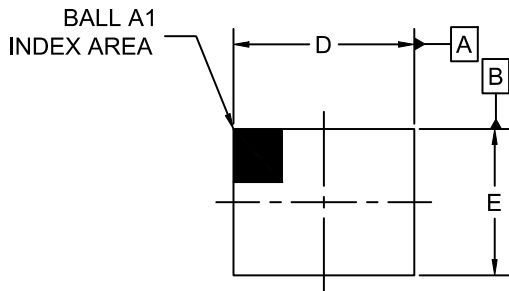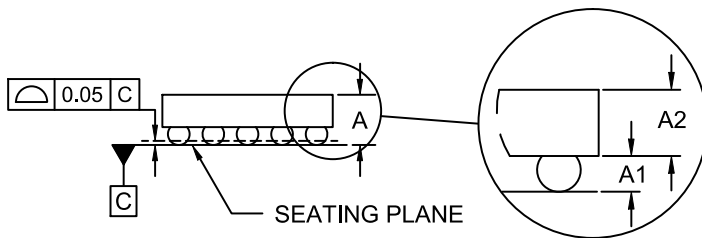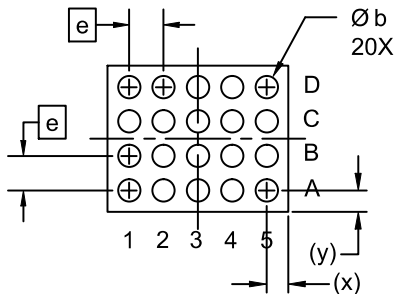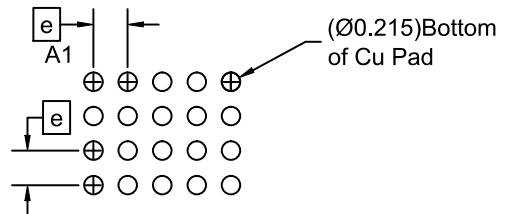
RECOMMENDED
MOUNTING FOOTPRINT
(NSMD PAD TYPE)

◊