NLAS4717EP

4.5 Ω High Bandwidth, Dual SPDT Analog Switch

The NLAS4717EP is an advanced CMOS analog switch fabricated in sub−micron silicon gate CMOS technology. The device is a dual independent Single Pole Double Throw (SPDT) switch featuring low $R_{DS(on)}$ of 4.5 Ω at 3.0 V.

The device also features guaranteed Break−Before−Make (BBM) switching, assuring the switches never short the driver.

The NLAS4717EP is available in two small size packages:

- Microbump: 2.0 x 1.5 mm
- WQFN−10: 1.4 x 1.8 mm

Features

- Low $R_{DS(on)}$: 4.5 Ω @ 3.0 V
- Matching Between the Switches ±0.5 Ω
- Wide Voltage Range: 1.8 V to 5.5 V
- High Bandwidth > 90 MHz
- 1.65 V to 5.5 V Operating Range
- Low Threshold Voltages on Pins 4 and 8 (CTRL Pins)
- Ultra−Low Charge Injection ≤ 6.0 pC
- Low Standby Current: I_{CC} = 1.0 nA (Max) @ T_A = 25°C
- *OVT on Pins 4 and 8 (CTRL Logic Pins)
- These are Pb−Free Devices

Typical Applications

- Cell Phones
- PDAs
- MP3s
- Digital Still Cameras
- USB 2.0 Full Speed (USB1.1) − 12 Mbps Compliant

Important Information

- ESD Protection:
  - Human Body Model (HBM) = 2500 V,
  - Machine Model (MM) = 200 V
- Latchup Max Rating: 200 mA (Per JEDEC EIA/JESD78)
- Pin−to−Pin Compatible with MAX4717

*OVT

- Overvoltage Tolerant (OVT) specific pins operate higher than normal supply voltages, with no damage to the devices or to signal integrity.

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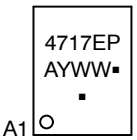
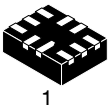
MARKING DIAGRAMS

A1

Microbump−10
CASE 489AA



A = Assembly Location
Y = Year
W, WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)



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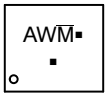
WQFN−10
CASE 488AQ



AW = Specific Device Code
M = Date Code
▪ = Pb−Free Device
(Note: Microdot may be in either location)

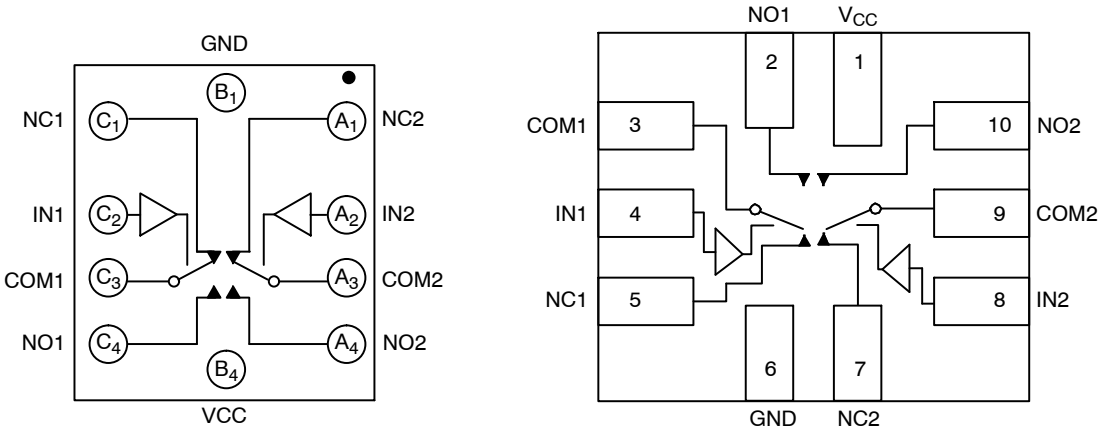
FUNCTION TABLE

IN_	NO_	NC_
0	OFF	ON
1	ON	OFF

ORDERING INFORMATION

Device	Package	Shipping†
NLAS4717EPFCT1G	Microbump−10 (Pb−Free)	3000 / Tape & Reel
NLAS4717EPMTR2G	WQFN−10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



Microbump
(Top View)

WQFN
(Top View)

Figure 1. Device Circuit Diagrams and Pin Configurations

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V+	DC Supply Voltage	−0.5 to +7.0	V
V_{IS}	Analog Input Voltage (V_{NO}, V_{NC}, or V_{COM}) (Note 1)	$-0.5 \le V_{IS} \le V_{CC} + 0.5$	V
V_{IN}	Digital Select Input Voltage	$-0.5 \le V_I \le +7.0$	V
I_{IK}	DC Current, Into or Out of Any Pin (Continuous)	±100	mA
I_{PK}	Peak Current (10% Duty Cycle)	±200	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Signal voltage on NC, NO, and COM exceeding VCC or GND are clamped by the internal diodes. Limit forward diode current to maximum current rating.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V+	DC Supply Voltage	1.8	5.5	V
V_{IN}	Digital Select Input Voltage	GND	5.5	V
V_{IS}	Analog Input Voltage (NC, NO, COM)	GND	V_{CC}	V
T_A	Operating Temperature Range	−40	+85	°C
t_r, t_f	Input Rise or Fall Time, SELECT V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	 0 0	 100 20	ns/V

ANALOG SWITCH DC CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	−40°C to +85°C		Unit
				Min	Max	
V_{IH}	Input Logic High Voltage	V_{OUT} = 0.1 V I_{OUT} ≤ 20 μA	1.65 to 2.2 2.7 to 3.6 4.5 to 5.5	V_{CC} x 0.55 V_{CC} x 0.5 2.0	– – –	V
V_{IL}	Input Logic Low Voltage	V_{OUT} = −V_{CC} − 0.1 V I_{OUT} ≤ 20 μA	1.65 to 2.2 2.7 to 3.6 4.5 to 5.5	– – –	V_{CC} x 0.2 V_{CC} x 0.2 0.8	V
I_{IN}	Input Leakage Current	V_{IN} = V_{CC} or GND	5.5	−100	+100	nA
V_{CC}	Power Supply Range	All	–	1.65	5.5	V
I_{CC}	Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	1.8 3.3 5.5	– – –	1.0 1.0 1.0	μA

ANALOG SWITCH CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} (V)	−40°C to +85°C			Unit
				Min	Typ	Max	
R_{ON}	ON Resistance (Note 2)	I_{COM} = 10 mA V_{IS} = 0 to V_{CC}	3.0	–	3.2	4.5	Ω
			5.0	–	2.1	3.5	
ΔR_{ON}	ON Resistance Match Between Channels (Note 2 and 3)	I_{COM} = 10 mA V_{IS} = 0 to V_{CC}	3.0	–	0.1	0.4	Ω
			5.0	–	0.1	0.4	
$R_{FLAT[ON]}$	ON Resistance Flatness (Note 4)	I_{COM} = 10 mA V_{IS} = 0 to V_{CC}	3.0	–	1.12	1.5	Ω
			5.0	–	0.55	1.36	
$I_{NO\_[OFF]}$ $I_{NC\_[OFF]}$	NO_, NC_ Off−Leakage Current (Note 5)	V_{COM} = 0.3 V or 3.3 V V_{NO} or V_{NC} = 0.3 V or 3.3 V	3.6	−1.0	0.01	+1.0	nA
		V_{COM} = 0 V or 5.0 V V_{NO} or V_{NC} = 0 V or 5.0 V	5.5	−1.0	0.01	+1.0	
$I_{COM\_[ON]}$	COM_ On−Leakage Current (Note 5)	V_{COM} = 0.3 V or 3.3 V V_{NO} or V_{NC} = 0.3 V or 3.3 V	3.6	−2.0	0.01	+2.0	nA
		V_{COM} = 0 V or 5.0 V V_{NO} or V_{NC} = 0 V or 5.0 V	5.5	−2.0	0.01	+2.0	

ANALOG SWITCH AC CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	−40°C to +85°C			Unit
				Min	Typ	Max	
t_{ON}	Turn−On Time	$V_{NC\_}$, $V_{NO\_}$ = V_{IH} or V_{IL} R_L = 300 Ω, C_L = 35 pF $V_{IN[x]}$ = V_{IH} or V_{IL}	1.8 to 5.5	−	−	30	nS
t_{OFF}	Turn−Off Time	$V_{NC\_}$, $V_{NO\_}$ = V_{IH} or V_{IL} R_L = 300 Ω, C_L = 35 pF $V_{IN[x]}$ = V_{IH} or V_{IL}	1.8 to 5.5	−	−	40	nS
t_{BBM}	Break−Before−Make Time Delay (Note 5)	$V_{NC\_}$, $V_{NO\_}$ = 1.5 V R_L = 300 Ω, C_L = 35 pF	−	−	8.0	−	nS
t_{SKEW}	Skew (Note 5)	R_S = 39 Ω, C_L = 50 pF	−	−	0.15	2.0	nS

2. R_{ON} characterized for V_{CC} range (1.65 V to 5.5 V).
3. $\Delta R_{ON} = R_{ON}(MAX) - R_{ON}(MIN)$.
4. $R_{FLAT[ON]} = R_{ON}(MAX) - R_{ON}(MIN)$, measured over V_{CC} range.
5. Guaranteed by design.

ANALOG SWITCH APPLICATION CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	−40°C to +85°C			Unit
				Min	Typ	Max	
Q	Charge Injection	V_{IN} = V_{CC} to GND R_{In} = 0 Ω, C_L = 1.0 nF $Q = C_L - \Delta V_{OUT}$	3.0 5.0		6.0 9.0		pC
VISO	Off−Isolation	f = 10 MHz $V_{NO\_}$, $V_{NC\_}$ = 1.0 Vp−p R_L = 50 Ω, C_L = 5.0 pF	1.65 to 5.5		−50		dB
		f = 1.0 MHz $V_{NO\_}$, $V_{NC\_}$ = 1.0 Vp−p R_L = 50 Ω, C_L = 5.0 pF			−75		
VCT	Cross−Talk	f = 10 MHz $V_{NO\_}$, $V_{NC\_}$ = 1.0 Vp−p R_L = 50 Ω, C_L = 5.0 pF	1.65 to 5.5		−80		dB
		f = 1.0 MHz $V_{NO\_}$, $V_{NC\_}$ = 1.0 Vp−p R_L = 50 Ω, C_L = 5.0 pF			−110		
BW	On−Channel −3.0 db Bandwidth	Signal = 0 dB R_L = 50 Ω, C_L = 5.0 pF	1.8 to 5.0		90		MHz
THD	Total Harmonic Distortion	V_{COM} = 2.0 Vp−p, RL = 600 Ω, T_A = 25°C	−		0.02		%
$C_{NO\_[OFF]}$ $C_{NC\_[OFF]}$	NO_, NC_ OFF−Capacitance	F = 1.0 MHz	−		15		pF
$C_{NO\_[ON]}$ $C_{NC\_[ON]}$	NO_, NC_ ON−Capacitance	F = 1.0 MHz	−		38		pF

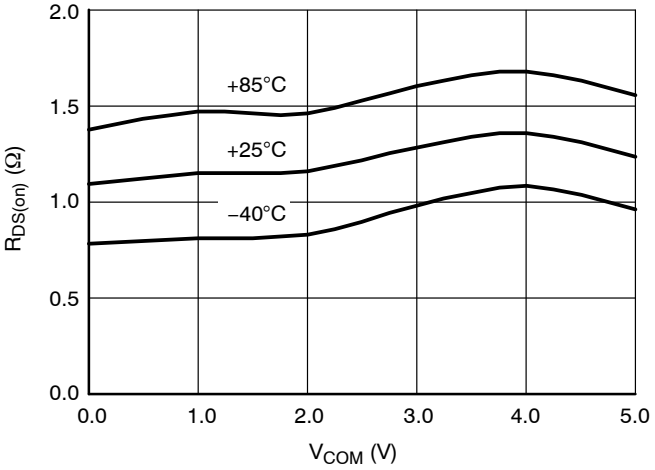


Figure 2. $R_{DS(on)}$ @ V_{CC} = 5.0 V

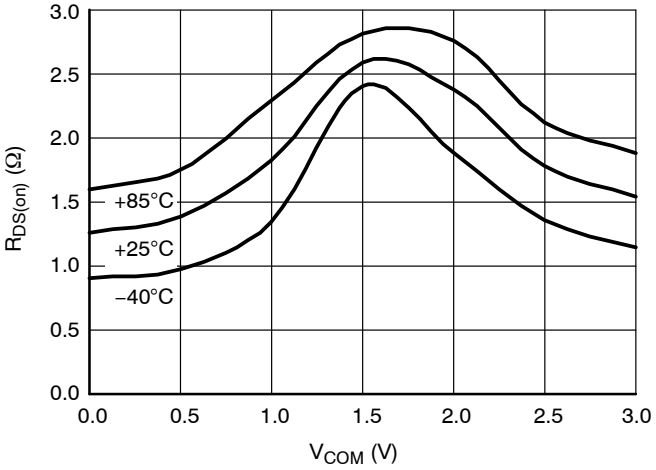


Figure 3. $R_{DS(on)}$ @ V_{CC} = 3.0 V

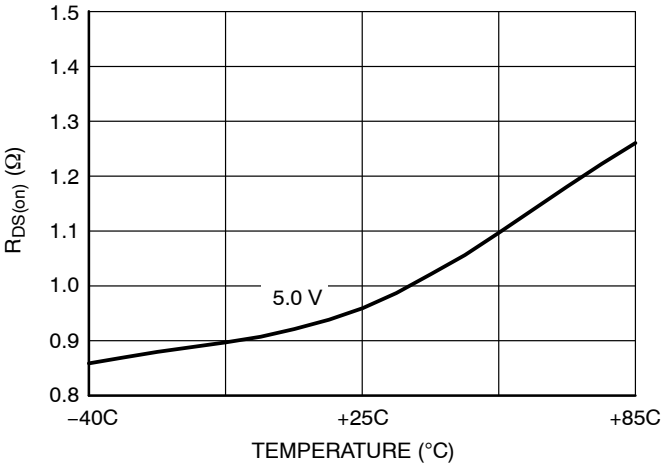


Figure 4. Delta $R_{DS(on)}$ @ V_{CC} = 5.0 V

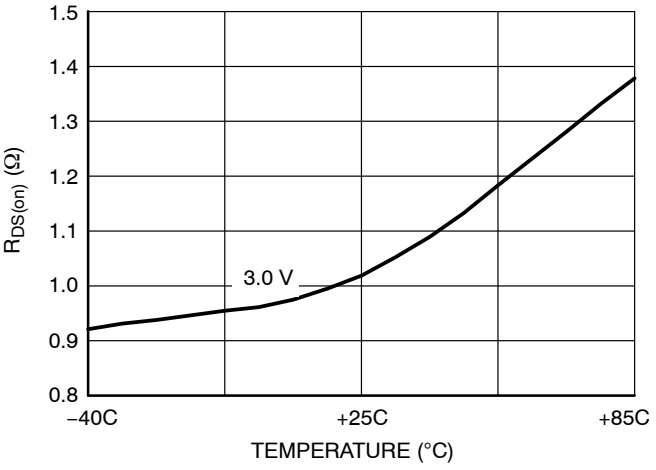


Figure 5. Delta $R_{DS(on)}$ @ V_{CC} = 3.0 V

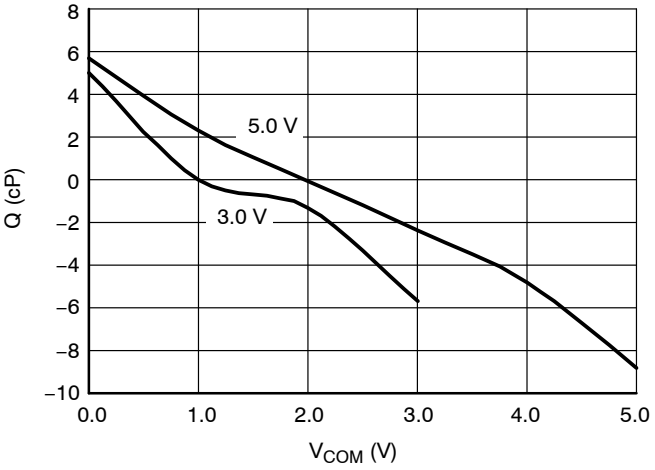


Figure 6. Charge Injection

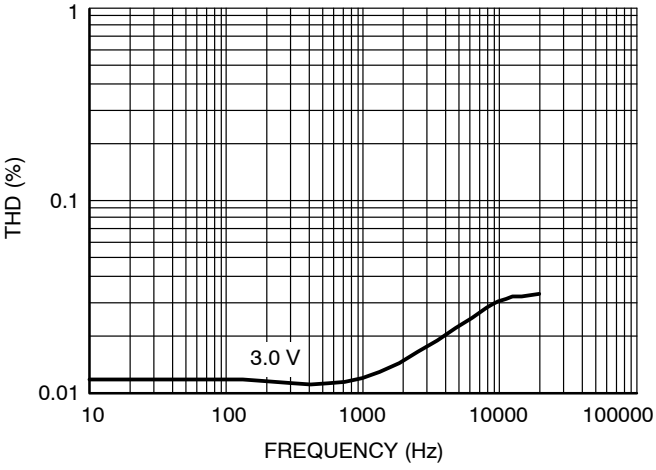


Figure 7. Total Harmonic Distortion

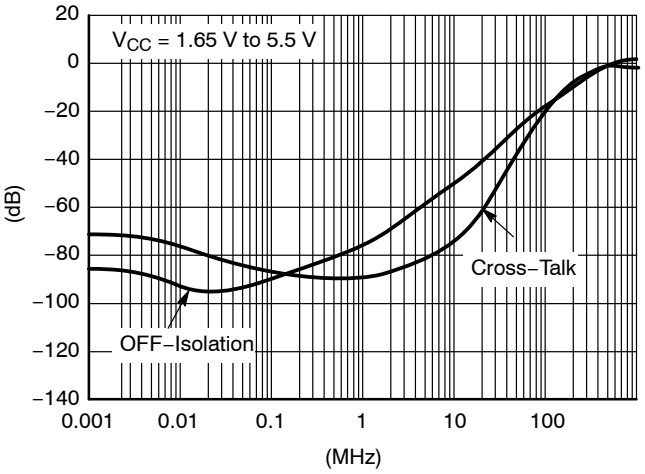


Figure 8. Frequency Response

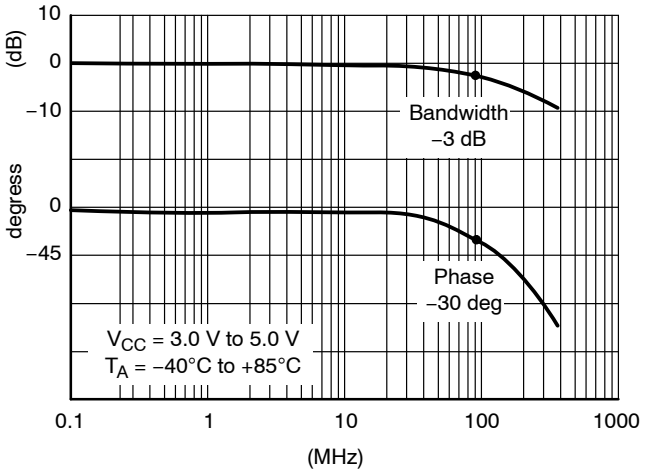


Figure 9. Bandwidth and Phase

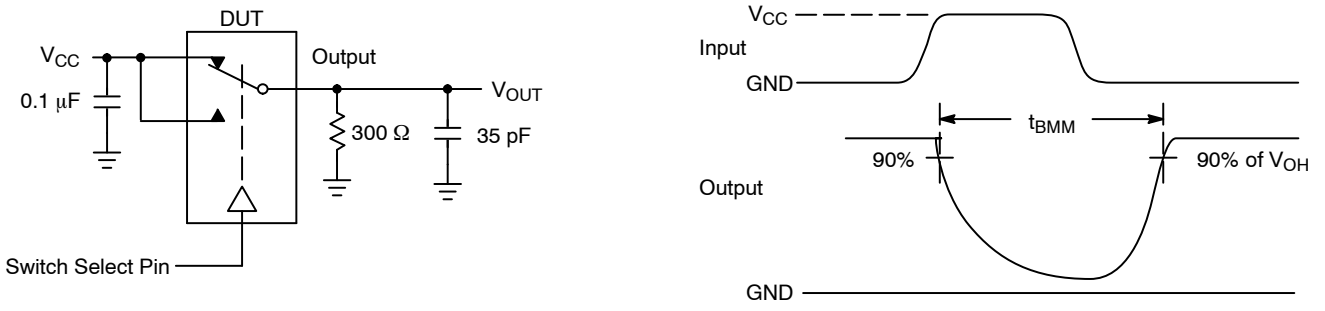


Figure 10. t_{BBM} (Time Break−Before−Make)

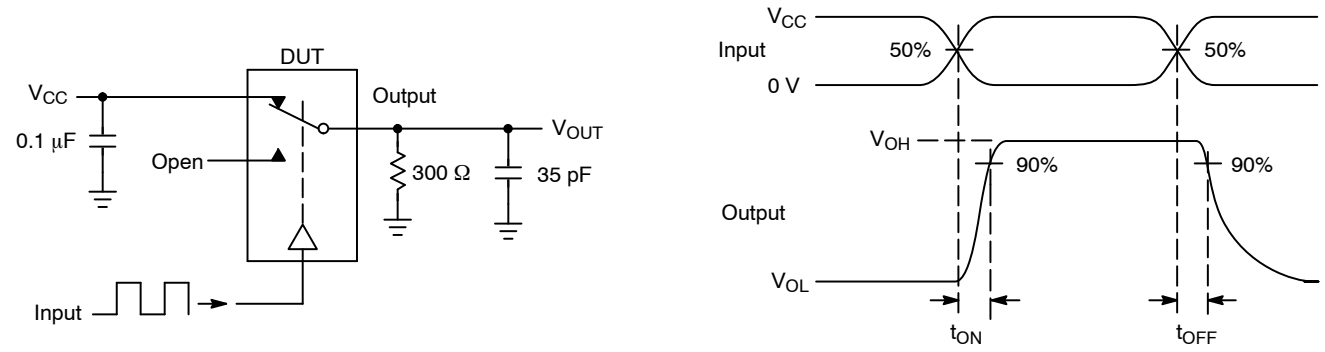


Figure 11. t_{ON}/t_{OFF}

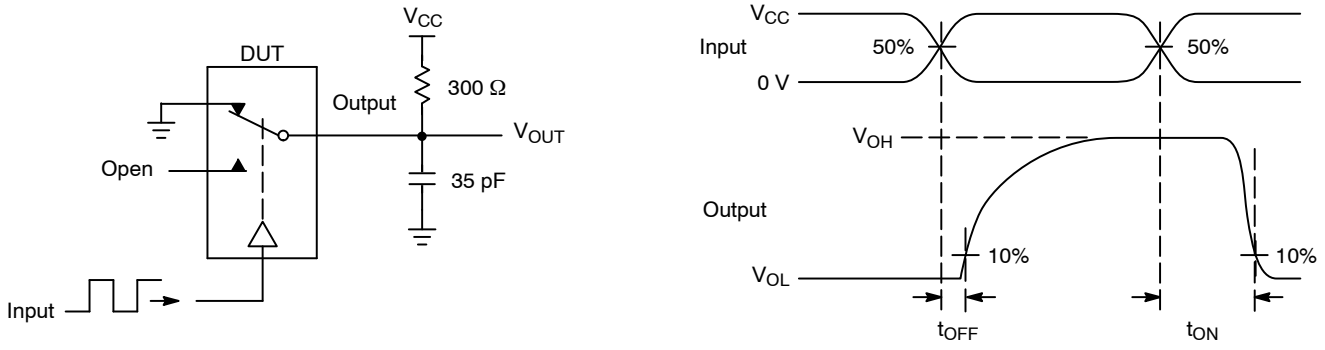
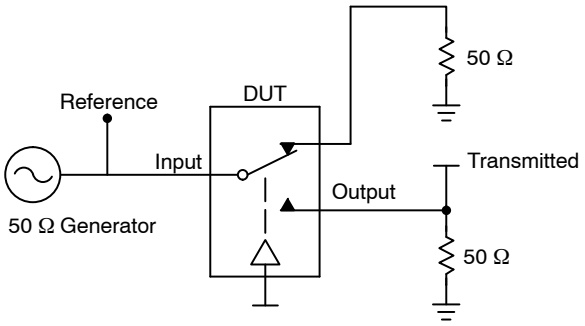


Figure 12. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

V_{ISO} = Off Channel Isolation = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz

V_{ONL} = On Channel Loss = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3.0 dB below V_{ONL}
V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 13. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

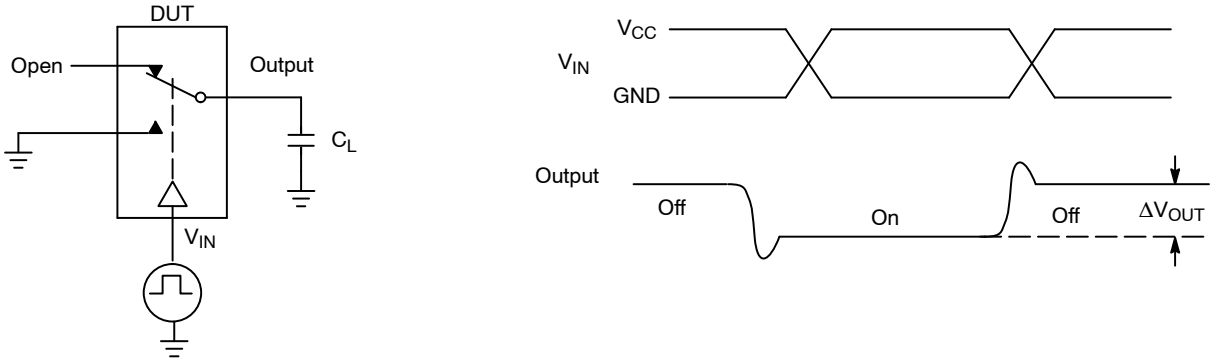


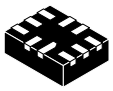
Figure 14. Charge Injection: (Q)

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

WQFN10, 1.4x1.8, 0.4P
CASE 488AQ−01
ISSUE C

DATE 19 JUN 2007



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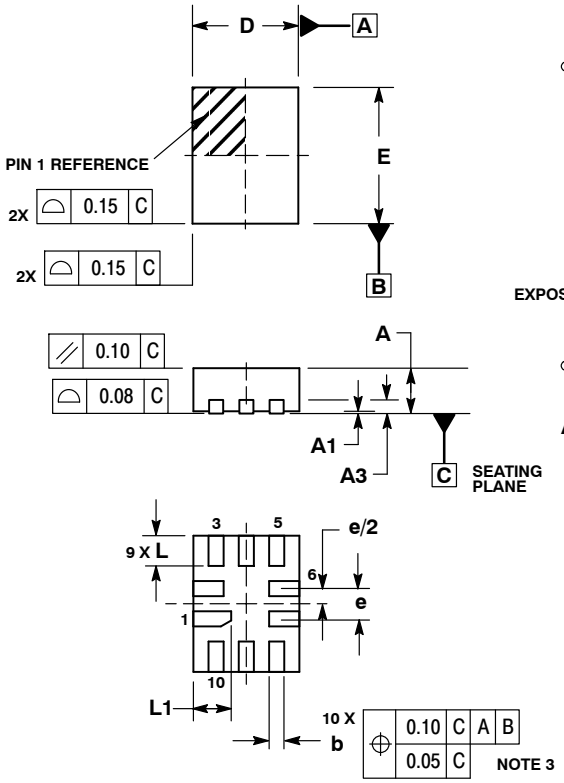
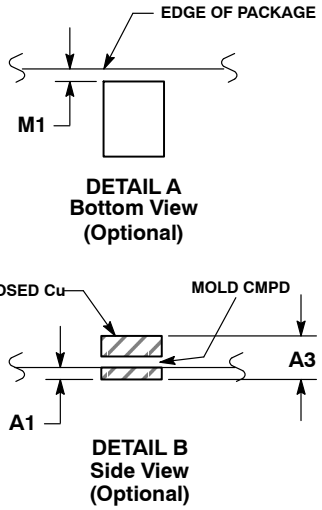
SCALE 5:1

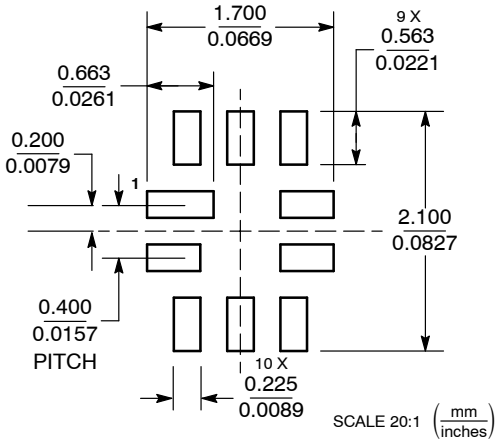




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED PADS CONNECTED TO DIE FLAG. USED AS TEST CONTACTS.

DIM	MILLIMETERS MIN	MAX
A	0.70	0.80
A1	0.00	0.050
A3	0.20 REF	
b	0.15	0.25
D	1.40 BSC	
E	1.80 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.40	0.60
M1	0.00	0.05

MOUNTING FOOTPRINT



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DESCRIPTION:	**WQFN10, 1.4 X 1.8, 0.4P**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

10 PIN FLIP−CHIP
CASE 489AA−01
ISSUE A

DATE 04 MAY 2004

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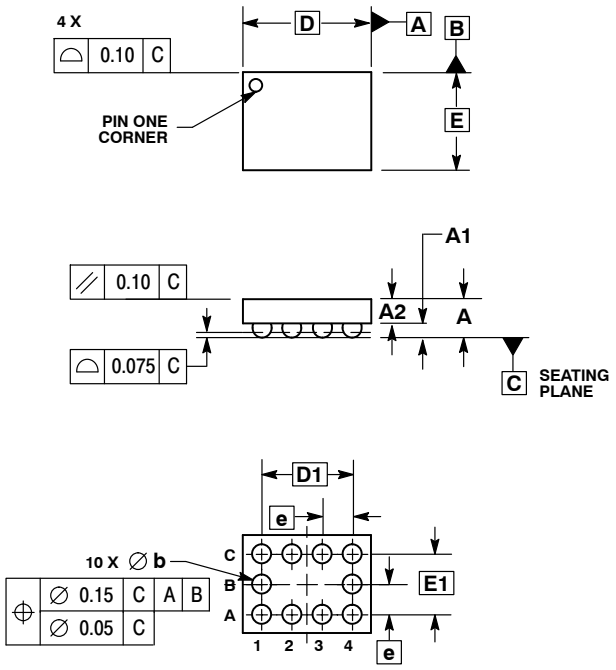
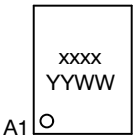
SCALE 4:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.650
A1	0.210	0.270
A2	0.280	0.380
D	1.965 BSC	
E	1.465 BSC	
b	0.250	0.350
e	0.500 BSC	
D1	1.500 BSC	
E1	1.000 BSC	

GENERIC MARKING DIAGRAM*



xxxx = Specific Device Code
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**10 PIN FLIP−CHIP**	**PAGE 1 OF 1**

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