Teralane Semiconductor
Product Data Sheet

TLS8204

102 x 68 Dot Matrix

STN Segment/Common Driver with Controller

Precautions for light: Light has the effect of causing the electrons of semiconductor to move and may change the characteristics of semiconductor devices. For this reason, it is necessary to take account of effective protection measures for the packages (such as COB, COG, TCP and COF, etc) causing chip to be exposed to a light environment in order to isolate the projection of light on any part of the chip, including top, bottom and the area around the chip. Follow the precautions below when using this product:
1) During the design stage, it is necessary to notice and confirm the light sensitivity and preventive measures for using IC on substrate (PCB, Glass or Film) or product.
2) Test and inspect the product under an environment free of light source penetration.
3) Confirm that all surfaces around the IC will not be exposed to light source.

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INTRODUCTION

The TLS8204 is a low power single-chip driver IC with embedded controller for dot matrix Mono STN LCDs. It contains 170 high voltage driving output circuits and is capable of driving maximum 102 segments, 67 commons with 1 icon LCD panel. In addition to low power COM and SEG drivers, the TLS8204 contains all necessary circuits for high voltage LCD power supply, bias voltage generation, timing generation and dot-matrix display data memory.

The TLS8204 contains an on-chip 102×68 = 6,936 bits display data RAM while supporting both parallel and serial MPU interfaces: 8 bits 6800/8080 series parallel interface and 4-line/3-line serial peripheral interface.

Featuring build-in booster and voltage follower capacitors, the TLS8204 requires the fewest peripheral passive components so that the total cost of the display system can be minimized.

FEATURES

- Driver outputs:
  - 102 segments / 67 common + 1 ICON common (1/68 duty)
  - 102 segments / 32 common + 1 ICON common (1/33 duty)
  - 102 segments / 16 common + 1 ICON common (1/17 duty)

  (1/33 duty and 1/17 duty are under partial mode)
- On-chip display data RAM with the capacity of 102×68=6936 bits
- Multiple MPU interfaces selectable:
  - 6800 series parallel interface
  - 8080 series parallel interface
  - 4-line Serial Peripheral interface (4-line SPI)
  - 3-line Serial Peripheral interface (3-line SPI)
- Multiple command functions:
  - Display start line set enabling a vertical scroll function
  - Segment/Common output mode select
  - Display normal/reverse mode, display all points on/off mode
  - Partial mode with start COM selectable
  - Read-modify-write mode
  - LCD bias set, LCD operation voltage regulator ratio set, static indicator set.
- On-chip power supply circuits with booster and voltage follower capacitor built-in
  - On-chip LCD driving voltage generator or external power supply selectable
  - On-chip DC-DC booster with programmable booster ratio: 2x, 3x, 4x, 5x
  - On-chip oscillator for display clock or external clock selectable
  - Supports 220-steps of contrast
  - Adjustable LCD driving voltage bias ratio: 1/4~1/11
  - Thermal gradient = -0.11%/℃
- Power supply voltage:

  VDD = 1.7 - 3.3V (power for logic)
  VDD2 = 2.4 - 3.3V (power for analog)
  VLCD = 4.0 - 10.5 V (LCD driving voltage)
- Package type: COG

BLOCK DIAGRAM

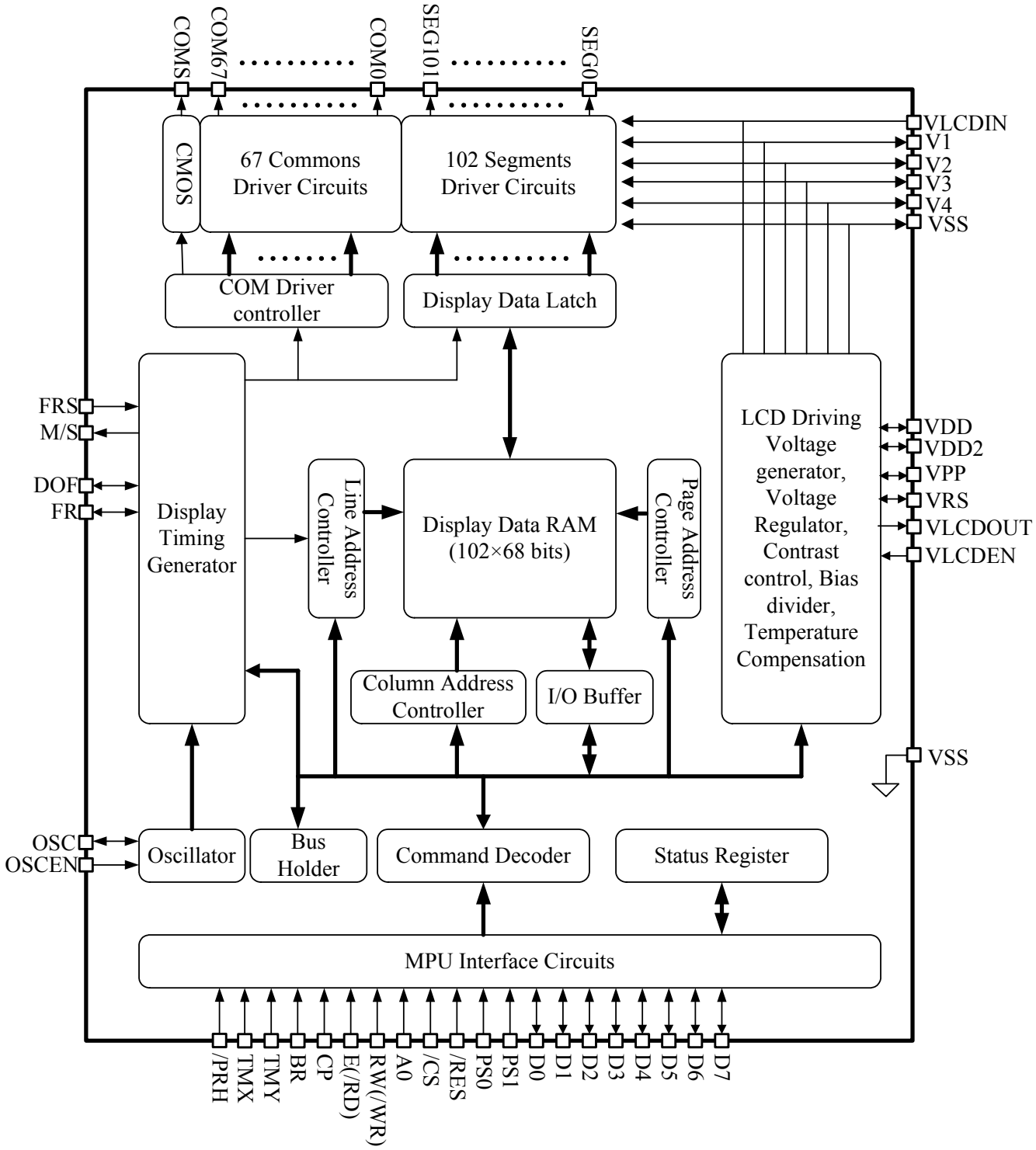

Figure 1 the block diagram of TLS8204

PIN DESCRIPTION

Name	I/O	Description	No. of Pins
Power Supply Pins			
VDD	Power Supply	Power supply for logic circuits. VDD and VDD2 can be connected together.	8
VDD2	Power Supply	Power supply for analog circuits. VDD and VDD2 can be connected together.	4
VSS	Power Supply	Ground	13
VRS	Power Supply	Power supply for the internal LCD operation voltage regulator reference circuits.	2
VLCDIN	Power Supply	This is the LCD operation voltage and power supply for internal HV circuits. When internal voltage booster is used, this pin must be connected to VLCDOUT; when the internal voltage booster is disabled, an external LCD operation voltage should be provided through this pin.	4
VLCDOUT	Power Supply	This is the output of LCD operation voltage VLCD generated by the internal voltage booster. When the internal voltage booster is used, this pin must be connected to VLCDIN; when the internal voltage booster is disabled, this pin should be left open.	2
V1, V2, V3, V4	Power Supply	This is the power supply for the multi-level driving voltage of the LCDs. The voltage supply applied depends on the driving polarity, and the following relationship should be always maintained: $VLCD \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq VSS$ These driving voltages can be generated internally. VLCD, V1-V4 are in the relationship of: $V1=(b-1)\times V0/b;\ V2=(b-2)\times V0/b;\ V3=2\times V0/b;\ V4=V0/b.$ Where b is defined as the bias ratio. The bias ratio can be selected from 1/4 to 1/11 by software.	4
VPP	Power Supply	OTP programming voltage supply. Left this pin open when normal function.	2
MPU Interface I/O Pins			
A0	I	Thin pin is used to indicate that whether the data bus is data or command. A0 = "H": D7 – D0 are data. A0 = "L": D7 – D0 are command.	1
/RES	I	This is the reset pin. When this pin is set to "L", the system registers are set to the initialized status. Refer to the descriptions of Reset Circuits.	1

<table>
<tr><td>/CS</td><td>I</td><td>These are the chip select pins. The chip is set to active when /CS= “H”.</td><td>1</td></tr>
<tr><td>E
(/RD)</td><td>I</td><td>This pin is the enable indicator (6800 interface mode) or the read operation indicator (8080 interface mode).
For 6800 series interface applications:
This is the E pin. Setting E = “H” indicates a write/read operation.
For 8080 series interface applications:
This is the /RD pin. Setting /RD = “L” indicates the read operation and the data bus can be read by MPU.
When using serial interface, this pin should be fixed to “VDD” or left open.</td><td>1</td></tr>
<tr><td>R/W
(/WR)</td><td>I</td><td>This pin is the read/write indicator (6800 interface mode) or write operation indicator (8080 interface mode).
For 6800 series interface applications:
This is the R/W pin. Setting R/W = “H” indicates a read operation (MPU can read data from the data bus) while setting R/W = “L” indicates the write (the TLS8204 chip reads the data bus).
For 8080 series interface applications:
This is the /WR pin. Setting /WR = “L” indicates the write operation and the data bus are to be read by the TLS8204 chip.
When use serial interface, this pin should be fixed to “VDD” or left open.</td><td>1</td></tr>
<tr><td>D7,
D6,
D5,
D4,
D3,
D2,
D1,
D0</td><td>I/O</td><td>D7-D0 are the data bus in parallel interface mode. When using serial interface, the functionality of D7-D0 is very flexible: D7 or D0 serves as SCK, D6 or D1, D2, D3 serves as SDA, A0 or D5 serves as A0, /CS or D4 serves as /CS.
<table>
<tr><th>Pin name</th><th>Parallel I/F</th><th>4wire SPI I/F</th><th>3wire SPI I/F</th></tr>
<tr><td>/CS</td><td>/CS</td><td>/CS or fixed to “H”</td><td>/CS or fixed to “H”</td></tr>
<tr><td>A0</td><td>A0</td><td>A0 or fixed to “H”</td><td>Fixed to “H”</td></tr>
<tr><td>D7</td><td>D7</td><td>SCK or fixed to “H”</td><td>SCK or fixed to “H”</td></tr>
<tr><td>D6</td><td>D6</td><td>SDA or fixed to “H”</td><td>SDA or fixed to “H”</td></tr>
<tr><td>D5</td><td>D5</td><td>A0 or fixed to “H”</td><td>Fixed to “H”</td></tr>
<tr><td>D4</td><td>D4</td><td>/CS or fixed to “H”</td><td>/CS or fixed to “H”</td></tr>
<tr><td>D3</td><td>D3</td><td>SDA or fixed to “H”</td><td>SDA or fixed to “H”</td></tr>
<tr><td>D2</td><td>D2</td><td>SDA or fixed to “H”</td><td>SDA or fixed to “H”</td></tr>
<tr><td>D1</td><td>D1</td><td>SDA or fixed to “H”</td><td>SDA or fixed to “H”</td></tr>
<tr><td>D0</td><td>D0</td><td>SCK or fixed to “H”</td><td>SCK or fixed to “H”</td></tr>
</table>
Note that left any one of /CS, A0, D7-D0 floating is not allowed. The do not used terminal must be fixed to “VDD”.</td><td>8</td></tr>
</table>

<table>
<tr><th colspan="4">Configuration Pins</th></tr>
<tr><td>PS1, PS0</td><td>I</td><td><table><tr><th>PS0</th><th>PS1</th><th>State</th></tr><tr><td>L</td><td>L</td><td>4 wire-SPI MPU Interface</td></tr><tr><td>L</td><td>H</td><td>3 wire-SPI MPU Interface</td></tr><tr><td>H</td><td>L</td><td>8080-series parallel MPU interface</td></tr><tr><td>H</td><td>H</td><td>6800-series parallel MPU interface</td></tr></table></td><td>2</td></tr>
<tr><td>OSCEN</td><td>I</td><td>When connected to VDD, the internal oscillator will be used for display controller clock;
When connected to VSS, the internal oscillator is disabled. In this case, an external clock should be input through the OSC pin.
Please be noted that this pin must not be left open.</td><td>1</td></tr>
<tr><td>OSC</td><td>I/O</td><td>If the internal oscillator is used (OSCEN pin=‘H’), this pin is the output of the internal clock;
If the internal oscillator is disabled (OSCEN pin = ‘L’), this pin is used for clock input.</td><td>1</td></tr>
<tr><td>VLCDEN</td><td>I</td><td>When connected to VDD, the internal dc-dc booster is selected;
When connected to VSS, the internal dc-dc booster is disabled; an external LCD operating voltage can be input through VLCDIN pin.
Please be noted that this pin must not be left open.</td><td>1</td></tr>
<tr><td>CP</td><td>I</td><td>Set Booster stages default ratio.
CP = “L”: 4X booster ratio;
CP = “H”: 5X booster ratio.
CP pin set the default value of booster stages after reset; besides, the booster stage can be changed by software command</td><td>1</td></tr>
<tr><td>BR</td><td>I</td><td>Set LCD bias ratio default state.
BR = “L”: 1/7 bias;
BR = “H”: 1/9 bias.
BR pin set the default value of bias ratio after reset; besides, the bias ratio can be re-configured by software command</td><td>1</td></tr>
<tr><td>/PRH</td><td>I</td><td>Select LCD operation voltage range.
/PRH = “L”: The VLCD high range is selected;
/PRH = “H”. The VLCD low range is selected as initial setting, and the state can be re-configured by the “set VLCD range” command.
Please be noted that, when /PRH connected to VSS, the VLCD range can not be re-configured by software.</td><td>1</td></tr>
<tr><td>TMX</td><td>I</td><td>This pin selects SEG output direction.
TMX = “L”: normal direction. (SEG0 → SEG101)
TMY = “H”: reverse direction (SEG101 → SEG0)
When TMX connected to VSS, the SEG output direction can be re-configured through the “Function set” command. However, when TMX connected to VDD, the SEG output direction can not be re-configured by software.</td><td>1</td></tr>
</table>

<table>
<tr><td>TMY</td><td>I</td><td>This pin selects COM scan direction.
TMY = “L”: normal direction.
TMY = “H”: reverse direction.
When TMY connected to VSS, the COM scanning direction can be re-configured through the “Function set” command. However, when TMY connected to VDD, the COM scanning direction can not be re-configured by software.</td><td>1</td></tr>
<tr><td colspan="4">LCD Driver Pins</td></tr>
<tr><td>SEG0 – SEG101</td><td>O</td><td>LCD segment driver outputs.
This display data and the M signal control the output voltage of segment driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M (internal)</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td><td>VSS</td></tr>
</table></td><td>102</td></tr>
<tr><td>COM0 – COM66</td><td>O</td><td>LCD column driver outputs
This internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M (internal)</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">VSS</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">VSS</td></tr>
</table></td><td>67</td></tr>
<tr><td>COMS1, COMS2</td><td>O</td><td>These are the LCD common output pins for the indicator (Icon). Both pins output the same signal. If not use, left these pins open.</td><td>2</td></tr>
<tr><td colspan="4">Test Pins</td></tr>
<tr><td>T1- T7</td><td>O</td><td>These pins should be left open.</td><td>7</td></tr>
</table>

Functional Descriptions

The MPU interface

The TLS8204 supports both parallel interface and serial peripheral interface (SPI). Either interface can be selected through the PS1 and PS0 pins. When parallel interface is selected (PS0 = “H”), the D7-D0 is the 8-bit parallel data bus for data transfer. When parallel interface is the selection, both 8080-seires (Intel) MPU and 6800-series (Moto) MPU can be connected to the TLS8204 chip. The PS0 pin selects whether it is 6800-series (PS1 = “H”) or 8080-series (PS1 = “L”) parallel interface. When serial interface is selected (PS0 = “L”), the PS1 pin selects whether it is a 4-line SPI or 3-line SPI. The terminals selected to serve as the serial clock (SCK), serial data (SDA), chip select (/CS) or A0 in 4-line SPI is very flexible so that the restriction on design of system bus connection can be minimized. Table 1 shows the selection of interface type.

Table 1

PS0	PS1	/CS	A0	State
L	L	/CS	A0	4 wire-SPI MPU Interface
L	H	/CS	*	3 wire-SPI MPU Interface
H	L	/CS	A0	8080-series parallel MPU interface
H	H	/CS	A0	6800-series parallel MPU interface

The parallel interface

With the parallel interface, the data can be bi-directional transferred between the MPU and the TLS8204 chip through combinational use of D7-D0 data bus and A0, E (/RD), R/W (/WR) terminals. See Table 2.

Table 2

PS0	PS1	/CS	A0	E(/RD)	R/W(/WR)	D7~D0	MPU Bus
H	H	/CS	A0	E	E/W	D7~D0	6800 series
H	L	/CS	A0	/RD	/WR	D7~D0	8080 series

When using the 6800 series interface, R/W = “H” indicates a read operation from the display data RAM or the internal status register and R/W = “L” indicates a write operation to display data RAM or internal command registers depending on the status of A0 pin. The E pin serves as data latch signal when high during chip select is active. Refer to Table 3. In order to realize the pipeline data read from the display data RAM, a dummy read should be inserted before the first actual display data read. This is shown in Figure 3.

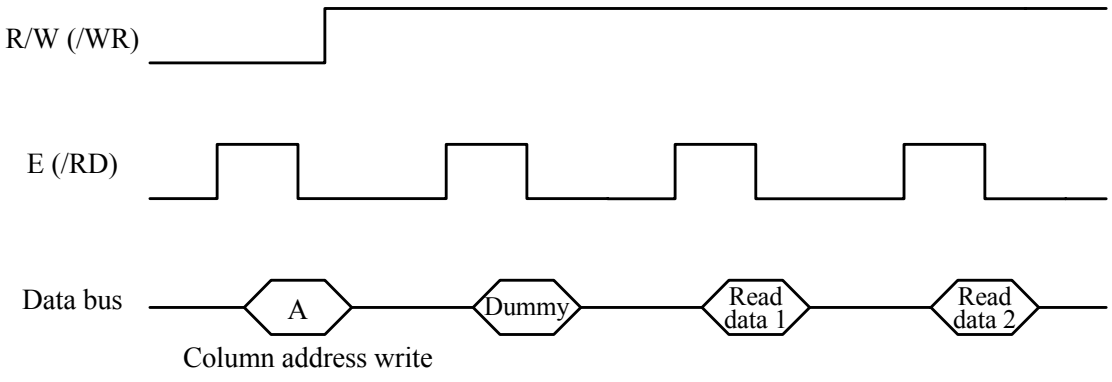

Figure 2 Read sequence (6800 interface mode)

When /RD(E) pin is always pulled high for 6800-series interface, it can be used CSB for enable signal. In this case, interface data is latched at the rising edge of CSB and type of data transfer is determined by signals at A0, /WR(R/W) as in case of 6800-series mode.

When 8080-series interface is selected, providing that the chip select is active, the /RD pin serves as data read latch signal when low and the /WR pin serves as data write latch signal when low. Whether the data to be read (or write) from (to) internal display data RAM or internal status register (or command register) is controlled through A0 pin.

Refer to Table 3. Please be noted that a dummy read should also be inserted before the first actual data read.

Table 3

Shared	6800 Series		8080 Series		Function
A0	E	R/W	/RD	/WR	
1	1	1	0	1	Reads the display data
1	1	0	1	0	Writes the display data
0	1	1	0	1	Status read
0	1	0	1	0	Write control data (command)

The Serial Interface

When the TLS8204 is active (/CS = "L") and PS0 = "L", the serial interface is selected. The display data / command indication may be controlled either through software or the register select pin giving two types of serial interface: 4-line SPI and 3-line SPI. See Table 4.

Table 4

PS0	PS1	/CS	A0	MPU Bus
L	L	/CS	Used	4-line SPI
L	H	/CS	Not used, fix to "H"	3-line SPI

Moreover, the hardware pins serving as the serial data (SDA), serial clock (SCK), chip select(/CS) and data/command indication (A0, when using 4-line SPI) are chosen from /CS, A0, D7-D0 pins of the TLS8204 chip. The choice can be very flexible. Table 5 shows the mapping relationship between hardware /CS/A0/D7-D0 pins and /CS/A0/SCK/SDA terminals for serial interface.

Table 5

Hardware Pins	4-line SPI	3-line SPI
	SPI Terminal Mapping	SPI Terminal Mapping
/CS	/CS	/CS
A0	A0	Fixed to "VDD"
D7	SCK	SCK
D6	SDA	SDA
D5	A0	Fixed to "VDD"
D4	/CS	/CS
D3	SDA	SDA
D2	SDA	SDA
D1	SDA	SDA
D0	SCK	SCK

For example, if 4-line SPI is selected, any one of D6, D3, D2, D1 hardware pins can be chose as serial data input terminal, they can be connected together or used alone. Please be noted that if any one hardware pin out of /CS, A0, D7 – D0 is not used, it must be fixed to "VDD".

With the SPI interface, the data is read from the serial data input (SDA) at the rising edge of the SPI clock (SCK). The SPI interface circuits treats the serial data in the order of D7, D6 … D0. Internally, data read from SDA is shifted in the internal 8-bit shift registers and would be processed as an 8-bit parallel data every 8th shifting clocks. When the A0 terminal is used, data is display data when A0 is high, and command data when A0 is low. When the A0 is not used, the LCD driver will receive command from MCU by default. If messages on the data pin are data rather than command, MCU should send Data direction command to control the data direction and then one more command to define the number of data bytes will be wrote. After these two continuous commands are sending, the following messages will be data rather than command. Serial data can be read on the rising edge of serial clock going into SCK and processed as 8-bit parallel data on the eighth serial clock. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string are handled as command data. This is referred in Figure 4 and 5.

Note that the above processing is enabled only when the chip select is active. When the chip is not active, the shift

registers and the counter are reset to their initial status. Please also be noted that the read operation is not available with the SPI interface mode. Caution is required on the SCK signal when it comes to line-end reflections and external noise. It is recommend that operation be rechecked on the actual equipment.

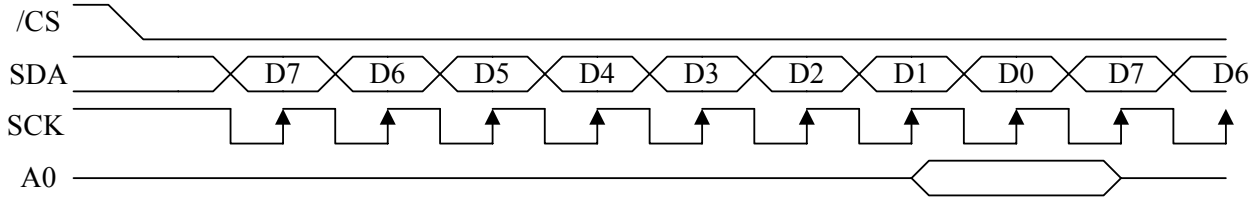

Figure 3 4-line SPI Timing

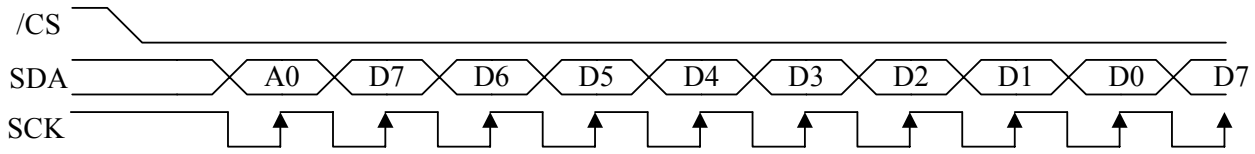

Figure 4 3-line SPI Timing

Display Data RAM

There is a static display data RAM (DDRAM) embedded in the TLS8204 chip supporting 102×68 dot-matrix display pattern storage. The internal DDRAM is constructed with 8pages×8bits + 1page×3bits + 1 line×1bit by 102 columns as shown in Figure 6. The DDRAM has a one-to-one correspondence to the dot-matrix display pixel.

Although MPU access and LCD access to the DDRAM could possibly happen simultaneously, the internal DDRAM response to the MPU access through the I/O buffer while process LCD reading request independently, enabling a flicker-free display.

The Page Address Circuit

Page address of the internal DDRAM is specified by the Page Address Set command. When the page to access is changed, the page address should be set again. Refer to Figure 6, the 10th page (page address 9) is a special page for icon display, it only contain 1 bit and D0 is used for data access.

The Column Addresses Circuit

Column address of the internal DDRAM is specified by the Column Address Set command. For continuously data access, the column address is automatically incremented by 1 with each data read/write command.

Register MX and MY selection command makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing MX select command.

Segment Output

MX	SEG0		SEG101
"0"	seg0	→ Segment Address →	seg101
"1"	seg101	← Segment Address ←	seg0

Common Output

MY	COM0	COM66	COMS
"0"	com0 → Common Address →	com66	coms
"1"	com66← Common Address ←	com0	coms

The Line Address Circuit

For liquid crystal displaying access, the DDRAM is addressed line by line. The content for first line display is determined by the start line address and is specified by the Start Line Address Set command. As shown in Figure 6, by changing the start line address, the display pattern can be swapped. By continuously increment or decrement the start line address, the screen scroll effect can be achieved.

Display Data Latch Circuit

The line of data to be displayed is temporarily stores in the display data latch. Because the normal/inverse display, display ON/OFF status and display all points ON/OFF is realized within the display data latch, the data within the DDRAM itself do not change.

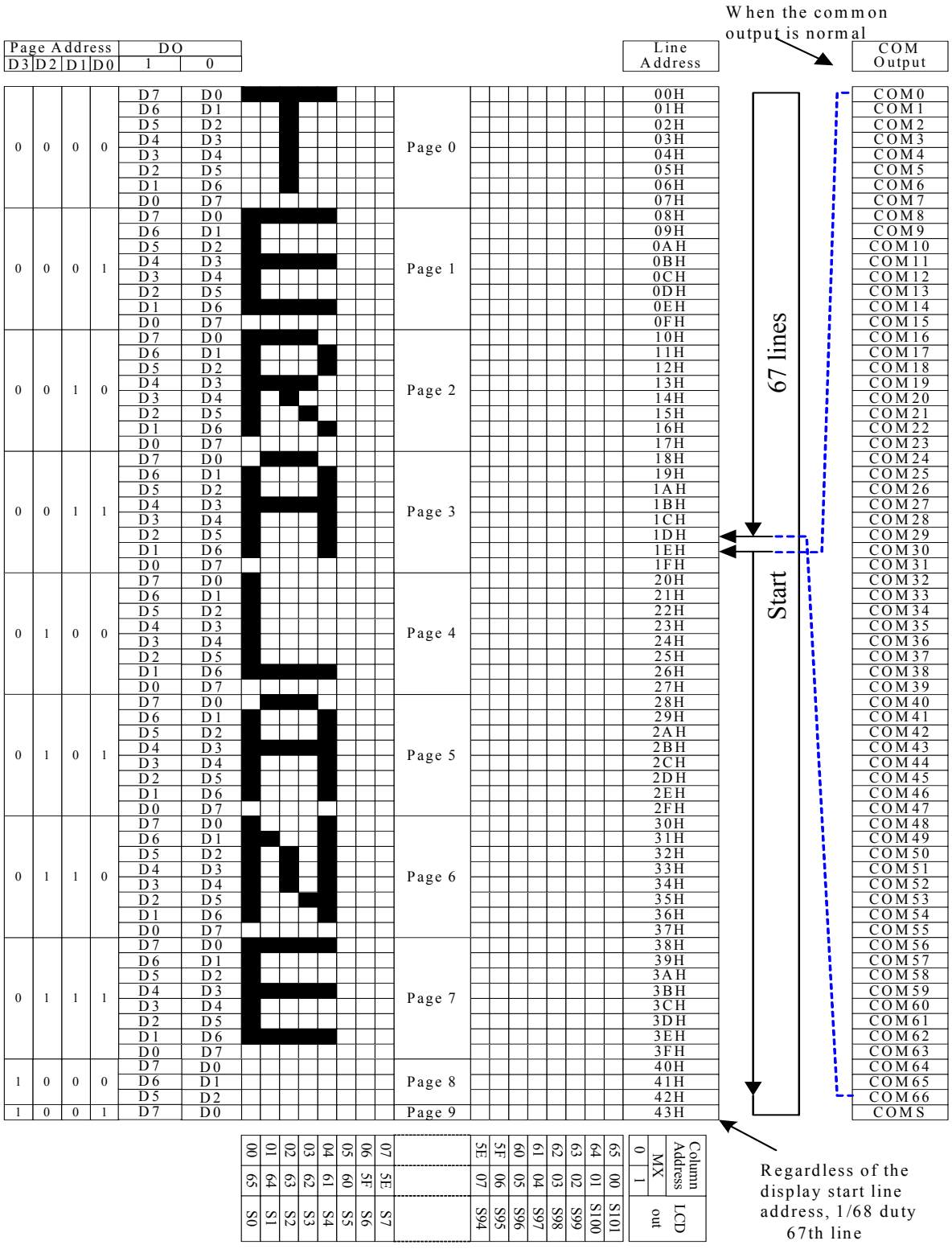

Figure 5 Display data RAM map (68 COM)

The Oscillator Circuit

There is an internal oscillator circuit that generates the display clock. The oscillator circuit is only enabled when OSCEN = “H”. External display clock is also accepted by the TLS8204 chip. In this case, set OSCEN = “L” to disable the internal oscillator circuit and the external clock is input through the OSC pin.

The Display Timing Controller Circuit

The timing of common scan and its synchronization with segment outputs is controlled by the display timing controller circuits. Based on display clock, the display data is read, latched and sent to the segment driver circuits in synchronous with the common scanning. Frame alternating polarity driving is provided to give an ac drive to liquid crystal displays. The driving polarity is inversed by every frame controlled by the alternating drive signal (FR) generated internally by the timing controller circuits. This is referred in Figure 7.

The LCD Driver Circuit

The driver circuits output the driving waveforms required by a liquid crystal display. The waveform is jointly determined by the common scan signal, display pattern and the FR signal. Figure 7 shows an example of the COM and SEG output waveforms.

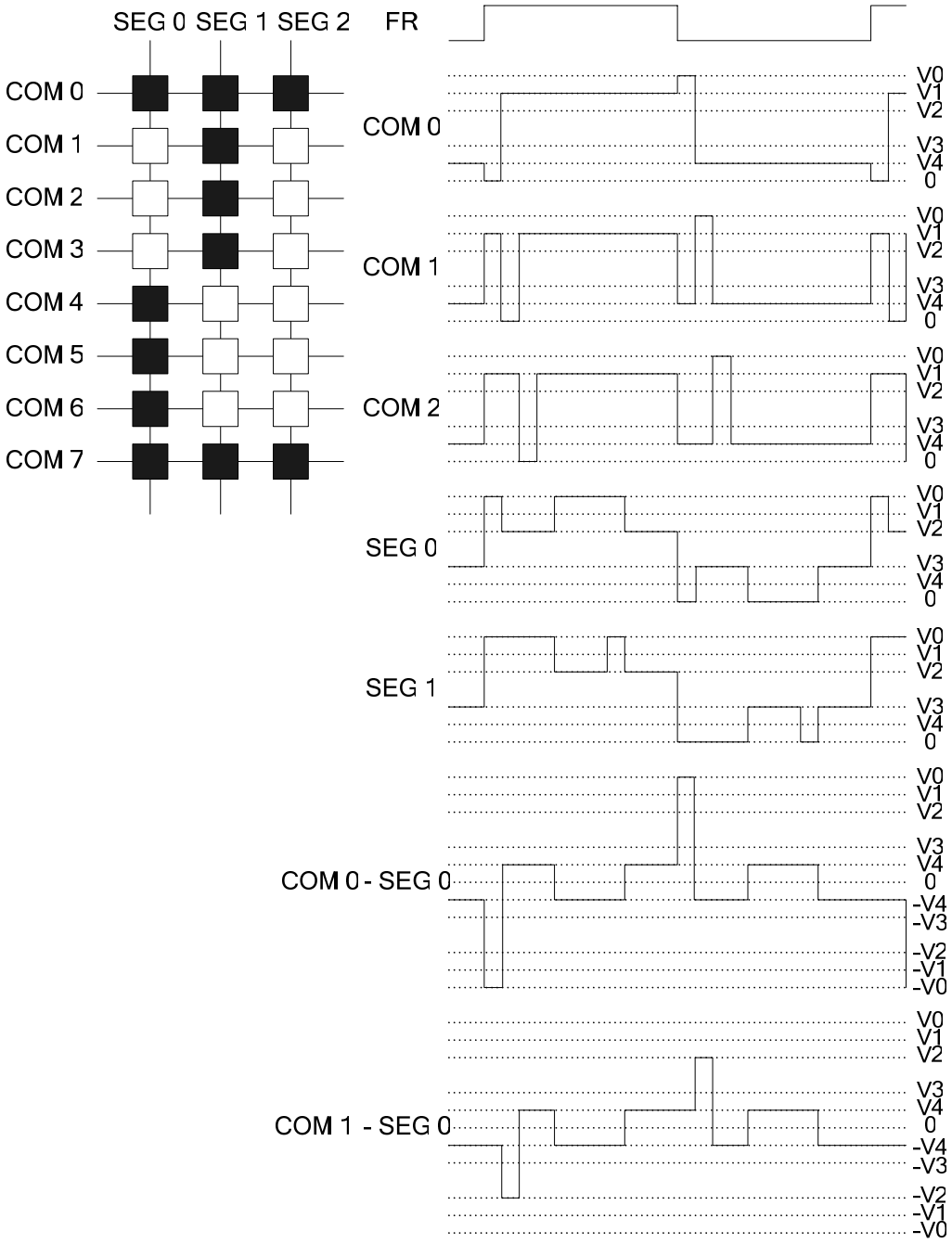

Figure 6 Example of COM and SEG waveform

The Partial Display on LCD

The TLS8204 incorporates the partial display function on LCD with low-duty driving for saving power consumption. To show the various display duty on LCD, LCD driving duty and bias are programmable by software.

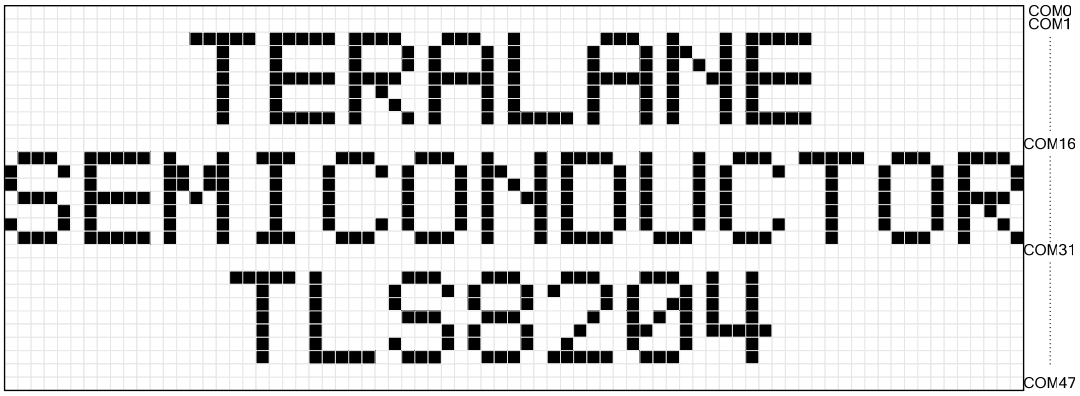

Figure 7 Reference example for Partial Display (full display case)

Figure 8 Reference example for Partial Display (Partial Display duty=32, initial COM0=0)

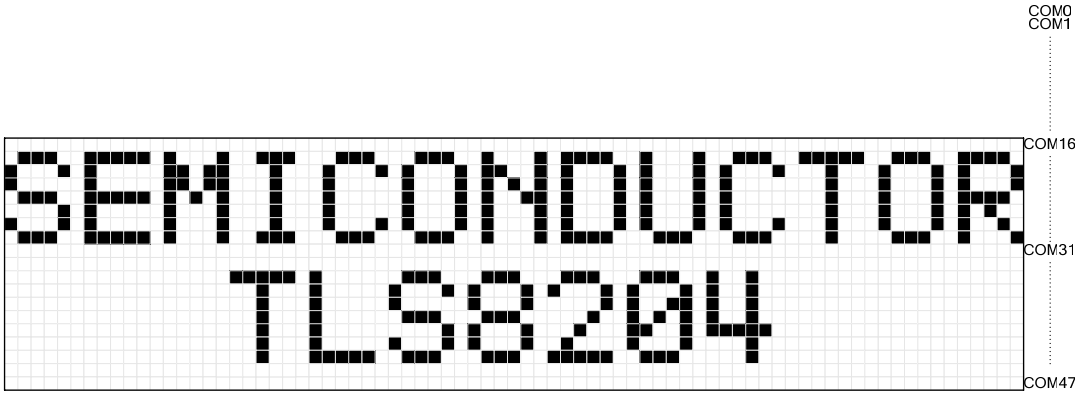

Figure 9 Reference example for Partial Display (Moving display, duty=32, initial COM0=16)

The One-Time-Programming (OTP) Calibration Mode

The TLS8204 embeds dual OTP for electric volume offset calibration. OTP is the method to eliminate the variations of LCD module in term of electric volumes so that every LCD module can achieve its best display performance. Figure 11 shows the functional diagram for OTP calibration. By default, the control data would be loaded from internal registers. Once the OTP1 be programmed, the control data would be automatically loaded from OTP1. Once the OTP2 be programmed, the control data would be automatically loaded from OTP2. Please be careful to program OTP1 before OTP2. If OTP2 has been programmed, the control data would be loaded from OTP2, no matter OTP1 has been programmed or not. Please also be noted that if the OTP1/OTP2 has not been programmed, the default value of the OTP1/OTP2 data read out would be all zero.

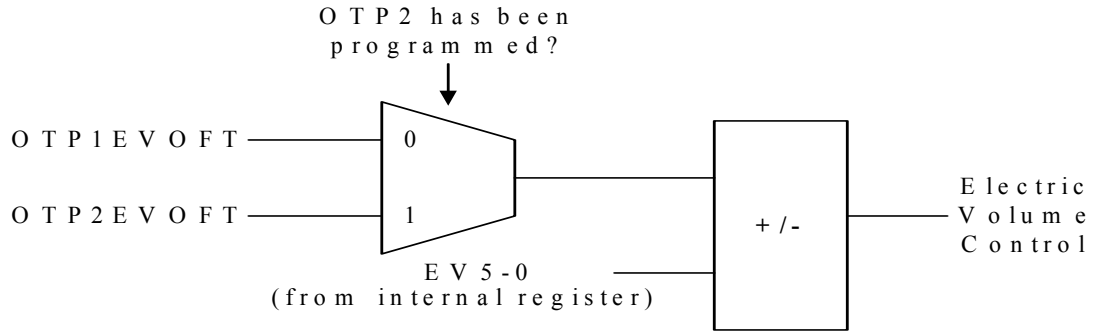

Figure 10 OTP Calibration for VLCD

The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the LCD drivers. They are Booster circuits, voltage regulator circuits, and voltage follower circuits. In TLS8204, the capacitors used for LCD driving voltages generator are built-in so that the least external capacitors are required.

The Reset Circuits

When the /RES input comes to the “L” level, these LSIs return to the default state. Their default states are as follows:

Page address: 0
Column address: 0
Display control: Display blank
COM Scan Direction MY: 0
SEG Select Direction MX: 0
DO=0
FR[2:0]=100
Oscillator: OFF
N-line inversion register: 0 (disable)
Power down mode (PD=1)
Normal command set (H[1:0]=00)
Display blank (E=D=0)
Address counter X[6:0]=0, Y[3:0]=0
Bias system (BS[2:0]=BR setting)
The HV generator is switched off
After power on , RAM data are undefined.

When /RES is “L” or soft reset command is executed, no command except read status can be accepted. With the soft reset command, the reset status appears at D0. After D0 becomes “L”, any command can be accepted. /RES must be connected to the reset pin of the MPU and initialize the MPU and this LSI at the same time. The initialization by /RES is essential before used.

COMMAND TABLE

H-independent											
Command	**A0**	**WR**	**D_7**	**D_6**	**D_5**	**D_4**	**D_3**	**D_2**	**D_1**	**D_0**	**Description**
NOP	0	0	0	0	0	0	0	0	0	0	No operation
Reserved	0	0	0	0	0	0	0	0	0	1	Do not use
Function Set	0	0	0	0	1	MX	MY	PD	H1	H0	
Read status byte	0	1	PD	0	0	D	E	MX	MY	DO	
Read data	1	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Write data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
OTP command mode	0	0	0	0	0	0	0	0	1	OM	Enter/exit OTP command mode
H1H0=00											
Command	**A0**	**WR**	**D_7**	**D_6**	**D_5**	**D_4**	**D_3**	**D_2**	**D_1**	**D_0**	**Description**
Set VLCD range	0	0	0	0	0	0	0	1	0	PRS	VLCD range select
End read modify	0	0	0	0	0	0	0	1	1	0	Release read modify write
Read modify write	0	0	0	0	0	0	0	1	1	1	RAM address R:+0; W:+1
Display Control	0	0	0	0	0	0	1	D	0	E	Sets display configuration
Reserved	0	0	0	0	0	1	0	0	*	*	Do not use
Set Y addr of RAM	0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0	
Set X addr of RAM	0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	
H1H0=01											
Command	**A0**	**WR**	**D_7**	**D_6**	**D_5**	**D_4**	**D_3**	**D_2**	**D_1**	**D_0**	**Description**
Set start line S6	0	0	0	0	0	0	0	1	0	S6	Set S6 for start line
Display Configure	0	0	0	0	0	0	1	DO	*	*	
System bias set	0	0	0	0	0	1	0	BS2	BS1	BS0	
Set start line	0	0	0	1	S5	S4	S3	S2	S1	S0	Set S5-S0 for start line
Set EVR	0	0	1	EV_6	EV_5	EV_4	EV_3	EV_2	EV_1	EV_0	Set electric volume register
H1H0=10											
Command	**A0**	**WR**	**D_7**	**D_6**	**D_5**	**D_4**	**D_3**	**D_2**	**D_1**	**D_0**	**Description**
Partial screen mode	0	0	0	0	0	0	0	1	0	PS	Partial screen enable
Partial screen size	0	0	0	0	0	0	1	0	0	WS	Set partial screen size
Display part	0	0	0	0	0	1	0	DP_2	DP_1	DP_0	Set display part for PM
H1H0=11											
Command	**A0**	**WR**	**D_7**	**D_6**	**D_5**	**D_4**	**D_3**	**D_2**	**D_1**	**D_0**	**Description**
RESET	0	0	0	0	0	0	0	0	1	1	Software reset
Frame frequency	0	0	0	0	0	0	1	FR_2	FR_1	FR_0	Frame rate control
Set Booster	0	0	1	0	0	1	BE_1	BE_0	PC_1	PC_0	Efficiency & stage
N line inversion	0	0	0	1	0	NL_4	NL_3	NL_2	NL_1	NL_0	Sets N line inversion
Read register/OTP	0	0	1	0	0	0	1	0	0	RO	Select read register or OTP
H-independent, OM=0 (OTP command mode)											
Command	**A0**	**WR**	**D_7**	**D_6**	**D_5**	**D_4**	**D_3**	**D_2**	**D_1**	**D_0**	**Description**
Write OTP data	0	0	0	0	0	0	0	0	0	1	Write the programming data
	0	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
OTP program mode	0	0	1	1	0	0	0	1	0	PRG	Enter/Exit OTP program mode
OTP program enable	0	0	1	1	0	0	0	1	1	PE	OTP program enable
Set OTP address	0	0	1	1	0	0	1	0	PA_1	PA_0	Set OTP programming address

COMMAND DESCRIPTION

The commands of TLS8204 are divided into several groups defined by H[1:0] register. A command can be correctly executed only when the H register is currently points to the corresponding H1H0 value which the command is belonged to. But for those commands that are H-independent, they can be correctly executed no matter what value the H register points to. Moreover, the OTP programming commands are only enabled at OTP command mode defined by OM register. Once OM=0, these OTP programming commands are valid independent of H register.

H independent Groups

Function Set

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	MX	MY	PD	H1	H0

Register	Description
MX	SEG bi-directional selection MX=0: normal direction (SEG0 → SEG101) MX=1: reverse direction (SEG101 → SEG0)
MY	COM bi-directional selection MY=0: normal direction (COM0 → COM66) MY=1: reverse direction (COM66 → COM0)
PD	PD=0: chip is active with normal function. PD=1: chip is step into power down mode. When the power down mode is stepped in: - All LCD outputs at V_{SS} (display off) - Bias generator and VLCD generator is turned off - Internal oscillator is turned off (external clock possible) - RAM contents not cleared - RAM data can be written
H1 H0	H1,H0 are used to select different command group. Follow the command table.

Note that the MX and MY register can be set through both this function set command and hardware configuration pin TMX and TMY. The MX and MY control registers is determined by:

MX (control register) = TMX (hardware pin) **OR** MX (software set)
MY (control register) = TMY (hardware pin) **OR** MY (software set)

For both MX and MY control registers, “0” specifies normal direction and “1” specifies reverse direction. That is, if the TMX pin is fixed to “H”, then the SEG output direction is always from SEG101 to SEG0 (reverse direction) no matter what is sent to MX by command; if the TMX pin is fixed to “L”, then the SEG output direction is determined by the software set value to MX, “0” for normal and “1” for reverse. It is very similar for MY control register, when TMY hardware pin is fixed to “H”, the common scan direction is reverse and can not be re-configured by software, and when it is fixed to “L”, whether the common scan direction is normal or reverse is determined by the command set.

Read status byte

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	PD	0	0	D	E	MX	MY	DO

The explanation for each flag is referred in command description sections for “Function set”, “Display control” and “Display configure” commands.

Read data

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor.

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Read data							

Write data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Write data							

NOP

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0

This command takes on operation.

OTP command mode

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1	OM

OM=0: OTP command mode. The OTP programming commands are become valid only during this mode.
OM=1: OTP command mode release.

H[1:0]=[0:0] Groups

Set VLCD range

This command sets the high or low range of VLCD. Refer to Figure 14.

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	PRS

PRS=0: VLCD range is set to low;
PRS=1: VLCD range is set to high.

The VLCD range can be set through both this command and hardware configuration pin /PRH. When /PRH is fixed to “L”, the VLCD high range is fixed, and the set VLCD range command can not change this status. When /PRH is fixed to “H”, the VLCD range is determined by this command.

Display control

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	0	E

The bits D and E select the display mode.

Registers		Description
D	E	
0	0	Display off
1	0	Normal display
0	1	All display segments on
1	1	Inverse video mode

Set Y address of RAM

Y [3:0] defines the Y address vector address of the display RAM.

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0

Y_3	Y_2	Y_1	Y_0	Content
0	0	0	0	Page 0 (display RAM)
0	0	0	1	Page 1 (display RAM)
0	0	1	0	Page 2 (display RAM)
0	0	1	1	Page 3 (display RAM)
0	1	0	0	Page 4 (display RAM)
0	1	0	1	Page 5 (display RAM)
0	1	1	0	Page 6 (display RAM)
0	1	1	1	Page 7 (display RAM)
1	0	0	0	Page 8 (display RAM)
1	0	0	1	Page 9 (display RAM)

Set X address of RAM

The X address points to the columns. The range of X is 0 … 101.

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0

The X[6:0] varies from 0 to 101 correspond to the column address from 0 to 101.

Read modify write

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1	1

This command is used paired with the “End read modify” command. Once this command has been input, the display data read command does not change the column and row address, but only the display data write command increments (+1) the address. This mode is maintained until the End read modify command is input. When the End read modify command is entered, the address returns to the address it was at when the read modify write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

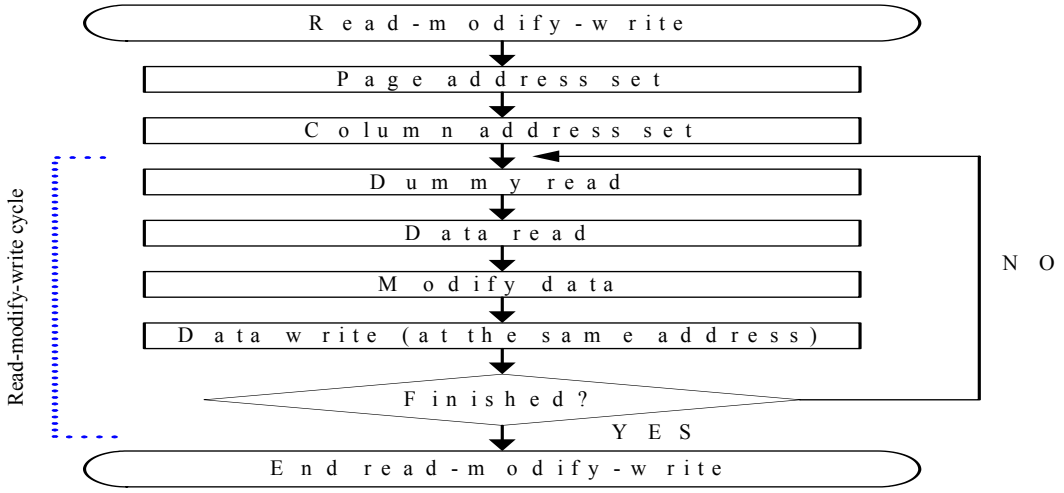

Figure 11 Command sequence using Read-modify-write mode

Note that other commands beside Display data read/write commands can also be used even in Read-modify-write mode.

End read modify

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1	0

This command releases the read/modify/write mode, and returns the column and row address to the address it was at when the mode was entered.

H[1:0]=[0:1] Groups

Display configuration

This command sets the data byte oriental in the display data RAM. As shown in Figure 13, the MSB is on the top side or the bottom side depends on the setting of the DO register.

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	DO	*	*

"*" refers to don't care bit.

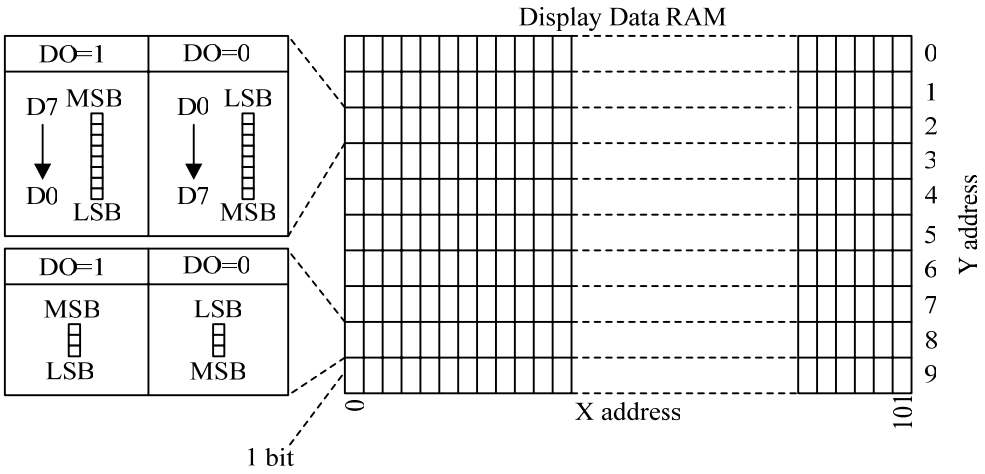

Figure 12 RAM data structure depends on the DO setting

System bias set

The command sets the system bias ratio.

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	BS_2	BS_1	BS_0

BS_2	BS_1	BS_0	Bias	Recommended Duty
0	0	0	11	1/100
0	0	1	10	1/81
0	1	0	9	1/65, 1/68
0	1	1	8	1/49
1	0	0	7	1/40, 1/36
1	0	1	6	1/24
1	1	0	5	1/18, 1/16
1	1	1	4	1/10, 1/9, 1/8

The TLS8204 chip give a R-R-nR-R-R bias system, where R = VLCD–V1 = V1–V2 = V3–V4 = V4–VSS and

nR=V2-V3. The bias ratio is calculated as 1/b=1/(n+4).

Set start line

This command sets the line address of display data RAM as the initial display line. The RAM display data is displayed at the top of row (COM0) of LCD panel. The S_6 must be defined first, and then defined S_5 to S_0.

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	S_6

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	S_5	S_4	S_3	S_2	S_1	S_0

The S_6-$_0$ sets the start line address. Because the line address of internal data RAM is addressed from 0-66 for MPU accessible display area, a value of S_6-$_0$ larger than 66 is not allowed.

Set EVR

This command sets the Electric Volume Register. The level of VLCD (=V0) voltage is determined by the Electric Volume Register. Different level of VLCD gives different contrast at human vision from liquid crystal display.

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	EV_6	EV_5	EV_4	EV_3	EV_2	EV_1	EV_0

In TLS8204, steps of contrast are divided into two parts: low VLCD range and high VLCD range. Which range is set to active depends on the setting of the PRS register that can be set by the set VLCD range command. The VLCD voltage can be programmed through software according to the formula as below:

$$VLCD = a + EV \times b$$

The parameters of “a” and “b” are explained in the table below.

Symbol	Value	Unit
a1	2.94 (PRS=0)	V
a2	6.75 (PRS=1)	V
b	0.03	V

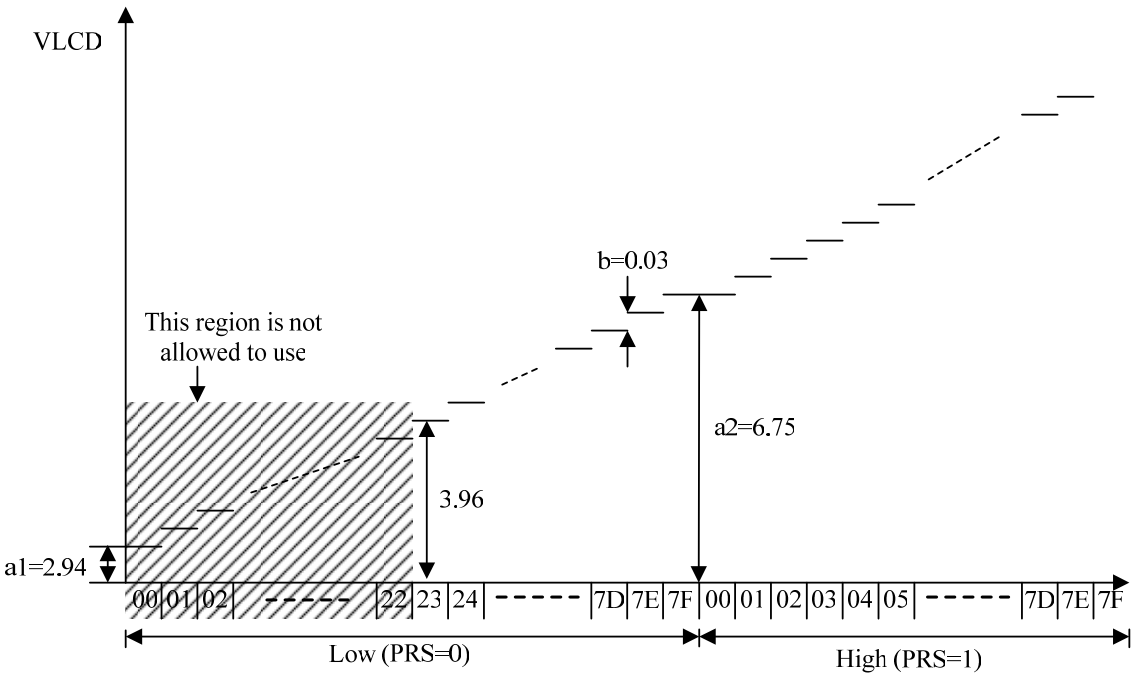

Figure 13 sketch of Electric Volume steps

The maximum VLCD level also depends on the VDD2 voltage and the display load current. For those situations that the higher VLCD voltage and larger load current are required, higher booster level and higher VDD2 level are also required; for those situations that relatively lower VLCD voltage is satisfied with the display performance, both the booster level and the VDD2 can be relatively lower so that the power consumption can be reduced.

When /PRH hardware pin is fixed to "H", two overlapping VLCD ranges are selectable via the set VLCD range command. For the low VLCD range (PRS=0) "a"=a1 and for the high VLCD range (PRS=1) "a"=a2 with steps equal to "b" in both ranges. During normal or partial display, the EV[6:0] can be programmed in the range of 00H-7FH while PRS=1 and in the range of 23H-7FH while PRS=0, giving a 220 steps of programmable contrast levels as shown in Figure 14.

When /PRH hardware pin is fixed to "L", only high range VLCD is valid.

Please be noted that:

*** When PRS and EV[6:0] is set to all zero, the internal booster circuits is turned off, no matter the /PRH pin is fixed to high or low.**

*** When low VLCD range is selected (PRS=0), the EV[6:0]≥ 23 should be kept. While PRS=0, if the EV[6:0] smaller than 23 is set (except for the case EV[6:0]=0), the VLCD will keep the volume determined by EV[6:0]=23.**

*** For the normal or partial display mode application, the VLCD level must be operated in the range of 4V to 9.5V. Situations that VLCD is lower than 4V or higher than 9.5V are only for testing.**

H[1:0]=[1:0] Groups

Partial screen mode

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	PS

Register	Description
PS	PS=0: Full display mode with MUX 1:68
	PS=1: Partial screen mode, the partial screen size of MUX 1:17 or 1:33 is determined by the WS register.

When enter Partial screen mode, COMS also works. The DDRAM position of COMS is at page9.

Partial screen size

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0	0	WS

Register	Description
WS	WS=0: Partial screen mode with MUX 1:17(16 Common + COMS)
	PS=1: Partial screen mode with MUX 1:33(32 Common + COMS)

Display Part

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	DP_2	DP_1	DP_0

The range of display common and DDRAM depends on the "WS" register . For example , if WS=1 and DP[2:0]=001, then display common is common 8 to common 39 and the DDRAM position is page 1 to page4 and COMS is at page9.

Moreover, the bottom of DP[2:0] is common 66, when the range is over common66, there will be no more common output to display. Thus, please set the DP[2:0] properly so that the last common address would not exceed the bottom address (common 66).

Registers	Status			Description	
				Display common	DDRAM position
DP_2 DP_1 DP_0	0	0	0	Start from common 0	Start from page 0
	0	0	1	Start from common 8	Start from page 1
	0	1	0	Start from common 16	Start from page 2
	0	1	1	Start from common 24	Start from page 3
	1	0	0	Start from common 32	Start from page 4
	1	0	1	Start from common 40	Start from page 5
	1	1	0	Start from common 48	Start from page 6
	1	1	1	Start from common 56	Start from page 7

H[1:0]=[1:1] Groups

Soft Reset

This command resets initial display line, column address, page address, and common output status select to their initial status .This command cannot initialize the LCD power supply, which is initialized by the RESB pin.

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1	1

Frame frequency

This command is used to set the frame frequency.

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	FR_2	FR_1	FR_0

Registers	Status			Description
				FR Frequency
FR_2 FR_1 FR_0	0	0	0	55 Hz ± 15%
	0	0	1	65 Hz ± 15%
	0	1	0	68 Hz ± 15%
	0	1	1	70 Hz ± 15%
	1	0	0	73 Hz ± 15%
	1	0	1	76 Hz ± 15%
	1	1	0	80 Hz ± 15%
	1	1	1	137 Hz ± 15%

By default, the $FR_{2\text{-}0}$ is 100.

Set N-line inversion

This command sets the N-line inversion method for liquid crystal ac drive.

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	NL_4	NL_3	NL_2	NL_1	NL_0

The TLS8204 chip incorporates the N-line inversion method to reduce the crosstalk effects on liquid crystal display and consequently to improve the display quality. The polarity of LCD driving waveform can be set to invert by the number of lines in the range from 3 to 33 depending on the setting of NL[4:0].

Please be noted that the N-line inversion mode will be disabled when partial display mode entered. After the partial

display mode end, the N-line inversion mode will return as it was.

Registers	Status						Description
							Selected n-line inversion
FR_2 FR_1 FR_0	0	0	0	0	0	0	0-line inversion (frame inversion)
	0	0	0	0	0	1	3-line inversion
	0	0	0	0	1	0	4-line inversion
	0	0	0	0	1	1	5-line inversion
	:	:	:	:	:	:	:
	1	1	1	1	1	0	32-line inversion
	1	1	1	1	1	1	33-line inversion

Set Booster

This command sets the booster efficiency and the boosting level.

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	BE_1	BE_0	PC_1	PC_0

With the internal voltage booster circuits, higher VLCD level generally consumes larger power. In TLS8204, software configuration of booster efficiency and booster level is allowed so that the optimized trade-off between the VLCD level and the power consumption can be achieved according to the application requirements. Four levels of booster efficiency can be set by BE[1:0]. Using lower booster efficiency level will get lower VLCD and lower power consumption. The booster efficiency level 2 is the default setting of the TLS8204 chip. The boosting level can be set to 5X, 4X, 3X, 2X. The default value of boosting level after hardware reset (/RES) is decided by the "CP" pin. 5X boosting level mode will be the default setting if CP is connected to "H", otherwise, the default boosting level will be 4X when CP = "L".

Flag	Status		Description
BE_1 BE_0	BE_1	BE_0	Selecting booster efficiency level
	0	0	Booster Efficiency level 4
	0	1	Booster Efficiency level 3
	1	0	Booster Efficiency level 2 (by default)
	1	1	Booster Efficiency level 1
PC_1 PC_0	PC_1	PC_0	Selecting boosting level
	0	0	2X boosting level
	0	1	3X boosting level
	1	0	4X boosting level
	1	1	5X boosting level

OTP Programming Commands

NOTE: The OTP programming commands below are H-independent and are only valid at OTP command mode (OM=0).

OTP Program Mode

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	0	1	0	PRG

PRG = 1: Enter OTP programming mode.
PRG = 0: Exit OTP programming mode.

Refer to the section of "VLCD Calibration by OTP" for details.

OTP Program Enable

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	0	1	1	PE

At OTP programming mode (PRG=1), set PE = "1" to write the program data into OTP memory, after the program data is wrote into the OTP memory, the PE should be released to "0". To assure reliable program write operation, the programming address and data sent to OTP memory should keep stable during PE is high. Thus, the OTP address and program data should be sent before set PE=1, and set PE=0 before new OTP address or data are sent.

Refer to the section of "VLCD Calibration by OTP" for details.

Set OTP Address

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	1	0	PA_1	PA_0

This command set the OTP programming address. The embedded dual OTP uses 2 bits address, PA1-0. The address map is as below:

OTP1

PA[1:0]	PD07	PD06	PD05	PD04	PD03	PD02	PD01	PD00
00	Reserved							

PA[1:0]	PD23	PD22	PD21	PD20	PD19	PD18	PD17	PD16
10	Reserved		OTP1EVOFT5-0					

OTP2

PA[1:0]	PD15	PD14	PD13	PD12	PD11	PD10	PD09	PD08
01	Reserved							

PA[1:0]	PD23	PD22	PD21	PD20	PD19	PD18	PD17	PD16
11	Reserved		OTP2EVOFT5-0					

Write OTP data

A0	/WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	1
0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

This command is used to write program data while OTP programming. This is a double-byte command. During OTP command mode, once 01H is sent, the write OTP data mode is entered, the next 8 bit byte sent to the TLS8204 chip would be recognized as the OTP data to be programmed. The write OTP data mode is released once the DB7-DB0 is sent.

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Initialization Sequence of Power Supply Circuits

(Reference Example)

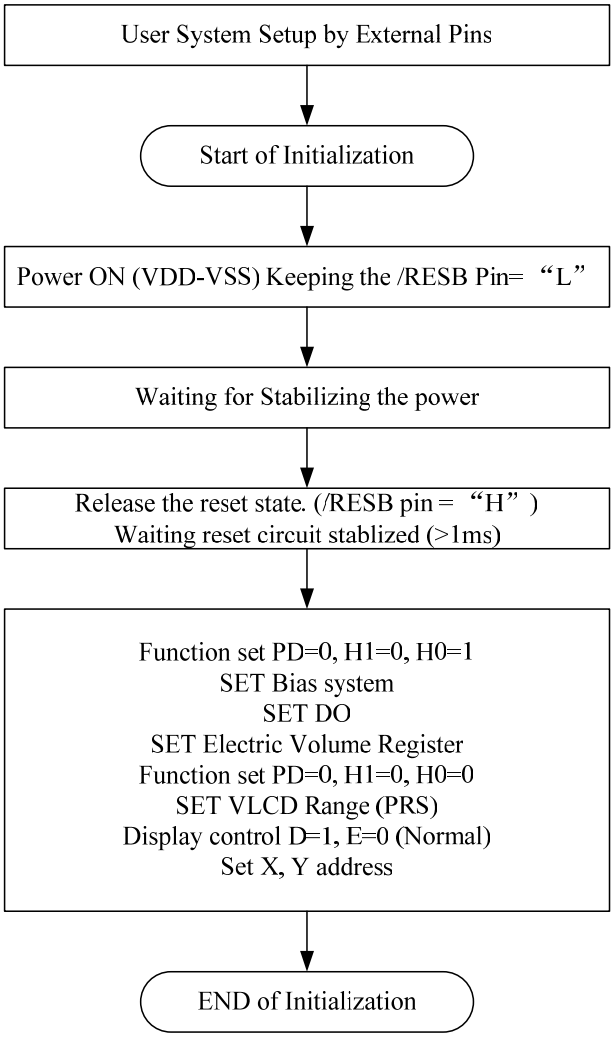
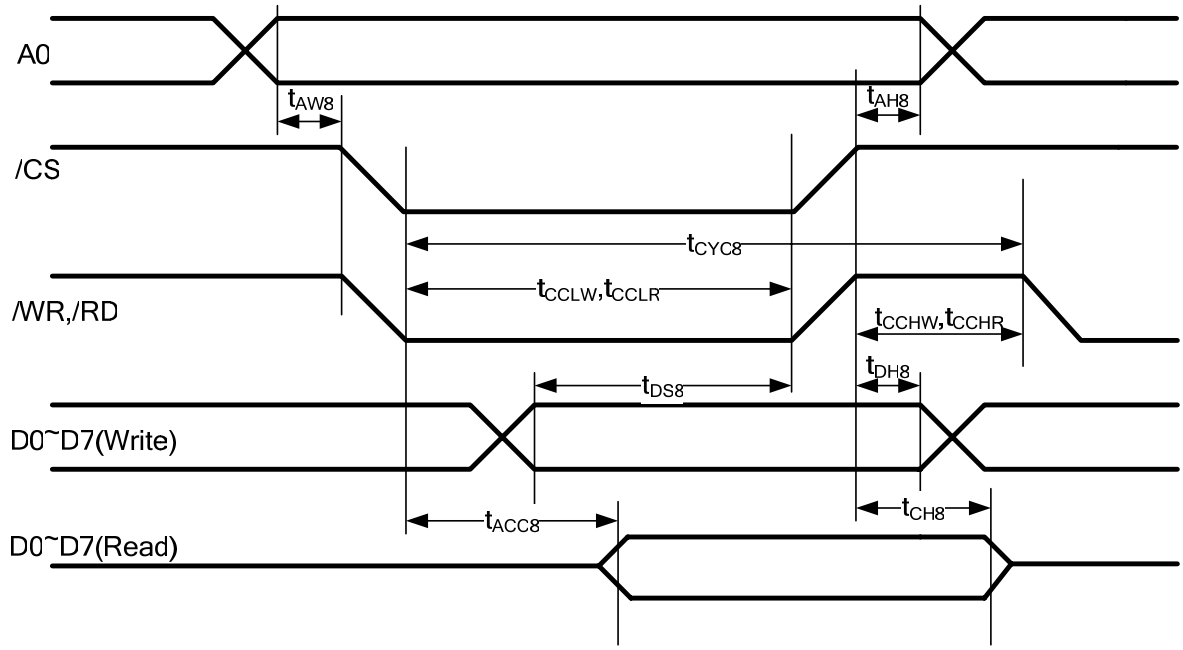


Figure 14 Reference example for build-in power supply circuits initialization command flow

AC CHARACTERISTICS

System Buses Read/Write Timing Characteristics (for 8080 Series MPU)



(VDD = 3.3V, Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		10	--	ns
Address setup time		t_{AW8}		100	--	
System cycle time		t_{CYC8}		400	--	
Enable L pulse width (WRITE)	/WR	t_{CCLW}		80	--	
Enable H pulse width (WRITE)		t_{CCHW}		80	--	
Enable L pulse width (READ)	/RD	t_{CCLR}		140	--	
Enable H pulse width (READ)		t_{CCHR}		80	--	
WRITE Data setup time	D0 to D7	t_{DS8}		80	--	
WRITE Address hold time		t_{DH8}		10	--	
READ access time		t_{ACC8}	CL = 100 pF	--	70	
READ Output disable time		t_{OH8}	CL = 100 pF	5	50	

(VDD = 2.8V,Ta = –30 to 85℃)

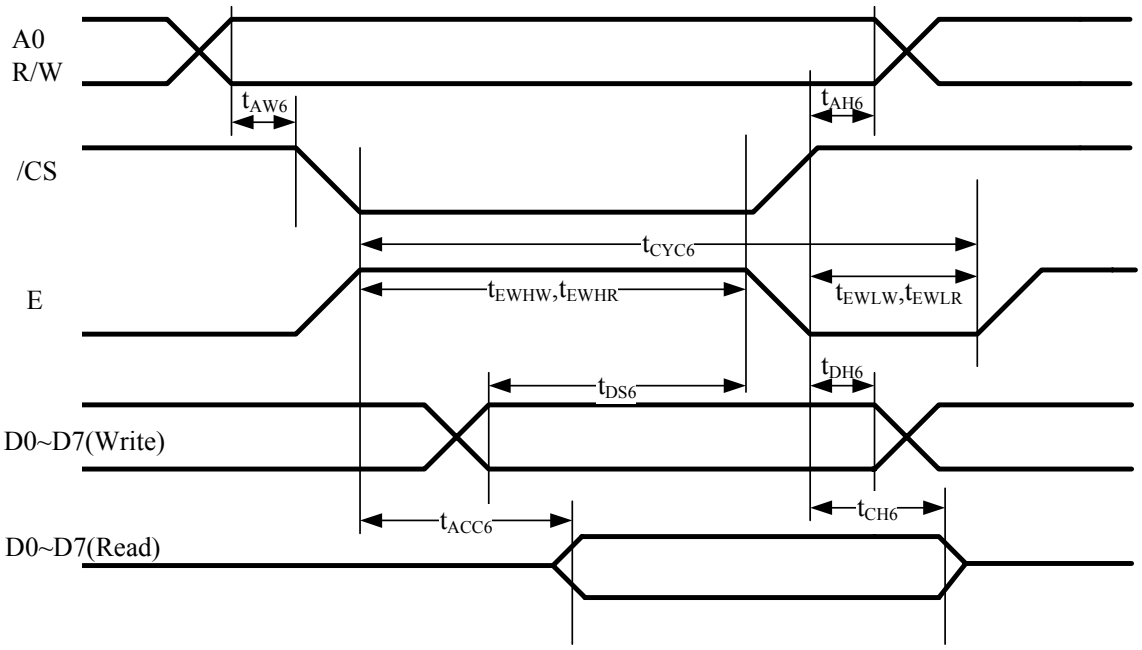
Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		15	--	ns
Address setup time		t_{AW8}		150	--	
System cycle time		t_{CYC8}		600	--	
Enable L pulse width (WRITE)	/WR	t_{CCLW}		220	--	
Enable H pulse width (WRITE)		t_{CCHW}		180	--	
Enable L pulse width (READ)	/RD	t_{CCLR}		220	--	
Enable H pulse width (READ)		t_{CCHR}		180	--	
WRITE Data setup time	D0 to D7	t_{DS8}		120	--	
WRITE Address hold time		t_{DH8}		15	--	
READ access time		t_{ACC8}	CL = 100 pF	--	140	
READ Output disable time		t_{OH8}	CL = 100 pF	10	100	

(VDD = 1.8V,Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		30	--	ns
Address setup time		t_{AW8}		200	--	
System cycle time		t_{CYC8}		1000	--	
Enable L pulse width (WRITE)	/WR	t_{CCLW}		360	--	
Enable H pulse width (WRITE)		t_{CCHW}		280	--	
Enable L pulse width (READ)	/RD	t_{CCLR}		360	--	
Enable H pulse width (READ)		t_{CCHR}		280	--	
WRITE Data setup time	D0 to D7	t_{DS8}		200	--	
WRITE Address hold time		t_{DH8}		30	--	
READ access time		t_{ACC8}	CL = 100 pF	--	240	
READ Output disable time		t_{OH8}	CL = 100 pF	10	200	

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less, When the system cycle time is extremely fast, $(tr + tf) \leqq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $(tr + tf) \leqq (t_{CYC8} - t_{CCLR} - t_{CCHR})$ are specified.
2. All timing is specified using 20% and 80% of VDD as the reference.
3. t_{CCLW} and t_{CCLR} are specified as the overlap interval when /CS is low and /WR or /RD is low.

System Bus Read/Write Timing Characteristics 2 (For the 6800 Series MPU)



(VDD = 3.3V,Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Address hold time	A0	t_{AH6}		10	--	ns
Address setup time		t_{AW6}		0	--	
System cycle time		t_{CYC6}		240	--	
Enable L pulse width (WRITE)	/WR	t_{EWLW}		80	--	
Enable H pulse width (WRITE)		t_{EWHW}		80	--	
Enable L pulse width (READ)	/RD	t_{EWLR}		80	--	
Enable H pulse width (READ)		t_{EWHR}		140	--	
WRITE Data setup time	D0 to D7	t_{DS6}		80	--	
WRITE Address hold time		t_{DH6}		10	--	
READ access time		t_{ACC6}	CL = 100 pF	--	70	
READ Output disable time		t_{OH6}	CL = 100 pF	5	50	

(VDD = 2.7V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Address hold time	A0	t_{AH6}		15	--	ns
Address setup time		t_{AW6}		0	--	
System cycle time		t_{CYC6}		400	--	
Enable L pulse width (WRITE)	/WR	t_{EWLW}		220	--	
Enable H pulse width (WRITE)		t_{EWHW}		180	--	
Enable L pulse width (READ)	/RD	t_{EWLR}		220	--	
Enable H pulse width (READ)		t_{EWHR}		180	--	
WRITE Data setup time	D0 to D7	t_{DS6}		120	--	
WRITE Address hold time		t_{DH6}		15	--	
READ access time		t_{ACC6}	CL = 100 pF	--	140	
READ Output disable time		t_{OH6}	CL = 100 pF	10	100	

(VDD = 1.8V,Ta = –30 to 85°C)

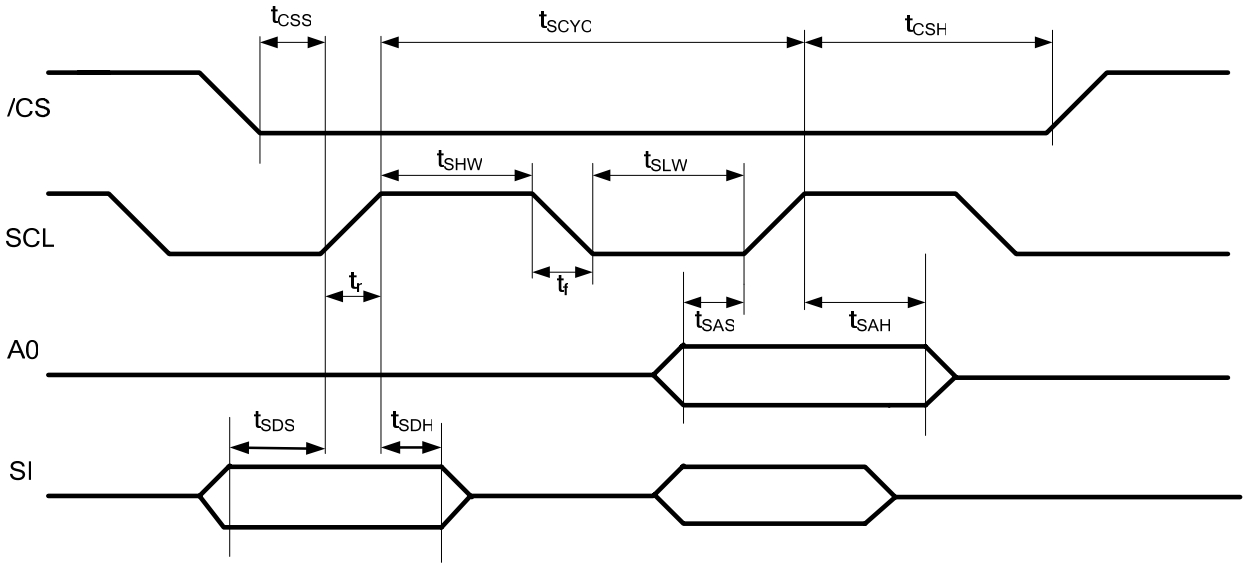
Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Address hold time	A0	t_{AH6}		30	--	ns
Address setup time		t_{AW6}		0	--	
System cycle time		t_{CYC6}		640	--	
Enable L pulse width (WRITE)	/WR	t_{EWLW}		360	--	
Enable H pulse width (WRITE)		t_{EWHW}		280	--	
Enable L pulse width (READ)	/RD	t_{EWLR}		360	--	
Enable H pulse width (READ)		t_{EWHR}		280	--	
WRITE Data setup time	D0 to D7	t_{DS6}		200	--	
WRITE Address hold time		t_{DH6}		30	--	
READ access time		t_{ACC6}	CL = 100 pF	--	240	
READ Output disable time		t_{OH6}	CL = 100 pF	10	200	

1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) or (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

2 All timing is specified using 20% and 80% of VDD as the reference.

3 tEWLW and tEWLR are specified as the overlap between /CS being “L” and E is how.

4-line Serial Interface Timing



(VDD = 3.3V,Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
4-line SPI Clock Period	SCK	t_{SCYC}		150	--	ns
SCK “H” pulse width		t_{SHW}		75	--	
SCK “L” pulse width		t_{SLW}		75	--	
Address setup time	A0	t_{SAS}		20	--	
Address hold time		t_{SAH}		100	--	
Data setup time	SDA	t_{SDS}		20	--	
Data hold time		t_{SDH}		10	--	
CS-SCK time	/CS	t_{CSS}		20	--	
CS-SCK time		t_{CSH}		140	--	

(VDD = 2.8V,Ta = –30 to 85℃)

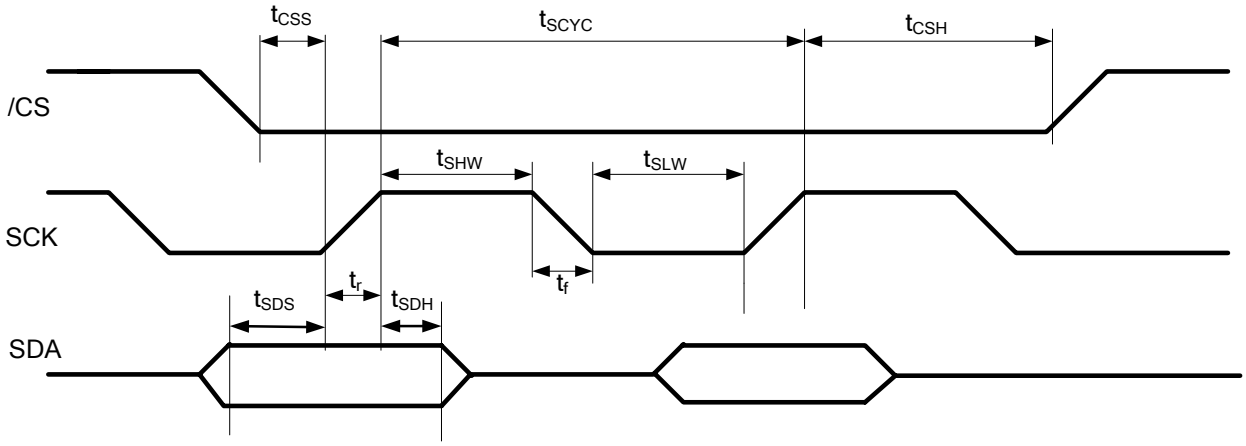
Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
4-line SPI Clock Period	SCK	t_{SCYC}		300	--	ns
SCK “H” pulse width		t_{SHW}		150	--	
SCK “L” pulse width		t_{SLW}		150	--	
Address setup time	A0	t_{SAS}		30	--	
Address hold time		t_{SAH}		150	--	
Data setup time	SDA	t_{SDS}		30	--	
Data hold time		t_{SDH}		20	--	
CS-SCK time	/CS	t_{CSS}		30	--	
CS-SCK time		t_{CSH}		200	--	

(VDD = 1.8V,Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
4-line SPI Clock Period	SCK	t_{SCYC}		500	--	ns
SCK “H” pulse width		t_{SHW}		250	--	
SCK “L” pulse width		t_{SLW}		250	--	
Address setup time	A0	t_{SAS}		60	--	
Address hold time		t_{SAH}		250	--	
Data setup time	SDA	t_{SDS}		60	--	
Data hold time		t_{SDH}		50	--	
CS-SCK time	/CS	t_{CSS}		40	--	
CS-SCK time		t_{CSH}		350	--	

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD as the standard.

3-line Serial Interface Timing



(VDD = 3.3V,Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
4-line SPI Clock Period	SCK	t_{SCYC}		150	--	ns
SCK “H” pulse width		t_{SHW}		75	--	
SCK “L” pulse width		t_{SLW}		75	--	
Data setup time	SDA	t_{SDS}		20	--	
Data hold time		t_{SDH}		10	--	
CS-SCK time	/CS	t_{CSS}		20	--	
CS-SCK time		t_{CSH}		140	--	

(VDD = 2.8V,Ta = –30 to 85℃)

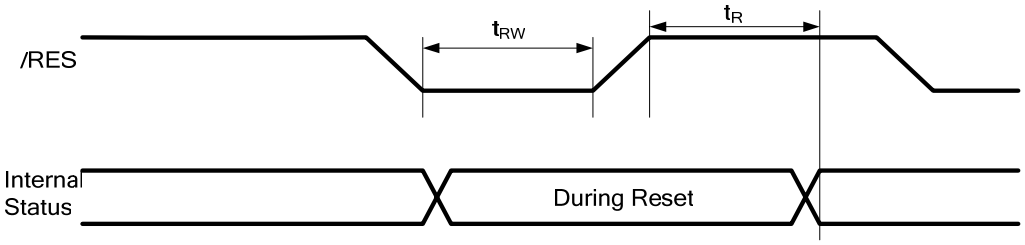
Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
4-line SPI Clock Period	SCK	t_{SCYC}		300	--	ns
SCK “H” pulse width		t_{SHW}		150	--	
SCK “L” pulse width		t_{SLW}		150	--	
Data setup time	SDA	t_{SDS}		30	--	
Data hold time		t_{SDH}		20	--	
CS-SCK time	/CS	t_{CSS}		30	--	
CS-SCK time		t_{CSH}		200	--	

(VDD = 1.8V,Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
4-line SPI Clock Period	SCK	t_{SCYC}		500	--	ns
SCK “H” pulse width		t_{SHW}		250	--	
SCK “L” pulse width		t_{SLW}		250	--	
Data setup time	SDA	t_{SDS}		60	--	
Data hold time		t_{SDH}		50	--	
CS-SCK time	/CS	t_{CSS}		40	--	
CS-SCK time		t_{CSH}		350	--	

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD as the standard.

Reset Timing



(VDD = 1.8 ~ 3.3V, Ta = 25℃)

Item	Symbol	Condition	Rating		Unit
			Min.	Max.	
Reset time	tR		--	3.0	µs
Reset low pulse width	tRW	/RES	3.0	--	µs

DC CHARACTERISTICS

(Unless otherwise specified, V_{DD}=3.0V,VSS=0, TA = -30 to 85 ºC)

Symbol	Parameter	Condition		Min	Type	Max	Unit
V_{DD}	Logic Supply Voltage			1.8	-	3.3	V
V_{DD2}	Analog Supply Voltage			2.4	-	3.3	V
V_{LCD}	LCD Operating Voltage			-	-	10.5	V
V_{RS}	Reference Voltage			-	2.10	-	V
V_{OH}	High Logic Output Level			0.8*V_{DD}	-	V_{DD}	V
V_{OL}	Low Logic Output Level			0	-	0.2*V_{DD}	V
V_{IH}	High Logic Input Level	I_{OH} = -0.5mA		0.8*V_{DD}	-	V_{DD}	V
V_{IL}	Low Logic Input Level	I_{OL} = 0.5mA		0	-	0.2*V_{DD}	V
I_{LI}	Input leakage Current			-1.0	-	1.0	uA
I_{LO}	Output leakage Current			-3.0	-	3.0	uA
I_{DD}	Dynamic Current Consumption	Power down mode		-	0.01	TBD	uA
		V_{DD}=V_{DD2}=3.0V, V_{LCD}-V_{SS}=9.0 V, bias=1/9, boosting level 4x, displaying all ON pattern, Ta =25 ºC, with out panel		-	TBD	TBD	uA
		V_{DD}=V_{DD2}=3.0V, V_{LCD}-V_{SS}=9.0 V, bias=1/9, boosting level 4x, displaying checker pattern, Ta=25 ºC, with out panel		-	TBD	TBD	uA
R_{ON}	Liquid Crystal Driver ON Resistance	Ta=25℃ (Relative to V_{SS})	V_{LCDIN}= 10V	-	2.0	TBD	KΩ
			V_{LCDIN} =8V	-	3.2	TBD	KΩ
C_{IN}	Input Terminal Capacitance	Ta=25℃ Freq= 1MHZ		-	5	8	pF
FR	Frame frequency			TBD	73	TBD	Hz

ABSOLUTE MAXIMUM RATING

Item	Symbol	Rating	Unit
Power Supply voltage	V_{DD}	-0.3 to 3.6	V
	V_{DD2}	-0.3 to 3.6	V
	V_{LCD}	-0.3 to 13.5	V
	V1, V2, V3, V4	-0.3 to V_{LCD}	V
Operating Temperature	T_A	-30 to +85	ºC
Storage Temperature(Bare chip)	T_{stg}	-65 to +150	ºC

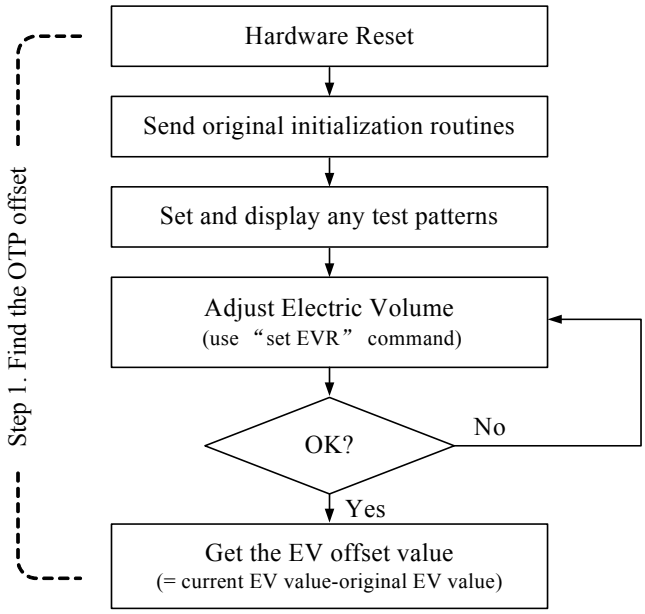
Comments

Notes and Cautions

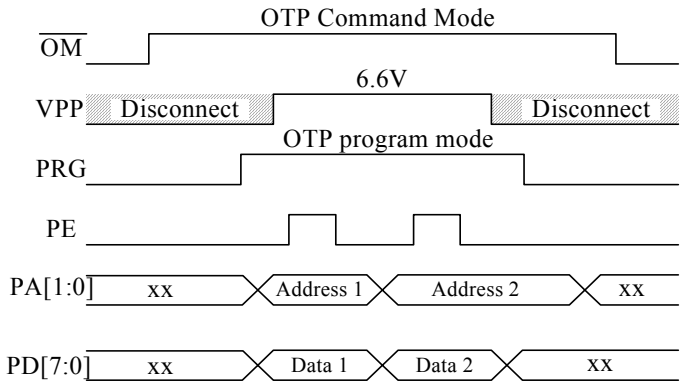
1. The V_{DD2}, V_0 to V_4 and V_{OUT} are relative to the V_{SS} = 0V reference.
2. Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that $V_{OUT} \geqq V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4$.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

VLCD Calibration by OTP

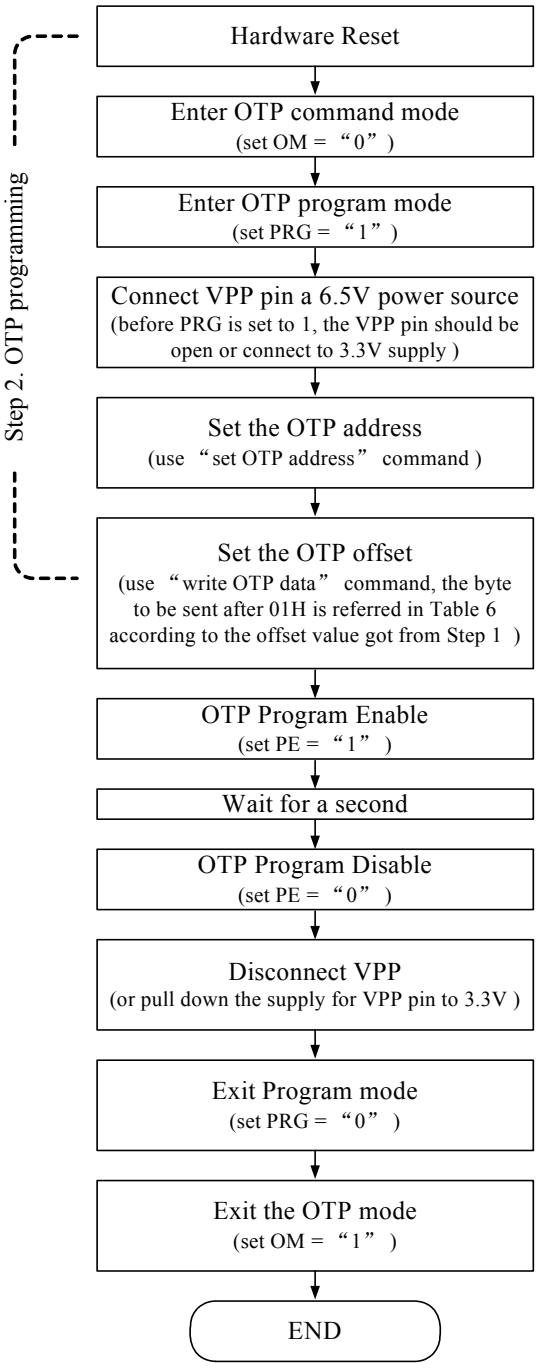
Generally, the operation voltage V_{OP} for different panels has a normal distribution. With one-time-programming method, the difference of display performance can be minimized. Besides, the OTP calibration method is also an effective way to minimize the variations of IC's characteristics due to the process. The TLS8204 incorporates dual OTP for fine calibration of electric volumes. When OTP is used for VLCD calibration, there are two major steps to do this. The first step is to find the offset value, and the second is to program the OTP.



(a) Step 1 : Find the OTP offset



(b) OTP Program signal sequence



(c) Step 2 : OTP programming flow

Figure 15 use of OTP for VLCD calibration

Step 1 – Find the OTP offset

With TLS8204, it is available to trim the VLCD electric volume by +/- 31 steps. The data stored in OTP1EVOFT

and OTP2EVOFT is essentially the offset value.

Table 6

OTP1EVOFT / OTP2EVOFT						Offset value
DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	Original
0	0	0	0	0	1	-1 step
0	0	0	0	1	0	-2 steps
0	0	0	0	1	1	-3 steps
:	:	:	:	:	:	:
:	:	:	:	:	:	:
0	1	1	1	1	0	-30 steps
0	1	1	1	1	1	-31 steps
1	0	0	0	0	0	Original
1	0	0	0	0	1	+1 step
1	0	0	0	1	0	+2 steps
1	0	0	0	1	1	+3 steps
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	+30 steps
1	1	1	1	1	1	+31 steps

The function of OTP1EVOFT and OTP2EVOFT is the same; OTP2 is provided so that there is one more chance to modify the offset value.

To find the EV offset for specific panel, use the “set EVR” command to adjust the electric volume until the best quality is achieved, and the offset value just equals the electric volume value with best performance subtract the original value set in the initialization code. See Figure 16.

Step 2 – OTP Programming

Figure 16(b) shows the program cycle of OTP. The programming sequence is shown in Figure 16(c). For each bit of OTP memory, it can be programmed from “0” to “1” for one time.

Notes:

(1) The command sequence shown in Figure 16 should be strictly followed when program the OTP, otherwise, unexpected errors may be caused.

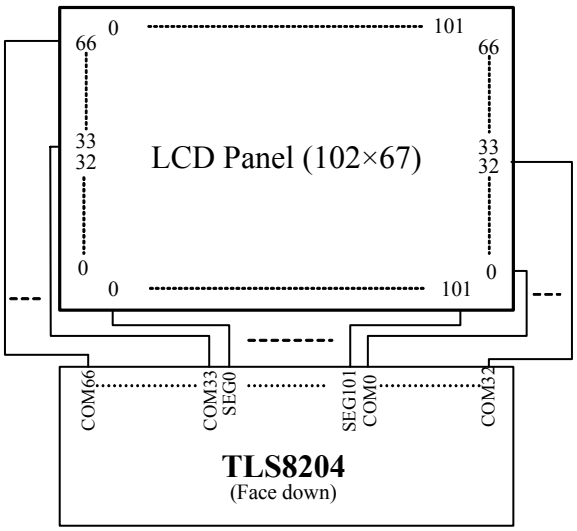
(2) After the OTP programming flow performed, the programmed memory will be valid after next hardware reset.

(3) Once OTP2 has been programmed, the OTP data would always be loaded from OTP2, no matter OTP1 has been programmed or not. So please program the OTP1 in prior.

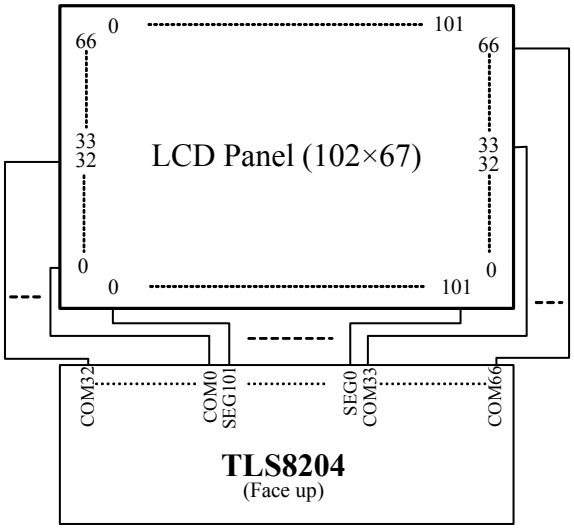
APPLICATION NOTES

Application Information for LCD Panel (Reference Example)

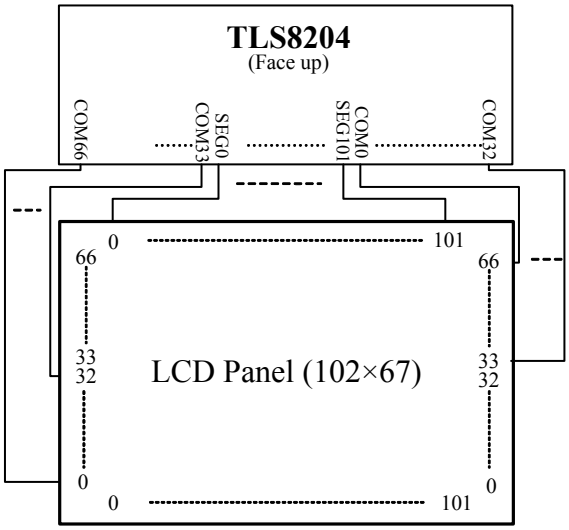
Case1. MX=0, MY=0



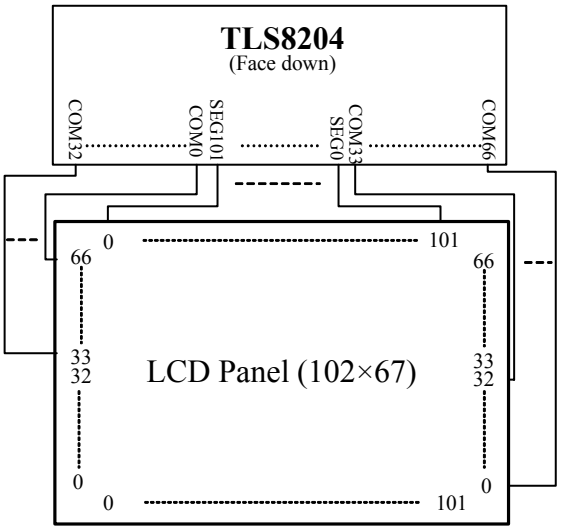
Case2. MX=1, MY=0



Case3. MX=0, MY=1

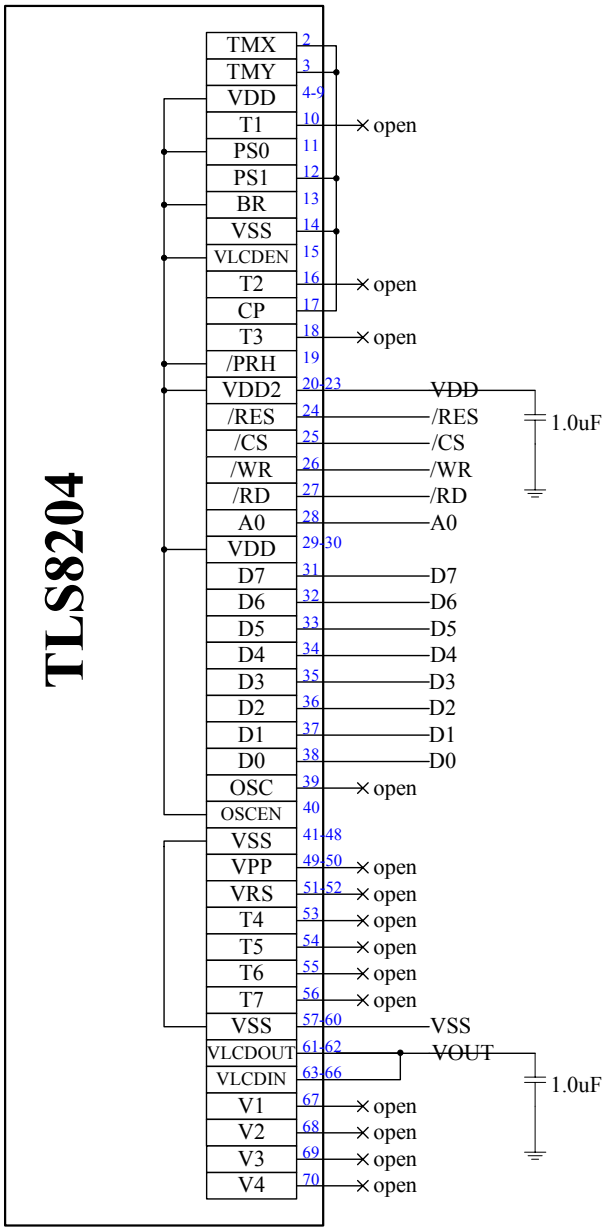


Case4. MX=1, MY=1

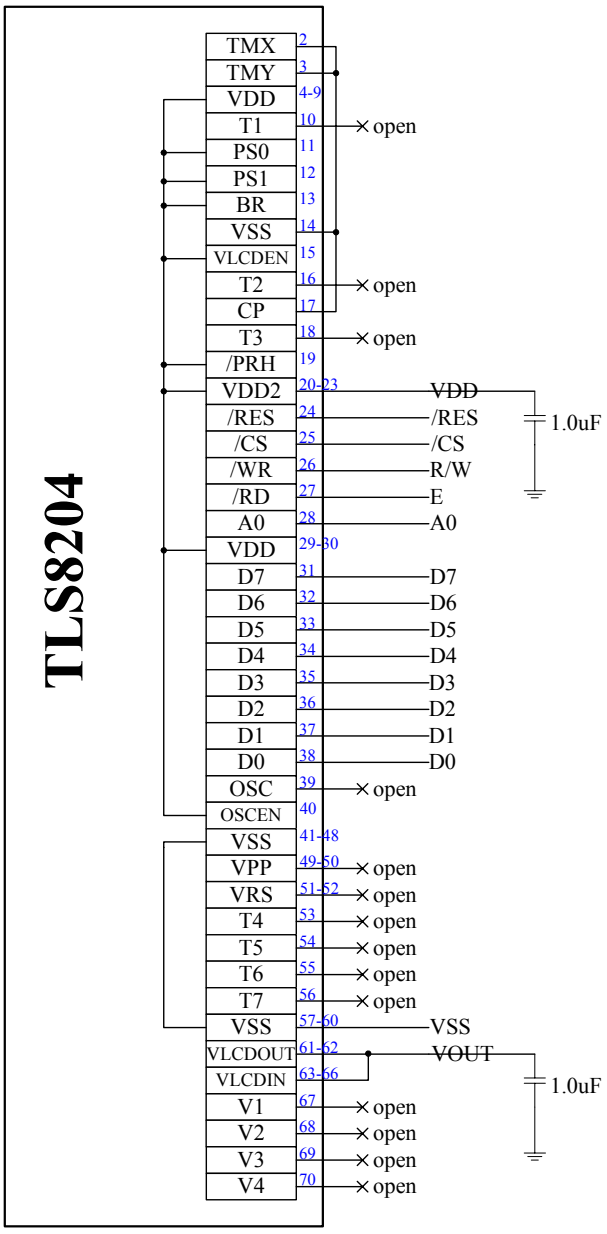


Application Information for Pin Connection to MPU (Reference Example)

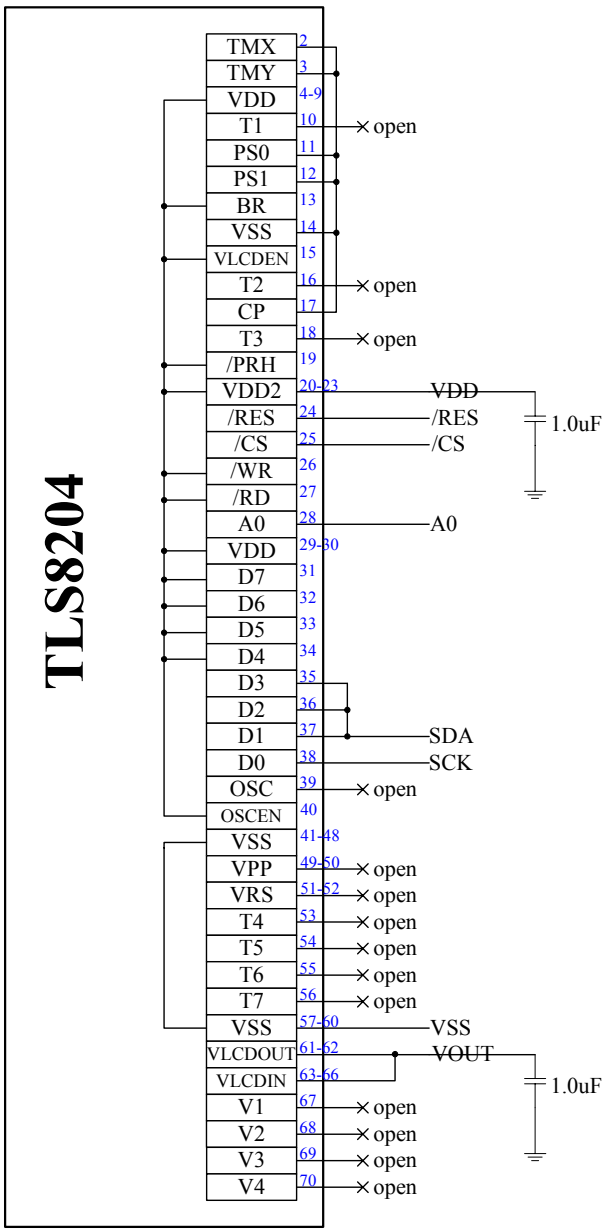
8080 series interface
Internal Power supply circuits
Internal Oscillator
Configuration pins:
CP: VSS (4X boosting level by default)
BR: VDD (1/9 bias by default)
TMX: VSS (normal SEG output direction and can be re-configured by software)
TMY: VSS (COM scan direction is normal and can be re-configured by software)
/PRH: VDD (Enable both high- and low- LCD range)
C=1.0uF



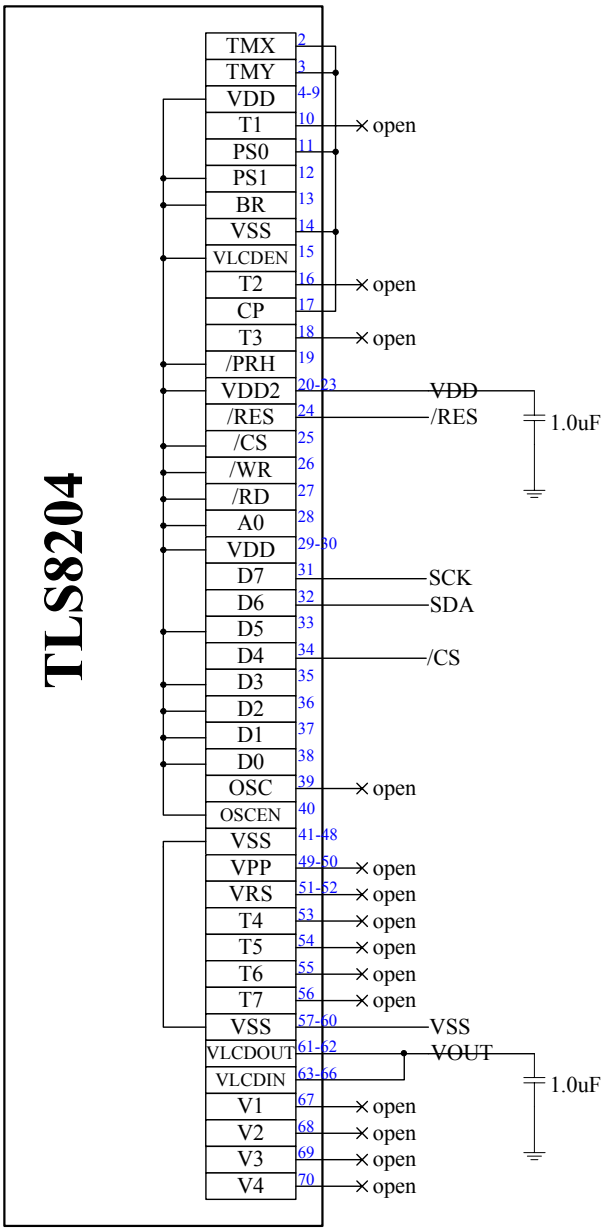
6800 series interface
Internal Power supply circuits
Internal Oscillator
Configuration pins:
CP: VSS (4X boosting level by default)
BR: VDD (1/9 bias by default)
TMX: VSS (normal SEG output direction and can be re-configured by software)
TMY: VSS (COM scan direction is normal and can be re-configured by software)
/PRH: VDD (Enable both high- and low- LCD range)
C=1.0uF



4-line serial interface
Internal Power supply circuits
Internal Oscillator
Configuration pins:
CP: VSS (4X boosting level by default)
BR: VDD (1/9 bias by default)
TMX: VSS (normal SEG output direction and can be re-configured by software)
TMY: VSS (COM scan direction is normal and can be re-configured by software)
/PRH: VDD (Enable both high- and low- LCD range)
C=1.0uF



3-line serial interface
Internal Power supply circuits
Internal Oscillator
Configuration pins:
CP: VSS (4X boosting level by default)
BR: VDD (1/9 bias by default)
TMX: VSS (normal SEG output direction and can be re-configured by software)
TMY: VSS (COM scan direction is normal and can be re-configured by software)
/PRH: VDD (Enable both high- and low- LCD range)
C=1.0uF



PAD ARRANGEMENT

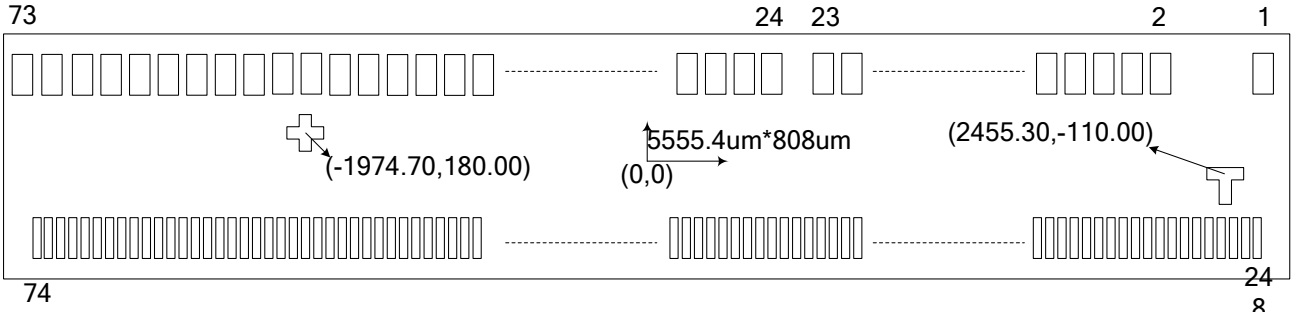
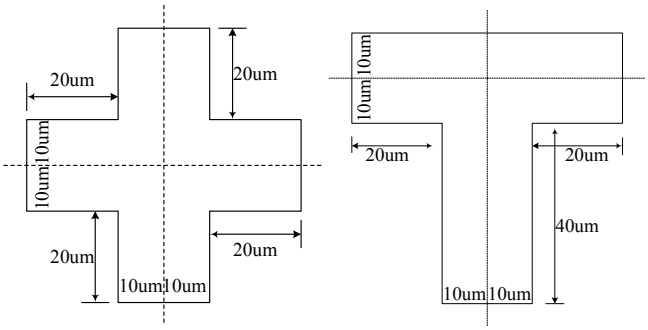


Figure 16 Pad arrangement diagram

Alignment Keys:



NO	X	Y
L	-1974.70	180.00
R	2455.30	-110.00

Chip size	5555.4um * 808um		
Bump Pitch	30um (Min.)		
Bump Size	PAD No.	X	Y
	1 – 73	36um	49um
	74-248	17um	112um
Bump Height	16um±3um		
Chip Thickness	480um		

PAD CENTER COORDINATES

NO.	NAME	X	Y
1	Dummy	2705.8	354.5
2	TMX	1791.25	354.5
3	TMY	1741.25	354.5
4	VDD	1678.4	354.5
5	VDD	1628.4	354.5
6	VDD	1562.9	354.5
7	VDD	1512.9	354.5
8	VDD	1453.9	354.5
9	VDD	1403.9	354.5
10	T1	1344.15	354.5
11	PS0	1294.15	354.5
12	PS1	1244.15	354.5
13	BR	1194.15	354.5
14	VSS	1144.15	354.5
15	VLCDEN	1094.15	354.5
16	T2	1044.15	354.5
17	CP	994.15	354.5
18	T3	944.15	354.5
19	/PRH	894.15	354.5
20	VDD2	831.3	354.5
21	VDD2	781.3	354.5
22	VDD2	715.8	354.5
23	VDD2	665.8	354.5
24	RESB	296.75	354.5
25	CSB	246.75	354.5
26	/WR	196.75	354.5
27	/RD	146.75	354.5
28	A0	96.75	354.5
29	VDD	33.9	354.5
30	VDD	-16.1	354.5
31	D7	-78.05	354.5
32	D6	-128.05	354.5
33	D5	-178.05	354.5
34	D4	-228.05	354.5
35	D3	-278.05	354.5
36	D2	-328.05	354.5
37	D1	-378.05	354.5
38	D0	-428.05	354.5
39	OSC	-478.05	354.5
40	OSCEN	-528.05	354.5
41	VSS	-578.05	354.5
42	VSS	-628.05	354.5

NO.	NAME	X	Y
43	VSS	-678.05	354.5
44	VSS	-728.05	354.5
45	VSS	-778.05	354.5
46	VSS	-828.05	354.5
47	VSS	-878.05	354.5
48	VSS	-928.05	354.5
49	VPP	-985.85	354.5
50	VPP	-1035.85	354.5
51	VRS	-1185.7	354.5
52	VRS	-1235.7	354.5
53	T4	-1285.7	354.5
54	T5	-1335.7	354.5
55	T6	-1385.7	354.5
56	T7	-1435.7	354.5
57	VSS	-1485.7	354.5
58	VSS	-1535.7	354.5
59	VSS	-1585.7	354.5
60	VSS	-1635.7	354.5
61	VLCDOUT	-1685.7	354.5
62	VLCDOUT	-1735.7	354.5
63	VLCDIN	-1985.7	354.5
64	VLCDIN	-2035.7	354.5
65	VLCDIN	-2085.7	354.5
66	VLCDIN	-2135.7	354.5
67	V1	-2285.7	354.5
68	V2	-2335.7	354.5
69	V3	-2385.7	354.5
70	V4	-2435.7	354.5
71	Dummy	-2485.7	354.5
72	Dummy	-2621.2	354.5
73	Dummy	-2671.2	354.5
74	Dummy	-2681.8	-324
75	Dummy	-2651.8	-324
76	COMS2	-2621.8	-324
77	COM66	-2591.8	-324
78	COM65	-2561.8	-324
79	COM64	-2531.8	-324
80	COM63	-2501.8	-324
81	COM62	-2471.8	-324
82	COM61	-2441.8	-324
83	COM60	-2411.8	-324
84	COM59	-2381.8	-324

NO.	NAME	X	Y
85	COM58	-2351.8	-324
86	COM57	-2321.8	-324
87	COM56	-2291.8	-324
88	COM55	-2261.8	-324
89	COM54	-2231.8	-324
90	COM53	-2201.8	-324
91	COM52	-2171.8	-324
92	COM51	-2141.8	-324
93	COM50	-2111.8	-324
94	COM49	-2081.8	-324
95	COM48	-2051.8	-324
96	COM47	-2021.8	-324
97	COM46	-1991.8	-324
98	COM45	-1961.8	-324
99	COM44	-1931.8	-324
100	COM43	-1901.8	-324
101	COM42	-1871.8	-324
102	COM41	-1841.8	-324
103	COM40	-1811.8	-324
104	COM39	-1781.8	-324
105	COM38	-1751.8	-324
106	COM37	-1721.8	-324
107	COM36	-1691.8	-324
108	COM35	-1661.8	-324
109	COM34	-1631.8	-324
110	COM33	-1601.8	-324
111	SEG0	-1571.8	-324
112	SEG1	-1541.8	-324
113	SEG2	-1511.8	-324
114	SEG3	-1481.8	-324
115	SEG4	-1451.8	-324
116	SEG5	-1421.8	-324
117	SEG6	-1391.8	-324
118	SEG7	-1361.8	-324
119	SEG8	-1331.8	-324
120	SEG9	-1301.8	-324
121	SEG10	-1271.8	-324
122	SEG11	-1241.8	-324
123	SEG12	-1211.8	-324
124	SEG13	-1181.8	-324
125	SEG14	-1151.8	-324
126	SEG15	-1121.8	-324

NO.	NAME	X	Y
127	SEG16	-1091.8	-324
128	SEG17	-1061.8	-324
129	SEG18	-1031.8	-324
130	SEG19	-1001.8	-324
131	SEG20	-971.8	-324
132	SEG21	-941.8	-324
133	SEG22	-911.8	-324
134	SEG23	-881.8	-324
135	SEG24	-851.8	-324
136	SEG25	-821.8	-324
137	SEG26	-791.8	-324
138	SEG27	-761.8	-324
139	SEG28	-731.8	-324
140	SEG29	-701.8	-324
141	SEG30	-671.8	-324
142	SEG31	-641.8	-324
143	SEG32	-611.8	-324
144	SEG33	-581.8	-324
145	SEG34	-551.8	-324
146	SEG35	-521.8	-324
147	SEG36	-491.8	-324
148	SEG37	-461.8	-324
149	SEG38	-431.8	-324
150	SEG39	-401.8	-324
151	SEG40	-371.8	-324
152	SEG41	-341.8	-324
153	SEG42	-311.8	-324
154	SEG43	-281.8	-324
155	SEG44	-251.8	-324
156	SEG45	-221.8	-324
157	SEG46	-191.8	-324
158	SEG47	-161.8	-324
159	SEG48	-131.8	-324
160	SEG49	-101.8	-324
161	SEG50	-71.8	-324
162	SEG51	-41.8	-324
163	SEG52	-11.8	-324
164	SEG53	18.2	-324
165	SEG54	48.2	-324
166	SEG55	78.2	-324
167	SEG56	108.2	-324
168	SEG57	138.2	-324

NO.	NAME	X	Y
169	SEG58	168.2	-324
170	SEG59	198.2	-324
171	SEG60	228.2	-324
172	SEG61	258.2	-324
173	SEG62	288.2	-324
174	SEG63	318.2	-324
175	SEG64	348.2	-324
176	SEG65	378.2	-324
177	SEG66	408.2	-324
178	SEG67	438.2	-324
179	SEG68	468.2	-324
180	SEG69	498.2	-324
181	SEG70	528.2	-324
182	SEG71	558.2	-324
183	SEG72	588.2	-324
184	SEG73	618.2	-324
185	SEG74	648.2	-324
186	SEG75	678.2	-324
187	SEG76	708.2	-324
188	SEG77	738.2	-324
189	SEG78	768.2	-324
190	SEG79	798.2	-324
191	SEG80	828.2	-324
192	SEG81	858.2	-324
193	SEG82	888.2	-324
194	SEG83	918.2	-324
195	SEG84	948.2	-324
196	SEG85	978.2	-324
197	SEG86	1008.2	-324
198	SEG87	1038.2	-324
199	SEG88	1068.2	-324
200	SEG89	1098.2	-324
201	SEG90	1128.2	-324
202	SEG91	1158.2	-324
203	SEG92	1188.2	-324
204	SEG93	1218.2	-324
205	SEG94	1248.2	-324
206	SEG95	1278.2	-324
207	SEG96	1308.2	-324
208	SEG97	1338.2	-324
209	SEG98	1368.2	-324
210	SEG99	1398.2	-324

NO.	NAME	X	Y
211	SEG100	1428.2	-324
212	SEG101	1458.2	-324
213	COMS	1488.2	-324
214	COM0	1518.2	-324
215	COM1	1548.2	-324
216	COM2	1578.2	-324
217	COM3	1608.2	-324
218	COM4	1638.2	-324
219	COM5	1668.2	-324
220	COM6	1698.2	-324
221	COM7	1728.2	-324
222	COM8	1758.2	-324
223	COM9	1788.2	-324
224	COM10	1818.2	-324
225	COM11	1848.2	-324
226	COM12	1878.2	-324
227	COM13	1908.2	-324
228	COM14	1938.2	-324
229	COM15	1968.2	-324
230	COM16	1998.2	-324
231	COM17	2028.2	-324
232	COM18	2058.2	-324
233	COM19	2088.2	-324
234	COM20	2118.2	-324
235	COM21	2148.2	-324
236	COM22	2178.2	-324
237	COM23	2208.2	-324
238	COM24	2238.2	-324
239	COM25	2268.2	-324
240	COM26	2298.2	-324
241	COM27	2328.2	-324
242	COM28	2358.2	-324
243	COM29	2388.2	-324
244	COM30	2418.2	-324
245	COM31	2448.2	-324
246	COM32	2478.2	-324
247	Dummy	2508.2	-324
248	Dummy	2538.2	-324

Revision History

TLS8204 Datasheet Revision History		
Version	**Content**	**Date**
1.0	● Original	Jan., 2007
1.1	● Modify PAD No. 87->73, 88->74 on Page 41	Mar., 2007
1.2	● Modify “Set Booster” D7 bit from 0->1 on command table ● Modify “set booster” description	Mar., 2007