

CD4094B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | VDD (V) | LIMITS | | UNITS |
|--|---------|--------|------|---------------|
| | | MIN. | MAX. | |
| Supply-Voltage Range (For T_A =Full Package-Temperature Range) | | 3 | 18 | V |
| Data Setup Time, t_S | 5 | 125 | — | ns |
| | 10 | 55 | — | |
| | 15 | 35 | — | |
| Clock Pulse Width, t_W | 5 | 200 | — | ns |
| | 10 | 100 | — | |
| | 15 | 83 | — | |
| Clock Input Frequency, f_{CL} | 5 | | 1.25 | MHz |
| | 10 | dc | 2.5 | |
| | 15 | | 3 | |
| Clock Input Rise or Fall time, t_{rCL}, t_{fCL} * | 5 | | 15 | μs |
| | 10 | — | 5 | |
| | 15 | | 5 | |
| Strobe Pulse Width, t_W | 5 | 200 | — | ns |
| | 10 | 80 | — | |
| | 15 | 70 | — | |

*If more than one unit is cascaded t_{rCL} (for Q_S only) should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the output driving stage for the estimated capacitive load.

TRUTH TABLE

| CL [▲] | Output Enable | Strobe | Data | Parallel Outputs | | Serial Outputs | |
|-----------------|---------------|--------|------|------------------|------|----------------|----|
| | | | | Q1 | Q2 | Q3* | Q4 |
| ↘ | 0 | X | X | OC | OC | Q7 | NC |
| ↘ | 0 | X | X | OC | OC | NC | Q7 |
| ↘ | 1 | 0 | X | NC | NC | Q7 | NC |
| ↘ | 1 | 1 | 0 | 0 | QN-1 | Q7 | NC |
| ↘ | 1 | 1 | 1 | 1 | QN-1 | Q7 | NC |
| ↘ | 1 | 1 | 1 | NC | NC | NC | Q7 |

▲ = Level Change
 X = Don't Care
 NC = No Change
 OC = Open Circuit
 Logic 1 \equiv High
 Logic 0 \equiv Low
 * At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q_S output.

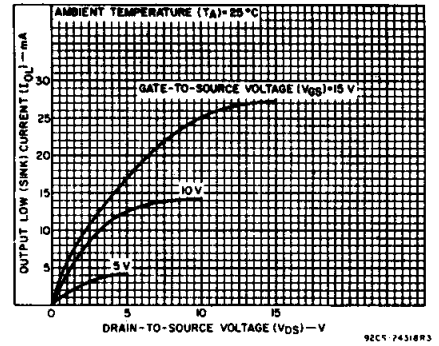


Fig. 4 — Typical output low (sink) current characteristics.

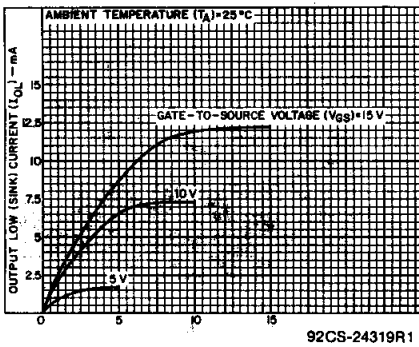


Fig. 5 — Minimum output low (sink) current characteristics.

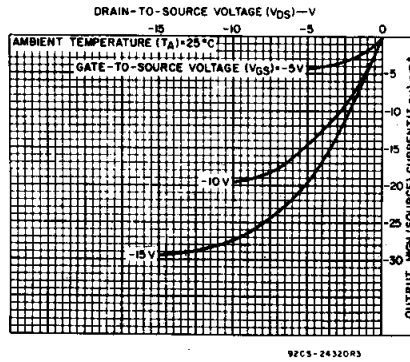


Fig. 6 — Typical output high (source) current characteristics.

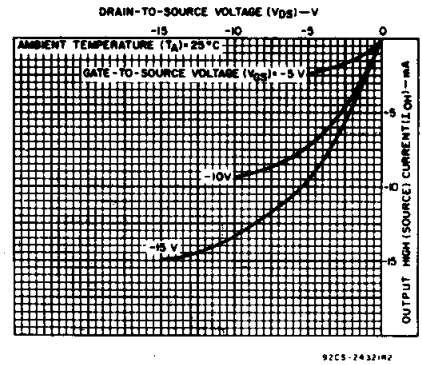


Fig. 7 — Minimum output high (source) current characteristics.

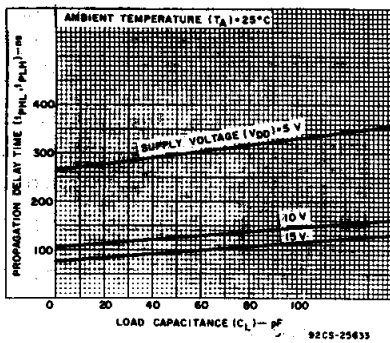


Fig. 8 — Clock-to-serial output Q_S propagation delay vs C_L .

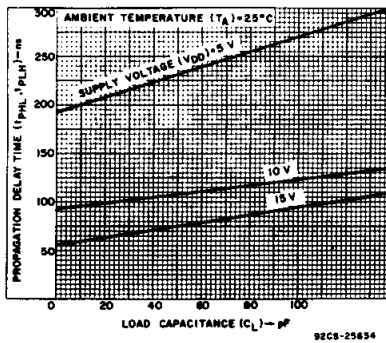


Fig. 9 — Clock-to-serial output Q'_S propagation delay vs C_L .

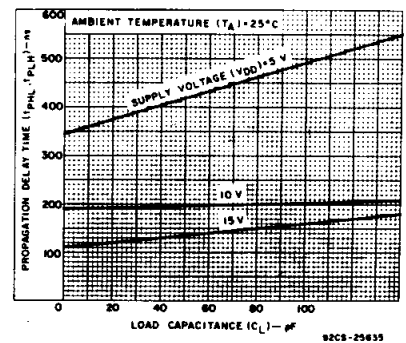


Fig. 10 — Clock-to-parallel output propagation delay vs C_L .

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STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | -55 | | | +25 | | | Max. | |
| | | | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Quiescent Device Current, I _{DD} Max. | - | 0.5 | 5 | 5 | 5 | 150 | 150 | - | 0.04 | 5 | μA |
| | - | 0.10 | 10 | 10 | 10 | 300 | 300 | - | 0.04 | 10 | |
| | - | 0.15 | 15 | 20 | 20 | 600 | 600 | - | 0.04 | 20 | |
| | - | 0.20 | 20 | 100 | 100 | 3000 | 3000 | - | 0.08 | 100 | |
| Output Low (Sink) Current, I _{OL} Min. | 0.4 | 0.5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | - | mA |
| | 0.5 | 0.10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | - | |
| | 1.5 | 0.15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | - | |
| Output High (Source) Current, I _{OH} Min. | 4.6 | 0.5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | - | mA |
| | 2.5 | 0.5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | - | |
| | 9.5 | 0.10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | - | |
| | 13.5 | 0.15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | - | |
| Output Voltage: Low-Level, V _{OL} Max. | - | 0.5 | 5 | 0.05 | | | 0 | | | 0.05 | V |
| | - | 0.10 | 10 | 0.05 | | | 0 | | | 0.05 | |
| | - | 0.15 | 15 | 0.05 | | | 0 | | | 0.05 | |
| Output Voltage: High-Level, V _{OH} Min. | - | 0.5 | 5 | 4.95 | | | 4.95 | | | 5 | V |
| | - | 0.10 | 10 | 9.95 | | | 9.95 | | | 10 | |
| | - | 0.15 | 15 | 14.95 | | | 14.95 | | | 15 | |
| Input Low Voltage, V _{IL} Max. | 0.5, 4.5 | - | 5 | 1.5 | | | - | | | 1.5 | V |
| | 1.9 | - | 10 | 3 | | | - | | | 3 | |
| | 1.5, 13.5 | - | 15 | 4 | | | - | | | 4 | |
| Input High Voltage, V _{IH} Min. | 0.5, 4.5 | - | 5 | 3.5 | | | 3.5 | | | - | V |
| | 1.9 | - | 10 | 7 | | | 7 | | | - | |
| | 1.5, 13.5 | - | 15 | 11 | | | 11 | | | - | |
| Input Current I _{IN} Max. | - | 0.18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | - | ±10 ⁻⁵ | ±0.1 | μA |
| 3-State Output Leakage Current I _{OUT} Max. | 0.18 | 0.18 | 18 | ±0.4 | ±0.4 | ±12 | ±12 | - | ±10 ⁻⁴ | ±0.4 | μA |

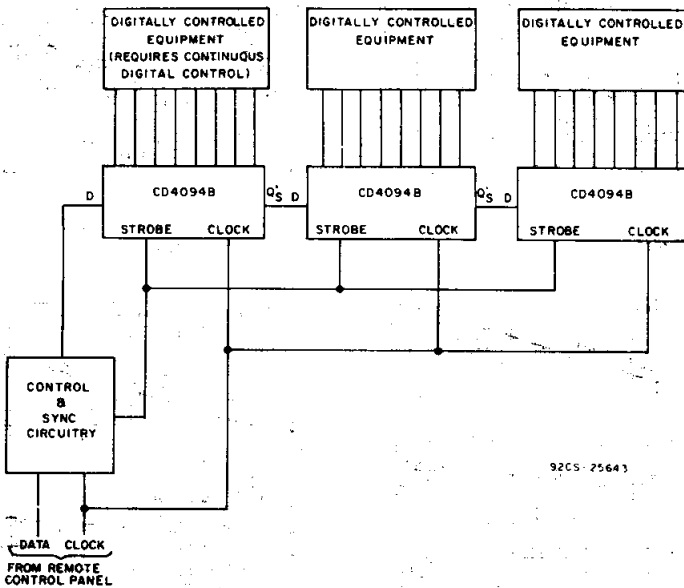


Fig. 14 - Remote control holding register.

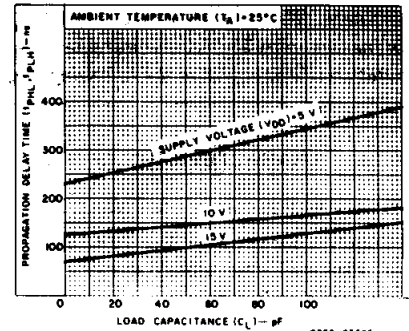


Fig. 11 - Strobe-to-parallel output propagation delay vs. C_L.

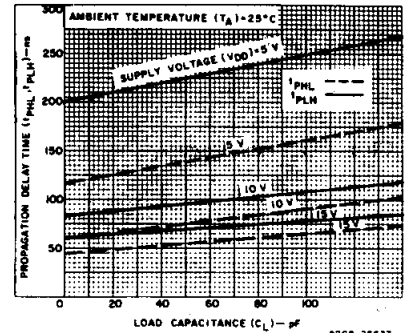


Fig. 12 - Output enable-to-parallel output propagation delay vs. C_L.

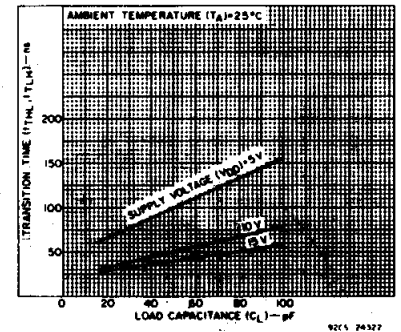


Fig. 13 - Typical transition time vs. load capacitance.

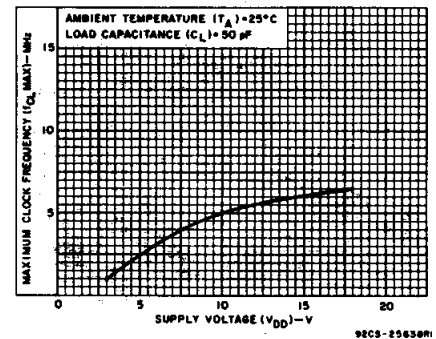


Fig. 15 - Typical maximum-clock-frequency vs. supply voltage.

CD4094B Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC | VDD (V) | LIMITS | | | UNITS |
|--|---------|--------|------|------|---------------|
| | | MIN. | TYP. | MAX. | |
| Propagation Delay Time, t_{PHL}, t_{PLH} Clock to Serial Output Q_S | 5 | — | 300 | 600 | ns |
| | 10 | — | 125 | 250 | |
| | 15 | — | 95 | 190 | |
| Clock to Serial Output Q'_S | 5 | — | 230 | 460 | ns |
| | 10 | — | 110 | 220 | |
| | 15 | — | 75 | 150 | |
| Clock to Parallel Output | 5 | — | 420 | 840 | ns |
| | 10 | — | 195 | 390 | |
| | 15 | — | 135 | 270 | |
| Strobe to Parallel Output | 5 | — | 290 | 580 | ns |
| | 10 | — | 145 | 290 | |
| | 15 | — | 100 | 200 | |
| Output Enable to Parallel Output: t_{PHZ}, t_{PZH} | 5 | — | 140 | 280 | ns |
| | 10 | — | 60 | 120 | |
| | 15 | — | 45 | 90 | |
| t_{PLZ}, t_{PZL} | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 80 | |
| Minimum Strobe Pulse Width, t_W | 5 | — | 100 | 200 | ns |
| | 10 | — | 40 | 80 | |
| | 15 | — | 35 | 70 | |
| Minimum Clock Pulse Width, t_W | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 83 | |
| Minimum Data Setup Time, t_S | 5 | — | 60 | 125 | ns |
| | 10 | — | 30 | 55 | |
| | 15 | — | 20 | 35 | |
| Transition Time; t_{THL}, t_{TLH} | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 80 | |
| Maximum Clock Input Rise or Fall Time, t_{rCL}, t_{fCL} | 5 | 15 | — | — | μs |
| | 10 | 5 | — | — | |
| | 15 | 5 | — | — | |
| Maximum Clock Input Frequency, f_{CL} | 5 | 1.25 | 2.5 | — | MHz |
| | 10 | 2.5 | 5 | — | |
| | 15 | 3 | 6 | — | |
| Input Capacitance C_{iN} (Any Input) | — | — | 5 | 7.5 | pF |

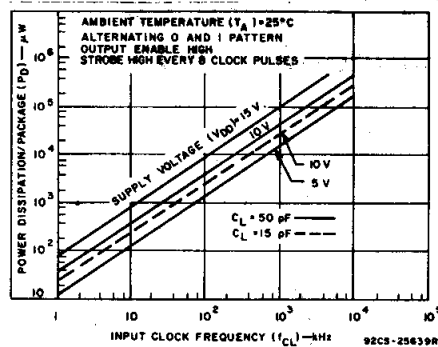


Fig. 16 — Dynamic power dissipation vs input clock frequency.

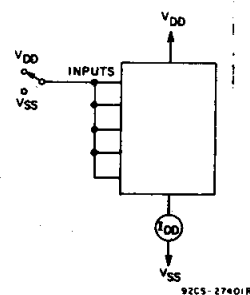


Fig. 17 — Quiescent device current test circuit.

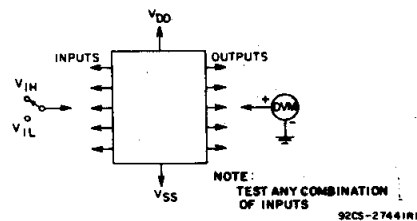


Fig. 18 — Input voltage test circuit.

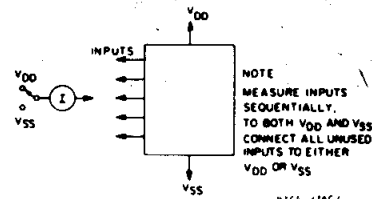
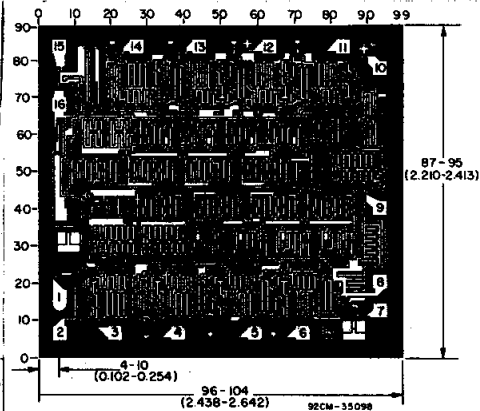


Fig. 19 — Input current test circuit.



Dimensions and Pad Layout for CD4094B Chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| 7702501EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 7702501EA CD4094BF3A | Samples |
| CD4094BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD4094BE | Samples |
| CD4094BEE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD4094BE | Samples |
| CD4094BF | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | CD4094BF | Samples |
| CD4094BF3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 7702501EA CD4094BF3A | Samples |
| CD4094BNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4094B | Samples |
| CD4094BPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM094B | Samples |
| CD4094BPWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM094B | Samples |
| CD4094BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM094B | Samples |
| CD4094BPWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM094B | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4094B, CD4094B-MIL :

- Catalog: [CD4094B](#)
- Military: [CD4094B-MIL](#)

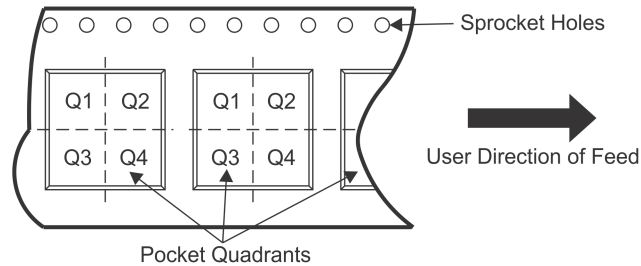
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4094BPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4094BPWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

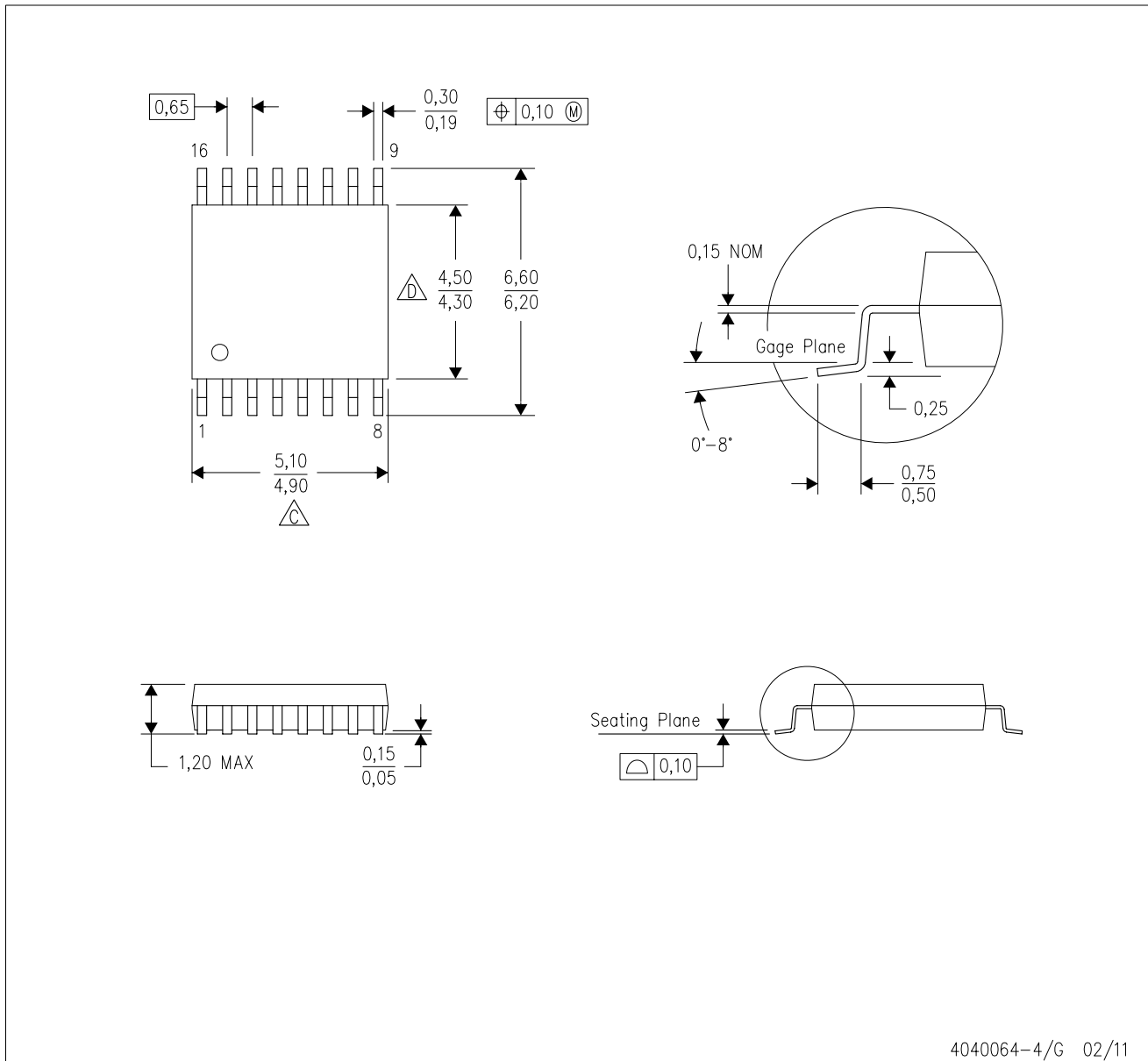


4040083/F 03/03



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

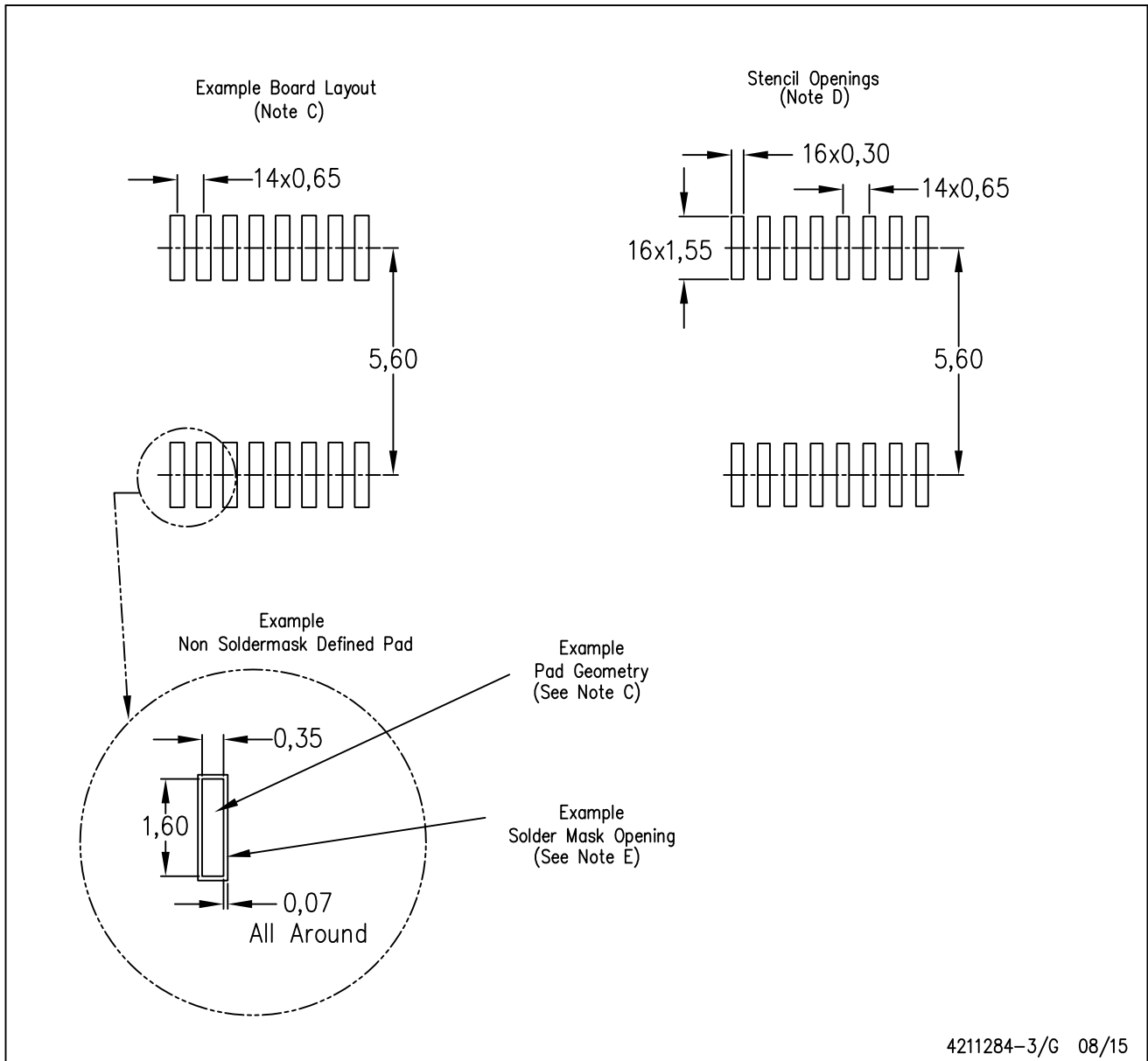


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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