

## CMOS 8-Input NOR/OR Gate

High-Voltage Types (20-Volt Rating)

■ CD4078B NOR/OR Gate provides the system designer with direct implementation of the positive-logic 8-input NOR and OR functions and supplements the existing family of CMOS gates.

The CD4078B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

|  |       |   |
|--|-------|---|
| Voltages referenced to $V_{SS}$ Terminal)                                    | ..... | -0.5V to +20V                                       |
| INPUT VOLTAGE RANGE, ALL INPUTS  | ..... | -0.5V to $V_{DD}$ +0.5V                             |
| DC INPUT CURRENT, ANY ONE INPUT  | ..... | $\pm 10$ mA   |
| POWER DISSIPATION PER PACKAGE ( $P_D$ ):                                     |       |   |
| For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$                        | ..... | 500mW   |
| For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$                       | ..... | Derate Linearity at 12mW/ $^\circ\text{C}$ to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR                                     |       |   |
| FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$        | ..... | 100mW   |
| OPERATING-TEMPERATURE RANGE ( $T_A$ )  | ..... | $-55^\circ\text{C}$ to $+125^\circ\text{C}$         |
| STORAGE TEMPERATURE RANGE ( $T_{stg}$ )                                      | ..... | $-65^\circ\text{C}$ to $+150^\circ\text{C}$         |
| LEAD TEMPERATURE (DURING SOLDERING):   |       |   |
| At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79$ mm) from case for 10s max | ..... | $+265^\circ\text{C}$                                |

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC   | Min. | Max. | Units |
|--|------|------|-------|
| Supply-Voltage Range<br>(For $T_A$ Full Package Temperature Range) | 3    | 18   | V     |

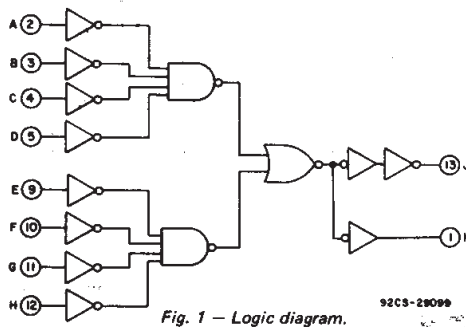


Fig. 1 - Logic diagram.

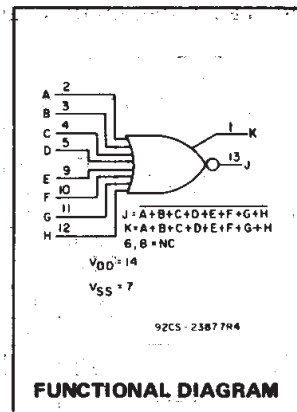
### DYNAMIC ELECTRICAL CHARACTERISTICS

At  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20$  ns,  $C_L = 50$  pF,  $R_L = 200$  k $\Omega$

| CHARACTERISTIC                             | TEST CONDITIONS | LIMITS         |      | UNITS |      |
|--|-----------------|----------------|------|-------|------|
|  |                 | $V_{DD}$ VOLTS | TYP. |       | MAX. |
| Propagation Delay Time, $t_{PHL}, t_{PLH}$ |                 | 5              | 150  | 300   | ns   |
|  |                 | 10             | 75   | 150   |      |
|  |                 | 15             | 55   | 110   |      |
| Transition Time, $t_{THL}, t_{TLH}$        |                 | 5              | 100  | 200   | ns   |
|  |                 | 10             | 50   | 100   |      |
|  |                 | 15             | 40   | 80    |      |
| Input Capacitance, $C_{IN}$                | Any Input       |                | 5    | 7.5   | pF   |

### Features:

- Medium-Speed Operation:  
 $t_{PHL}, t_{PLH} = 75$  ns (typ.) at  $V_{DD} = 10$  V
- Buffered inputs and output
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of  $1 \mu\text{A}$  at 18 V over full package-temperature range:  
100 nA at 18 V and  $25^\circ\text{C}$
- Noise margin (over full package-temperature range):  
1 V at  $V_{DD} = 5$  V  
2 V at  $V_{DD} = 10$  V 2.5 V at  $V_{DD} = 15$  V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



FUNCTIONAL DIAGRAM

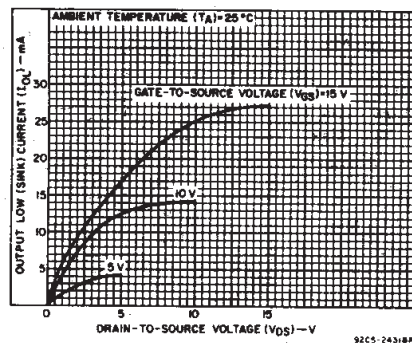


Fig. 2 - Typical output low (sink) current characteristics.

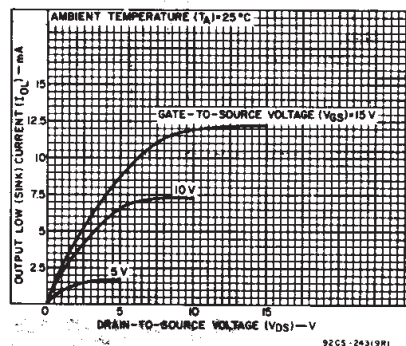


Fig. 3 - Minimum output low (sink) current characteristics.

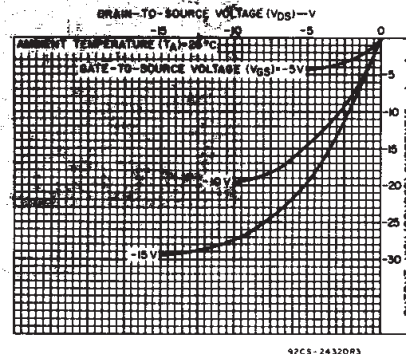


Fig. 4 - Typical output high (source) current characteristics.

# CD4078B Types

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC                                     | CONDITIONS         |                     |                     | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|--|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|  | V <sub>O</sub> (V) | V <sub>IN</sub> (V) | V <sub>DD</sub> (V) | -55                                   | -40   | +85   | +125  | +25   |                   |      |       |
|  |                    |                     |                     |                                       |       |       |       | Min.  | Typ.              | Max. |       |
| Quiescent Device Current, I <sub>DD</sub> Max.     | -                  | 0.5                 | 5                   | 0.25                                  | 0.25  | 7.5   | 7.5   | -     | 0.01              | 0.25 | μA    |
|  | -                  | 0.10                | 10                  | 0.5                                   | 0.5   | 15    | 15    | -     | 0.01              | 0.5  |       |
|  | -                  | 0.15                | 15                  | 1                                     | 1     | 30    | 30    | -     | 0.01              | 1    |       |
|  | -                  | 0.20                | 20                  | 5                                     | 5     | 150   | 150   | -     | 0.02              | 5    |       |
| Output Low (Sink) Current, I <sub>OL</sub> Min.    | 0.4                | 0.5                 | 5                   | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 |      | mA    |
|  | 0.5                | 0.10                | 10                  | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               |      |       |
|  | 1.5                | 0.15                | 15                  | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               |      |       |
| Output High (Source) Current, I <sub>OH</sub> Min. | 4.6                | 0.5                 | 5                   | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                |      | mA    |
|  | 2.5                | 0.5                 | 5                   | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              |      |       |
|  | 9.5                | 0.10                | 10                  | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              |      |       |
|  | 13.5               | 0.15                | 15                  | -4.2                                  | -4    | -2.8  | -2.4  | -3.4  | -6.8              |      |       |
| Output Voltage: Low Level, V <sub>OL</sub> Max.    | -                  | 0.5                 | 5                   |                                       |       | 0.05  |       |       | 0                 | 0.05 | V     |
|  | -                  | 0.10                | 10                  |                                       |       | 0.05  |       |       | 0                 | 0.05 |       |
|  | -                  | 0.15                | 15                  |                                       |       | 0.05  |       |       | 0                 | 0.05 |       |
| Output Voltage: High Level, V <sub>OH</sub> Min.   | -                  | 0.5                 | 5                   |                                       |       | 4.95  |       |       | 4.95              | 5    | V     |
|  | -                  | 0.10                | 10                  |                                       |       | 9.95  |       |       | 9.95              | 10   |       |
|  | -                  | 0.15                | 15                  |                                       |       | 14.95 |       |       | 14.95             | 15   |       |
| Input Low Voltage, V <sub>IL</sub> Max.            | 0.5, 4.5           | -                   | 5                   |                                       |       | 1.5   |       |       | -                 | 1.5  | V     |
|  | 1.9                | -                   | 10                  |                                       |       | 3     |       |       | -                 | 3    |       |
|  | 1.5, 13.5          | -                   | 15                  |                                       |       | 4     |       |       | -                 | 4    |       |
| Input High Voltage, V <sub>IH</sub> Min.           | 0.5, 4.5           | -                   | 5                   |                                       |       | 3.5   |       |       | 3.5               | -    | V     |
|  | 1.9                | -                   | 10                  |                                       |       | 7     |       |       | 7                 | -    |       |
|  | 1.5, 13.5          | -                   | 15                  |                                       |       | 11    |       |       | 11                | -    |       |
| Input Current I <sub>IN</sub> Max.                 |                    | 0.18                | 18                  | ±0.1                                  | ±0.1  | ±1    | ±1    | -     | ±10 <sup>-5</sup> | ±0.1 | μA    |

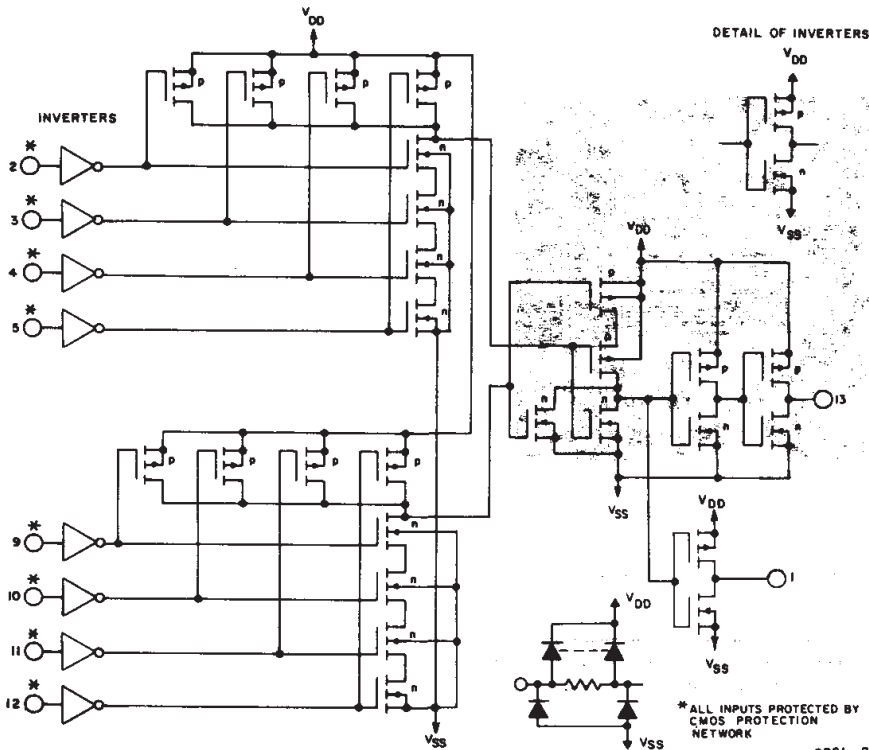
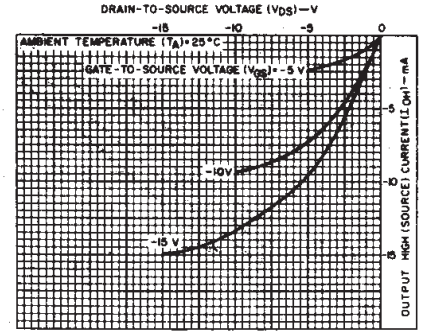


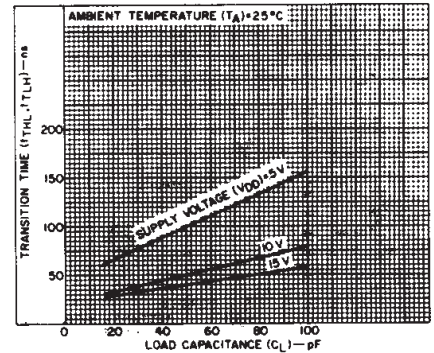
Fig. 8 - Schematic diagram.

92CL-29098



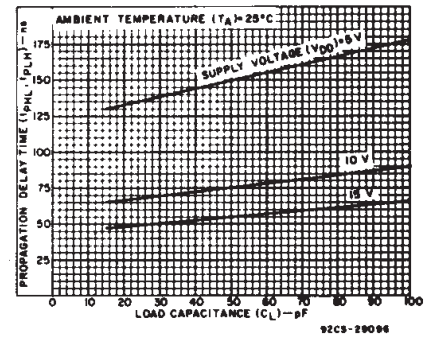
92CS-24321R2

Fig. 5 - Minimum output high (source) current characteristics.



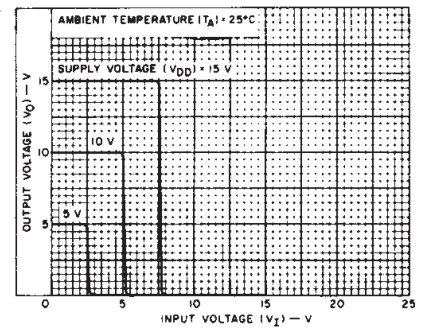
92CS-24322

Fig. 6 - Typical transition time as a function of load capacitance.



92CS-29096

Fig. 7 - Typical propagation delay time as a function of load capacitance.



92CS-28904

Fig. 9 - Typical voltage transfer characteristics (NOR output).

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

# CD4078B Types

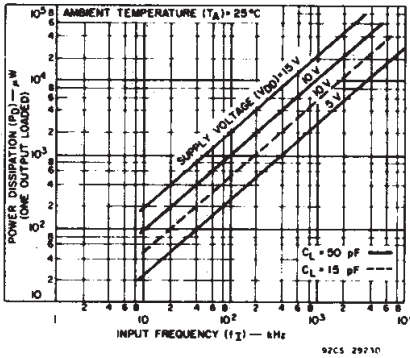


Fig. 10 – Typical dynamic power dissipation as a function of frequency.

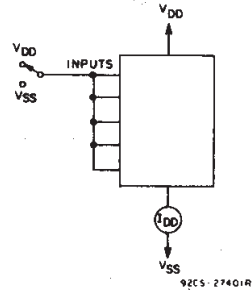


Fig. 11 – Quiescent-device-current test circuit.

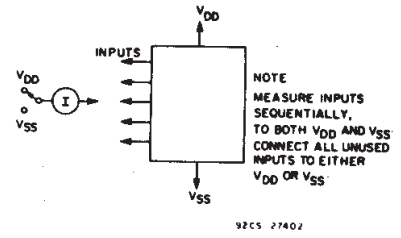


Fig. 12 – Input current test circuit.

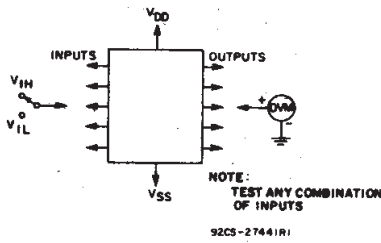
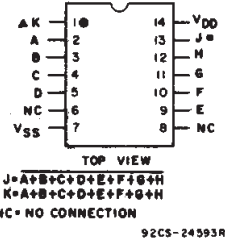


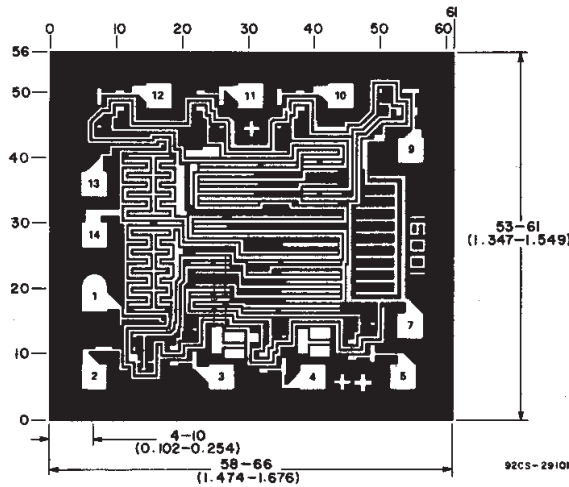
Fig. 13 – Input-voltage test circuit.



Fig. 14 – Dynamic power dissipation test circuit.



## TERMINAL ASSIGNMENT



Dimensions and pad layout for CD4078BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)            | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| 7704402CA        | ACTIVE        | CDIP         | J               | 14   | 1           | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7704402CA<br>CD4078BF3A | <a href="#">Samples</a> |
| CD4078BE         | ACTIVE        | PDIP         | N               | 14   | 25          | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | N / A for Pkg Type   | -55 to 125   | CD4078BE                | <a href="#">Samples</a> |
| CD4078BF         | ACTIVE        | CDIP         | J               | 14   | 1           | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | CD4078BF                | <a href="#">Samples</a> |
| CD4078BF3A       | ACTIVE        | CDIP         | J               | 14   | 1           | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 7704402CA<br>CD4078BF3A | <a href="#">Samples</a> |
| CD4078BM         | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CD4078BM                | <a href="#">Samples</a> |
| CD4078BM96       | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CD4078BM                | <a href="#">Samples</a> |
| CD4078BMT        | ACTIVE        | SOIC         | D               | 14   | 250         | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CD4078BM                | <a href="#">Samples</a> |
| CD4078BNSR       | ACTIVE        | SO           | NS              | 14   | 2000        | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CD4078B                 | <a href="#">Samples</a> |
| CD4078BPW        | ACTIVE        | TSSOP        | PW              | 14   | 90          | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CM078B                  | <a href="#">Samples</a> |
| CD4078BPWE4      | ACTIVE        | TSSOP        | PW              | 14   | 90          | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CM078B                  | <a href="#">Samples</a> |
| CD4078BPWR       | ACTIVE        | TSSOP        | PW              | 14   | 2000        | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CM078B                  | <a href="#">Samples</a> |
| CD4078BPWRE4     | ACTIVE        | TSSOP        | PW              | 14   | 2000        | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CM078B                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD4078B, CD4078B-MIL :**

● Catalog: [CD4078B](#)

● Military: [CD4078B-MIL](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4078BM96 | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| CD4078BMT  | SOIC         | D               | 14   | 250  | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| CD4078BNSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| CD4078BPWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4078BM96 | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| CD4078BMT  | SOIC         | D               | 14   | 250  | 210.0       | 185.0      | 35.0        |
| CD4078BNSR | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |
| CD4078BPWR | TSSOP        | PW              | 14   | 2000 | 853.0       | 449.0      | 35.0        |

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



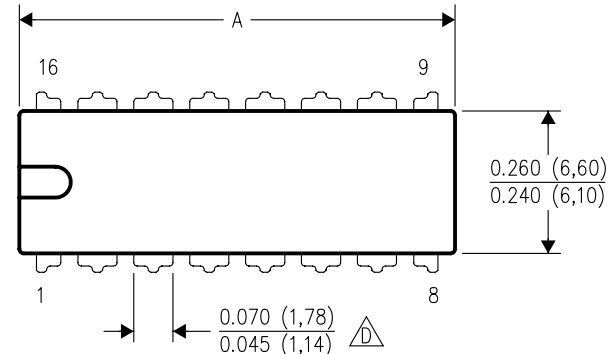
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



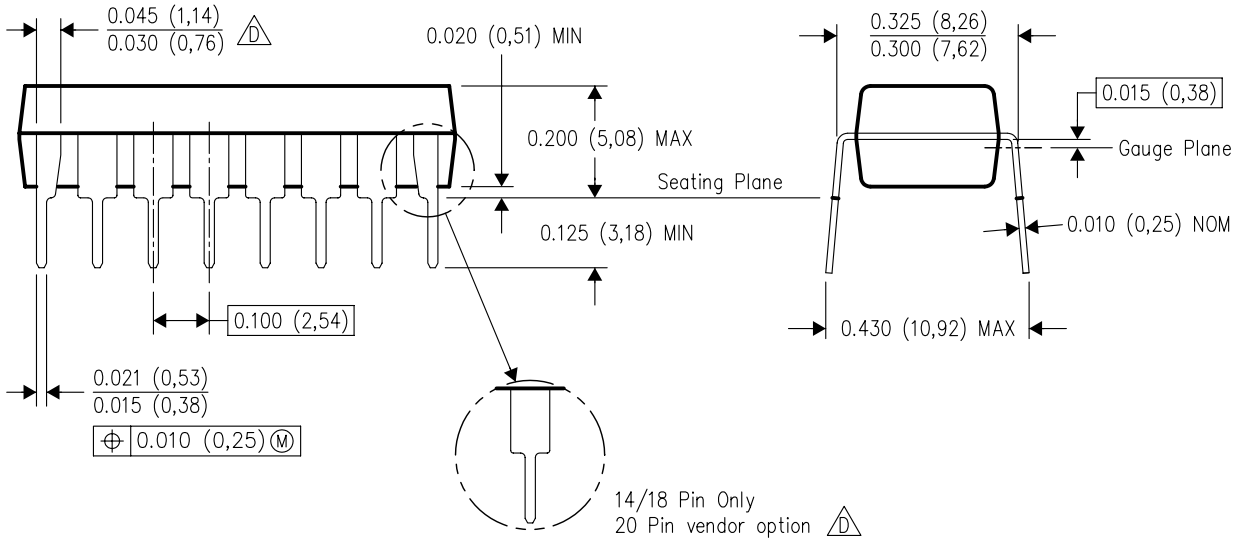
N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



| DIM \ PINS **    | 14               | 16               | 18               | 20               |
|------------------|------------------|------------------|------------------|------------------|
|                  | A MAX            | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) |
| A MIN            | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001 VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



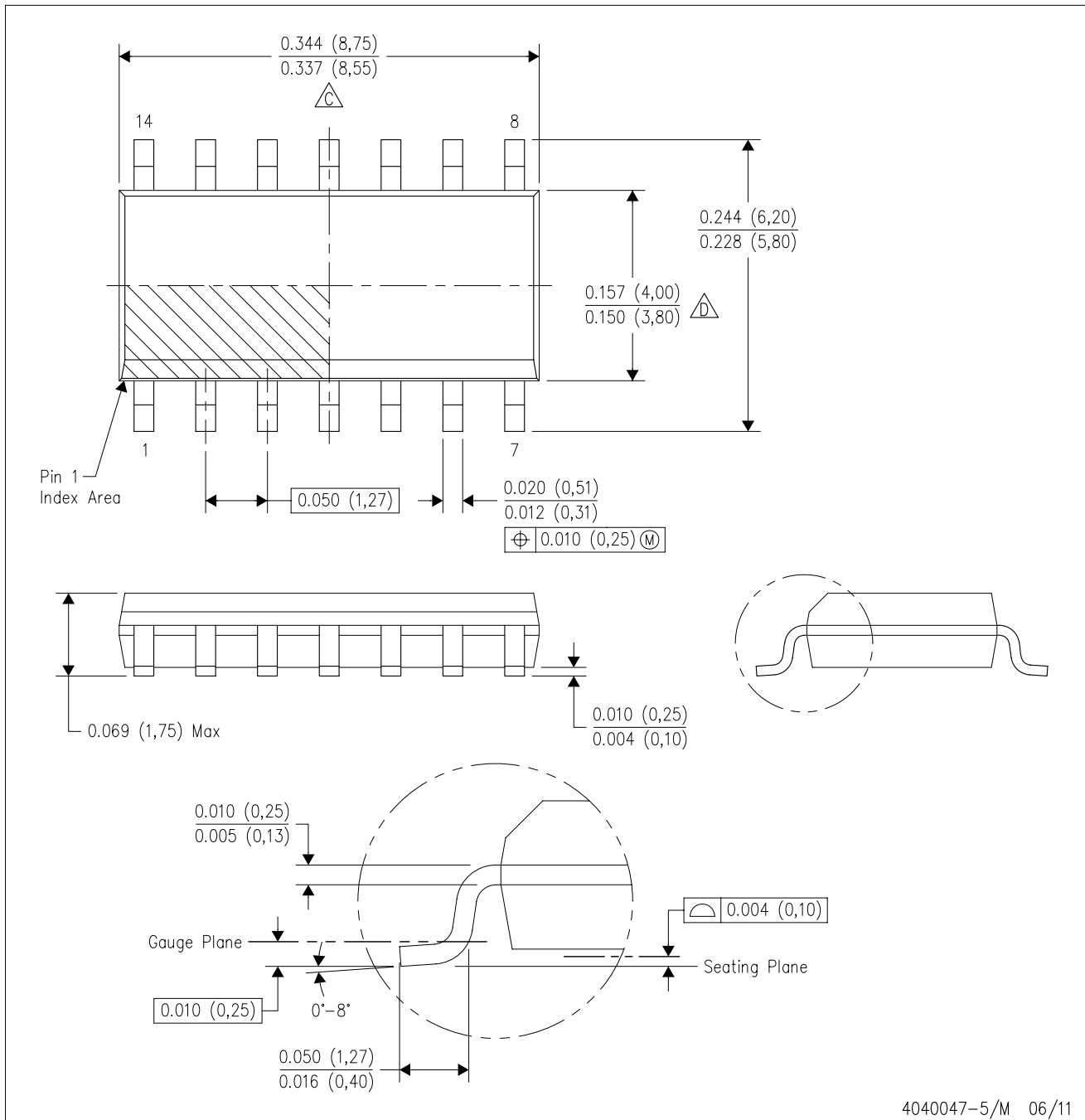
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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