ISO733x Robust EMC, Low Power, Triple-Channel Digital Isolators

1 Features

- Signaling Rate: 25 Mbps
- Integrated Noise Filter on the Inputs
- Default Output 'High' and 'Low' Options
- Low Power Consumption: Typical I_{CC} per Channel at 1 Mbps:
  - ISO7330: 1 mA (5 V Supplies), 0.8 mA (3.3 V Supplies)
  - ISO7331: 1.4 mA (5 V Supplies), 1 mA (3.3 V Supplies)
- Low Propagation Delay: 32 ns Typical (5V Supplies)
- Operates from 3.3 V and 5 V Supplies
- 3.3 V and 5 V Level Translation
- Wide Temperature Range: –40°C to 125°C
- 70 KV/µs Transient Immunity, Typical (5V Supplies)
- Robust Electromagnetic Compatibility (EMC)
  - System-level ESD, EFT, and Surge Immunity
  - Low Emissions
- Wide Body SOIC-16 Package
- Isolation Barrier Life: > 25 Years
- Safety and Regulatory Approvals:
  - 4242 V_{PK} Isolation per DIN V VDE V 0884-10 and DIN EN 61010-1
  - 3000 V_{RMS} Isolation for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 End Equipment Standards
  - CQC Certification per GB4943.1-2011

2 Applications

- Opto-Coupler Replacement in:
  - Industrial FieldBus
    - ProfiBus
    - ModBus
    - DeviceNet™ Data Buses
  - Servo Control Interface
  - Motor Control
  - Power Supplies
  - Battery Packs

3 Description

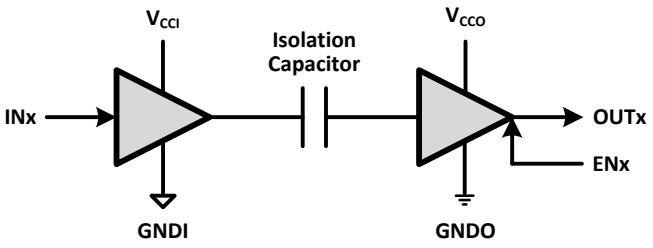
ISO733x provide galvanic isolation up to 3000 V_{RMS} for 1 minute per UL and 4242 V_{PK} per VDE. These devices have three isolated channels comprised of logic input and output buffers separated by a silicon dioxide (SiO_2) insulation barrier. ISO7330 has all three channels in the same direction while ISO7331 has two channels in forward and one channel in reverse direction. In case of input power or signal loss, default output is 'low' for devices with suffix 'F' and 'high' for devices without suffix 'F'. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. ISO733x has integrated noise filter for harsh industrial environment where short noise pulses may be present at the device input pins. ISO733x has TTL input thresholds and operates from 3 V to 5.5 V supply levels. Through innovative chip design and layout techniques, electromagnetic compatibility of ISO733x has been significantly enhanced to enable system-level ESD, EFT, Surge and Emissions compliance.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7330C	SOIC (16)	10,3mm x 7,5mm
ISO7330FC		
ISO7331C		
ISO7331FC		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



(1) V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

(2) V_{CCO} and GNDO are supply and ground connections respectively for the output.

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4 Revision History

Changes from Revision A (April 2015) to Revision B — **Page**

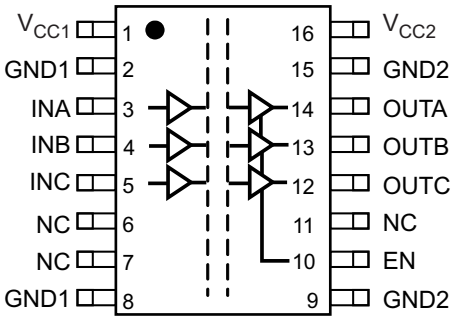
- Changed "(VDE V 0884-10):2006-12" To "and DIN EN 61010-1" in the 4242 V_{PK} in the *Features* ... 1
- Changed From: V_{CCI} To: V_{CC} in Figure 12 ... 10
- Deleted IEC from the section title: *Package Insulation Specifications* ... 13
- Changed the CTI Test Conditions in *Package Insulation Specifications* ... 13
- Changed V_{ISO} Test Condition in the *Insulation Characteristics* table ... 14
- Deleted the V_{ISO} Specification 3600 in the *Insulation Characteristics* table ... 14

Changes from Original (January 2015) to Revision A — **Page**

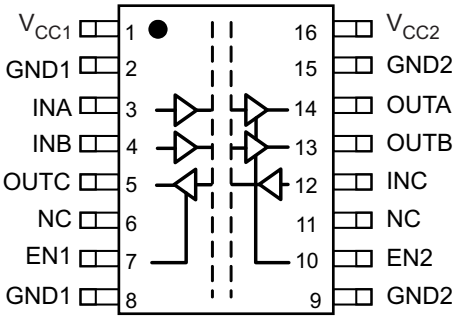
- Changed the device From: Product Preview To: Production data ... 1
- Changed *Features* From: ISO7330: TBD mA To: 1 mA ... 1
- Changed *Features* From: ISO731: TBD mA (3.3 V Supplies) To: 0.8 mA ... 1
- Changed *Features* From: ISO731: TBD mA (5 V Supplies) To: 1.4 mA ... 1
- Changed *Features* From: 65 KV/μs Transient Immunity To: 70 KV/μs Transient Immunity ... 1
- Changed the Safety and Regulatory Approvals *Features* ... 1
- Changed the *Simplified Schematic* and added Notes 1 and 2 ... 1

5 Pin Configuration and Functions

ISO7330
DW (SOIC) Package
(Top View)



ISO7331
DW (SOIC) Package
(Top View)



Pin Functions

PIN			I/O	DESCRIPTION
NAME	ISO7330	ISO7331		
V_{CC1}	1	1	–	Power supply, V_{CC1}
V_{CC2}	16	16	–	Power supply, V_{CC2}
GND1	2, 8	2, 8	–	Ground connection for V_{CC1}
GND2	9, 15	9, 15	–	Ground connection for V_{CC2}
INA	3	3	I	Input, channel A
INB	4	4	I	Input, channel B
INC	5	12	I	Input, channel C
NC	6, 7, 11	6, 11	–	No Connect. These pins have no internal connection.
OUTA	14	14	O	Output, channel A
OUTB	13	13	O	Output, channel B
OUTC	12	5	O	Output, channel C
EN	10	–	I	Output enable. OUTA, OUTB, and OUTC are enabled when EN is high or disconnected and disabled when EN is low.
EN1	–	7	I	Output enable 1. OUTC is enabled when EN1 is high or disconnected and disabled when EN1 is low.
EN2	–	10	I	Output enable 2. OUTA and OUTB are enabled when EN2 is high or disconnected and disabled when EN2 is low.

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Supply voltage(2)	V_{CC1} , V_{CC2}	–0.5	6	V
Voltage (2)	INx, OUTx, ENx	–0.5	V_{CC}+0.5(3)	V
Output current, I_O			±15	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

		VALUE	UNIT
V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	3		5.5	V
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage	0		0.8	V
t_{ui}	Input pulse duration	40			ns
1 / t_{ui}	Signaling rate	0		25	Mbps
T_J (1)	Junction temperature			136	°C
T_A	Ambient temperature	-40	25	125	°C

(1) To maintain the recommended operating conditions for T_J, see the *Thermal Information* table.

6.4 Thermal Information

THERMAL METRIC(1)			DW PACKAGE (16) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance		78.3	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance		40.9	
$R_{\theta JB}$	Junction-to-board thermal resistance		42.9	
ψ_{JT}	Junction-to-top characterization parameter		15.3	
ψ_{JB}	Junction-to-board characterization parameter		42.4	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance		N/A	
P_D (ISO7330)	Maximum Power Dissipation by ISO7330	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF, Input a 12.5 MHz 50% duty cycle square wave	70	mW
P_{D1} (ISO7330)	Maximum Power Dissipation by Side-1 of ISO7330		20	
P_{D2} (ISO7330)	Maximum Power Dissipation by Side-2 of ISO7330		50	
P_D (ISO7331)	Maximum Power Dissipation by ISO7331	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF, Input a 12.5 MHz 50% duty cycle square wave	84	mW
P_{D1} (ISO7331)	Maximum Power Dissipation by Side-1 of ISO7331		35	
P_{D2} (ISO7331)	Maximum Power Dissipation by Side-2 of ISO7331		49	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 11		V_{CCO} (1) – 0.5	4.7		V
		I_{OH} = –20 µA; see Figure 11		V_{CCO} (1) – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 11			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 11			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				480		mV
I_{IH}	High-level input current	IN = V_{CC}				10	µA
I_{IL}	Low-level input current	IN = 0 V		–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 14.		25	70		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
ISO7330							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	Disable	V_I = V_{CC} or 0 V, EN = 0 V		0.5	1.1	mA
I_{CC2}					0.4	0.9	
I_{CC1}		DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		0.5	1.1	
I_{CC2}					2.6	4.2	
I_{CC1}		10 Mbps	C_L = 15pF		1.1	1.9	
I_{CC2}					4.3	6	
I_{CC1}		25 Mbps	C_L = 15pF		2.1	3.3	
I_{CC2}					7	9.3	
ISO7331							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	Disable	V_I = V_{CC} or 0 V, EN1 = EN2 = 0 V		0.7	1.6	mA
I_{CC2}					0.7	1.3	
I_{CC1}		DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		1.8	3	
I_{CC2}					2.4	3.6	
I_{CC1}		10 Mbps	C_L = 15pF		2.8	4.1	
I_{CC2}					3.8	5.1	
I_{CC1}		25 Mbps	C_L = 15pF		4.3	6.2	
I_{CC2}					5.8	7.8	

(1) V_{CCO} is supply voltage, V_{CC1} or V_{CC2}, for the output channel being measured.

6.6 Electrical Characteristics

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 11		V_{CCO} (1) – 0.5	3		V
		I_{OH} = –20 µA; see Figure 11		V_{CCO} (1) – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 11			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 11			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				425		mV
I_{IH}	High-level input current	IN = V_{CC}				10	µA
I_{IL}	Low-level input curre	IN = 0 V		-10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 14		25	50		kV/µs
SUPPLY CURRENT(All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
ISO7330							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	Disable	V_I = V_{CC} or 0 V, EN = 0 V		0.3	0.6	mA
I_{CC2}					0.3	0.6	
I_{CC1}		DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		0.3	0.6	
I_{CC2}					2	3.1	
I_{CC1}		10 Mbps	C_L = 15pF		0.7	1.1	
I_{CC2}					3.1	4.3	
I_{CC1}		25 Mbps	C_L = 15pF		1.2	2	
I_{CC2}					4.8	6.3	
ISO7331							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	Disable	V_I = V_{CC} or 0 V, EN = 0 V		0.5	0.9	mA
I_{CC2}					0.5	0.8	
I_{CC1}		DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		1.3	2.1	
I_{CC2}					1.7	2.6	
I_{CC1}		10 Mbps	C_L = 15pF		1.9	2.7	
I_{CC2}					2.6	3.5	
I_{CC1}		25 Mbps	C_L = 15pF		2.9	4.2	
I_{CC2}					3.9	5.2	

(1) V_{CCO} is supply voltage, V_{CC1} or V_{CC2}, for the output channel being measured.

6.7 Switching Characteristics

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 11	20	32	58	ns
PWD(1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$					4	ns
$t_{sk(o)}$(2)	Channel-to-channel output skew time		Same direction channels			2.5	ns
			Opposite direction channels			17	
$t_{sk(pp)}$(3)	Part-to-part skew time					23	ns
t_r	Output signal rise time		See Figure 11		3		ns
t_f	Output signal fall time				2		ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output		See Figure 12		7	12	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output				7	12	
t_{PZH}	Enable propagation delay, high impedance-to-high output	ISO733xC			7	12	
		ISO733xFC			11000	23000(4)	
t_{PZL}	Enable propagation delay, high impedance-to-low output	ISO733xC			11000	23000(4)	
		ISO733xFC			7	12	
t_{fs}	Fail-safe output delay time from input power loss		See Figure 13		7		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate should be ≤ 43 Kbps

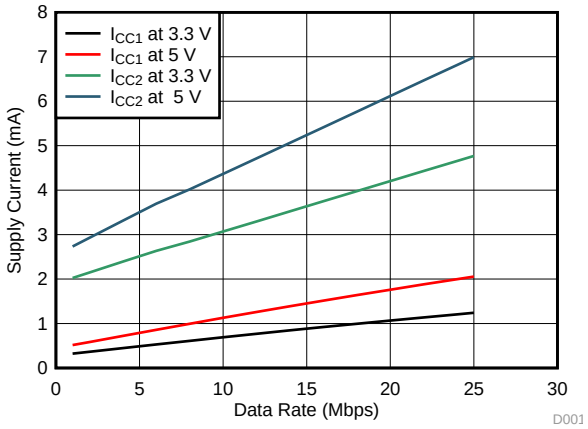
6.8 Switching Characteristics

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 11	22	36	66	ns
PWD(1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$					2.5	ns
$t_{sk(o)}$(2)	Channel-to-channel output skew time		Same direction channels			3	ns
			Opposite direction channels			16	
$t_{sk(pp)}$(3)	Part-to-part skew time					27	ns
t_r	Output signal rise time		See Figure 11		3		ns
t_f	Output signal fall time				2		ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output		See Figure 12		9	18	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output				9	18	
t_{PZH}	Enable propagation delay, high impedance-to-high output	ISO733xC			9	18	
		ISO733xFC			13000	24000(4)	
t_{PZL}	Enable propagation delay, high impedance-to-low output	ISO733xC			13000	24000(4)	
		ISO733xFC			9	18	
t_{fs}	Fail-safe output delay time from input power loss		See Figure 13		7		µs

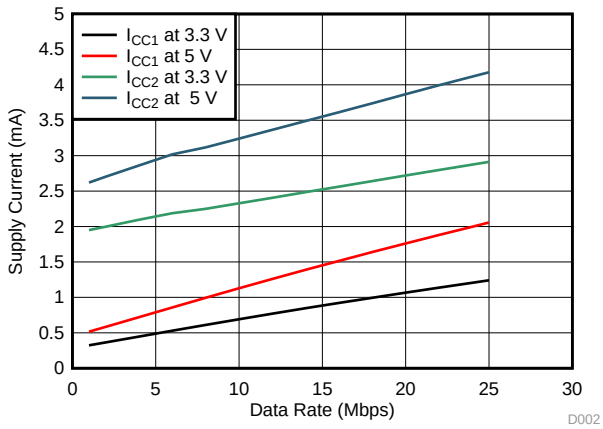
(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate should be ≤ 41 Kbps

6.9 Typical Characteristics



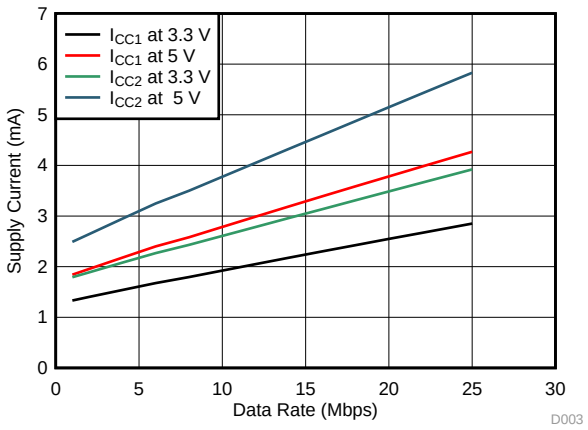
T_A = 25°C C_L = 15 pF

Figure 1. ISO7330 Supply Current vs Data Rate (with 15 pF Load)



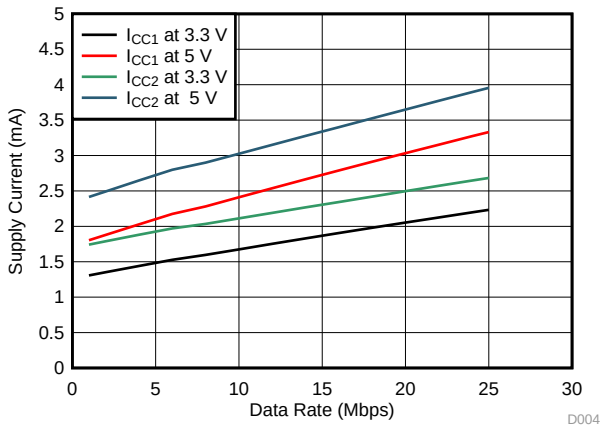
T_A = 25°C C_L = No Load

Figure 2. ISO7330 Supply Current vs Data Rate (with No Load)



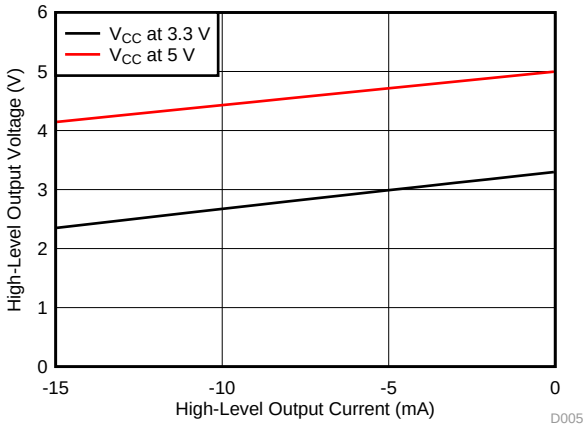
T_A = 25°C C_L = 15 pF

Figure 3. ISO7331 Supply Current vs Data Rate (with 15 pF Load)



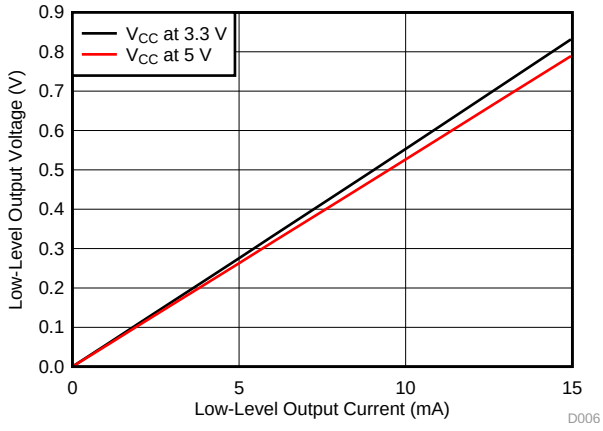
T_A = 25°C C_L = No Load

Figure 4. ISO7331 Supply Current vs Data Rate (with No Load)



T_A = 25°C

Figure 5. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

Figure 6. Low-Level Output Voltage vs Low-Level Output Current

Typical Characteristics (continued)

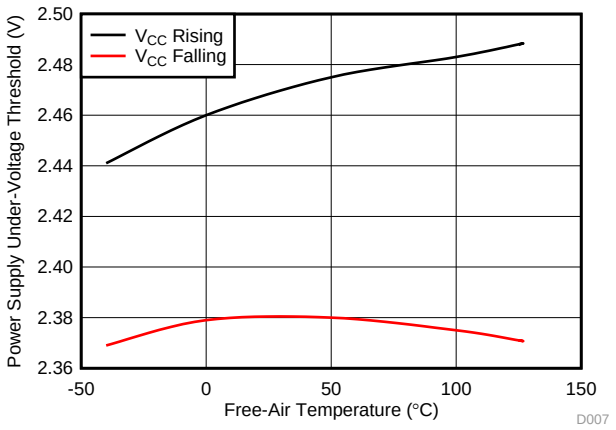


Figure 7. Power Supply Undervoltage Threshold vs Free-Air Temperature

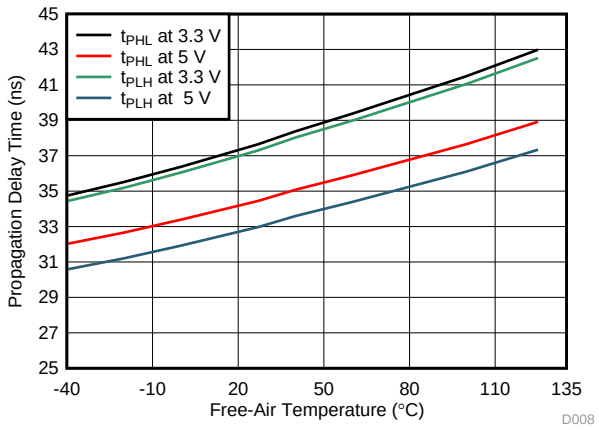


Figure 8. Propagation Delay Time vs Free-Air Temperature

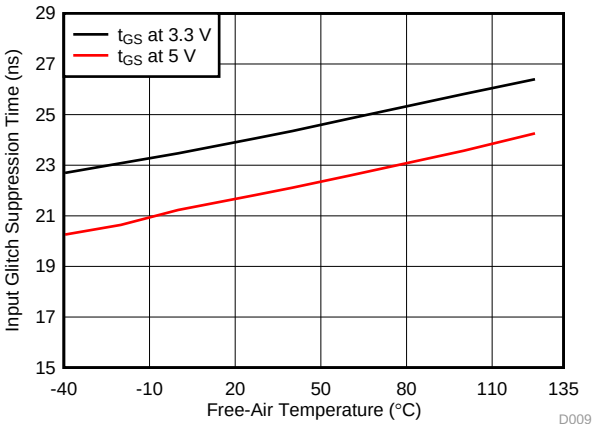


Figure 9. Input Glitch Suppression Time vs Free-Air Temperature

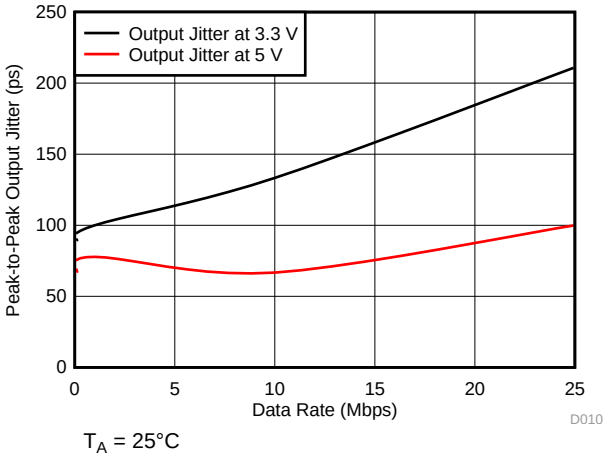
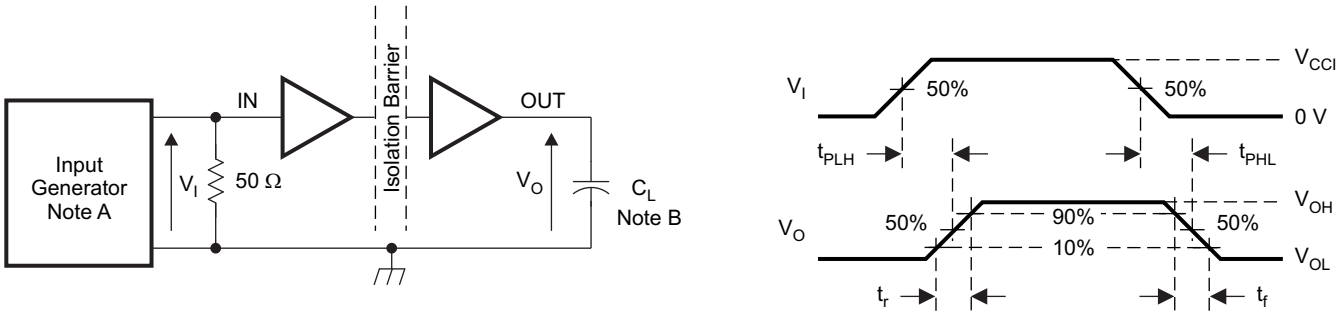


Figure 10. Output Jitter vs Data Rate

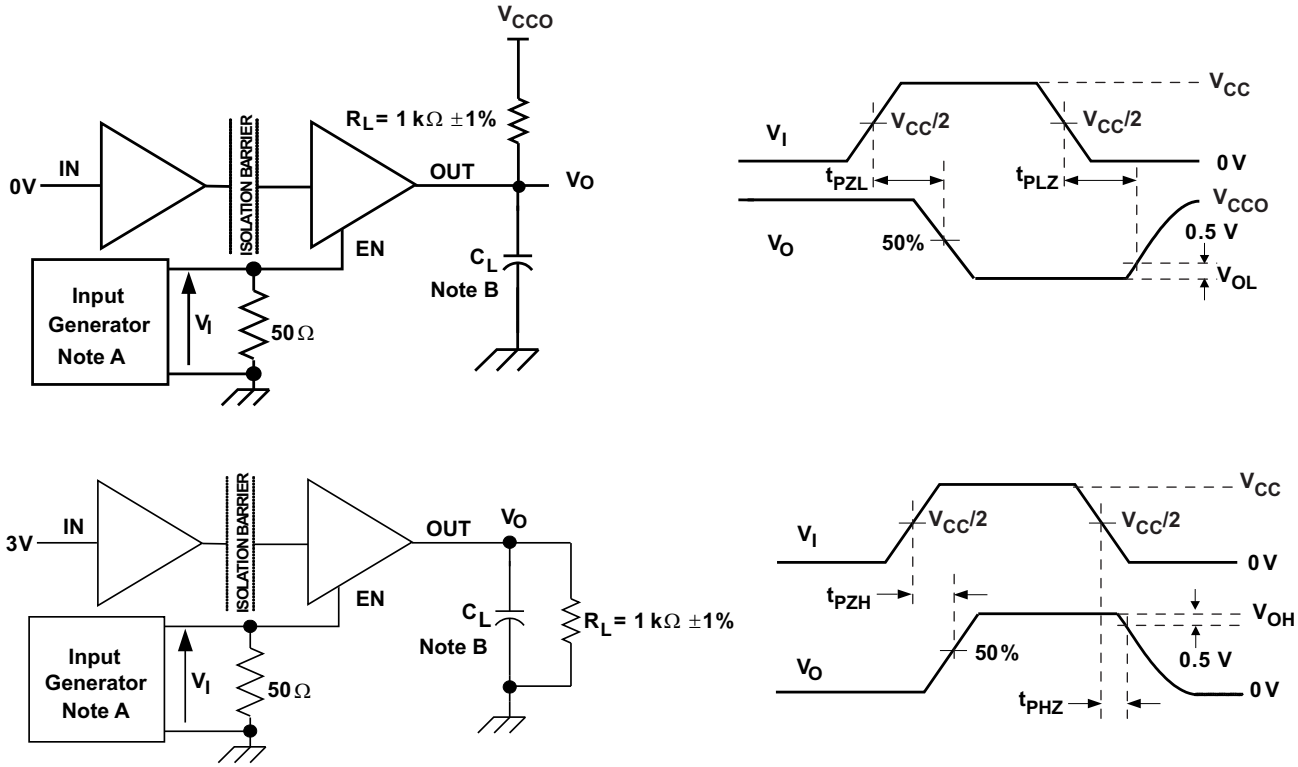
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 11. Switching Characteristic Test Circuit and Voltage Waveforms

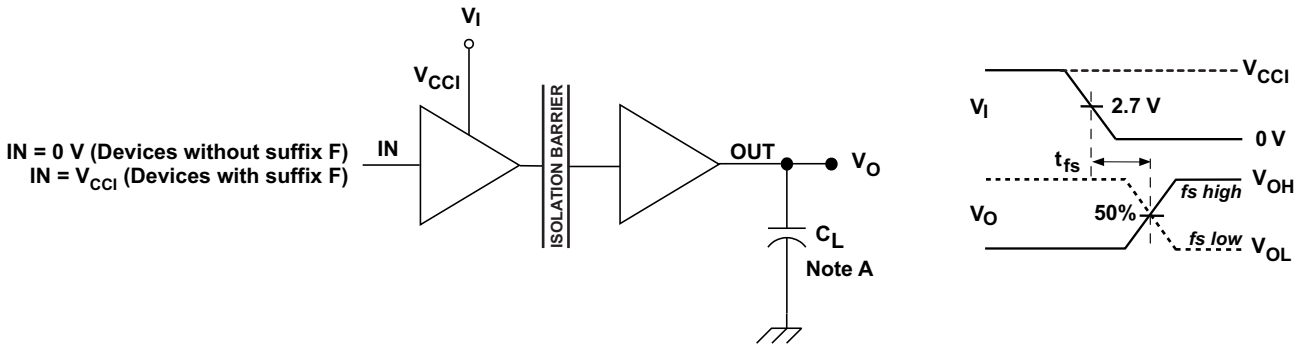


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

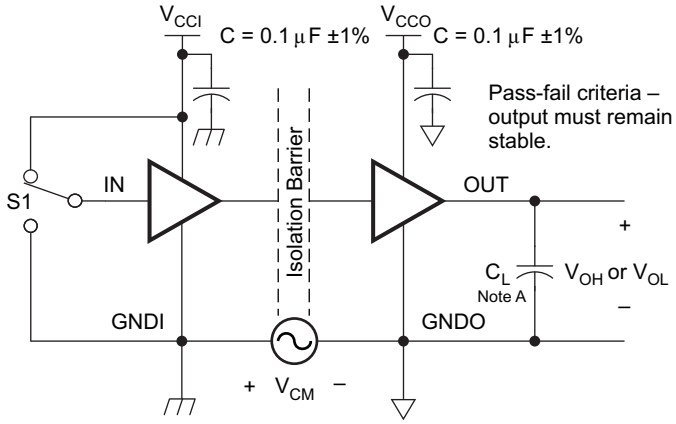
Figure 12. Enable/Disable Propagation Delay Time Test Circuit and Waveform

Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 13. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 14. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The isolator in Figure 15 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency (HF) channel with a bandwidth from 100 kbps up to 25 Mbps, and a low-frequency (LF) channel covering the range from 100 kbps down to DC.

In principle, a single-ended input signal entering the HF channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transient pulses, which then are converted into CMOS levels by a comparator. The transient pulses at the input of the comparator can be either above or below the common mode voltage V_{REF} depending on whether the input bit transitioned from 0 to 1 or 1 to 0. The comparator threshold is adjusted based on the expected bit transition. A decision logic (DCL) at the output of the HF channel comparator measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high-frequency to the low-frequency channel.

8.2 Functional Block Diagram

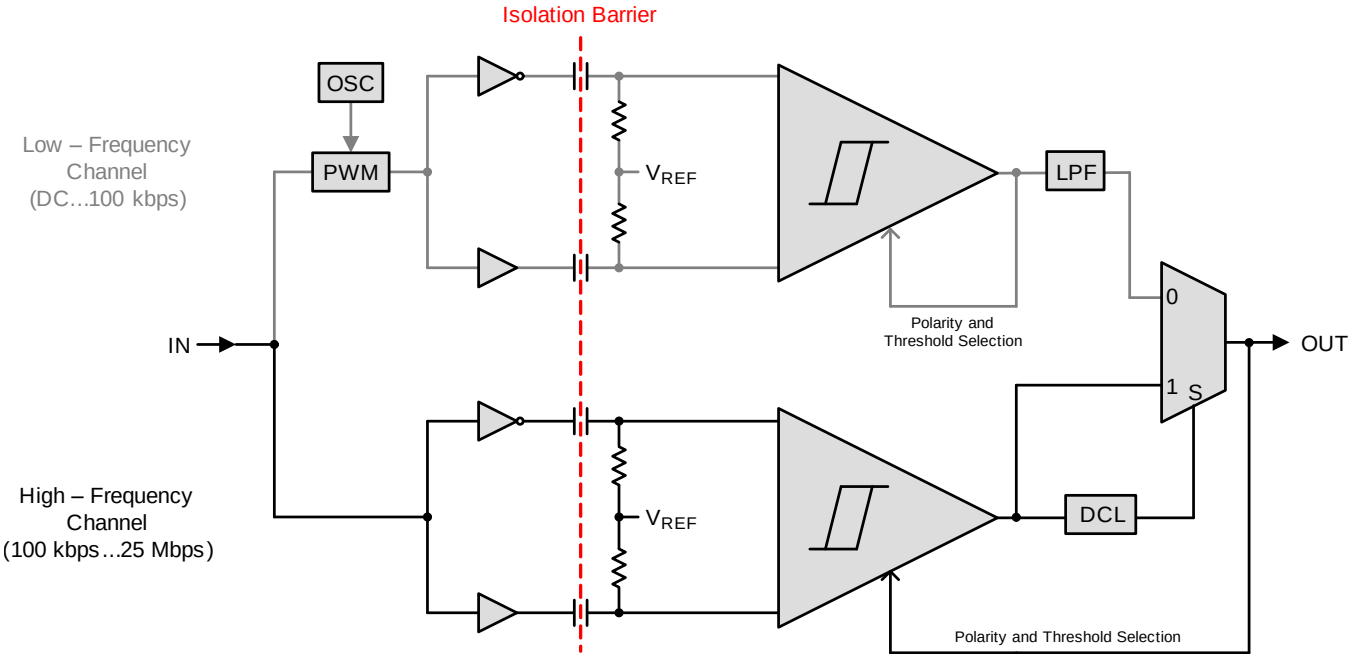


Figure 15. Conceptual Block Diagram of a Digital Capacitive Isolator

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.3 Feature Description

PRODUCT	CHANNEL DIRECTION	RATED ISOLATION	MAX DATA RATE	DEFAULT OUTPUT
ISO7330C	3 Forward, 0 Reverse	3000 V_{RMS} / 4242 V_{PK} (1)	25 Mbps	High
ISO7330FC				Low
ISO7331C	2 Forward, 1 Reverse			High
ISO7331FC				Low

(1) See the *Regulatory Information* section for detailed Isolation Ratings

8.3.1 High Voltage Feature Description

8.3.1.1 Package Insulation Specifications

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	8			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	8			mm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112	>400			V
DTI	Minimum internal gap (internal clearance)	Distance through the insulation	13			µm
R_{IO}	Isolation resistance, input to output(1)	V_{IO} = 500 V, T_A = 25°C		$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max		$>10^{11}$		Ω
C_{IO}	Isolation capacitance, input to output(1)	V_{IO} = 0.4 sin (2πft), f = 1 MHz		2		pF
C_I	Input capacitance(2)	$V_I = V_{CC}/2 + 0.4 \sin(2\pi ft)$, f = 1 MHz, V_{CC} = 5 V		2		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

8.3.1.2 Insulation Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IOWM}	Maximum isolation working voltage		1000	V_{RMS}
V_{IORM}	Maximum repetitive peak voltage per DIN V VDE V 0884-10		1414	V_{PK}
V_{PR}	Input-to-output test voltage per DIN V VDE V 0884-10	After Input/Output safety test subgroup 2/3, V_{PR} = V_{IORM} x 1.2, t = 10 s, Partial discharge < 5 pC	1697	V_{PK}
		Method a, After environmental tests subgroup 1, V_{PR} = V_{IORM} x 1.6, t = 10 s, Partial Discharge < 5 pC	2262	
		Method b1, V_{PR} = V_{IORM} x 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC	2651	
V_{IOTM}	Maximum transient overvoltage per DIN V VDE V 0884-10	V_{TEST} = V_{IOTM} t = 60 sec (qualification) t= 1 sec (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage per DIN V VDE V 0884-10	Test method per IEC 60065, 1.2/50 µs waveform, V_{TEST} = 1.3 x V_{IOSM} = 7800 V_{PK} (qualification)	6000	V_{PK}
V_{ISO}	Withstand isolation voltage per UL 1577	V_{TEST} = V_{ISO} = 3000 V_{RMS}, t = 60 sec (qualification) V_{TEST} = 1.2 x V_{ISO} = 3600 V_{RMS}, t = 1 sec (100% production)	3000	V_{RMS}
R_S	Insulation resistance	V_{IO} = 500 V at T_S	>10^9	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

Table 1. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 300 V_{RMS}	I–IV
	Rated mains voltage ≤ 600 V_{RMS}	I–III
	Rated mains voltage ≤ 1000 V_{RMS}	I–II

8.3.1.3 Regulatory Information

VDE	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 61010-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011
Basic Insulation Maximum Transient Overvoltage, 4242 V_{PK} ; Maximum Surge Isolation Voltage, 6000 V_{PK}; Maximum Repetitive Peak Isolation Voltage', 1414 V_{PK}	800 V_{RMS} Basic Insulation and 400 V_{RMS} Reinforced Insulation working voltage per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.+A1+A2; 300 V_{RMS} Basic Insulation working voltage per CSA 61010-1-12 and IEC 61010-1 3rd Ed.	Single protection, 3000 V_{RMS} (1)	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40016131	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716

(1) Production tested ≥ 3600 V_{RMS} for 1 second in accordance with UL 1577.

8.3.1.4 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 78.3 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			290	mA
		$R_{\theta JA}$ = 78.3 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			443	
T_S	Maximum case temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolut Maximun Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

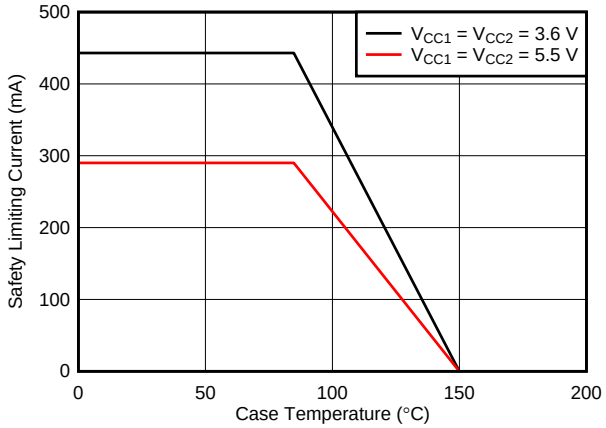


Figure 16. θ_{JC} Thermal Derating Curve per DIN V VDE V 0884-10

8.4 Device Functional Modes

Table 2. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	
				ISO733xC	ISO733xFC
PU	PU	H	H or Open	H	H
		L	H or Open	L	L
		X	L	Z	Z
		Open	H or Open	H(2)	L(3)
PD	PU	X	H or Open	H(2)	L(3)
X	PU	X	L	Z	Z
X	PD	X	X	Undetermined	Undetermined

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 3 V); PD = Powered down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High level; L = Low level; Open = Not connected
(2) In fail-safe condition, output defaults to high level
(3) In fail-safe condition, output defaults to low level

8.4.1 Device I/O Schematics

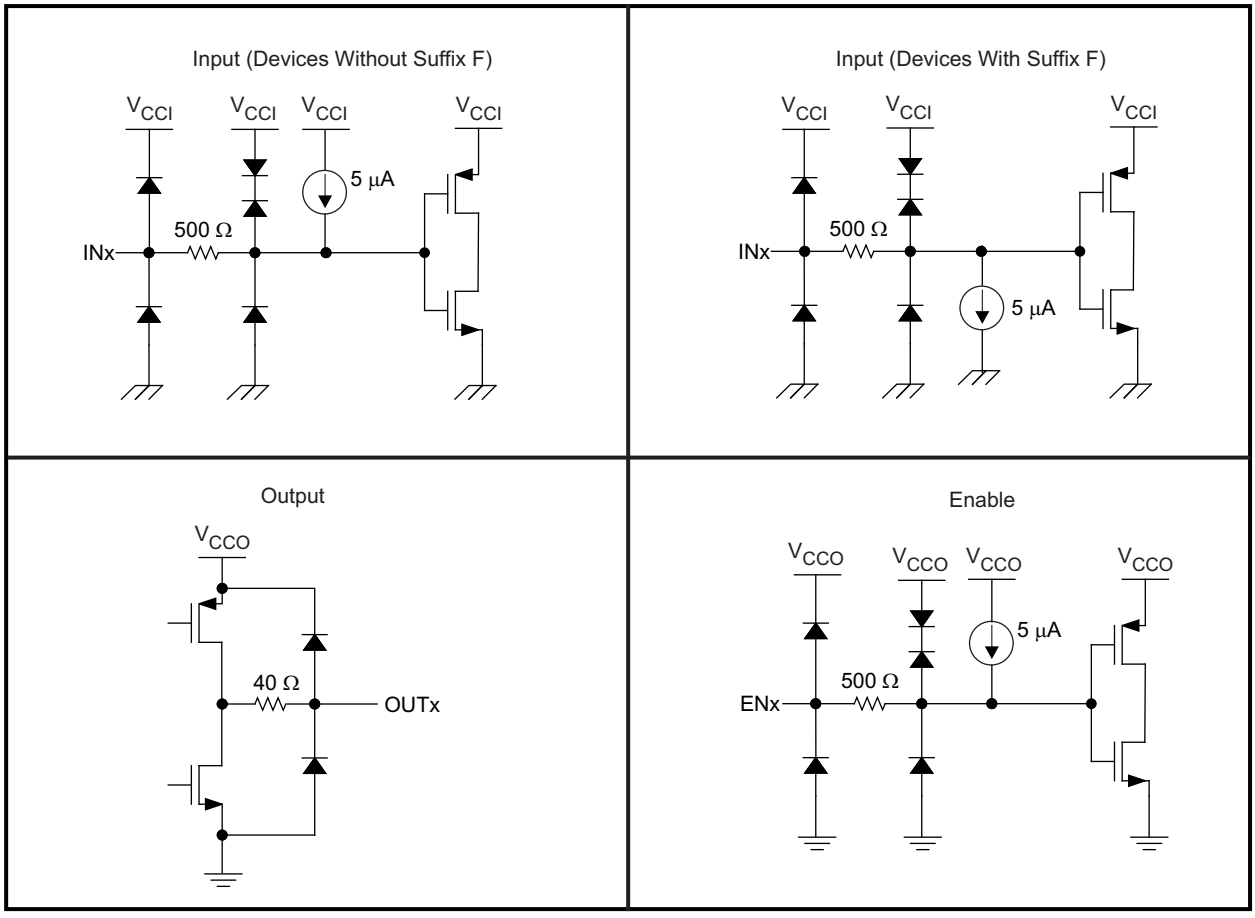


Figure 17. Device I/O Schematics

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

ISO733x utilize single-ended TTL-logic switching technology. Its supply voltage range is from 3 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

ISO7331C combined with Texas Instruments' mixed signal micro-controller, RS-485 transceiver, transformer driver, and voltage regulator can create an isolated RS-485 system as shown in Figure 18.

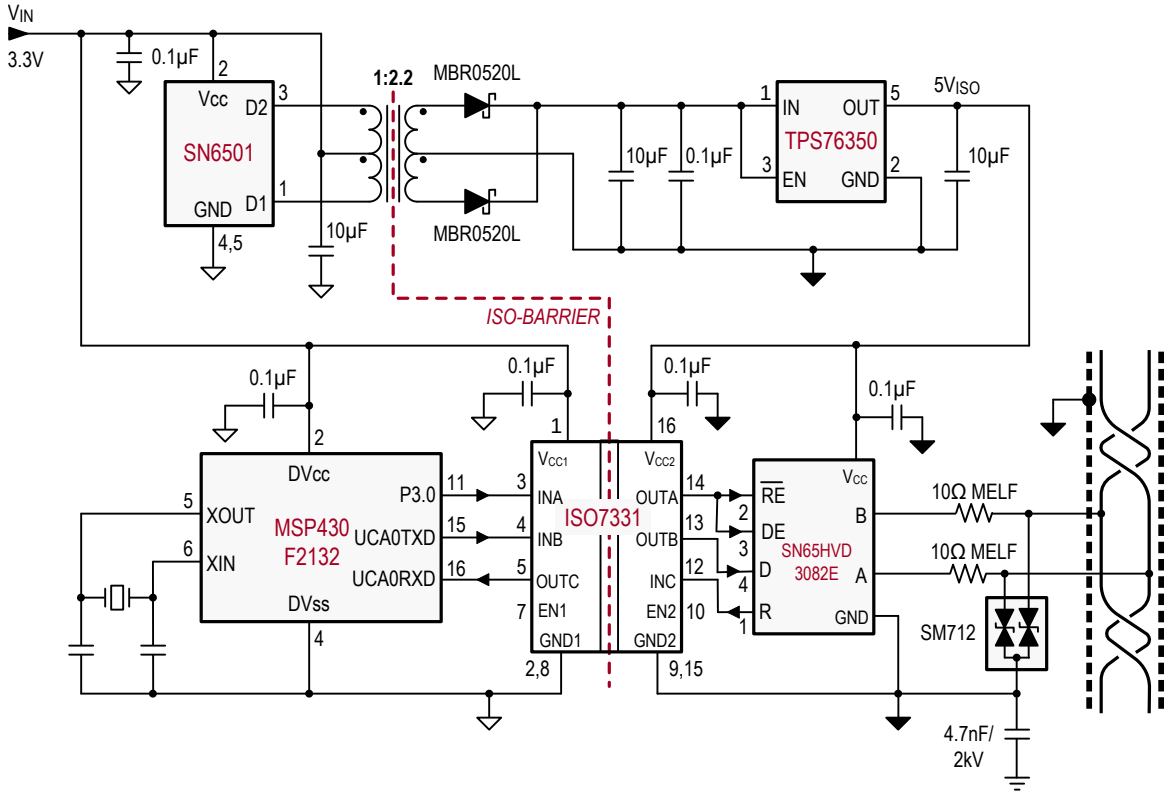


Figure 18. Typical ISO7331 Application Circuit

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Typical Supply Current Equations

ISO7330:

At $V_{CC1} = V_{CC2} = 5$ V
- $I_{CC1} = 0.46544 + (0.006455 \times f)$
- $I_{CC2} = 2.28021 + (0.08242 \times f) + (0.006237 \times f \times C_L)$

At $V_{CC1} = V_{CC2} = 3.3$ V
- $I_{CC1} = 0.29211 + (0.03588 \times f)$
- $I_{CC2} = 1.8414 + (0.02886 \times f) + (0.00548 \times f \times C_L)$

ISO7331:

At $V_{CC1} = V_{CC2} = 5$ V
- $I_{CC1} = 1.661 + (0.07916 \times f) + (0.00169 \times f \times C_L)$
- $I_{CC2} = 2.04 + (0.0778 \times f) + (0.00422 \times f \times C_L)$

At $V_{CC1} = V_{CC2} = 3.3$ V
- $I_{CC1} = 1.2402 + (0.03127 \times f) + (0.001954 \times f \times C_L)$
- $I_{CC2} = 1.53839 + (0.02933 \times f) + (0.0037285 \times f \times C_L)$

I_{CC1} and I_{CC2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF.

9.2.2 Detailed Design Procedure

9.2.2.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO733x incorporate many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

Typical Application (continued)

9.2.3 Application Performance Curves

Typical eye diagrams of ISO733x below indicate low jitter and wide open eye at the maximum data rate of 25 Mbps.

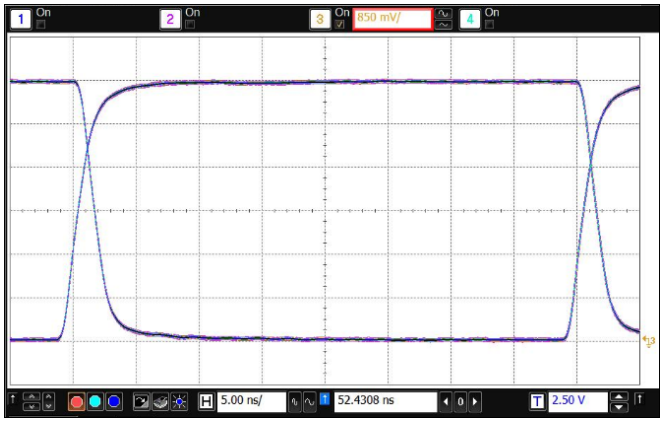


Figure 19. Eye Diagram at 25 Mbps, 5 V and 25°C

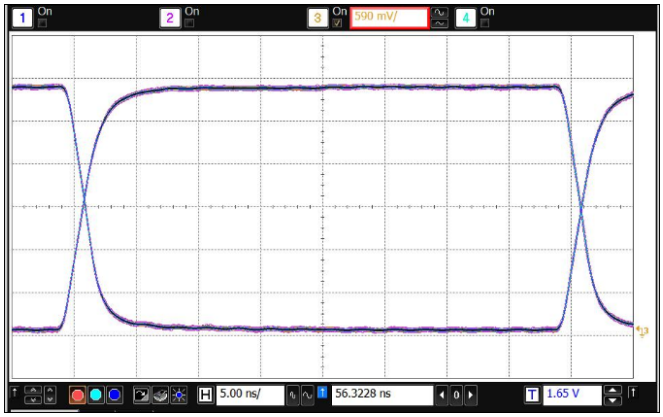


Figure 20. Eye Diagram at 25 Mbps, 3.3 V and 25°C

9.2.4 Systems Examples

Unlike Optocouplers, which need external components to improve performance, provide bias, or limit current, ISO733x only needs two external bypass capacitors to operate.

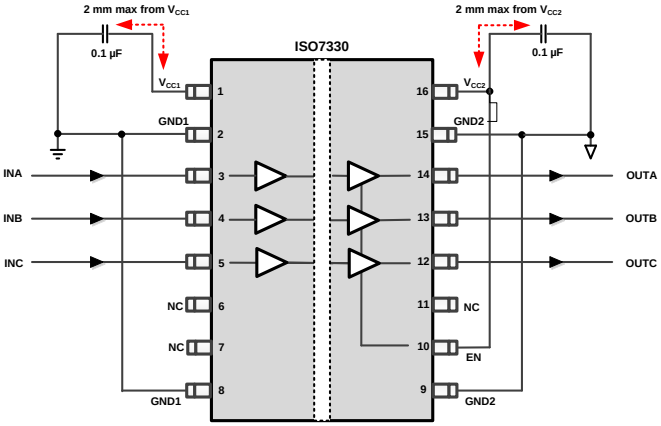


Figure 21. Typical ISO7330 Circuit Hook-up

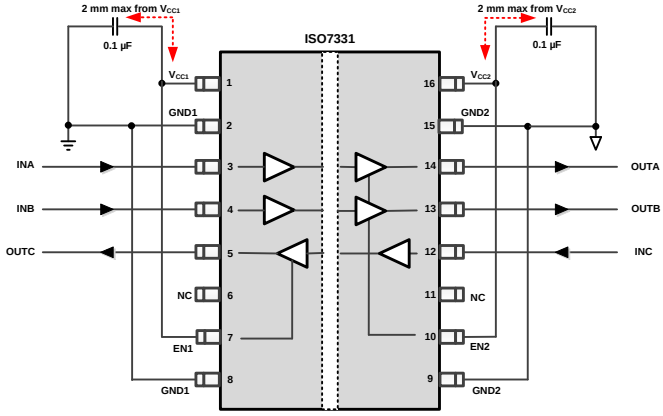


Figure 22. Typical ISO7331 Circuit Hook-up

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1 µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 datasheet (SLLSEA0) .

11 Layout

11.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

11.2 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 23). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

11.3 Layout Example

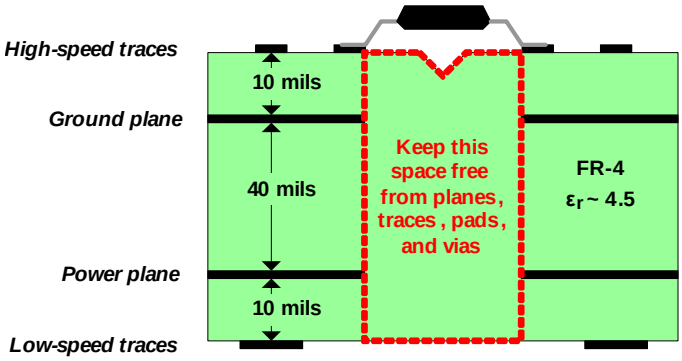


Figure 23. Recommended Layer Stack

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7330C	Click here	Click here	Click here	Click here	Click here
ISO7330FC	Click here	Click here	Click here	Click here	Click here
ISO7331C	Click here	Click here	Click here	Click here	Click here
ISO7331FC	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

DeviceNet is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

SLLA353, *Isolation Glossary*

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7330CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330C	Samples
ISO7330CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330C	Samples
ISO7330FCDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330FC	Samples
ISO7330FCDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330FC	Samples
ISO7331CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331C	Samples
ISO7331CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331C	Samples
ISO7331FCDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331FC	Samples
ISO7331FCDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331FC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

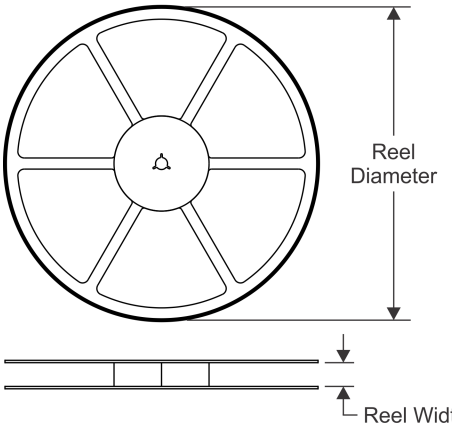
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

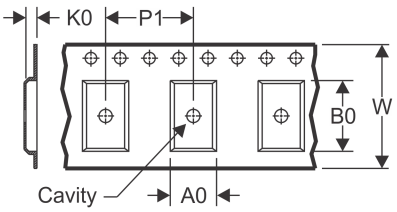
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

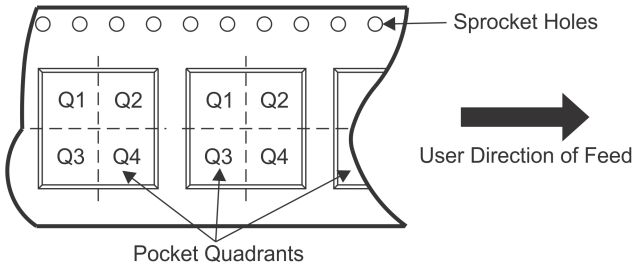


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

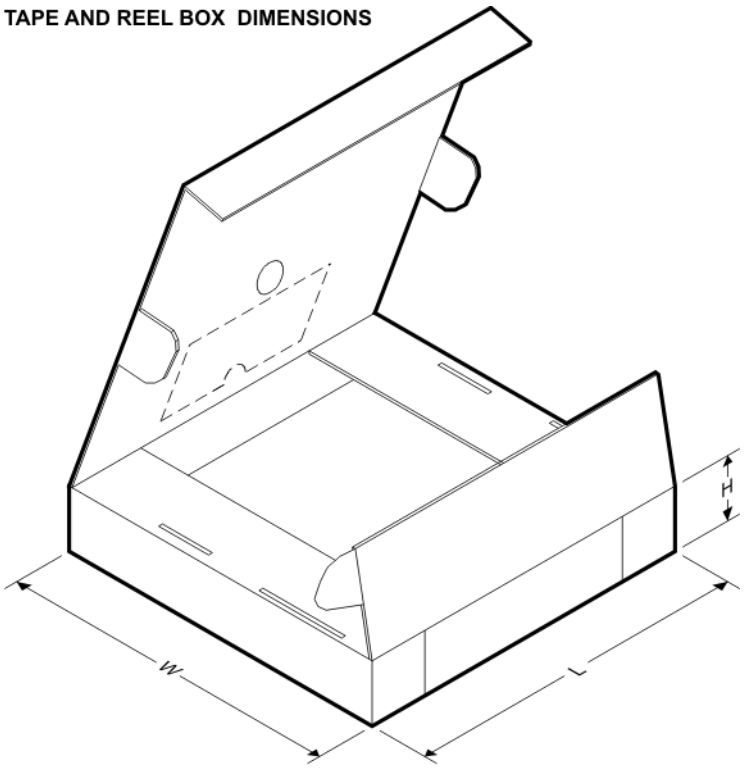
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7330CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7330FCDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7331CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7331FCDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7330CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7330FCDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7331CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7331FCDWR	SOIC	DW	16	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

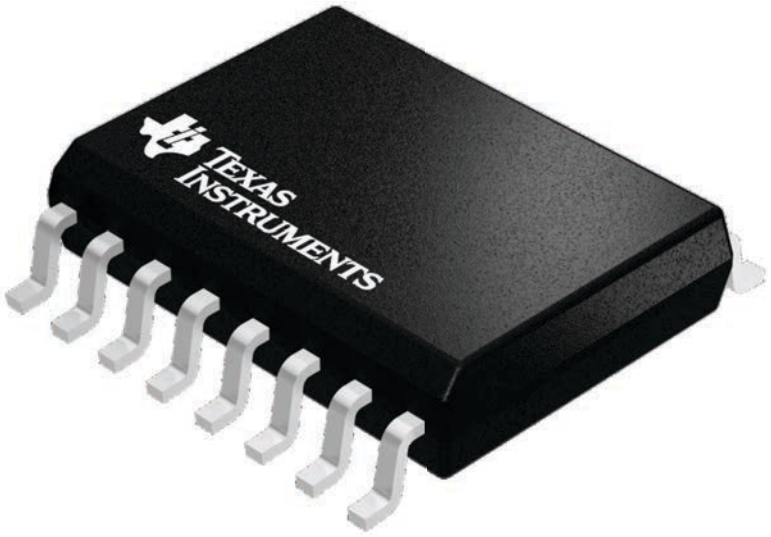
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

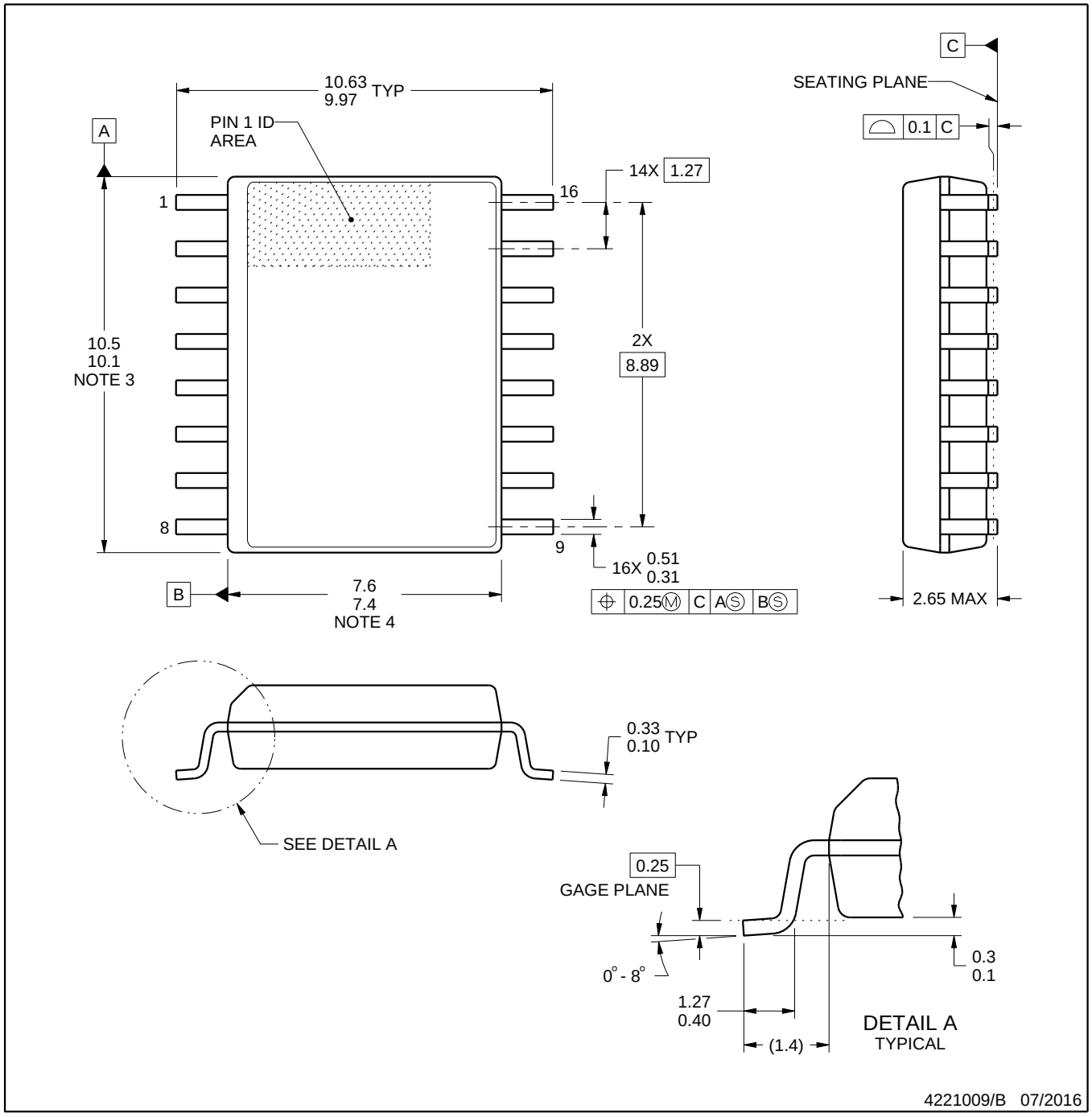
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



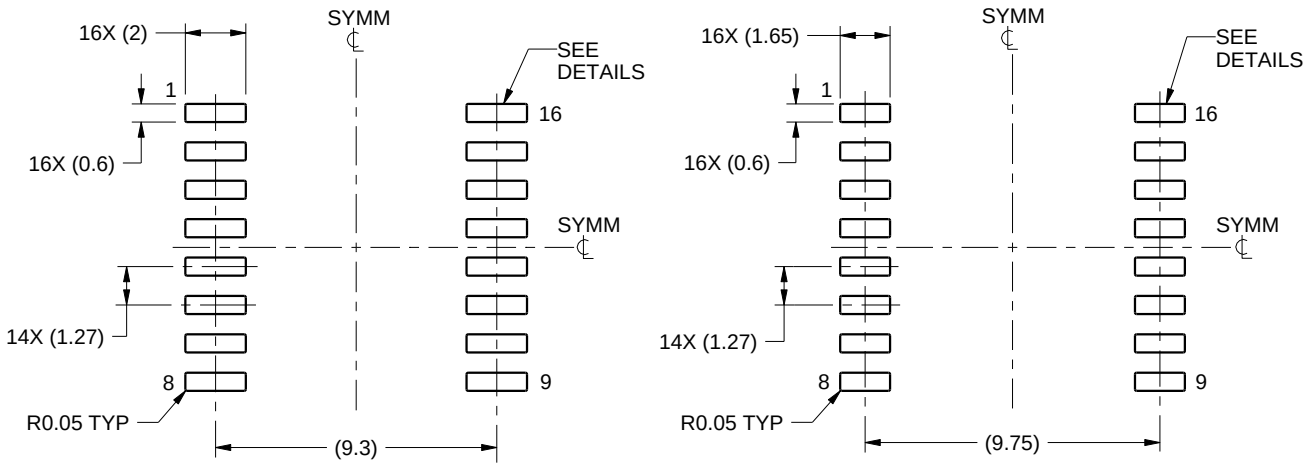
4224780/A

SOIC



NOTES:

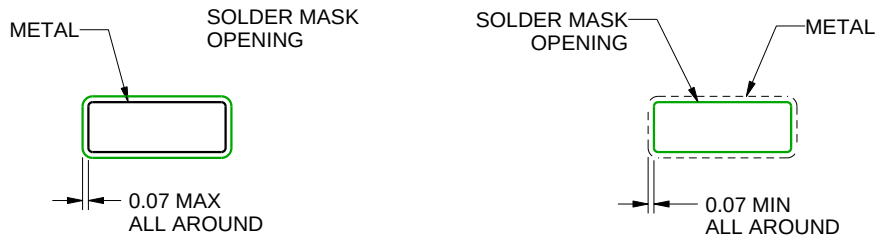
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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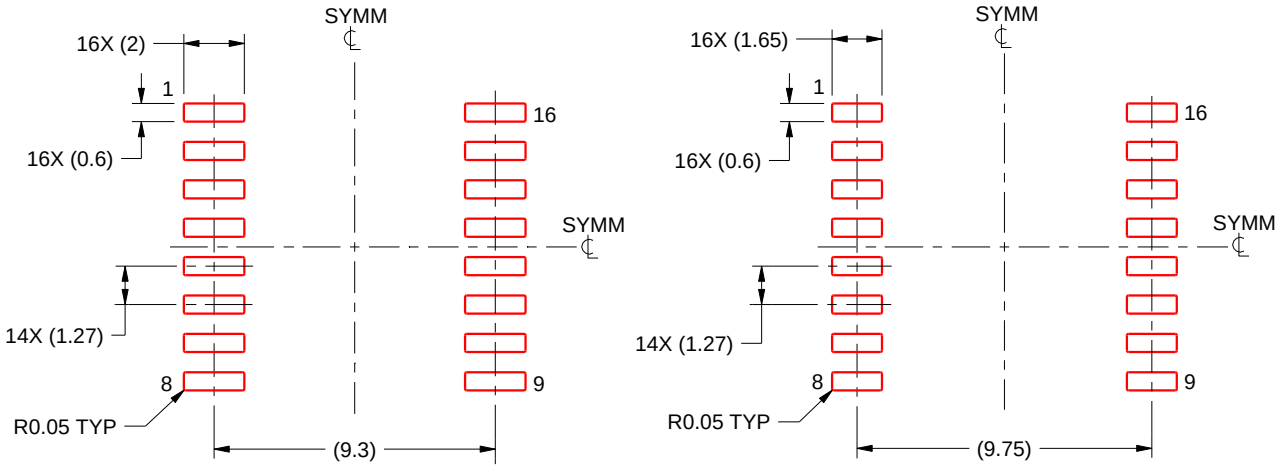
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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