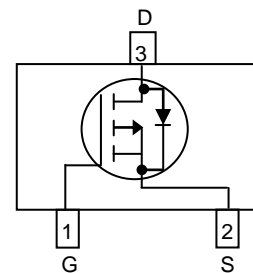


WPM3401
Single P-Channel, -30V, -4.6A, Power MOSFET
www.sh-willsemi.com

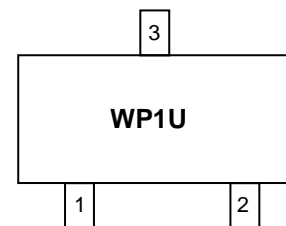
V_{DS} (V)	Max $R_{DS(on)}$ (m Ω)
-30	53@ $V_{GS}=-10V$
	56@ $V_{GS}=-4.5V$


SOT-23-3L
Descriptions

The WPM3401 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.


Pin configuration (Top view)
Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance for higher DC current
- Small package SOT-23-3L



WP1= Specific Device Code

U = Date Code

Marking
Applications

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

Order information

Device	Package	Shipping
WPM3401-3/TR	SOT-23-3L	3000/Reel&Tape

Absolute Maximum ratings

Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	-30		V
Gate-Source Voltage		V_{GS}	± 12		
Continuous Drain Current ^a	$T_A=25^\circ\text{C}$	I_D	-5.5	-4.6	A
	$T_A=70^\circ\text{C}$		-4.4	-3.6	
Maximum Power Dissipation ^a	$T_A=25^\circ\text{C}$	P_D	1.7	1.3	W
	$T_A=70^\circ\text{C}$		1.1	0.8	
Continuous Drain Current ^b	$T_A=25^\circ\text{C}$	I_D	-5.0	-4.2	A
	$T_A=70^\circ\text{C}$		-4.0	-3.4	
Maximum Power Dissipation ^b	$T_A=25^\circ\text{C}$	P_D	1.4	1.0	W
	$T_A=70^\circ\text{C}$		0.9	0.6	
Pulsed Drain Current ^c		I_{DM}	-20		A
Operating Junction Temperature		T_J	150		$^\circ\text{C}$
Lead Temperature		T_L	260		$^\circ\text{C}$
Storage Temperature Range		T_{stg}	-55 to 150		$^\circ\text{C}$

Thermal resistance ratings

Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance ^a	$t \leq 10 \text{ s}$	$R_{\theta JA}$	70	90	$^\circ\text{C/W}$
	Steady State		95	125	
Junction-to-Ambient Thermal Resistance ^b	$t \leq 10 \text{ s}$	$R_{\theta JA}$	85	105	
	Steady State		120	150	
Junction-to-Case Thermal Resistance		$R_{\theta JC}$	40	60	

a Surface mounted on FR-4 Board using 1 square inch pad size, 1oz copper

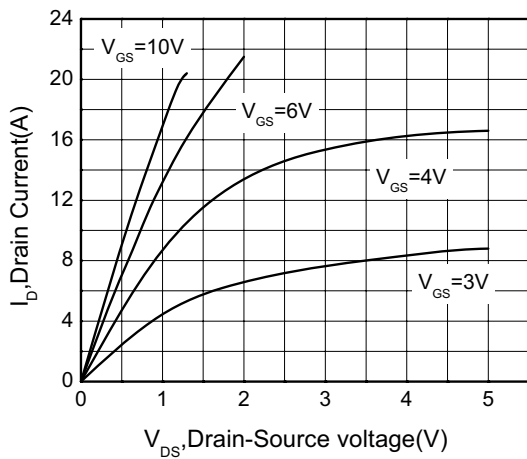
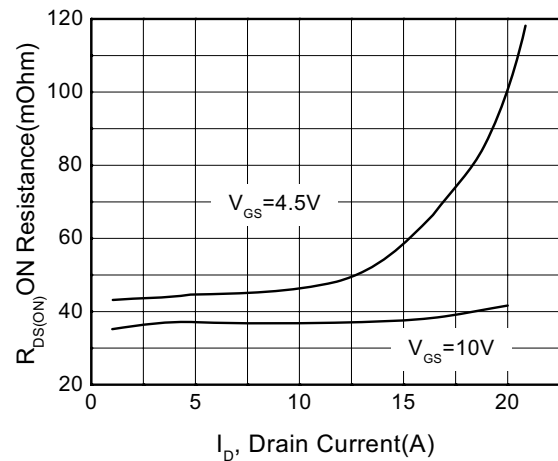
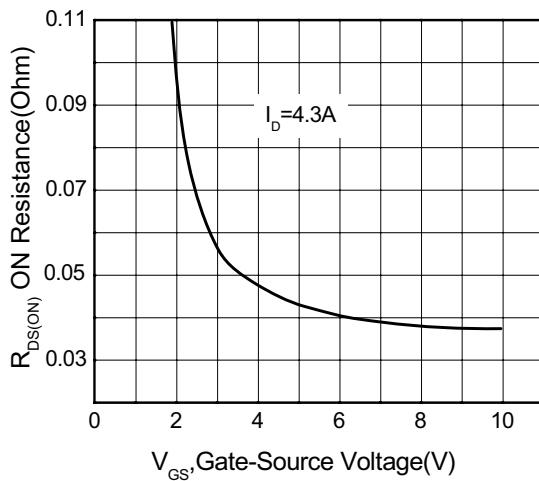
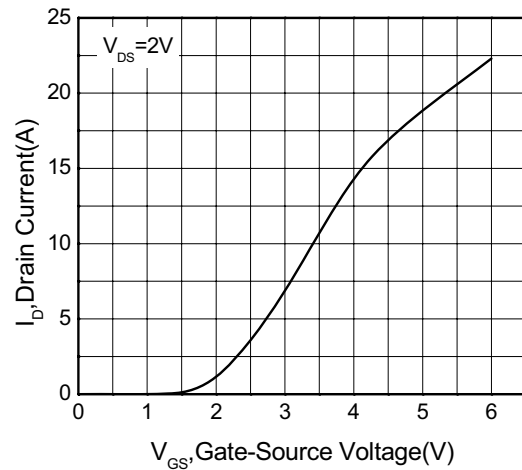
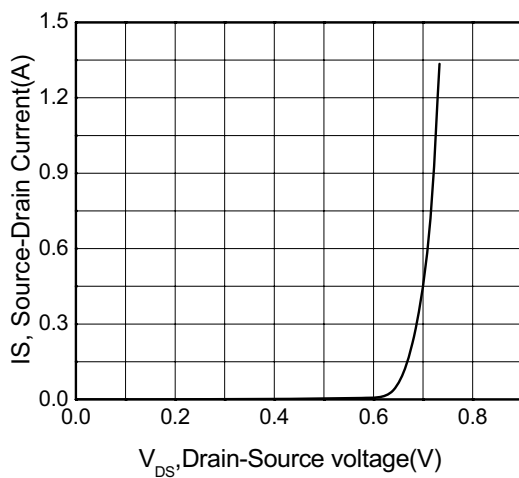
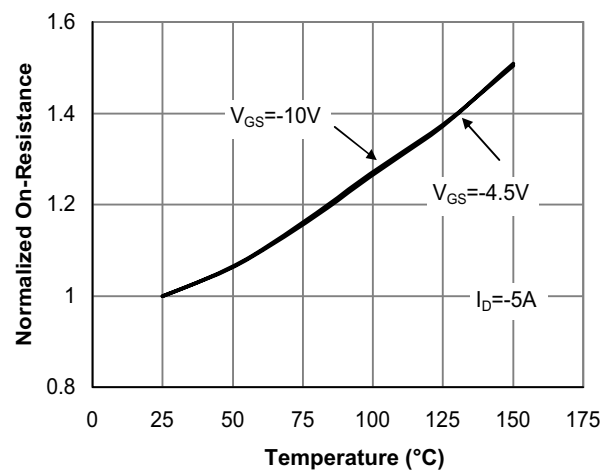
b Surface mounted on FR-4 board using minimum pad size, 1oz copper

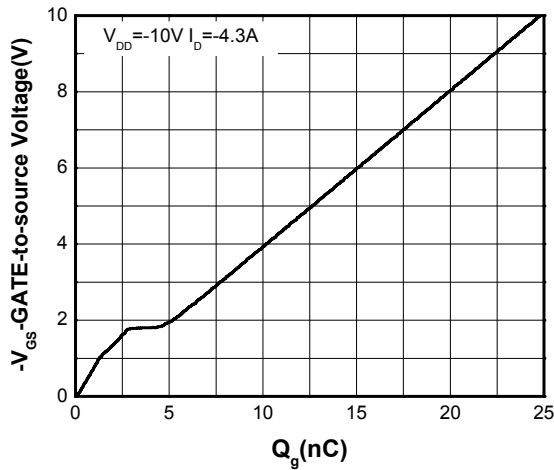
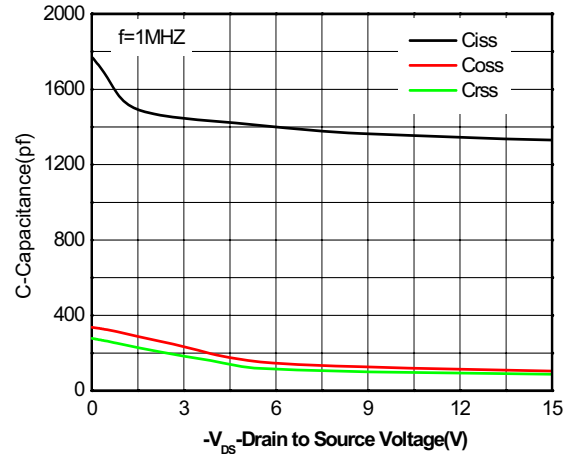
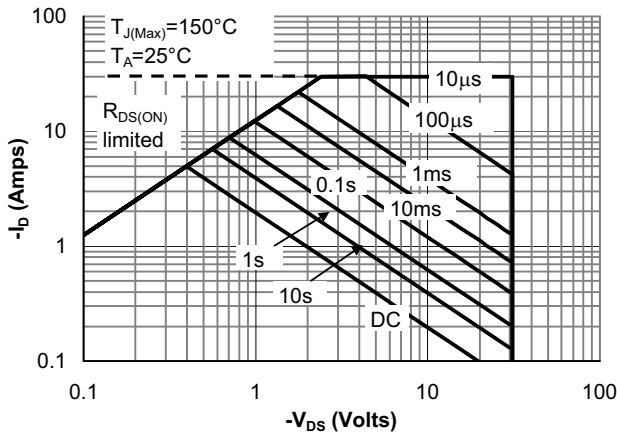
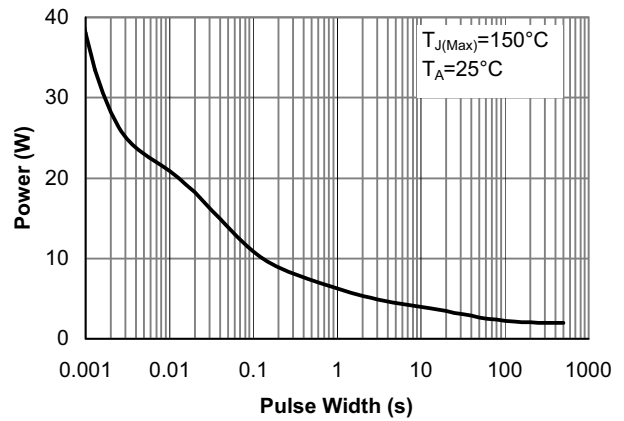
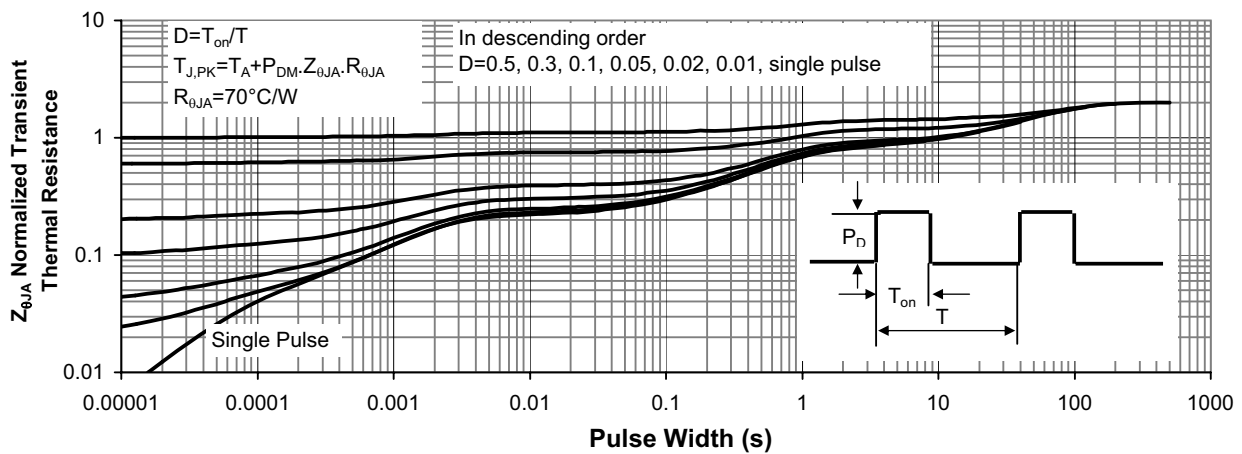
c Pulse width < 380 μs , Duty Cycle < 2%

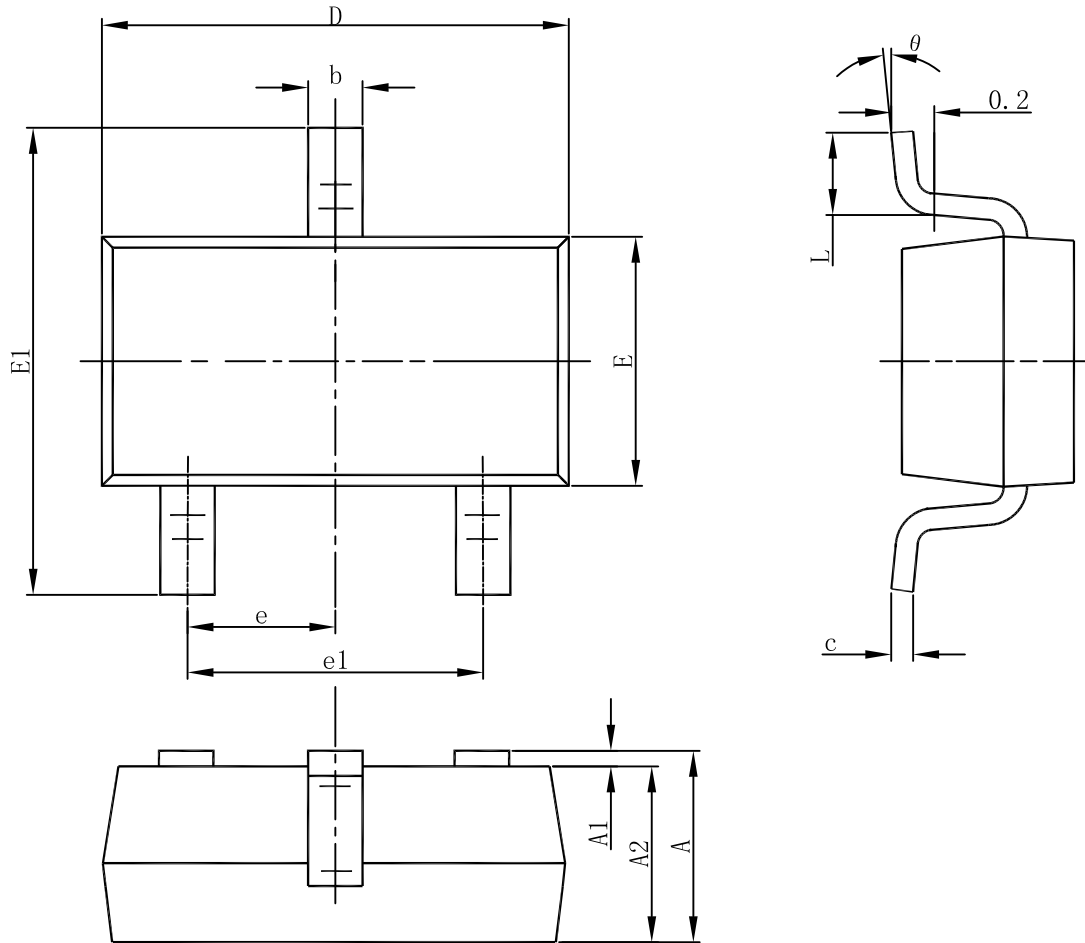
d Maximum junction temperature $T_J=150^\circ\text{C}$.

Electronics Characteristics (Ta=25°C, unless otherwise noted)

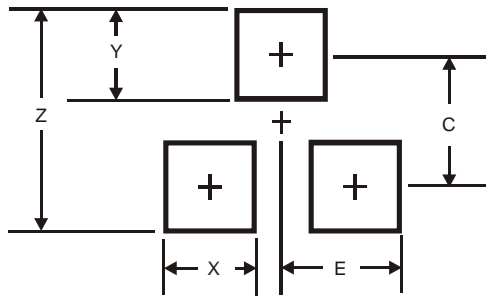
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = -250\mu\text{A}$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	uA
		$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}, T_J = 85^\circ\text{C}$			-5	
Gate-to-source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-0.5	-1.0	-1.5	V
On State Drain Current (Pulse) ^{b, c}	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -4.5\text{ V}$	-10			A
Drain-to-source On-resistance ^{b, c}	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -4.3\text{ A}$		38	53	mΩ
		$V_{GS} = -4.5\text{ V}, I_D = -3.5\text{ A}$		43	56	
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -1.0\text{ A}$		-0.75	-1.5	V
Forward Transconductance	G_{FS}	$V_{DS} = -15\text{ V}, I_D = -4.3\text{ A}$		13		s
CAPACITANCES, CHARGES						
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz},$ $V_{DS} = -15\text{ V}$		1250		pF
Output Capacitance	C_{OSS}			106		
Reverse Transfer Capacitance	C_{RSS}			90		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10\text{ V},$ $V_{DD} = -10\text{ V},$ $I_D = -4.3\text{ A}$		24.8		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.3		
Gate-to-Source Charge	Q_{GS}			2.2		
Gate-to-Drain Charge	Q_{GD}			1.8		
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_d(ON)$	$V_{GEN} = -10\text{ V}, V_{DD} = -15\text{ V},$ $I_D = -1.0\text{ A}, R_G = 6\Omega, R_L = 15\Omega$		10		ns
Rise Time	t_r			18		
Turn-Off Delay Time	$t_d(OFF)$			60		
Fall Time	t_f			9		

Typical Characteristics (Ta=25°C, unless otherwise noted)

Drain Current VS Drain-Source voltage

Drain Current vs ON Resistance

Gate-Source Voltage vs ON Resistance

Drain Current VS Gate-Source Voltage

Drain Current VS Source-Drain Current

On-Resistance vs. Junction


Gate Charge Characteristics

Capacitance Characteristics

Maximum Forward Biased Safe Operating Area (Note E)

Single Pulse Power Rating Junction-to-Ambient (Note E)

Normalized Maximum Transient Thermal Impedance

Package outline dimensions
SOT-23-3L


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Suggested Land Pattern
SOT-23-3L


Dimensions	Value (mm)
Z	2.9
X	0.8
Y	0.9
C	2.0
E	1.35