

USB Type-C Sink Port Detection and Protection IC

BD91N01NUX

General Description

BD91N01NUX integrates USB Type-C CC detection including plug attach, detach, orientation and current value for power sink side port.

The Pch-MOSFET switch control function protects next stage system side circuit from VBUS over voltage and under voltage.

Features

- USB Type-C Specification 1.0 to 1.3 Support
- USB Type-C Plug Attach and Detach Detection
- USB Type-C Plug Orientation Detection
- USB Type-C Current Detection
- VBUS Over Voltage and Under Voltage Protection
- Direct VBUS Power Supply Operation Support
- Dead-battery Operation Support
- Integrated Rd Resistor

Applications

USB Type-C Power Sink/UFP Side Equipment: Printer, Scanner, Electric Cigarette, Al Speaker, Camera

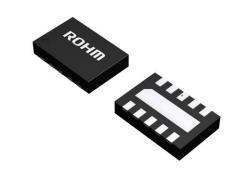
Typical Application Circuit

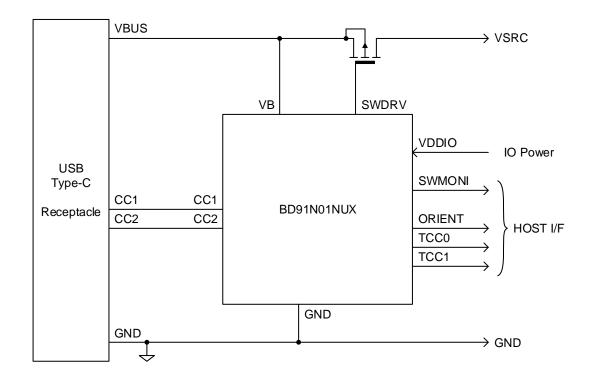


■ VBUS Voltage Range:
■ VDDIO Voltage Range:
■ VBUS, CC Pin Tolerance Voltage:
4.0 V to 5.5 V
1.7 V to 5.5 V
■ VBUS, CC Pin Tolerance Voltage:

■ Operation Temperature Range: -30 °C to +85 °C

Package W (Typ) x D (Typ) x H (Max) VSON010X3020 3.00 mm x 2.00 mm x 0.60 mm

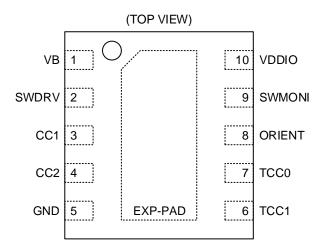




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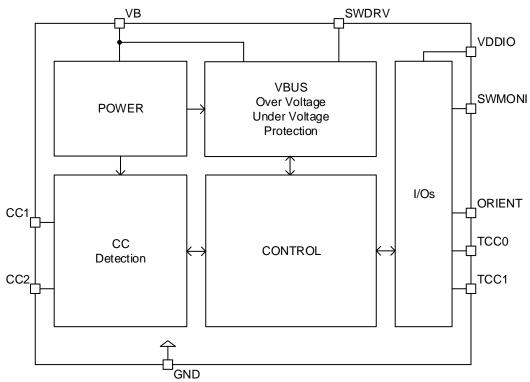
Pin Configuration



Pin Descriptions

Docompaione		
Pin No.	Pin Name	Description
1	VB	Power supply from VBUS
2	SWDRV	Pch-MOSFET switch driver output
3	CC1	USB Type-C configuration channel 1
4	CC2	USB Type-C configuration channel 2
5	GND	Ground
6	TCC1	USB Type-C current detection result data 1
7	TCC0	USB Type-C current detection result data 0
8	ORIENT	USB Type-C plug orientation detection result
9	SWMONI	Pch-MOSFET control state output
10	VDDIO	Power supply for I/O
-	EXP-PAD	The EXP-PAD is connected to GND.

Block Diagram



Description of Blocks

(CC Detection)

The CC pin has a built-in pull-down resistor Rd to connect to the USB Type-C Source device.

When the Source side is connected to the CC pin, a divided voltage is generated at the CC pin by the pull-up resistor (current source) on the Source side. With this voltage, the IC detects plug insertion (USB Type-C Plug Attach state), plug orientation, and USB Type-C Source side current type (USB Default, USB Type-C 1.5 A, USB Type-C 3.0 A).

CC1 Pin	CC2 Pin	Detection State	Pch-MOSFET	ORIENT	TCC1	TCC0	
< 0.15 V	< 0.15 V	USB Type-C Plug Detach	OFF	"L"	"L"	"L"	
USB Default		CC1 connection, USB Default			"L"	"H"	
USB Type-C 1.5 A	< 0.15 V	CC1 connection, USB Type-C 1.5 A	ON "	,	"L"	"H"	"L"
USB Type-C 3.0 A		CC1 connection, USB Type-C 3.0 A			"H"	"H"	
	USB Default	CC2 connection, USB Default		"H"	"L"	"H"	
< 0.15 V	USB Type-C 1.5 A	CC2 connection, USB Type-C 1.5 A	_		"H"	"L"	
	USB Type-C 3.0 A	CC2 connection, USB Type-C 3.0 A			"H"	"H"	

When the CC pin voltage is following case, it detects as abnormal condition.

	CC1 Pin	CC2 Pin	Detection State	Pch-MOSFET	ORIENT	TCC1	TCC0
0	.25 V to 2.18 V	0.25 V to 2.18 V	Connection of a product breaking the USB Type-C standard	OFF	"["	"["	"["
	> 2.5 V	-	Abnormality of the pull-up	OFF	L	L	
	-	> 2.5 V	resistance value at the DFP side				

(VBUS Over Voltage, Under Voltage Protection)

When the IC detects a VBUS over voltage, the SWDRV pin outputs a high and turns off the external Pch-MOSFET switch. If the over voltage detection state continues for a fixed period of time, the switch off state is latched. The latch state lasts until the VBUS voltage falls below the UVLO detection voltage and IC is reset.

If the over voltage detection state does not continue for a fixed period of time, the switch off state automatically recovers.

The SWDRV pin is a driver output for external Pch-MOSFET switch. The SWMONI pin outputs the state of the driver. The SWDRV pin is decided in a state of the CC pin when the IC is booted up by supply of VB. It does not be OFF even if the condition becomes OFF condition once after it is turned on.

SWDRV Pin Output	Pch-MOSFET Switch State	SWMONI Pin Data
"H" (VBUS Voltage)	OFF	"L"
"I " (GND Voltage)	ON	"H"

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
VBUS Input Range (VB Pin)	V _B	-0.3 to +28.0	V
GND Input Range	V_{G}	0	V
VDDIO Input Range	V_{DDIO}	-0.3 to +7.0	V
SWDRV Pin Voltage	V_{SWD}	-0.3 to +28.0	V
CC1/CC2 Pin voltage	Vcc	-0.3 to +28.0	V
Others Pins	V_{MAX}	-0.3 to +7.0	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance(Note 1)

Deversates	Curre le el	Thermal Res	l locit			
Parameter	Symbol	1s ^(Note 3)	2s2p ^(Note 4)	Unit		
VSON010X3020						
Junction to Ambient	θ_{JA}	274.8	39.4	°C/W		
Junction to Top Characterization Parameter ^(Note 2)	Ψ_{JT}	31	6	°C/W		

Footprints and Traces

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt
Тор	<u>'</u>	
Copper Pattern	Thickness	
Footprints and Traces	70 µm	
Layer Number of Measurement Board	Material	Board Size

Measurement board				FILCII	Diameter	
4 Layers FR-4		114.3 mm x 76.2 mm	x 1.6 mmt	1.20 mm	Ф0.30 mm	
Тор		2 Internal Laye	ers	Bottom		
Copper Pattern Thickness		Copper Pattern	Thickness	Copper Pattern	Thickness	

35 µm

74.2 mm x 74.2 mm

(Note 5) This thermal via connects with the copper pattern of all layers.

70 µm

Thermal Via^(Note 5)

70 µm

74.2 mm x 74.2 mm

Recommended Operating Conditions

Parameter	Symbol	Min	Тур	Max	Unit
VBUS Input Voltage (VB Pin)	V _B	4.0	5.0	5.5	V
VDDIO Input Voltage	V_{DDIO}	1.7	3.3	5.5	V
Operating Temperature	Topr	-30	+25	+85	°C

Electrical Characteristics

(Unless otherwise specified $V_B = 5.0 \text{ V}$, $V_{DDIO} = 3.3 \text{ V}$, $Ta = 25 ^{\circ}\text{C}$)

(Unless otherwise specified $V_B = 5.0$	$V, V_{DDIO} =$	3.3 V, Ia =	25 °C)	T	1	T
Parameter	Symbol	Min	Тур	Max	Unit	Condition
ICC	1				1	ı
VDDIO ICC	I _{DDIO}	-	-	15	μA	-
VB ICC	I _B	-	125	-	μA	-
VBUS Voltage Detection (VB)						
VBUS Detection Voltage	V_{UVREL}	-	-	3.67	V	UVLO release
VBUS UVLO Voltage	V _{UVDET}	2.95	-	-	V	UVLO detect
VBUS Over Voltage Detection	V _{OVDET}	6.0	6.7	7.0	V	-
CC Pin Detection (CC1, CC2)						
Power Source Attached Detection Voltage Range	V _{RPDET}	0.25	-	2.18	V	-
Type-C Current @USB Default Detection Voltage Range	V _{CDEF}	0.25	-	0.61	V	-
Type-C Current @1.5 A Detection Voltage Range	V _{C15}	0.70	-	1.16	V	-
Type-C Current @3.0 A Detection Voltage Range	V _{C30}	1.31	-	2.04	V	-
CC Pin Resistance Rd	R_D	4.59	5.10	5.61	kΩ	$I_L = 0.2 \text{ mA}$
SWDRV Characteristic						
H Level Output Voltage	V _{OHSW}	4.75	-	-	V	I _L = +1 mA
L Level Output Voltage	V_{OLSW}	-	-	0.12	V	$I_L = -1 \text{ mA}$
I/O Characteristic (SWMONI, ORIE	NT, TCC1,	TCC0)				
H Level Output Voltage	V_{OH}	2.805	-	-	V	I _L = +100 μA
L Level Output Voltage	V _{OL}	-	-	0.3	V	I _L = -100 μA
TCC Detection Removal Pulse Width	t _F	100	-	500	μs	-

Typical Performance Curves

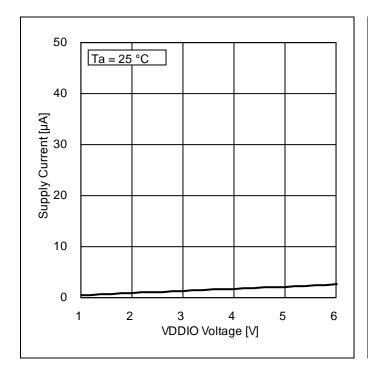


Figure 1. Supply Current vs VDDIO Voltage

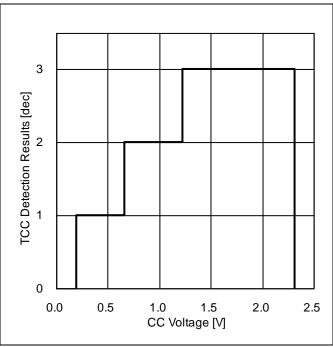


Figure 2. TCC Detection Results vs CC Voltage (TCC Detection Results:

0: Non-Connection, 1: Default, 2: 1.5 A, 3: 3.0 A)

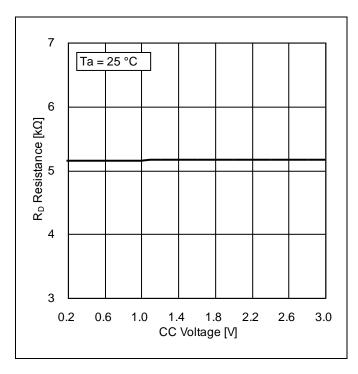


Figure 3. R_D Resistance vs CC Voltage

Timing Chart

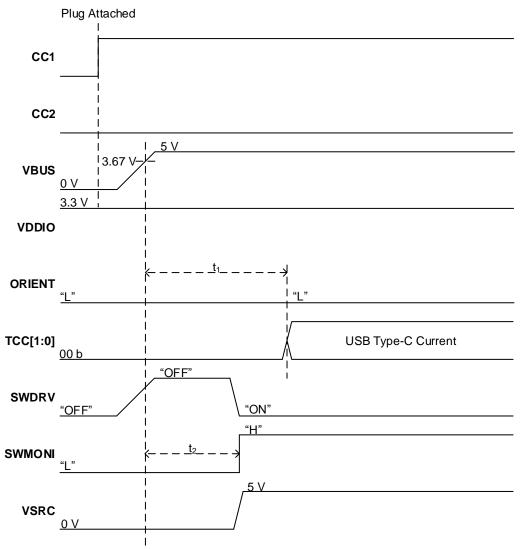


Figure 4. Plug Attached Timing Chart

Parameter	Symbol	Min	Тур	Max	Unit
Detection Data Invalid Time	t ₁	-	-	12	ms
SWDRV Turn on Time	t ₂	-	-	10	ms

Timing Chart - continued

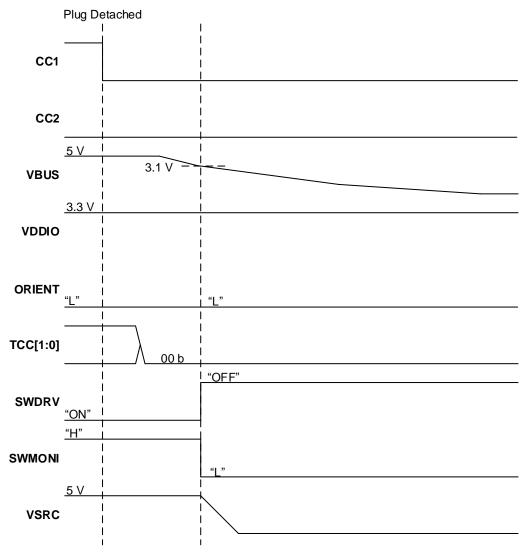


Figure 5. Plug Detached Timing Chart

Timing Chart - continued

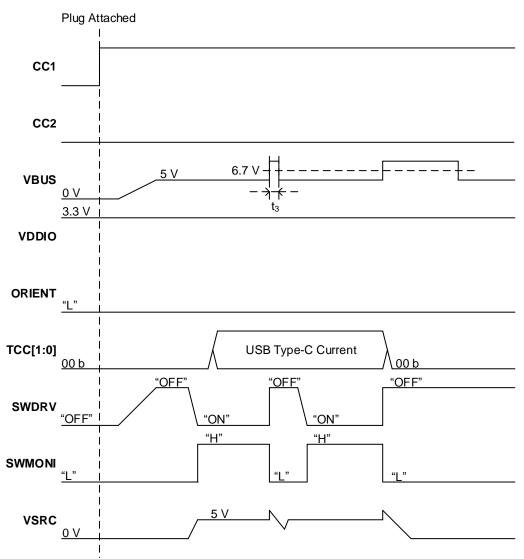


Figure 6. VBUS Over Voltage Detection Timing Chart

Parameter	Symbol	Min	Тур	Max	Unit
Auto Recovery Pulse Width(Note 6)	t ₃	-	-	10	μs

(Note 6) When VBUS Over Voltage Detection period is shorter than this, the Pch-MOSFET switch is turned on again.

Timing Chart - continued

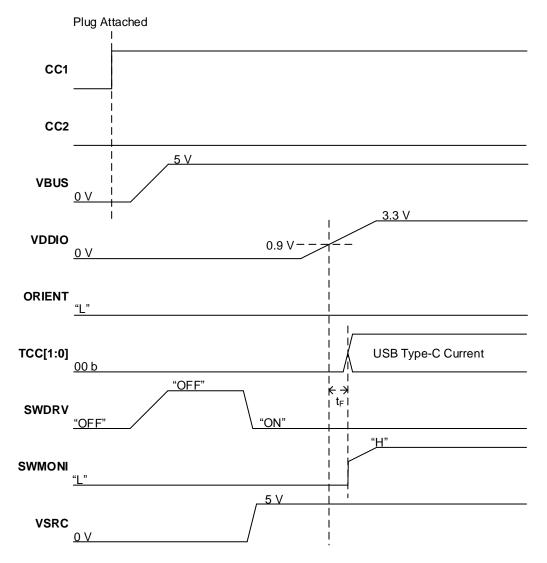
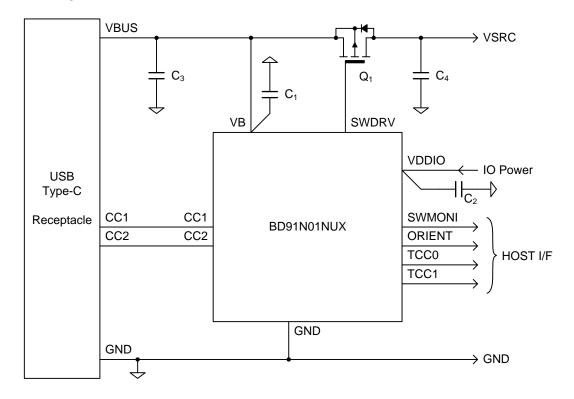


Figure 7. I/O Output Timing Chart

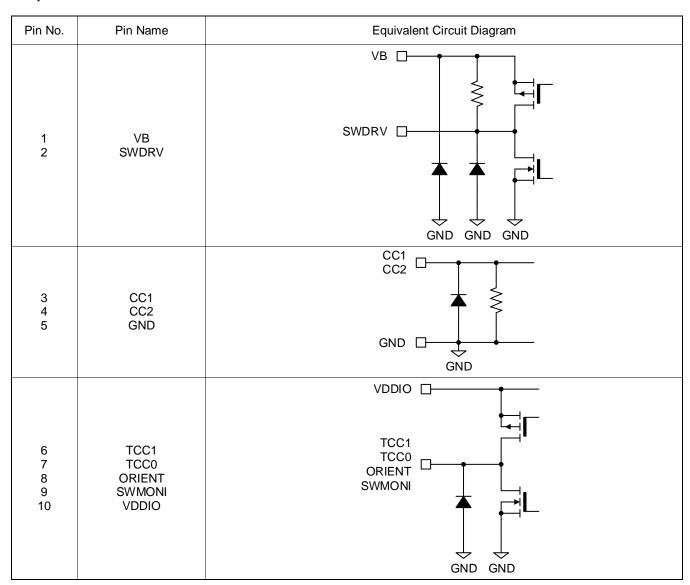
Application Example



Selection of Components Externally Connected

- Use Pch-MOSFET having tolerance voltage between the source gate more than the expected maximum abnormal VBUS voltage. Connect the source pin to the USB Type-C receptacle VBUS side so that VBUS current does not pass through the parasitic diode. When backflow by parasitic diode from the VSRC side to VBUS is an issue, use two Q_1 in a reverse direction each other. VBUS current of up to 3 A passes through Q_1 . Therefore, use Pch-MOSFET of the low "ON-Resistance" (R_{ON}).
- (C_1, C_2) Some sort of noise can occur and be a problem if the wiring between VBUS and the VB pin and between IO Power and the VDDIO pin become long. In this case, connect a power supply by-pass capacitor which has appropriate value of C_1 and C_2 against to the noise.
- (C_3)
 If the IC is connected to a Power Adapter corresponds to the USB Type-C Power Delivery (USBPD), capacitance of the sink port until connection complete (PD contract) is limited to 10 μ F or less in the USBPD Adaptor stipulation. Therefore, be careful about the sum total of C_1 and C_3 value.
- (C_4) If the IC is connected to a Power Adapter corresponds to the USB Type-C Power Delivery (USBPD), capacitance of the sink port until connection complete (PD contract) is limited to 100 μ F or less in the USBPD Adaptor stipulation. Therefore, be careful about the sum total of C_1 , C_3 and C_4 value.

I/O Equivalence Circuits



Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes - continued

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

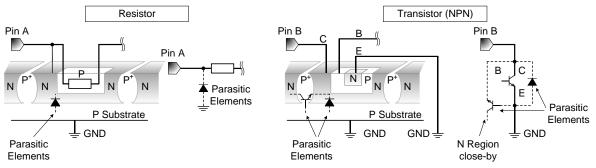
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode. When GND > Pin B, the P-N junction operates as a parasitic transistor.

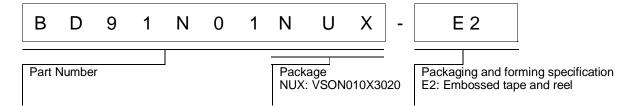
Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



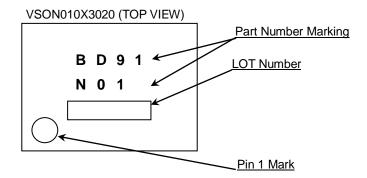
11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

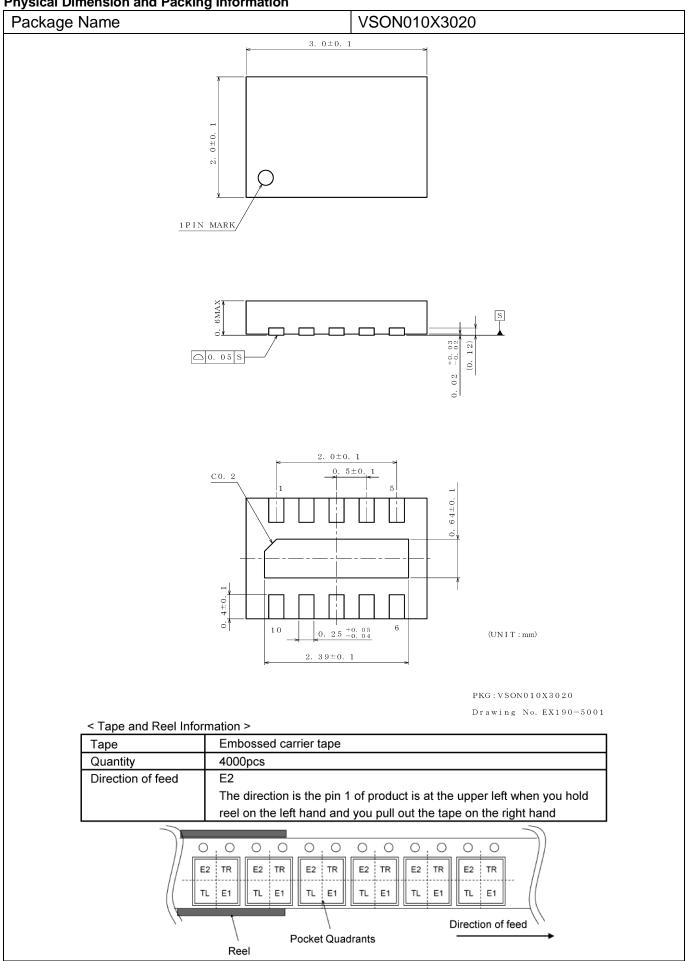
Ordering Information



Marking Diagram



Physical Dimension and Packing Information



Revision History

Date	Revision	Changes
07.Jun.2019	001	New Release

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JÁPAN	USA	EU	CHINA	
CLASSⅢ	CL ACCIII	CLASS II b	CLACCIII	
CLASSIV	CLASSⅢ	CLASSⅢ	CLASSⅢ	

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 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
- 4. The Products are not subject to radiation-proof design.
- 5. Please verify and confirm characteristics of the final or mounted products in using the Products.
- 6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- 7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- 8. Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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- 2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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- 1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
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- Even under ROHM recommended storage condition, solderability of products out of recommended storage time period
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 exceeding the recommended storage time period.
- 3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- 4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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