NCP1200

PWM Current-Mode Controller for Low-Power Universal Off-Line Supplies

Housed in SOIC−8 or PDIP−8 package, the NCP1200 represents a major leap toward ultra−compact Switchmode Power Supplies. Due to a novel concept, the circuit allows the implementation of a complete offline battery charger or a standby SMPS with few external components. Furthermore, an integrated output short−circuit protection lets the designer build an extremely low−cost AC−DC wall adapter associated with a simplified feedback scheme.

With an internal structure operating at a fixed 40 kHz, 60 kHz or 100 kHz, the controller drives low gate−charge switching devices like an IGBT or a MOSFET thus requiring a very small operating power. Due to current−mode control, the NCP1200 drastically simplifies the design of reliable and cheap offline converters with extremely low acoustic generation and inherent pulse−by−pulse control.

When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the skip cycle mode and provides excellent efficiency at light loads. Because this occurs at low peak current, no acoustic noise takes place.

Finally, the IC is self−supplied from the DC rail, eliminating the need of an auxiliary winding. This feature ensures operation in presence of low output voltage or shorts.

Features

- No Auxiliary Winding Operation
- Internal Output Short−Circuit Protection
- Extremely Low No−Load Standby Power
- Current−Mode with Skip−Cycle Capability
- Internal Leading Edge Blanking
- 250 mA Peak Current Source/Sink Capability
- Internally Fixed Frequency at 40 kHz, 60 kHz and 100 kHz
- Direct Optocoupler Connection
- Built−in Frequency Jittering for Lower EMI
- SPICE Models Available for TRANsient and AC Analysis
- Internal Temperature Shutdown
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- AC−DC Adapters
- Offline Battery Chargers
- Auxiliary/Ancillary Power Supplies (USB, Appliances, TVs, etc.)

ON Semiconductor®

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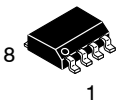
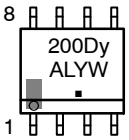
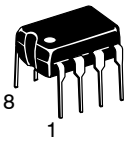
MARKING DIAGRAMS

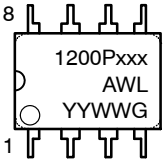


SOIC−8
D SUFFIX
CASE 751



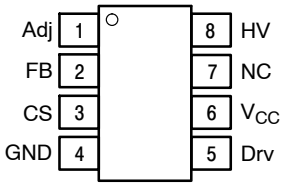


PDIP−8
P SUFFIX
CASE 626



xxx	= Device Code: 40, 60 or 100
y	= Device Code:
	4 for 40
	6 for 60
	1 for 100
A	= Assembly Location
L	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G, ▪	= Pb−Free Package

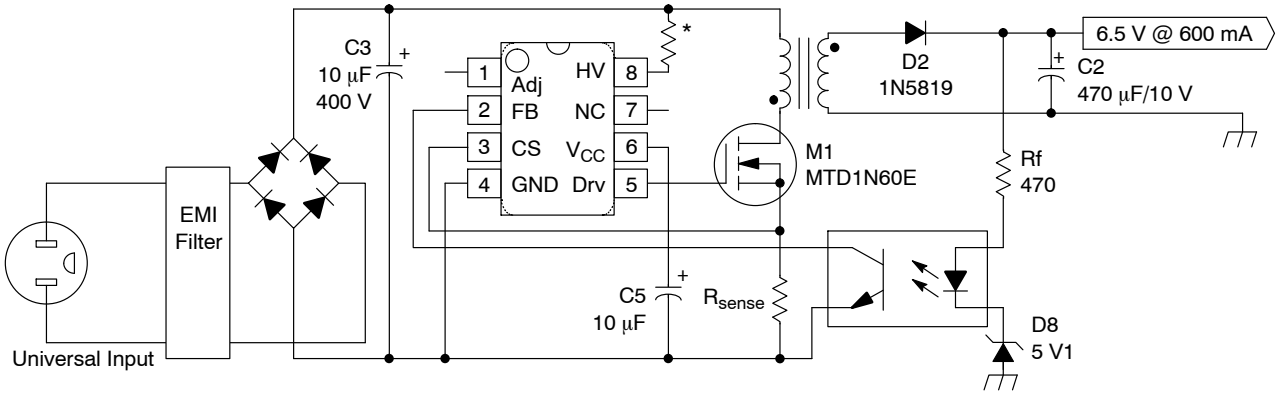
PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.



*Please refer to the application information section

Figure 1. Typical Application

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	Adj	Adjust the Skipping Peak Current	This pin lets you adjust the level at which the cycle skipping process takes place.
2	FB	Sets the Peak Current Setpoint	By connecting an Optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand.
3	CS	Current Sense Input	This pin senses the primary current and routes it to the internal comparator via an L.E.B.
4	GND	The IC Ground	
5	Drv	Driving Pulses	The driver's output to an external MOSFET.
6	V_{CC}	Supplies the IC	This pin is connected to an external bulk capacitor of typically 10 μF.
7	NC	No Connection	This un−connected pin ensures adequate creepage distance.
8	HV	Generates the V_{CC} from the Line	Connected to the high−voltage rail, this pin injects a constant current into the V_{CC} bulk capacitor.

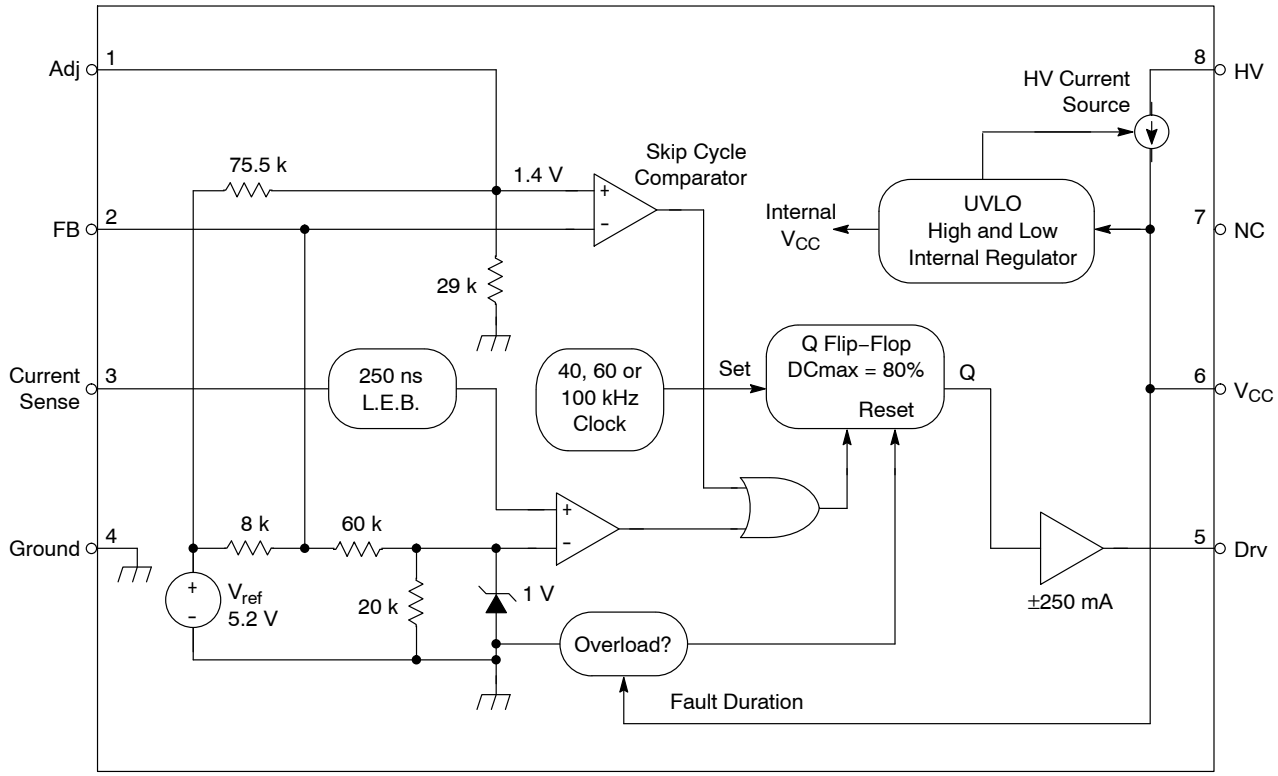


Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Units
Power Supply Voltage	V_{CC}	16	V
Thermal Resistance Junction−to−Air, PDIP−8 version Thermal Resistance Junction−to−Air, SOIC version Thermal Resistance Junction−to−Case	$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JC}$	100 178 57	°C/W
Maximum Junction Temperature Typical Temperature Shutdown	T_{Jmax} –	150 140	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
ESD Capability, HBM Model (All Pins except V_{CC} and HV)	–	2.0	kV
ESD Capability, Machine Model	–	200	V
Maximum Voltage on Pin 8 (HV), pin 6 (V_{CC}) Grounded	–	450	V
Maximum Voltage on Pin 8 (HV), Pin 6 (V_{CC}) Decoupled to Ground with 10 μF	–	500	V
Minimum Operating Voltage on Pin 8 (HV)	–	30	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection rated using the following tests:
   Human Body Model (HBM) 2000 V per JEDEC Standard JESD22, Method A114E.
   Machine Model (MM) 200 V per JEDEC Standard JESD22, Method A115A.

ELECTRICAL CHARACTERISTICS (For typical values T_J = +25°C, for min/max values T_J = −25°C to +125°C, Max T_J = 150°C, V_{CC}= 11 V unless otherwise noted)

Rating	Pin	Symbol	Min	Typ	Max	Unit
DYNAMIC SELF−SUPPLY (All Frequency Versions, Otherwise Noted)						
V_{CC} Increasing Level at Which the Current Source Turns−off	6	V_{CCOFF}	10.3	11.4	12.5	V
V_{CC} Decreasing Level at Which the Current Source Turns−on	6	V_{CCON}	8.8	9.8	11	V
V_{CC} Decreasing Level at Which the Latchoff Phase Ends	6	$V_{CClatch}$	−	6.3	−	V
Internal IC Consumption, No Output Load on Pin 5	6	I_{CC1}	−	710	880 Note 1	μA
Internal IC Consumption, 1 nF Output Load on Pin 5, F_{SW} = 40 kHz	6	I_{CC2}	−	1.2	1.4 Note 2	mA
Internal IC Consumption, 1 nF Output Load on Pin 5, F_{SW} = 60 kHz	6	I_{CC2}	−	1.4	1.6 Note 2	mA
Internal IC Consumption, 1 nF Output Load on Pin 5, F_{SW} = 100 kHz	6	I_{CC2}	−	1.9	2.2 Note 2	mA
Internal IC Consumption, Latchoff Phase	6	I_{CC3}	−	350	−	μA
INTERNAL CURRENT SOURCE						
High−voltage Current Source, V_{CC} = 10 V	8	I_{C1}	2.8	4.0	−	mA
High−voltage Current Source, V_{CC} = 0 V	8	I_{C2}	−	4.9	−	mA
DRIVE OUTPUT						
Output Voltage Rise−time @ CL = 1 nF, 10−90% of Output Signal	5	T_r	−	67	−	ns
Output Voltage Fall−time @ CL = 1 nF, 10−90% of Output Signal	5	T_f	−	28	−	ns
Source Resistance (drive = 0, Vgate = V_{CCHMAX} − 1 V)	5	R_{OH}	27	40	61	Ω
Sink Resistance (drive = 11 V, Vgate = 1 V)	5	R_{OL}	5	12	25	Ω
CURRENT COMPARATOR (Pin 5 Un−loaded)						
Input Bias Current @ 1 V Input Level on Pin 3	3	I_{IB}	−	0.02	−	μA
Maximum internal Current Setpoint	3	I_{Limit}	0.8	0.9	1.0	V
Default Internal Current Setpoint for Skip Cycle Operation	3	I_{Lskip}	−	350	−	mV
Propagation Delay from Current Detection to Gate OFF State	3	T_{DEL}	−	100	160	ns
Leading Edge Blanking Duration	3	T_{LEB}	−	230	−	ns
INTERNAL OSCILLATOR (V_{CC} = 11 V, Pin 5 Loaded by 1 kΩ)						
Oscillation Frequency, 40 kHz Version	−	f_{OSC}	36	42	48	kHz
Oscillation Frequency, 60 kHz Version	−	f_{OSC}	52	61	70	kHz
Oscillation Frequency, 100 kHz Version	−	f_{OSC}	86	103	116	kHz
Built−in Frequency Jittering, F_{SW} = 40 kHz	−	f_{jitter}	−	300	−	Hz/V
Built−in Frequency Jittering, F_{SW} = 60 kHz	−	f_{jitter}	−	450	−	Hz/V
Built−in Frequency Jittering, F_{SW} = 100 kHz	−	f_{jitter}	−	620	−	Hz/V
Maximum Duty Cycle	−	Dmax	74	80	87	%
FEEDBACK SECTION (V_{CC} = 11 V, Pin 5 Loaded by 1 kΩ)						
Internal Pullup Resistor	2	Rup	−	8.0	−	kΩ
Pin 3 to Current Setpoint Division Ratio	−	Iratio	−	4.0	−	−
SKIP CYCLE GENERATION						
Default skip mode level	1	Vskip	1.1	1.4	1.6	V
Pin 1 internal output impedance	1	Zout	−	25	−	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Max value @ T_J = −25°C.
2. Max value @ T_J = 25°C, please see characterization curves.

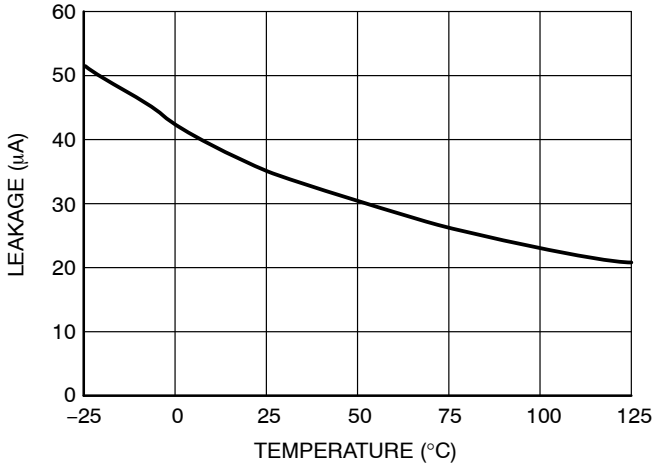


Figure 3. HV Pin Leakage Current vs. Temperature

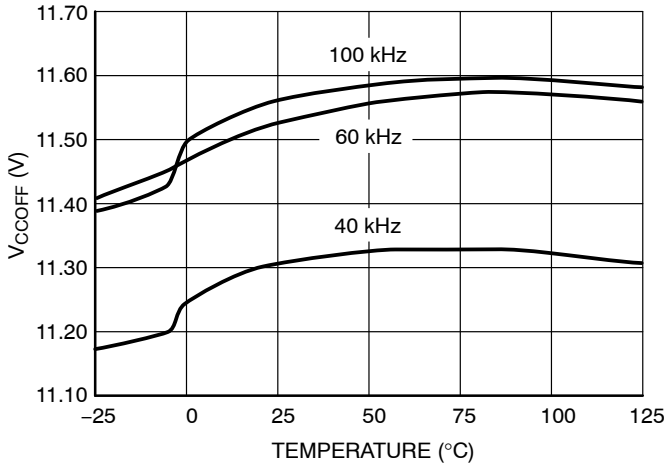


Figure 4. V_{CC} OFF vs. Temperature

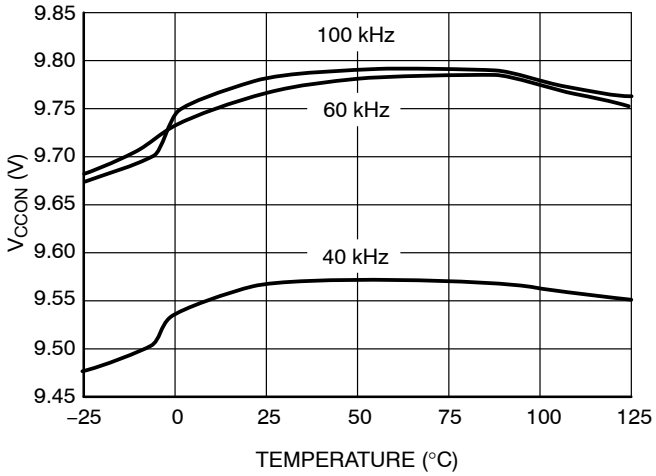


Figure 5. V_{CC} ON vs. Temperature

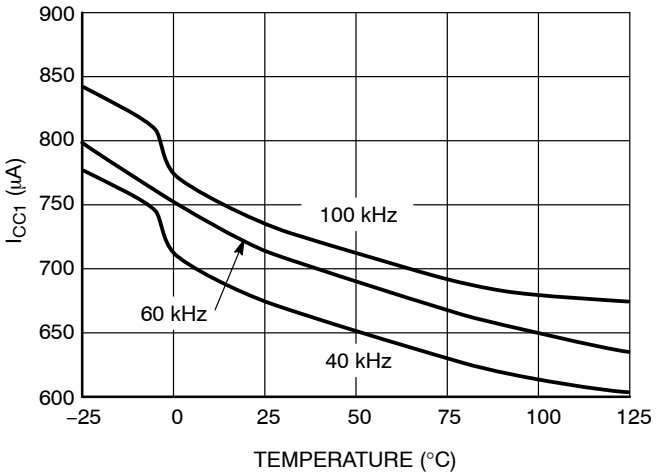


Figure 6. I_{CC1} vs. Temperature

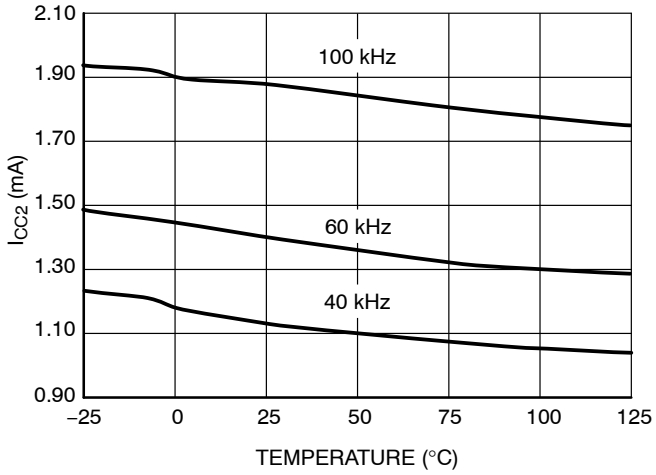


Figure 7. I_{CC2} vs. Temperature

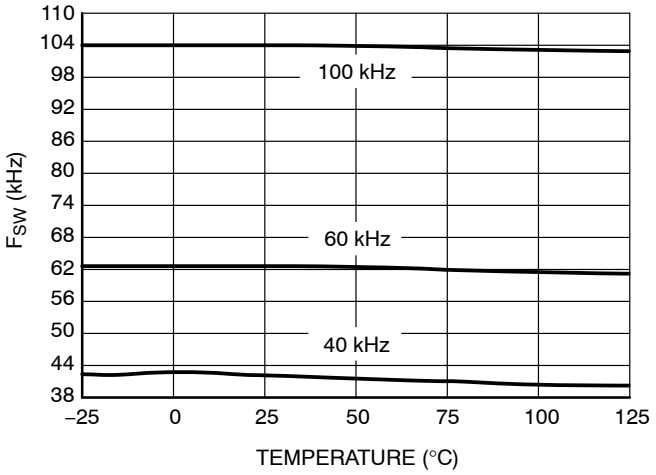


Figure 8. Switching Frequency vs. T_J

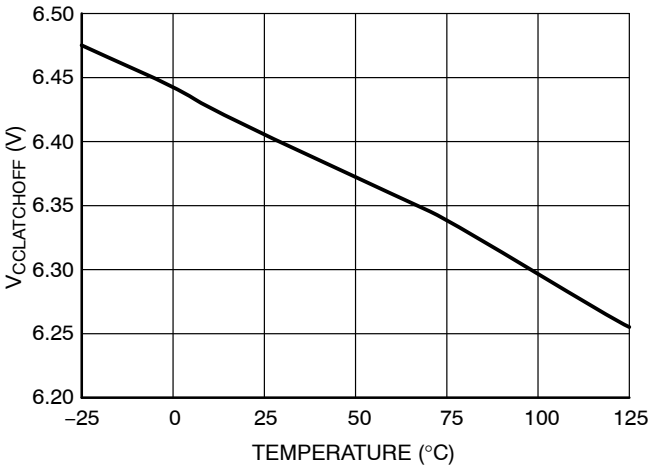


Figure 9. V_{CC} Latchoff vs. Temperature

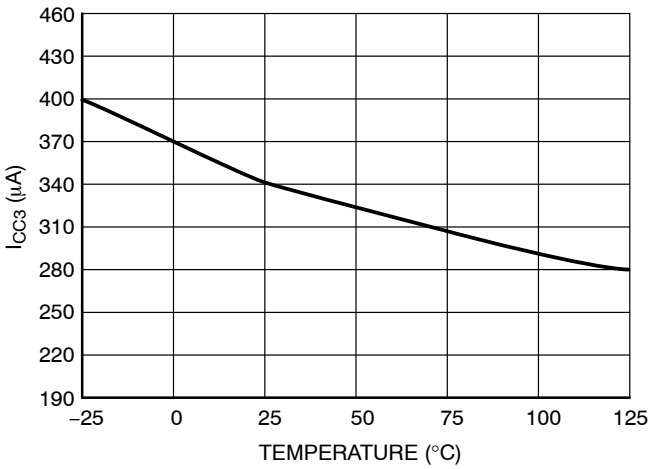


Figure 10. I_{CC3} vs. Temperature

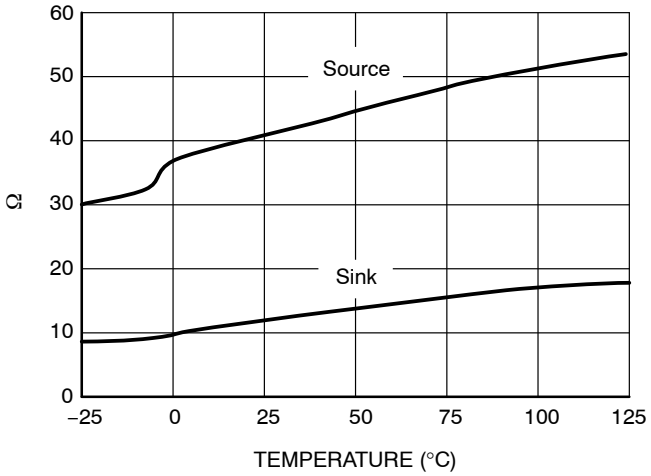


Figure 11. DRV Source/Sink Resistances

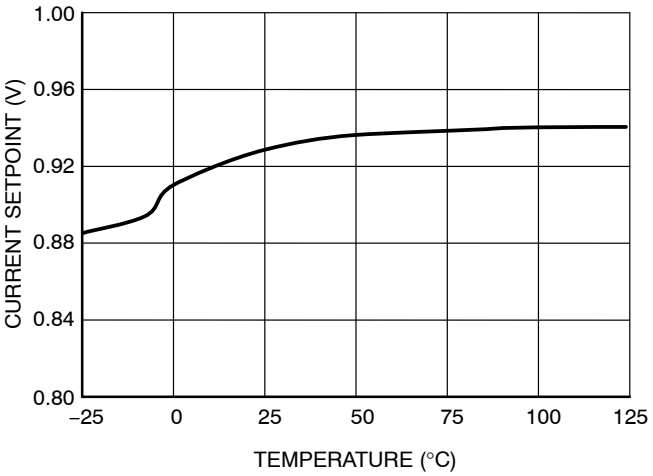


Figure 12. Current Sense Limit vs. Temperature

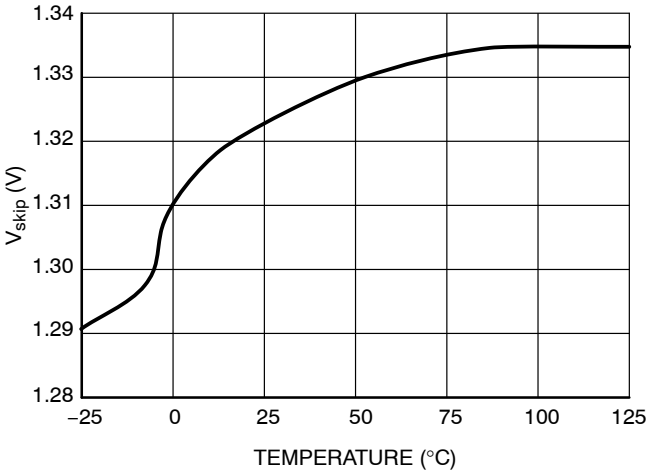


Figure 13. V_{skip} vs. Temperature

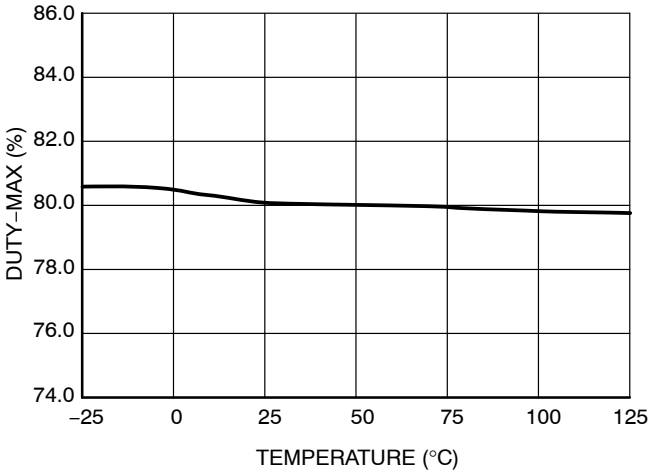


Figure 14. Max Duty Cycle vs. Temperature

APPLICATIONS INFORMATION

INTRODUCTION

The NCP1200 implements a standard current mode architecture where the switch−off time is dictated by the peak current setpoint. This component represents the ideal candidate where low part−count is the key parameter, particularly in low−cost AC−DC adapters, auxiliary supplies etc. Due to its high−performance High−Voltage technology, the NCP1200 incorporates all the necessary components normally needed in UC384X based supplies: timing components, feedback devices, low−pass filter and self−supply. This later point emphasizes the fact that ON Semiconductor's NCP1200 does NOT need an auxiliary winding to operate: the product is naturally supplied from the high−voltage rail and delivers a V_{CC} to the IC. This system is called the Dynamic Self−Supply (DSS).

Dynamic Self−Supply

The DSS principle is based on the charge/discharge of the V_{CC} bulk capacitor from a low level up to a higher level. We can easily describe the current source operation with a bunch of simple logical equations:

POWER−ON: IF $V_{CC} < V_{CCOFF}$ THEN Current Source is ON, no output pulses

IF V_{CC} decreasing > V_{CCON} THEN Current Source is OFF, output is pulsing

IF V_{CC} increasing < V_{CCOFF} THEN Current Source is ON, output is pulsing

Typical values are: V_{CCOFF} = 11.4 V, V_{CCON} = 9.8 V

To better understand the operational principle, Figure 15's sketch offers the necessary light:

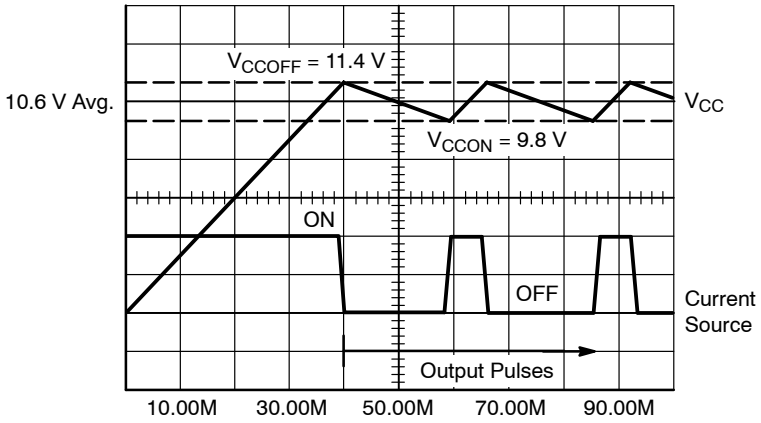


Figure 15. The Charge/Discharge Cycle Over a 10 μF V_{CC} Capacitor

The DSS behavior actually depends on the internal IC consumption and the MOSFET's gate charge, Qg. If we select a MOSFET like the MTD1N60E, Qg equals 11 nC (max). With a maximum switching frequency of 48 kHz (for the P40 version), the average power necessary to drive the MOSFET (excluding the driver efficiency and neglecting various voltage drops) is:

$Fsw \cdot Qg \cdot V_{CC}$ with

Fsw = maximum switching frequency

Qg = MOSFET's gate charge

$V_{CC} = V_{GS}$ level applied to the gate

To obtain the final driver contribution to the IC consumption, simply divide this result by V_{CC}: Idriver = $Fsw \cdot Qg$ = 530 μA. The total standby power consumption at no−load will therefore heavily rely on the internal IC consumption plus the above driving current (altered by the driver's efficiency). Suppose that the IC is supplied from a 400 V DC line. To fully supply the integrated circuit, let's imagine the 4 mA source is ON during 8 ms and OFF during 50 ms. The IC power contribution is therefore: 400 V . 4 mA . 0.16 = 256 mW. If for design reasons this contribution is still too high, several solutions exist to diminish it:

1. Use a MOSFET with lower gate charge Qg
2. Connect pin through a diode (1N4007 typically) to one of the mains input. The average value on pin 8 becomes $\frac{2 * V_{mains\ PEAK}}{\pi}$. Our power contribution example drops to: 160 mW.

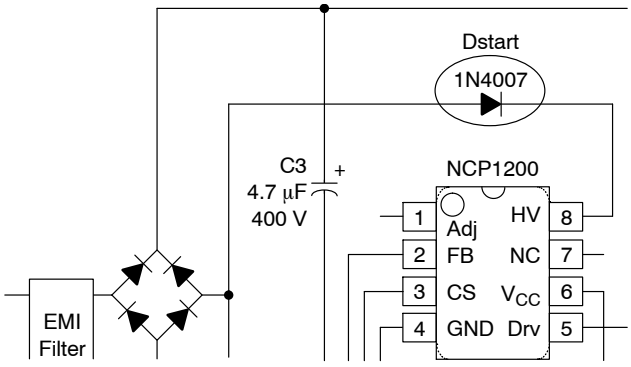


Figure 16. A simple diode naturally reduces the average voltage on pin 8

3. Permanently force the V_{CC} level above V_{CCH} with an auxiliary winding. It will automatically disconnect the internal startup source and the IC will be fully self−supplied from this winding. Again, the total power drawn from the mains will significantly decrease. Make sure the auxiliary voltage never exceeds the 16 V limit.

Skipping Cycle Mode

The NCP1200 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level, the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so−called skip cycle mode, also named controlled burst operation. The power transfer now depends upon the width of the pulse bunches (Figure 18). Suppose we have the following component values:

Lp, primary inductance = 1 mH

F_{SW}, switching frequency = 48 kHz

Ip skip = 300 mA (or 350 mV / Rsense)

The theoretical power transfer is therefore:

$$\frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw = 2.2\ W$$

If this IC enters skip cycle mode with a bunch length of 10 ms over a recurrent period of 100 ms, then the total power transfer is: 2.2 . 0.1 = 220 mW.

To better understand how this skip cycle mode takes place, a look at the operation mode versus the FB level immediately gives the necessary insight:

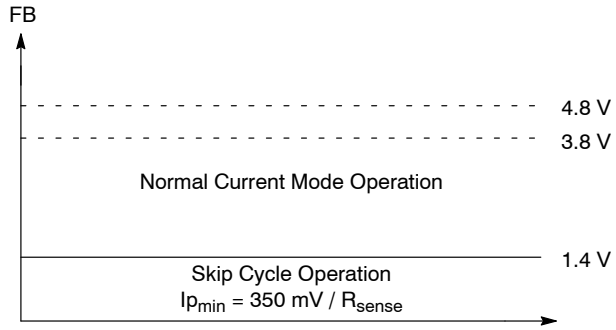


Figure 17. Feedback Voltage Variations

When FB is above the skip cycle threshold (1.4 V by default), the peak current cannot exceed 1 V/Rsense. When the IC enters the skip cycle mode, the peak current cannot go below Vpin1 / 4 (Figure 19). The user still has the flexibility to alter this 1.4 V by either shunting pin 1 to ground through a resistor or raising it through a resistor up to the desired level.

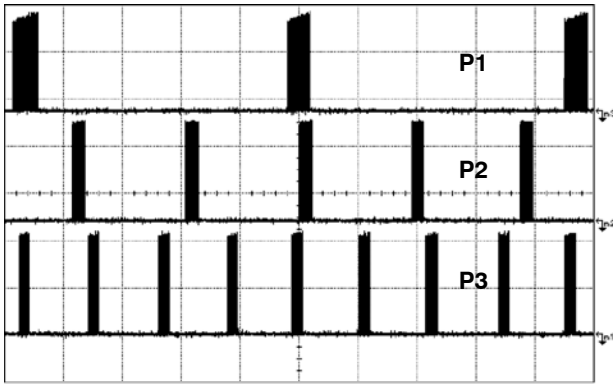


Figure 18. Output pulses at various power levels (X = 5 μs/div) P1<P2<P3

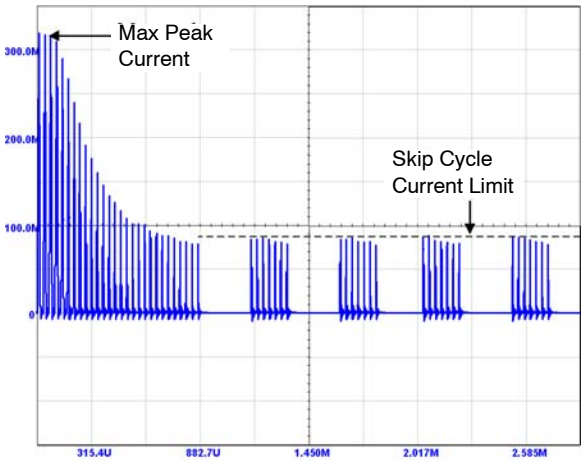


Figure 19. The skip cycle takes place at low peak currents which guarantees noise free operation

Power Dissipation

The NCP1200 is directly supplied from the DC rail through the internal DSS circuitry. The current flowing through the DSS is therefore the direct image of the NCP1200 current consumption. The total power dissipation can be evaluated using: $(V_{HVDC} - 11\ V) \cdot ICC2$. If we operate the device on a 250 VAC rail, the maximum rectified voltage can go up to 350 VDC. As a result, the worse case dissipation occurs on the 100 kHz version which will dissipate 340 . 1.8 mA@Tj = −25° C = 612 mW (however this 1.8 mA number will drop at higher operating temperatures). Please note that in the above example, I_{CC2} is based on a 1 nF capacitor loading pin 5. As seen before, I_{CC2} will depend on your MOSFET's Q_g: $I_{CC2} = I_{CC1} + F_{sw}$ x Q_g. Final calculations shall thus account for the total gate−charge Q_g your MOSFET will exhibit. A DIP8 package offers a junction−to−ambient thermal resistance of $R_{\theta J-A}$ 100° C/W. The maximum power dissipation can thus be computed knowing the maximum operating ambient temperature (e.g. 70° C) together with the maximum allowable junction temperature (125° C): $Pmax = \frac{T_{Jmax} - T_{Amax}}{R_{R\theta J-A}} = 550$ mW. As we can see, we do not reach the worse consumption budget imposed by the 100 kHz version. Two solutions exist to cure this trouble. The first one consists in adding some copper area around the NCP1200 DIP8 footprint. By adding a min−pad area of 80 mm^2 of 35 μ copper (1 oz.) $R_{\theta J-A}$ drops to about 75° C/W which allows the use of the 100 kHz version. The other solutions are:

1. Add a series diode with pin 8 (as suggested in the above lines) to drop the maximum input voltage down to 222 V ((2 × 350)/pi) and thus dissipate less than 400 mW
2. Implement a self−supply through an auxiliary winding to permanently disconnect the self−supply.

SOIC−8 package offers a worse $R_{\theta J-A}$ compared to that of the DIP8 package: 178°C/W. Again, adding some copper area around the PCB footprint will help decrease this number: 12 mm x 12 mm to drop $R_{\theta J-A}$ down to 100° C/W with 35 μ copper thickness (1 oz.) or 6.5 mm x 6.5 mm with 70 μ copper thickness (2 oz.). One can see, we do not recommend using the SOIC package for the 100 kHz version with DSS active as the IC may not be able to sustain the power (except if you have the adequate place on your PCB). However, using the solution of the series diode or the self−supply through the auxiliary winding does not cause any problem with this frequency version. These options are thoroughly described in the AND8023/D.

Overload Operation

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is interesting to implement a true short−circuit protection. A short−circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the optocoupler LED. As a result, the FB pin level is pulled up to 4.1 V, as internally imposed by the IC. The peak current setpoint goes to the maximum and the supply delivers a rather high power with all the associated effects. Please note that this can also happen in case of feedback loss, e.g. a broken optocoupler. To account for this situation, the NCP1200 hosts a dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty cycle. The system recovers when the fault condition disappears.

During the startup phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. This period of time depends on normal output load conditions and the maximum peak current allowed by the system. The time−out used by this IC works with the V_{CC} decoupling capacitor: as soon as the V_{CC} decreases from the V_{CCOFF} level (typically 11.4 V) the device internally watches for an overload current situation. If this condition is still present when V_{CCON} is reached, the controller stops the driving pulses, prevents the self−supply current source to restart and puts all the circuitry in standby, consuming as little as 350 μA typical (I_{CC3} parameter). As a result, the V_{CC} level slowly discharges toward 0. When this level crosses 6.3 V typical, the controller enters a new startup phase by turning the current source on: V_{CC} rises toward 11.4 V and again delivers output pulses at the $UVLO_H$ crossing point. If the fault condition has been removed before $UVLO_L$ approaches, then the IC continues its normal operation. Otherwise, a new fault cycle takes place. Figure 20 shows the evolution of the signals in presence of a fault.

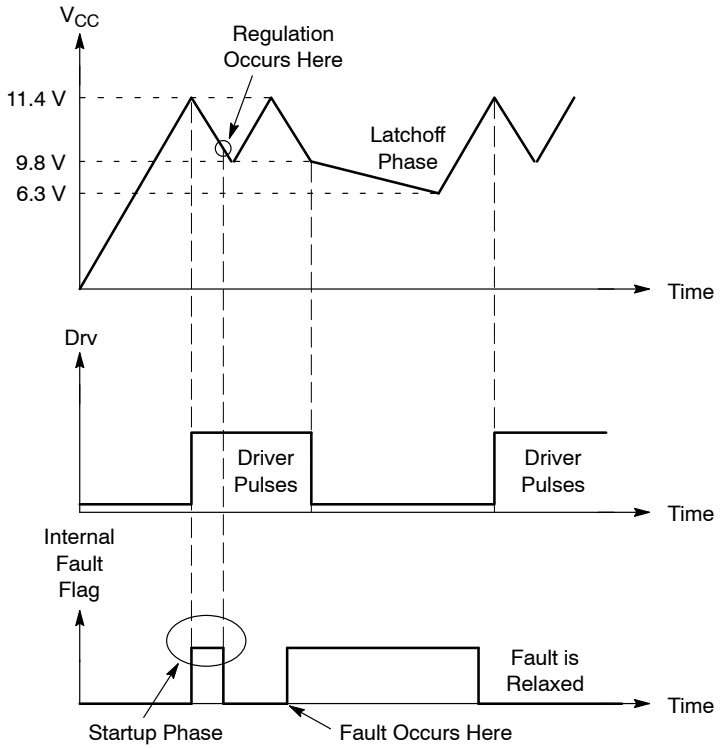


Figure 20. If the fault is relaxed during the V_{CC} natural fall down sequence, the IC automatically resumes. If the fault persists when V_{CC} reached $UVLO_L$, then the controller cuts everything off until recovery.

Calculating the V_{CC} Capacitor

As the above section describes, the fall down sequence depends upon the V_{CC} level: how long does it take for the V_{CC} line to go from 11.4 V to 9.8 V? The required time depends on the startup sequence of your system, i.e. when you first apply the power to the IC. The corresponding transient fault duration due to the output capacitor charging must be less than the time needed to discharge from 11.4 V to 9.8 V, otherwise the supply will not properly start. The test consists in either simulating or measuring in the lab how much time the system takes to reach the regulation at full load. Let's suppose that this time corresponds to 6ms. Therefore a V_{CC} fall time of 10 ms could be well appropriated in order to not trigger the overload detection circuitry. If the corresponding IC consumption, including the MOSFET drive, establishes at 1.5 mA, we can calculate the required capacitor using the following formula: $\Delta t = \frac{\Delta V \cdot C}{i}$, with ΔV = 2V. Then for a wanted Δt of 10 ms, C equals 8 μF or 10 μF for a standard value. When an overload condition occurs, the IC blocks its internal circuitry and its consumption drops to 350 μA typical. This appends at V_{CC} = 9.8 V and it remains stuck until V_{CC} reaches 6.5 V: we are in latchoff phase. Again, using the calculated 10 μF and 350 μA current consumption, this latchoff phase lasts: 109 ms.

Protecting the Controller Against Negative Spikes

As with any controller built upon a CMOS technology, it is the designer's duty to avoid the presence of negative spikes on sensitive pins. Negative signals have the bad habit to forward bias the controller substrate and induce erratic behaviors. Sometimes, the injection can be so strong that internal parasitic SCRs are triggered, engendering irremediable damages to the IC if they are a low impedance path is offered between V_{CC} and GND. If the current sense pin is often the seat of such spurious signals, the high−voltage pin can also be the source of problems in certain circumstances. During the turn−off sequence, e.g. when the user unplugs the power supply, the controller is still fed by its V_{CC} capacitor and keeps activating the MOSFET ON and OFF with a peak current limited by Rsense. Unfortunately, if the quality coefficient Q of the resonating network formed by Lp and Cbulk is low (e.g. the MOSFET Rdson + Rsense are small), conditions are met to make the circuit resonate and thus negatively bias the controller. Since we are talking about ms pulses, the amount of injected charge (Q = I x t) immediately latches the controller which brutally discharges its V_{CC} capacitor. If this V_{CC} capacitor is of sufficient value, its stored energy damages the controller. Figure 21 depicts a typical negative shot occurring on the HV pin where the brutal V_{CC} discharge testifies for latchup.

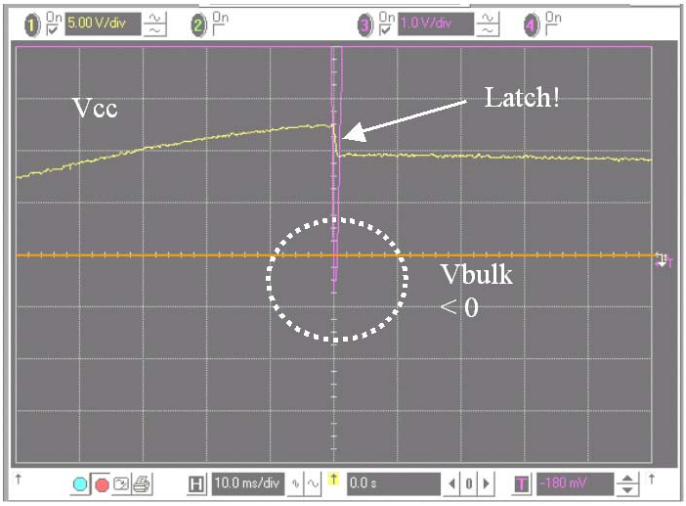


Figure 21. A negative spike takes place on the Bulk capacitor at the switch−off sequence

Simple and inexpensive cures exist to prevent from internal parasitic SCR activation. One of them consists in inserting a resistor in series with the high−voltage pin to keep the negative current to the lowest when the bulk becomes negative (Figure 22). Please note that the negative spike is clamped to –2 x Vf due to the diode bridge. Please refer to AND8069/D for power dissipation calculations.

Another option (Figure 23) consists in wiring a diode from V_{CC} to the bulk capacitor to force V_{CC} to reach UVLOlow sooner and thus stops the switching activity before the bulk capacitor gets deeply discharged. For security reasons, two diodes can be connected in series.

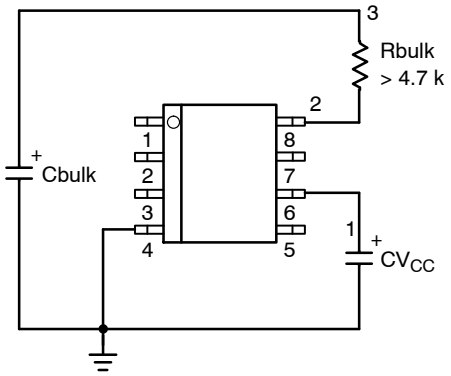


Figure 22. A simple resistor in series avoids any latchup in the controller

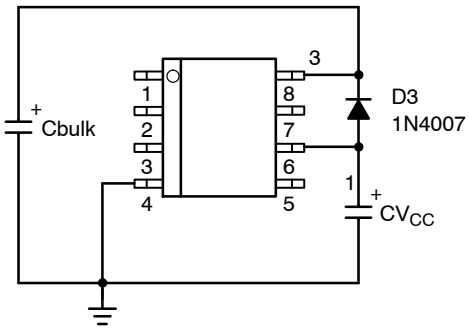


Figure 23. or a diode forces V_{CC} to reach UVLOlow sooner

A Typical Application

Figure 24 depicts a low−cost 3.5 W AC−DC 6.5 V wall adapter. This is a typical application where the wall−pack must deliver a raw DC level to a given internally regulated apparatus: toys, calculators, CD players etc. Due to the inherent short−circuit protection of the NCP1200, you only need a bunch of components around the IC, keeping the final cost at an extremely low level. The transformer is available from different suppliers as detailed on the following page.

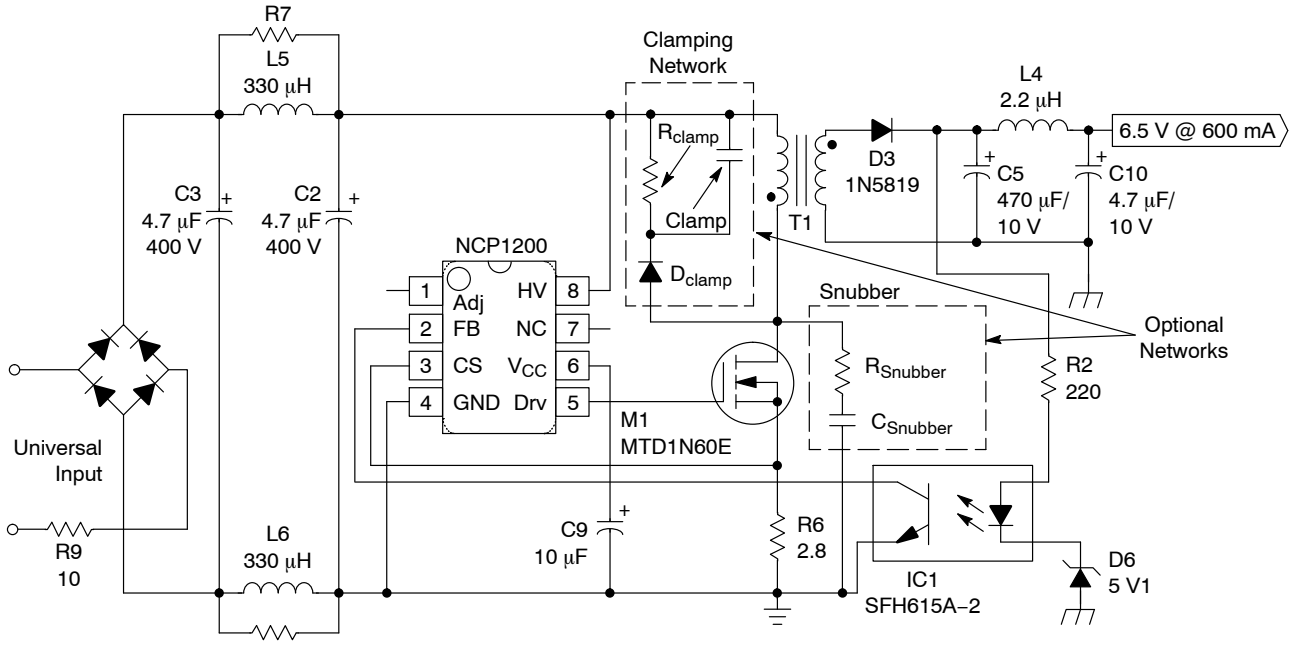


Figure 24. A typical AC−DC wall adapter showing the reduced part count due to the NCP1200

T1: Lp = 2.9 mH, Np:Ns = 1:0.08, leakage = 80 μH, E16 core, NCP1200P40

To help designers during the design stage, several manufacturers propose ready−to−use transformers for the above application, but can also develop devices based on your particular specification:

Eldor Corporation Headquarter
Via Plinio 10,
22030 Orsenigo
(Como) Italia
Tel.: +39−031−636 111
Fax : +39−031−636 280
Email: eldor@eldor.it
www.eldor.it
ref. 1: 2262.0058C: 3.5 W version
(Lp = 2.9 mH, Lleak = 80 μH, E16)
ref. 2: 2262.0059A: 5 W version
(Lp = 1.6 mH, Lleak = 45 μH, E16)

Atelier Special de Bobinage
125 cours Jean Jaures
38130 ECHIROLLES FRANCE
Tel.: 33 (0)4 76 23 02 24
Fax: 33 (0)4 76 22 64 89
Email: asb@wanadoo.fr
ref. 1: NCP1200−10 W−UM: 10 W for USB
(Lp = 1.8 mH, 60 kHz, 1:0.1, RM8 pot core)

Coilcraft
1102 Silver Lake Road
Cary, Illinois 60013 USA
Tel: (847) 639−6400
Fax: (847) 639−1469
Email: info@coilcraft.com
http://www.coilcraft.com
ref. 1: Y8844−A: 3.5 W version
(Lp = 2.9 mH, Lleak = 65 μH, E16)
ref. 2: Y8848−A: 10 W version
(Lp = 1.8 mH, Lleak = 45 μH, 1:01, E core)

Improving the Output Drive Capability

The NCP1200 features an asymmetrical output stage used to soften the EMI signature. Figure 25 depicts the way the driver is internally made:

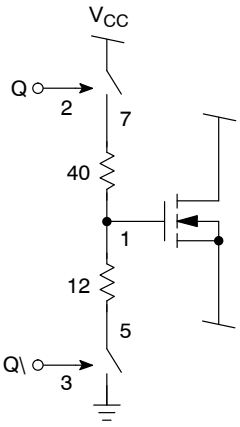


Figure 25. The higher ON resistor slows down the MOSFET while the lower OFF resistor ensures fast turn−off.

In some cases, it is possible to expand the output drive capability by adding either one or two bipolar transistors. Figures 26, 27, and 28 give solutions whether you need to improve the turn−on time only, the turn−off time or both. Rd is there to damp any overshoot resulting from long copper traces. It can be omitted with short connections. Results showed a rise fall time improvement by 5X with standard 2N2222/2N2907:

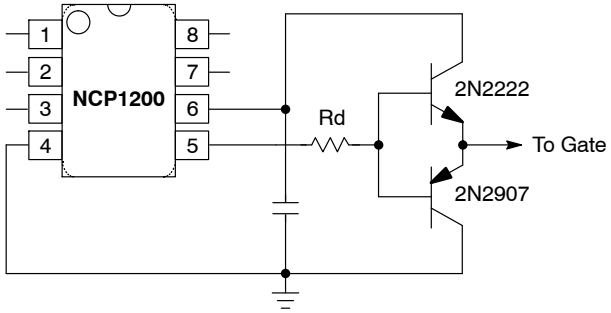


Figure 26. Improving Both Turn−On and Turn−Off Times

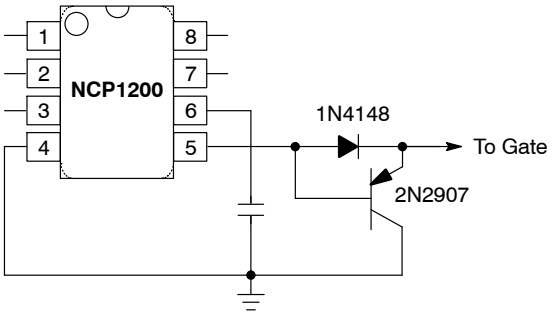


Figure 27. Improving Turn−Off Time Only

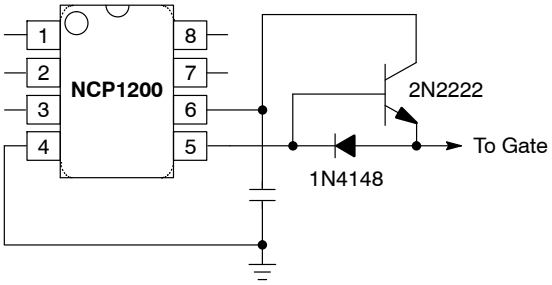


Figure 28. Improving Turn−On Time Only

If the leakage inductance is kept low, the MTD1N60E can withstand *accidental* avalanche energy, e.g. during a high−voltage spike superimposed over the mains, without the help of a clamping network. If this leakage path permanently forces a drain−source voltage above the MOSFET BVdss (600 V), a clamping network is mandatory and must be built around Rclamp and Clamp. Dclamp shall react extremely fast and can be a MUR160 type. To calculate the component values, the following formulas will help you:

$$R_{clamp} = \frac{2 \cdot V_{clamp} \cdot (V_{clamp} - (V_{out} + Vf\,sec) \cdot N)}{L_{leak} \cdot Ip^2 \cdot Fsw}$$

$$C_{clamp} = \frac{V_{clamp}}{V_{ripple} \cdot Fsw \cdot R_{clamp}}$$

with:

V_{clamp}: the desired clamping level, must be selected to be between 40 V to 80 V above the reflected output voltage when the supply is heavily loaded.

V_{out} + Vf: the regulated output voltage level + the secondary diode voltage drop

L_{leak}: the primary leakage inductance

N: the Ns:Np conversion ratio

F_{SW}: the switching frequency

V_{ripple}: the clamping ripple, could be around 20 V

Another option lies in implementing a snubber network which will damp the leakage oscillations but also provide more capacitance at the MOSFET's turn−off. The peak voltage at which the leakage forces the drain is calculated by:

$$V_{max} = Ip \cdot \sqrt{\frac{L_{leak}}{C_{lump}}}$$

where C_{lump} represents the total parasitic capacitance seen at the MOSFET opening. Typical values for Rsnubber and Csnubber in this 4W application could respectively be 1.5 kΩ and 47 pF. Further tweaking is nevertheless necessary to tune the dissipated power versus standby power.

Available Documents

"Implementing the NCP1200 in Low−cost AC−DC Converters", AND8023/D.

"Conducted EMI Filter Design for the NCP1200", AND8032/D.

"Ramp Compensation for the NCP1200", AND8029/D.

TRANSient and AC models available to download at: http://onsemi.com/pub/NCP1200

NCP1200 design spreadsheet available to download at: http://onsemi.com/pub/NCP1200

ORDERING INFORMATION

Device	Type	Marking	Package	Shipping†
NCP1200P40G	F_{SW} = 40 kHz	1200P40	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1200D40R2G		200D4	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1200P60G	F_{SW} = 60 kHz	1200P60	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1200D60R2G		200D6	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1200P100G	F_{SW} = 100 kHz	1200P100	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1200D100R2G		200D1	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

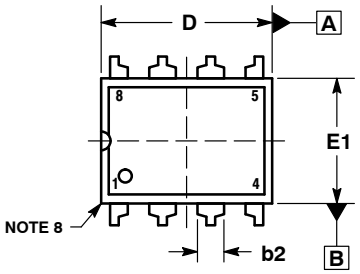
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

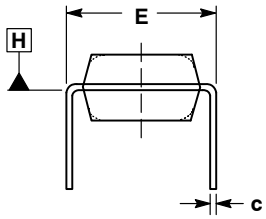
SCALE 1:1

PDIP–8
CASE 626–05
ISSUE P

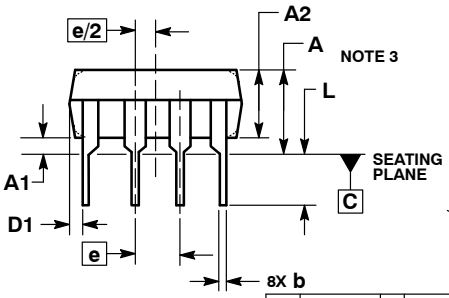
DATE 22 APR 2015



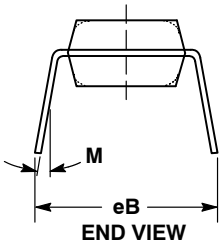
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



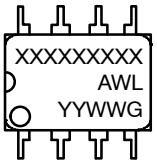
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98ASB42420B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	PDIP–8	PAGE 1 OF 1

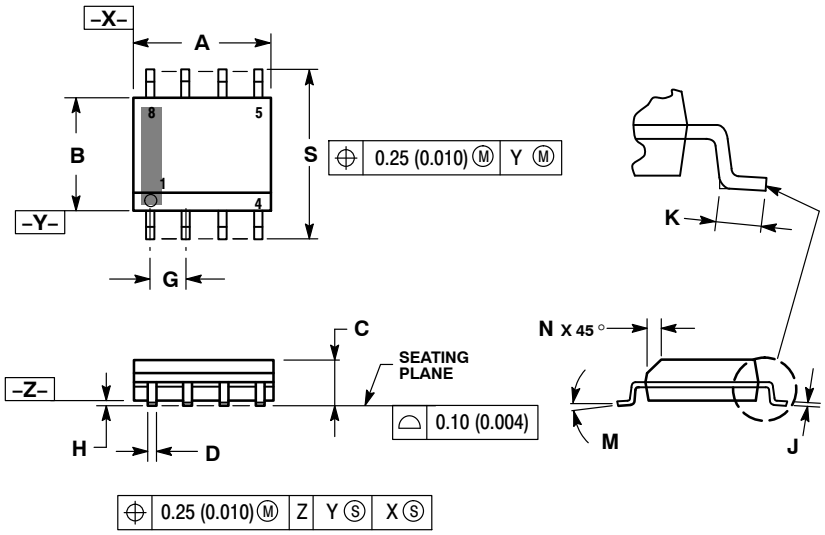
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

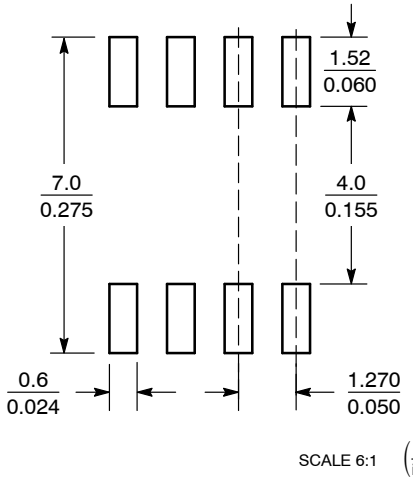
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

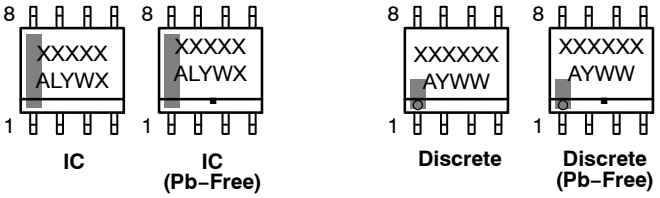
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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