NanoPower, 350nA, RRIO, CMOS Input, Operational Amplifier

Description

The TLV521 350 nA nanopower op amp offers optimum price performance in TI's nanopower family of operational amplifiers. The TLV521 has a carefully designed CMOS input stage enabling very low Ibias of 1 pA, thereby reducing I_{BIAS} and I_{OS} errors that would otherwise impact sensitive applications like Megaohm resistance, high-impedance photodiode and charge sense situations. Additionally, built-in EMI protection reduces sensitivity to unwanted RF signals from sources like mobile phones and RFID readers.

The TLV521 is offered in the 5-pin SC70 package, and operates from –40°C to 125°C.

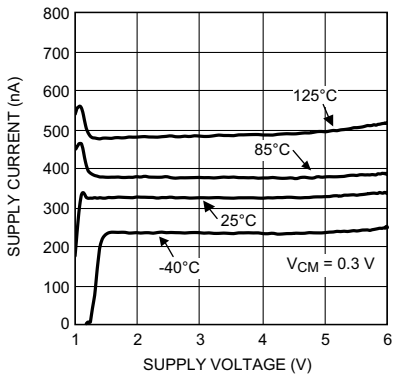
Features

- Unmatched Price Performance
- For V_S = 3.3 V, Typical Unless Otherwise Noted
  - Ultra-low Supply Current
    - 350 nA Typical, 500 nA Maximum
  - Wide Operating Voltage Range 1.7 V to 5.5 V
  - Low TCV_{OS} 1.5 µV/°C
  - V_{OS} 3 mV (Max)
  - Input Bias Current 1 pA
  - PSRR 100 dB
  - CMRR 90 dB
  - Open-Loop Gain 110 dB
  - Gain Bandwidth Product 6 kHz
  - Slew Rate 2.5 V/ms
  - Input Voltage Noise at f = 100 Hz 300 nV/√Hz
  - Temperature Range –40ºC to 125°C
  - Rail to Rail Input and Output (RRIO)

Applications

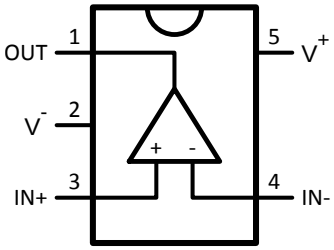
- Wireless Remote Sensors
- Powerline Monitoring
- Power Meters
- Battery Powered Industrial Sensors
- Micropower Oxygen Sensor and Toxic Gas Sensor
- Active RFID Readers
- Zigbee Based Sensors for HVAC Control
- Sensor Network Powered by Energy Scavenging
- Current Sensing
- Glucose Monitoring

Nanopower Supply Current



Pin Configuration and Functions

DCK Package
5-Pin SC70-5 Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT	O	Output
2	V–	P	Negative Power Supply
3	IN+	I	Noninverting Input
4	IN–	I	Inverting Input
5	V+	P	Positive Power Supply

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Any pin relative to V^-		−0.3	6	V
IN+, IN–, OUT Pins		V^- – 0.3 V	V^+ + 0.3 V	V
V^+, V^-, OUT Pins			40	mA
Differential Input Voltage (V_{IN+} - V_{IN-})		–300	300	mV
Junction Temperature		–40	150	°C
Mounting Temperature	Infrared or Convection (30 sec.)		260	°C
	Wave Soldering Lead Temp. (4 sec.)		260	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine Model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions (1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Temperature Range	−40	125	°C
Supply Voltage (V_S = V^+ - V^-)	1.7	5.5	V

(1) Absolute Maximum Ratings indicate limits beyond which damage may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and test conditions, see Electrical Characteristics.

Thermal Information

THERMAL METRIC(1)		TLV521 DCK (SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	269.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

Electrical Characteristics

Unless otherwise specified, all limits for T_A = 25°C, V^+ = 3.3 V, V^- = 0 V, V_{CM} = V_O = V^+/2, and R_L > 1 MΩ.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 0.3 V	–3	0.1	3	mV
		V_{CM} = 3 V	–3	0.1	3	
TCV_{OS}	Input Offset Voltage Drift			±1.5		µV/°C
I_{BIAS}	Input Bias Current			1		pA
I_{OS}	Input Offset Current			50		fA
CMRR	Common Mode Rejection Ratio	0 V ≤ V_{CM} ≤ 3.3 V	70	90		dB
		0 V ≤ V_{CM} ≤ 2.2 V		100		
PSRR	Power Supply Rejection Ratio	V^+ = 1.8 V to 3.3 V; V_{CM} = 0.3 V	80	100		dB
CMVR	Common Mode Voltage Range	CMRR ≥ 70 dB	0		3.3	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 V to 2.8 V R_L = 100 kΩ to V^+/2	80	110		dB
V_O	Output Swing High	R_L = 100 kΩ to V^+/2 V_{IN}(diff) = 100 mV		3	50	mV from either rail
	Output Swing Low	R_L = 100 kΩ to V^+/2 V_{IN} (diff) = −100 mV		2	50	
I_O	Output Current	Sourcing, V_O to V^- V_{IN}(diff) = 100 mV		11		mA
		Sinking, V_O to V^+ V_{IN}(diff) = −100 mV		12		
I_S	Supply Current	V_{CM} = 0.3 V		350	500	nA

AC Electrical Characteristics (1)

Unless otherwise specified, all limits for T_A = 25°C, V^+ = 3.3 V, V^- = 0 V, V_{CM} = V_O = V^+/2, and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
GBW	Gain-Bandwidth Product	C_L = 20 pF, R_L = 100 kΩ			6		kHz
SR	Slew Rate	A_V = +1, V_{IN} = 0 V to 3.3 V	Falling Edge		2.9		V/ms
			Rising Edge		2.5		
θ_m	Phase Margin	C_L = 20 pF, R_L = 100 kΩ			73		deg
G_m	Gain Margin	C_L = 20 pF, R_L = 100 kΩ			19		dB
e_n	Input-Referred Voltage Noise Density	f = 100 Hz			300		nV/√Hz
	Input-Referred Voltage Noise	0.1 Hz to 10 Hz			22		μV_{PP}
I_n	Input-Referred Current Noise	f = 100 Hz			100		fA/√Hz
EMIRR	EMI Rejection Ratio, IN+ and IN− (4)	V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 400 MHz			121		dB
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 900 MHz			121		
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 1800 MHz			124		
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 2400 MHz			142		

(1) Electrical Characteristics values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. Parametric performance, as indicated in the electrical tables, is not ensured under conditions of self heating where TJ > TA. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are ensured by testing, statistical analysis or design.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) The EMI Rejection Ratio is defined as EMIRR = 20log (VRF_PEAK/ΔVOS).

Typical Characteristics

At T_J = 25°C, unless otherwise specified.

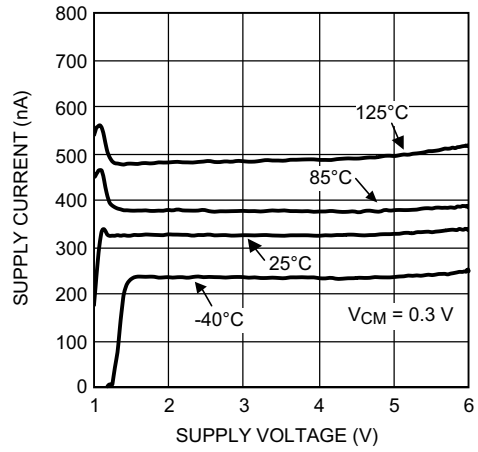


Figure 1. Supply Current vs. Supply Voltage

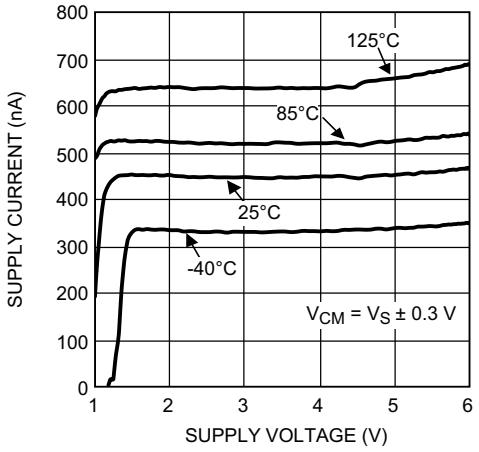


Figure 2. Supply Current vs. Supply Voltage

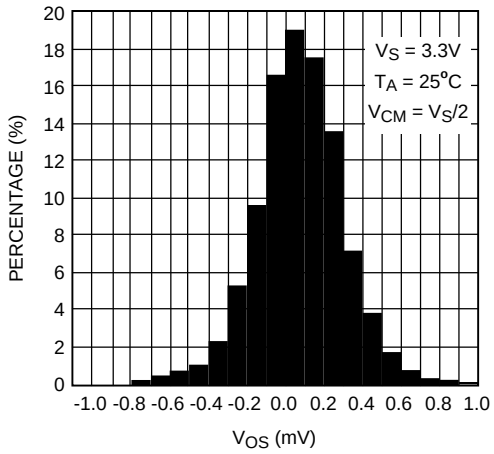


Figure 3. Offset Voltage Distribution

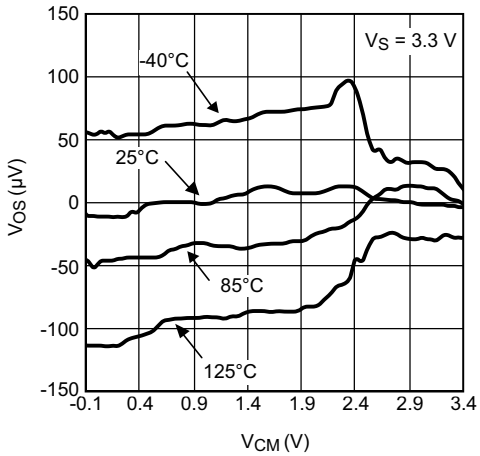


Figure 4. Input Offset Voltage vs. Input Common Mode

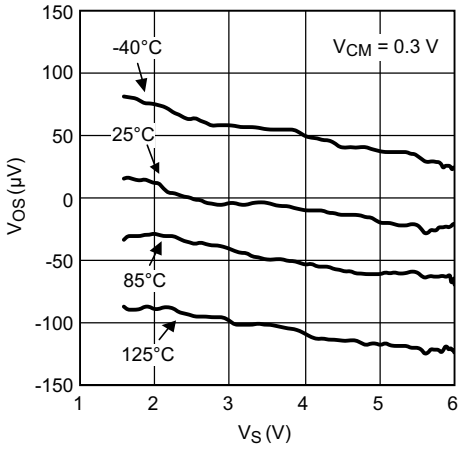


Figure 5. Input Offset Voltage vs. Supply Voltage

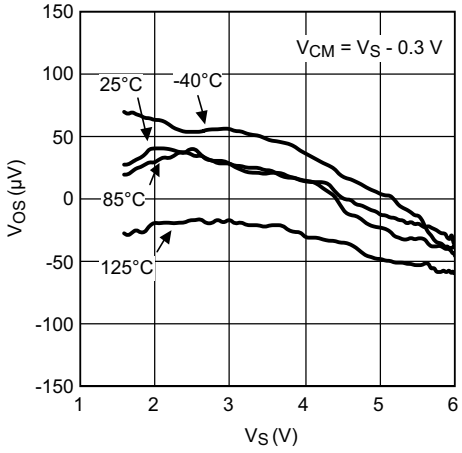


Figure 6. Input Offset Voltage vs. Supply Voltage

Typical Characteristics

At T_J = 25°C, unless otherwise specified.

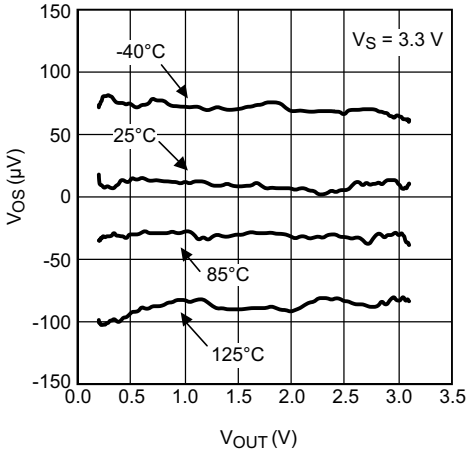


Figure 7. Input Offset Voltage vs. Output Voltage

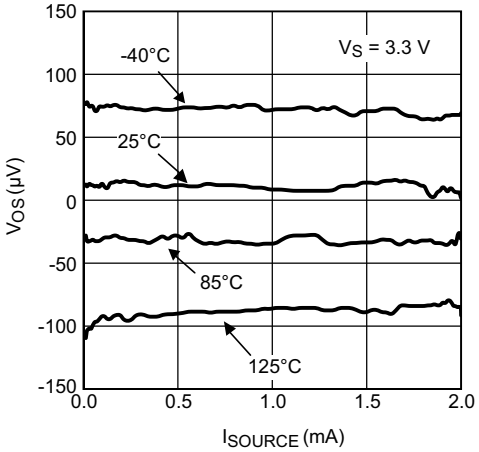


Figure 8. Input Offset Voltage vs. Sourcing Current

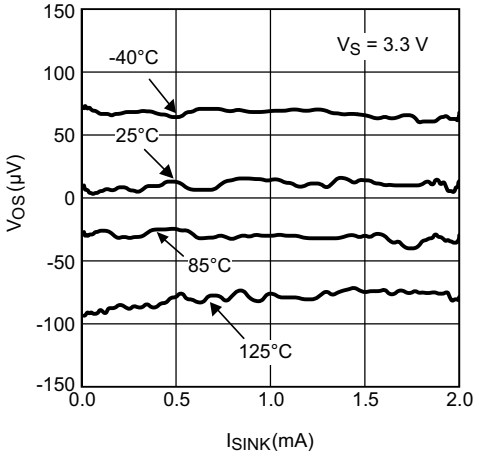


Figure 9. Input Offset Voltage vs. Sinking Current

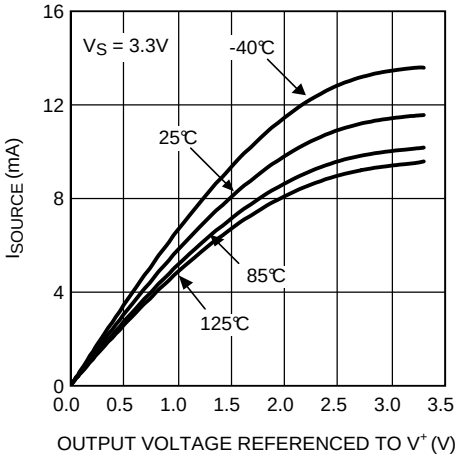


Figure 10. Sourcing Current vs. Output Voltage

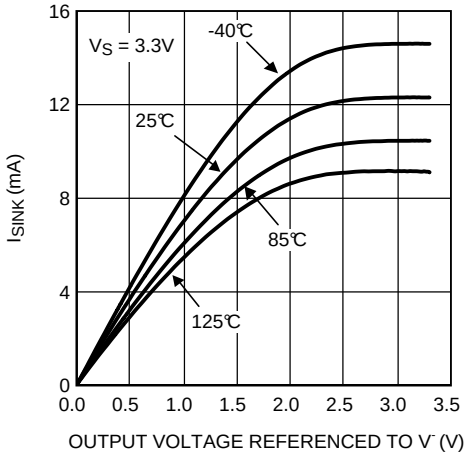


Figure 11. Sinking Current vs. Output Voltage

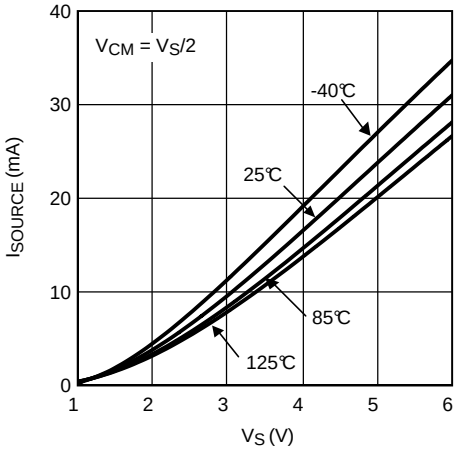


Figure 12. Sourcing Current vs. Supply Voltage

Typical Characteristics

At T_J = 25°C, unless otherwise specified.

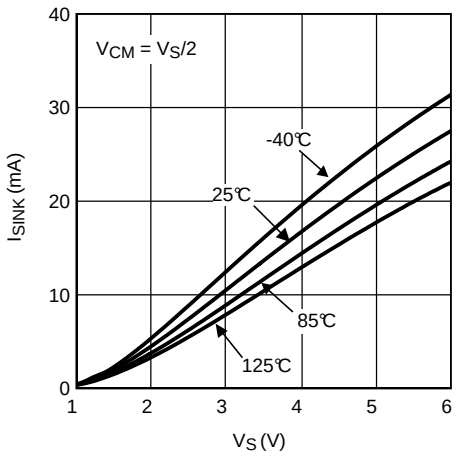


Figure 13. Sinking Current vs. Supply Voltage

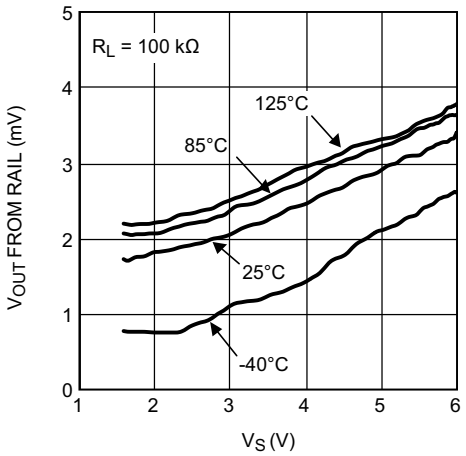


Figure 14. Output Swing High vs. Supply Voltage

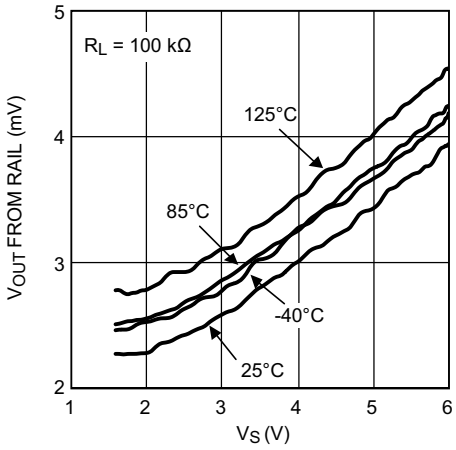


Figure 15. Output Swing Low vs. Supply Voltage

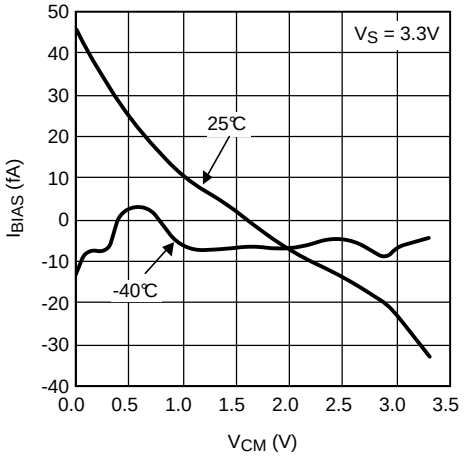


Figure 16. Input Bias Current vs. Common Mode Voltage

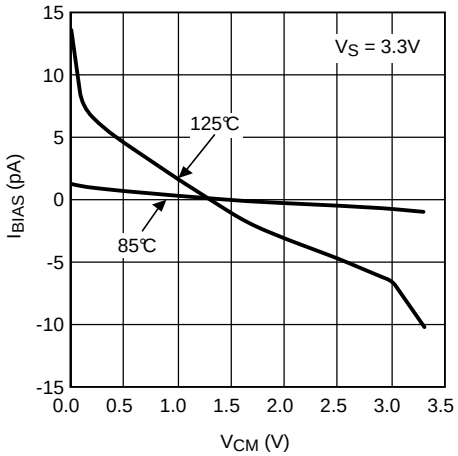


Figure 17. Input Bias Current vs. Common Mode Voltage

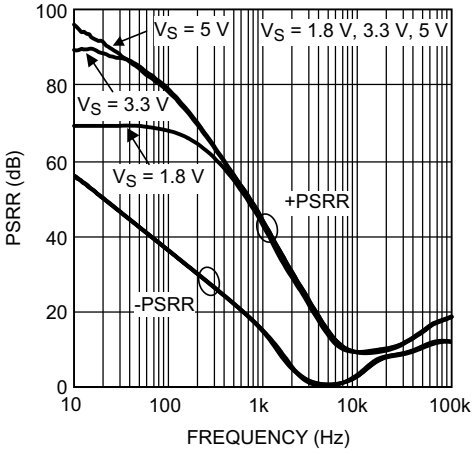


Figure 18. PSRR vs. Frequency

Typical Characteristics

At T_J = 25°C, unless otherwise specified.

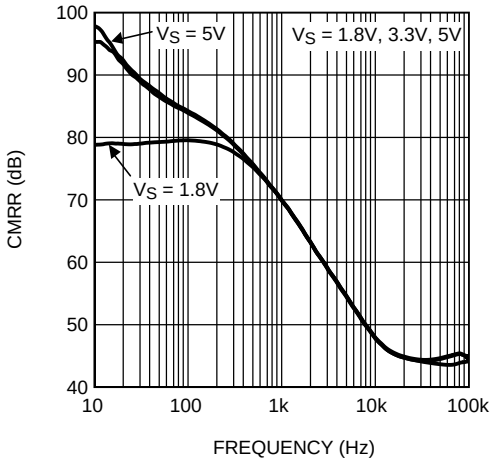


Figure 19. CMRR vs. Frequency

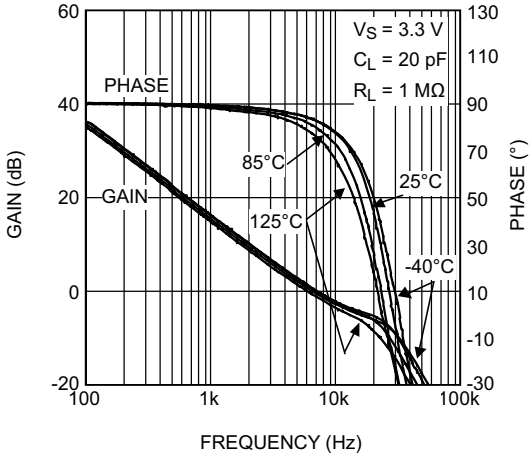


Figure 20. Frequency Response vs. Temperature

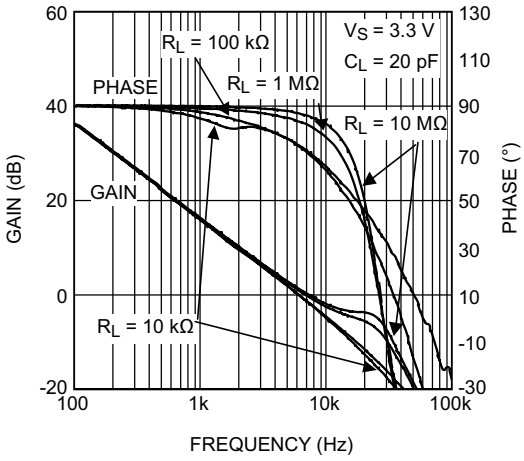


Figure 21. Frequency Response vs. R_L

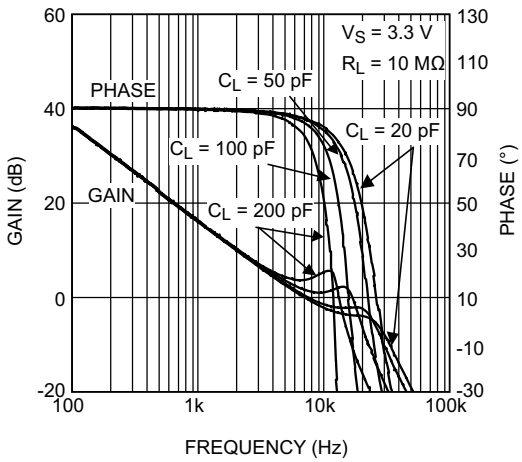


Figure 22. Frequency Response vs. C_L

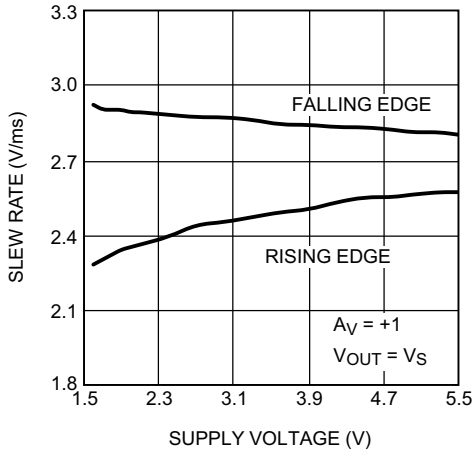


Figure 23. Slew Rate vs. Supply Voltage

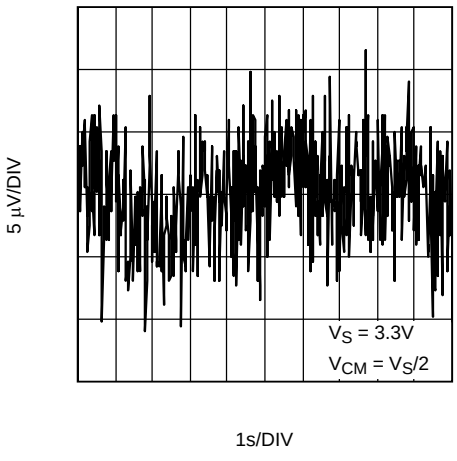


Figure 24. 0.1 to 10 Hz Time Domain Voltage Noise

Typical Characteristics

At T_J = 25°C, unless otherwise specified.

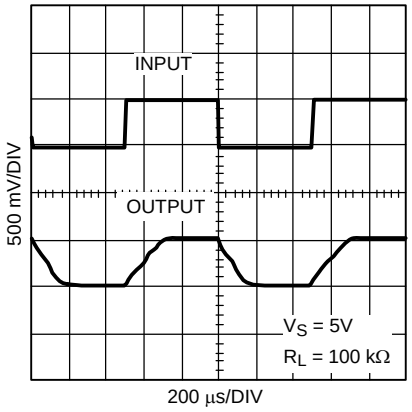


Figure 25. Large Signal Pulse Response

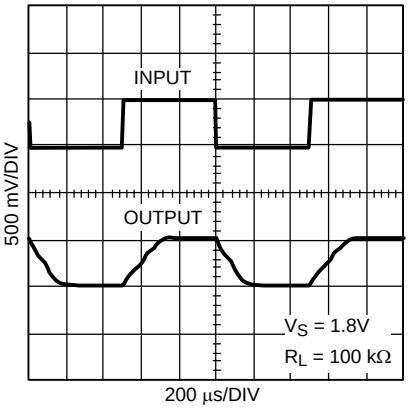


Figure 26. Large Signal Pulse Response

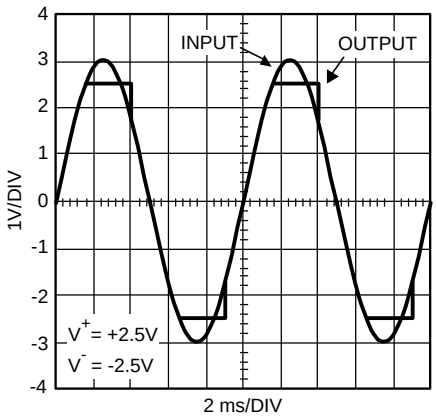


Figure 27. Overload Recovery Waveform

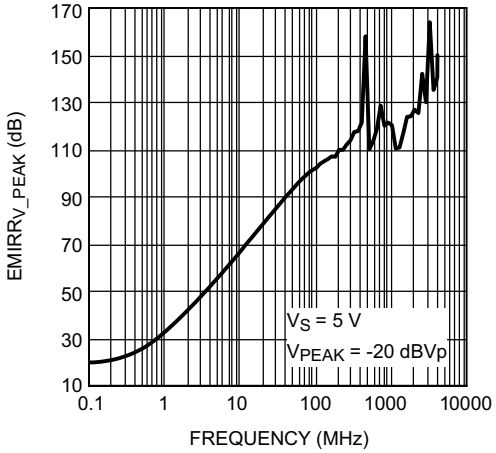
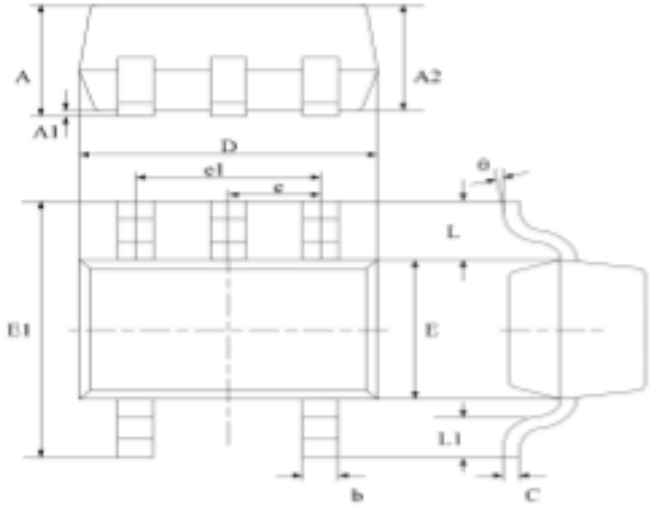


Figure 28. EMIRR vs. Frequency

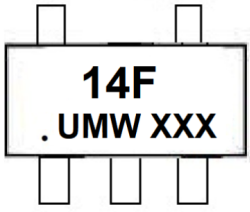
Package Dimension

SC70-5（SOT353）



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	0.900	0.035	0.039
b	0.150	0.350	0.006	0.014
C	0.080	0.150	0.003	0.006
D	1.8500	2.150	0.079	0.087
E	1.100	1.400	0.045	0.053
E1	1.950	2.200	0.085	0.096
e	0.850 typ.		0.026 typ.	
e1	1.200	1.400	0.047	0.055
L	0.42 ref.		0.021 ref.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW TLV521DCKR	SC70-5	3000	Tape and reel