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# FDMC86160ET100

## N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET 100 V, 43 A, 14 mΩ

### Features

- Extended  $T_J$  rating to 175°C
- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)} = 14\text{ m}\Omega$  at  $V_{GS} = 10\text{ V}$ ,  $I_D = 9\text{ A}$
- Max  $r_{DS(on)} = 23\text{ m}\Omega$  at  $V_{GS} = 6\text{ V}$ ,  $I_D = 7\text{ A}$
- High performance technology for extremely low  $r_{DS(on)}$
- Termination is Lead-free and RoHS Compliant

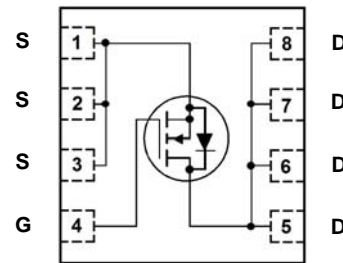
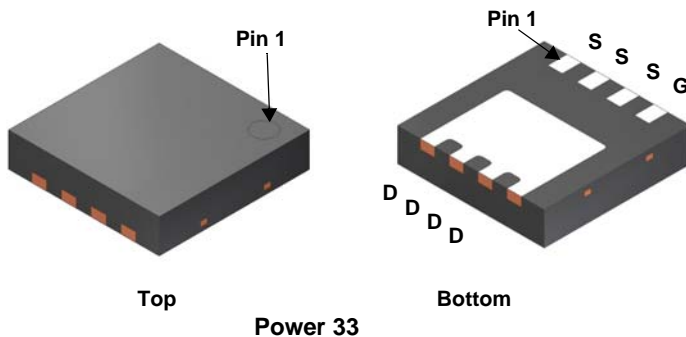


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance. This device is well suited for applications where ultra low  $R_{DS(on)}$  is required in small spaces such as High performance VRM, POL and orring functions.

### Applications

- Bridge Topologies
- Synchronous Rectifier



### MOSFET Maximum Ratings $T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous	$T_C = 25\text{ }^\circ\text{C}$ (Note 5)	43
	-Continuous	$T_C = 100\text{ }^\circ\text{C}$ (Note 5)	31
	-Continuous	$T_A = 25\text{ }^\circ\text{C}$ (Note 1a)	9
	-Pulsed	(Note 4)	204
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	181
$P_D$	Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	65
	Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$ (Note 1a)	2.8
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	2.3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86160ET	FDMC86160ET100	Power33	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		73		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2	2.9	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-9		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 9\ \text{A}$		11.2	14	m $\Omega$
		$V_{GS} = 6\ \text{V}, I_D = 7\ \text{A}$		16	23	
		$V_{GS} = 10\ \text{V}, I_D = 9\ \text{A}, T_J = 125\text{ }^\circ\text{C}$		21	26	
$g_{FS}$	Forward Transconductance	$V_{DD} = 10\ \text{V}, I_D = 9\ \text{A}$		43		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1\ \text{MHz}$		968	1290	pF
$C_{oss}$	Output Capacitance			241	320	pF
$C_{rss}$	Reverse Transfer Capacitance			11	20	pF
$R_g$	Gate Resistance		0.1	0.6	2.5	$\Omega$

### Switching Characteristics

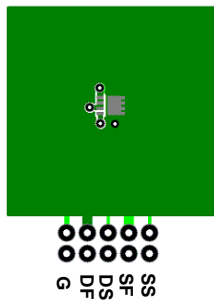
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}, I_D = 9\ \text{A},$ $V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$		9.7	19	ns
$t_r$	Rise Time			3.6	10	ns
$t_{d(off)}$	Turn-Off Delay Time			16	30	ns
$t_f$	Fall Time			3.4	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V to } 10\ \text{V}$	$V_{DD} = 50\ \text{V},$ $I_D = 9\ \text{A}$	15	22	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V to } 6\ \text{V}$		9.8	15	nC
$Q_{gs}$	Total Gate Charge			4.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			3.5		nC

### Drain-Source Diode Characteristics

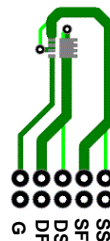
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 9\ \text{A}$ (Note 2)		0.79	1.3	V
		$V_{GS} = 0\ \text{V}, I_S = 1.9\ \text{A}$ (Note 2)		0.72	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 9\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		47	75	ns
$Q_{rr}$	Reverse Recovery Charge			45	73	nC

Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\ \text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\ \text{in.}$  board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



53  $^\circ\text{C/W}$  when mounted on a  
a.  $1\ \text{in}^2$  pad of 2 oz copper



125  $^\circ\text{C/W}$  when mounted on  
b. a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3.  $E_{AS}$  of 181 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\ \text{mH}$ ,  $I_{AS} = 11\ \text{A}$ ,  $V_{DD} = 100\ \text{V}$ ,  $V_{GS} = 10\ \text{V}$ . 100% test at  $L = 0.1\ \text{mH}$ ,  $I_{AS} = 35\ \text{A}$ .

4. Pulsed  $I_D$  please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

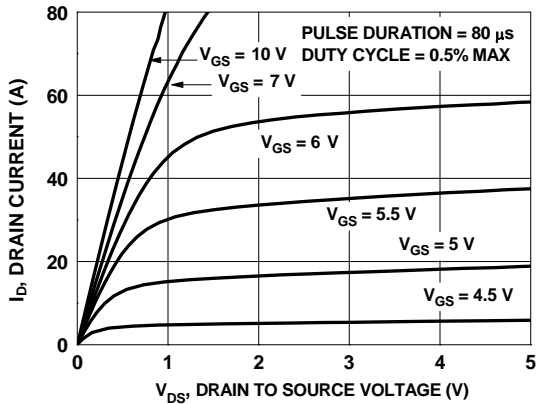


Figure 1. On-Region Characteristics

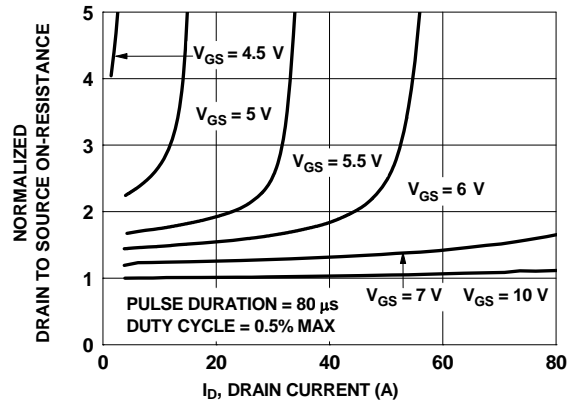


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

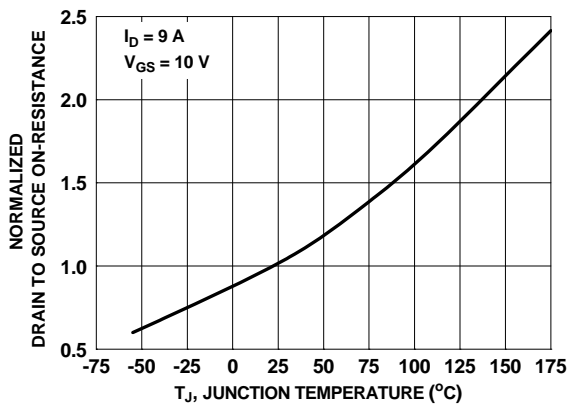


Figure 3. Normalized On-Resistance vs Junction Temperature

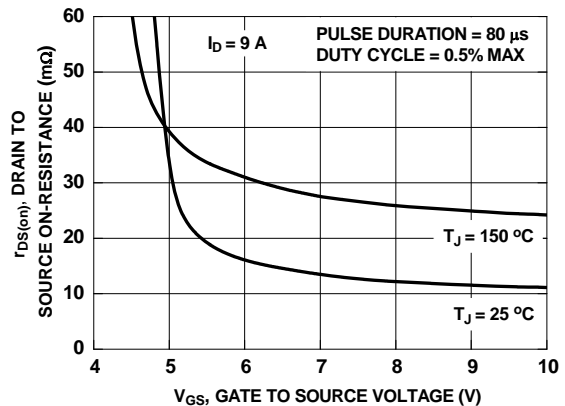


Figure 4. On-Resistance vs Gate to Source Voltage

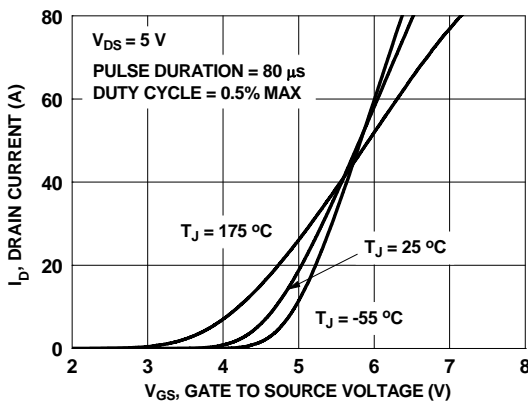


Figure 5. Transfer Characteristics

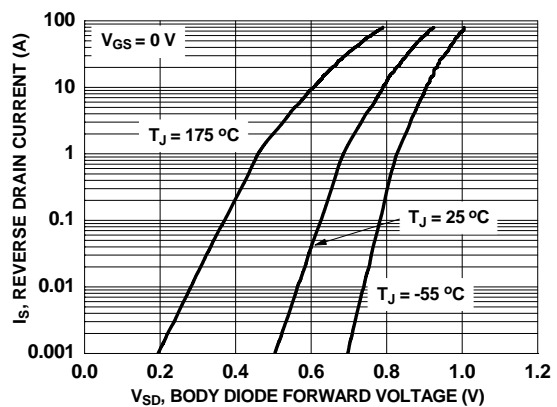
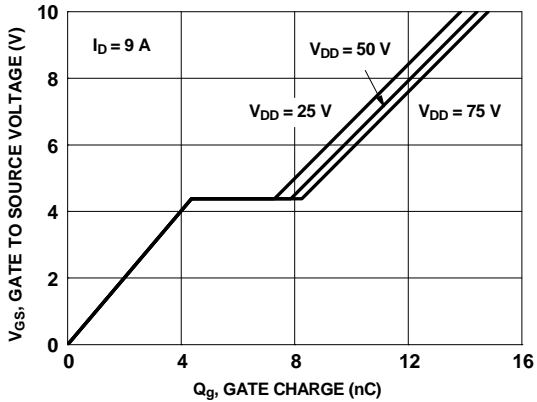
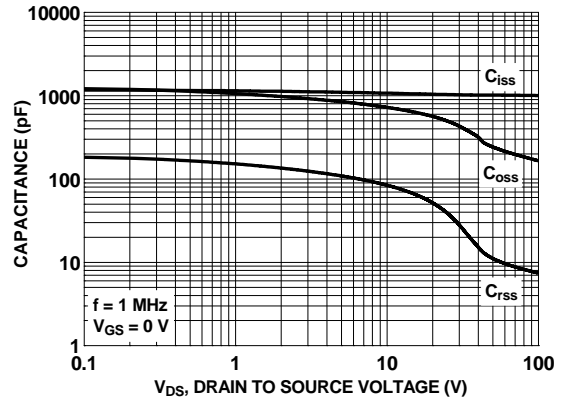


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

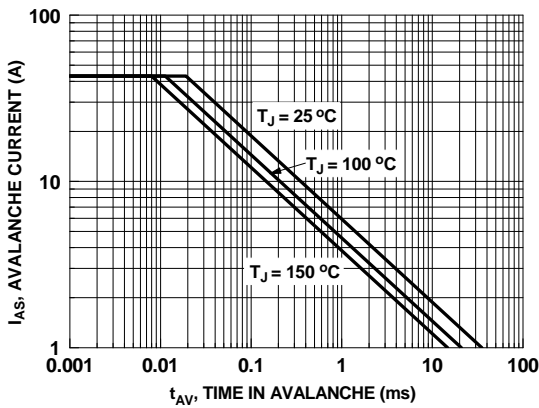
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



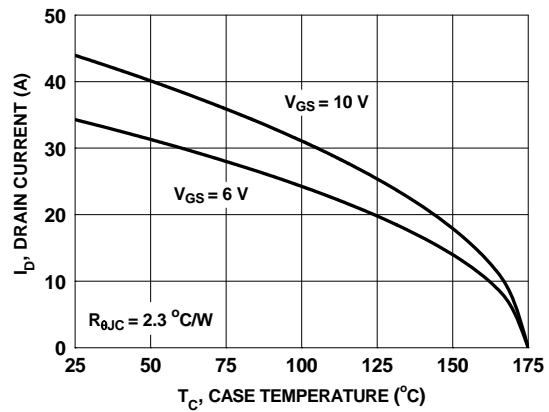
**Figure 7. Gate Charge Characteristics**



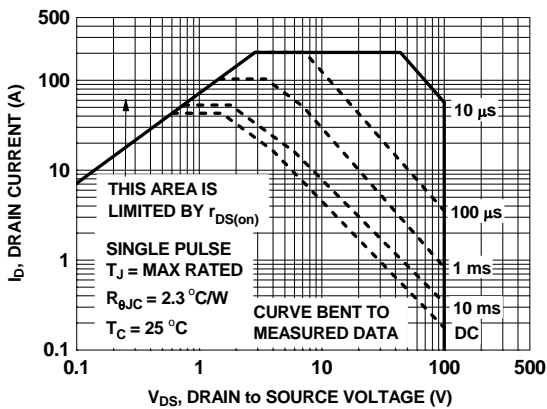
**Figure 8. Capacitance vs Drain to Source Voltage**



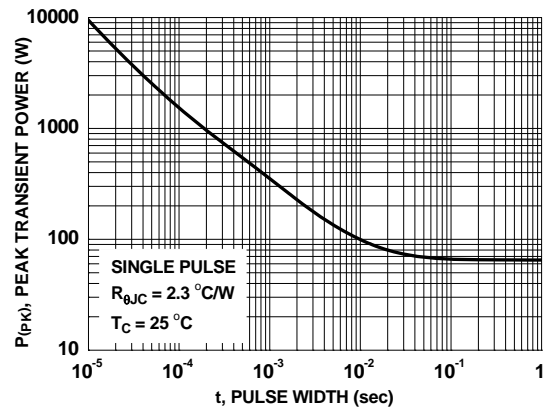
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

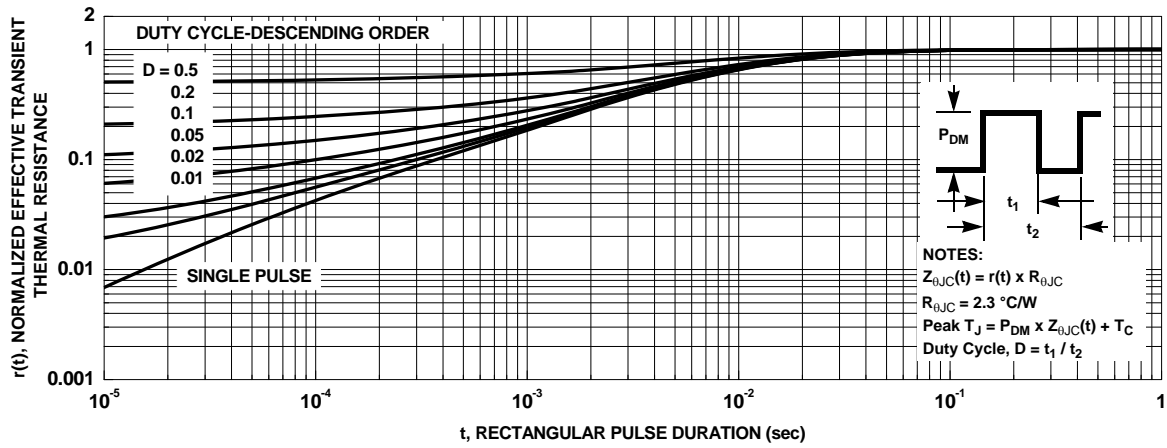


**Figure 11. Forward Bias Safe Operating Area**

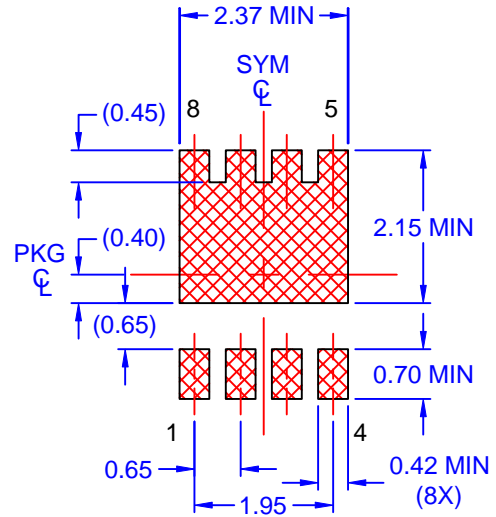
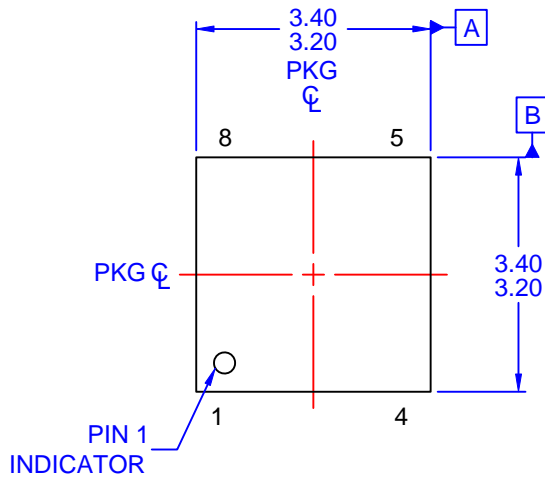


**Figure 12. Single Pulse Maximum Power Dissipation**

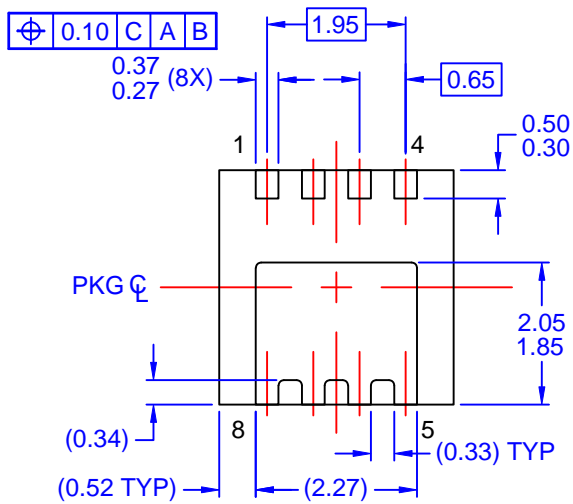
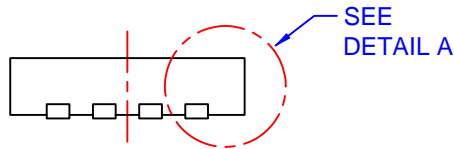
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Case Transient Thermal Response Curve**

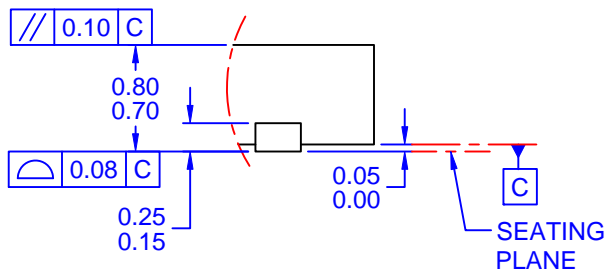


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- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
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