NEWHAVEN DISPLAY
INTERNATIONAL

Product Specification

NHD-2.7-12864WDW3

Graphic OLED Display Module

NHD-	Newhaven Display
2.7-	2.7" Diagonal Size
12864-	128x64 Pixel Resolution
WD-	Model
W-	Emitting Color: White
3-	+3.3V Power Supply

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REACH Compliant

RoHS Compliant

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Table of Contents

Additional Resources

- **Support Forum:** http://www.nhdforum.newhavendisplay.com
- **Github:** https://github.com/newhavendisplay
- **Example Code:** https://www.newhavendisplay.com/example_code.html
- **Knowledge Center:** https://www.newhavendisplay.com/knowledge_center.html
- **Quality Center:** https://www.newhavendisplay.com/quality_center.html
- **Precautions for using LCDs/LCMs:** https://www.newhavendisplay.com/specs/precautions.pdf
- **Warranty / Terms & Conditions:** https://www.newhavendisplay.com/terms.html

Document Revision History

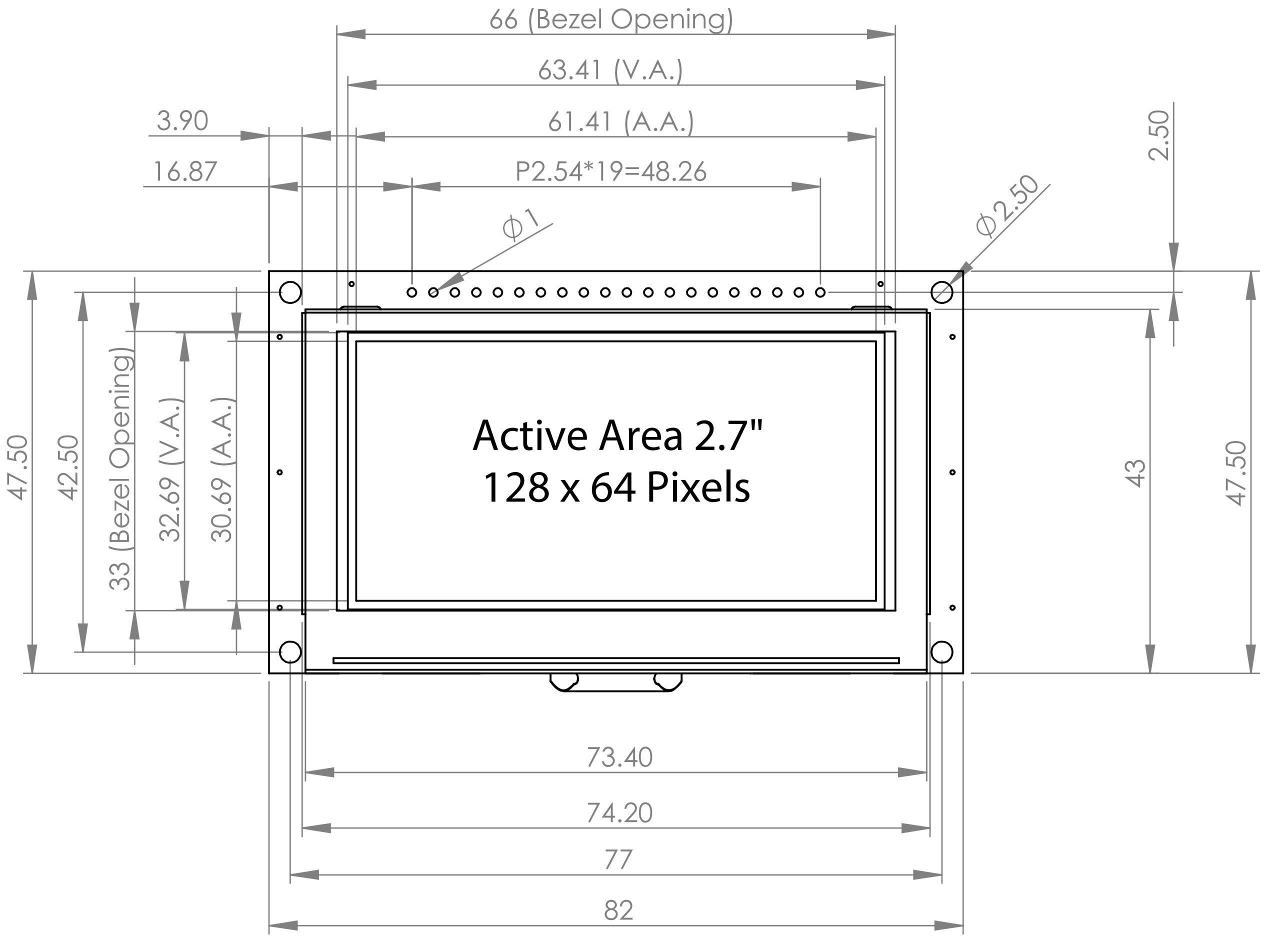
Revision	Date	Description	Changed By
-	6/9/2017	Initial Release	ML
1	7/25/2017	Update Storage Temperature range	ML
2	5/12/2020	Included Additional Dimensions on Mechanical Drawing	AS
3	2/4/2021	Bezel Redesign; Updated 2D Mechanical Drawing	AS
4	2/26/2021	Rectified error in MPU Pin Assignment Summary	AS

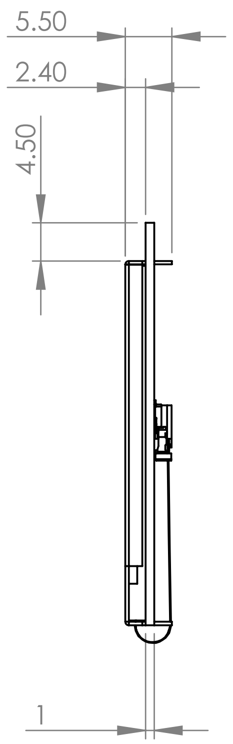
Functions and Features

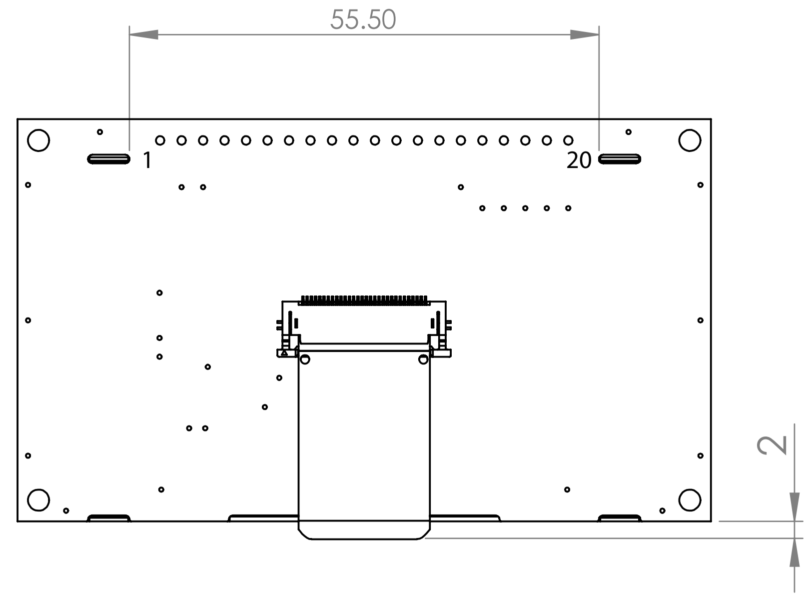
- **128 x 64 Pixel resolution**
- **Built-in SSD1322 controller**
- **Parallel or Serial MPU interface**
- **Single, low voltage power supply**
- **Power options via on-board jumpers**
- **RoHS Compliant**

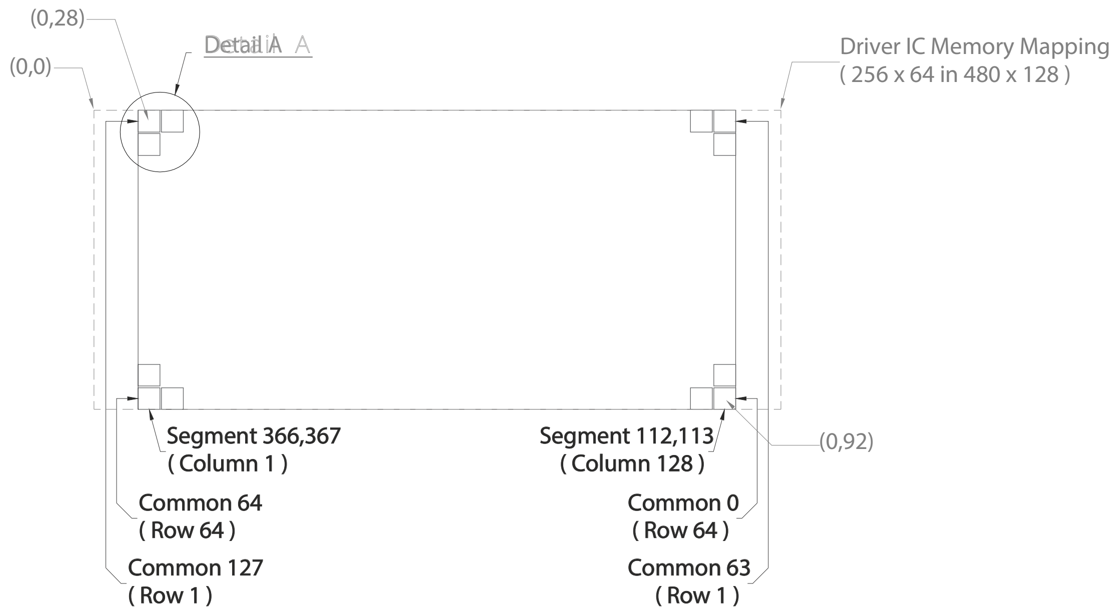
Mechanical Drawing

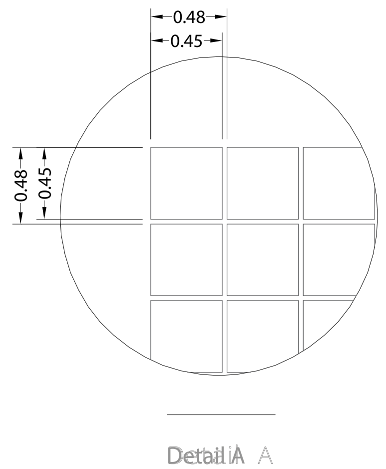
SYMBOL	REVISION	DATE











Pin No.	Symbol
1	Vss
2	Vdd
3	NC (BC_VDD)
4	D/C
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	N.C. (Vcc)
16	/RES
17	/CS
18	/SHDN (N.C.)
19	BS1
20	BS0

Notes:

1. Display Color: White
2. Interface: 8-bit 6800/8080 Parallel, 3/4-Wire SPI
3. Controller: SSD1322

Standard Tolerance:
(Unless otherwise specified)
Linear: ±0.3mm

Unless otherwise specified:
- Dimensions are in Millimeters
- Third Angle Projection

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Drawing/Part Number: NHD-2.7-12864WDW3			Revision: -
Drawn By: A. Shah	Approved By: A. Shah		Size: A3
Drawn Date: 2/4/2021	Approved Date: 2/4/2021		Scale: NS
Do Not Scale Drawing		Sheet 1 of 1	

Pin Description

Parallel Interface:

Pin No.	Symbol	External Connection	Function Description
1	V_{SS}	Power Supply	Ground
2	V_{DD}	Power Supply	Supply Voltage for OLED module
3	N.C. (BC_V_{DD})	-	No Connect by default. Can be configured to provide independent supply voltage (2.8V – 12V DC) for boost converter. (refer to On-Board Jumper Options table below)
4	D/C	MPU	Data/Command select signal, D/C=0: Command; D/C=1: Data (tie LOW for 3-wire Serial Interface)
5	R/W or /WR	MPU	**6800-interface:** Read/Write select signal, R/W=1: Read, R/W=0: Write **8080-interface:** Active LOW Write signal
6	E or /RD	MPU	**6800-interface:** Operation Enable signal Active High **8080-interface:** Active LOW Read signal
7-14	DB0 – DB7	MPU	8-bit bi-directional Data Bus
15	N.C. (VCC)	-	No Connect by default. Can be configured for external VCC (+15V). (refer to On-Board Jumper Options section below)
16	/RES	MPU	Active LOW Reset signal
17	/CS	MPU	Active LOW Chip Select signal
18	/SHDN (N.C.)	MPU	Active LOW Shutdown control pin for boost converter (pulled HIGH via on-board 15kΩ resistor) Can be made a No Connect by removing resistor R1.
19	BS1	MPU	MPU Interface select signal
20	BS0	MPU	MPU Interface select signal

Serial Interface:

Pin No.	Symbol	External Connection	Function Description
1	V_{SS}	Power Supply	Ground
2	V_{DD}	Power Supply	Supply Voltage for OLED module
3	N.C. (BC_V_{DD})	-	No Connect by default. Can be configured to provide independent supply voltage (2.8V – 12V DC) for boost converter. (refer to On-Board Jumper Options table below)
4	D/C	MPU	Data/Command select signal, D/C=0: Command; D/C=1: Data (tie LOW for 3-wire Serial Interface)
5-6	VSS	Power Supply	Ground
7	SCLK	MPU	Serial Clock signal
8	SDIN	MPU	Serial Data Input signal
9	N.C.	-	No Connect
10-14	VSS	Power Supply	Ground
15	N.C. (VCC)	-	No Connect by default. Can be configured for external VCC (+15V). (refer to On-Board Jumper Options section below)
16	/RES	MPU	Active LOW Reset signal
17	/CS	MPU	Active LOW Chip Select signal
18	/SHDN (N.C.)	MPU	Active LOW Shutdown control pin for boost converter (pulled HIGH via on-board 15kΩ resistor) Can be made a No Connect by removing resistor R1.
19	BS1	MPU	MPU Interface select signal
20	BS0	MPU	MPU Interface select signal

Interface Selection

MPU Interface Pin Selections

Pin Name	6800 Parallel 8-bit interface	8080 Parallel 8-bit interface	3-wire Serial Interface	4-wire Serial Interface
BS1	1	1	0	0
BS0	1	0	1	0

MPU Interface Pin Assignment Summary

Bus Interface	Data/Command Interface								Control Signals				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W	/CS	D/C	/RES
8-bit 6800	D[7:0]								E	R/W	/CS	D/C	/RES
8-bit 8080	D[7:0]								/RD	/WR	/CS	D/C	/RES
3-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		/CS	Tie LOW	/RES
4-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		/CS	D/C	/RES

On-Board Jumper Options

Default Jumper Setting

R4	R5	R7	Description
Close	Open	Open	**(default)** OLED controller and boost converter + OLED panel are powered from VDD (pin #2). This allows the full module to be powered by a single low-voltage supply.

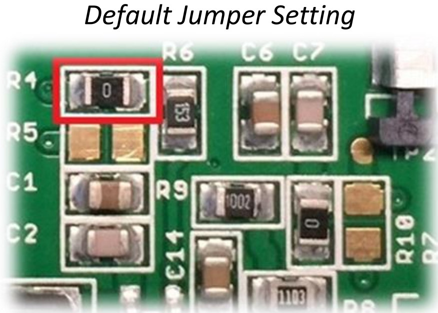
Jumper Option #1 - Independent Supply Voltage for Boost Converter (BC_VDD)

R4	R5	R7	Description
Open	**Close**	Open	Boost converter + OLED panel are powered from BC_VDD (pin #3). OLED controller is still powered from VDD (pin #2). This allows for increased efficiency through the boost converter, by allowing a supply voltage up to +12V at its input, BC_VDD (pin #3).

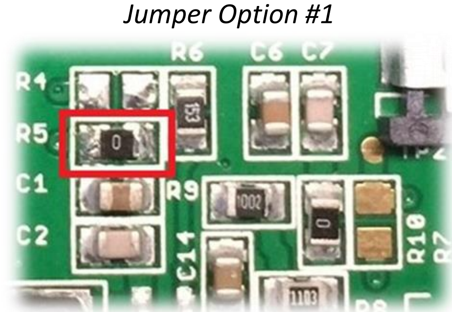
Jumper Option #2 – External Supply Voltage for OLED Panel (VCC)

R4	R5	R7	Description
Open	Open	**Close**	OLED panel is powered from VCC (pin #15) – boost converter is not used. OLED controller is still powered from VDD (pin #2). This allows for maximum module efficiency, and drastically reduced total current consumption.

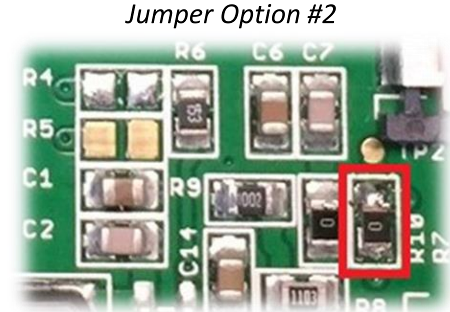
Default Jumper Setting



Jumper Option #1



Jumper Option #2



For detailed electrical information on each jumper option, please see the Electrical Characteristics table below.

Electrical Characteristics

Values for Current shown below are based on the recommended initialization provided on page 12.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	T_{OP}	Absolute Max	-40	-	+85	°C
Storage Temperature Range	T_{ST}	Absolute Max	-40	-	+85	°C
Default Jumper Setting						
Supply Voltage for Module	**V_{DD}**	**-**	**2.8**	**3.3**	**3.5**	**V**
Supply Current for Module	**I_{DD}**	**VDD=3.3V, 50% ON**	**-**	**215**	**235**	**mA**
		VDD=3.3V, 100% ON	**-**	**345**	**375**	**mA**
Jumper Option #1						
Supply Voltage for Module	V_{DD}	-	2.8	3.3	3.5	V
Supply Voltage for Boost Converter	BC_V_{DD}	-	2.8	-	12	V
Supply Current for Module	I_{DD}	VDD=3.3V	-	190	305	µA
Supply Current for Boost Converter	I_{DD_BC}	BC_VDD=5.0V, 50% ON	-	135	150	mA
		BC_VDD=5.0V, 100% ON	-	200	215	mA
		BC_VDD=12.0V, 50% ON	-	60	70	mA
		BC_VDD=12.0V, 100% ON	-	80	90	mA
Jumper Option #2						
Supply Voltage for Module	V_{DD}	-	2.8	3.3	3.5	V
Supply Voltage for OLED Panel	V_{CC}	-	14.5	15	15.5	V
Supply Current for Module	I_{DD}	V_{DD}=3.3V	-	180	300	µA
Supply Current for OLED Panel	I_{CC}	V_{CC}=15V, 50% ON	-	45	50	mA
		V_{CC}=15V, 100% ON	-	60	70	mA
Sleep Mode Current	I_{DD_SLEEP}	-	-	25	120	µA
"H" Level input	V_{IH}	-	0.8 * V_{DD}	-	V_{DD}	V
"L" Level input	V_{IL}	-	V_{SS}	-	0.2 * V_{DD}	V
"H" Level output	V_{OH}	-	0.9 * V_{DD}	-	V_{DD}	V
"L" Level output	V_{OL}	-	V_{SS}	-	0.1 * V_{DD}	V

Note: The electrical characteristics shown above for Jumper Option #1 and Jumper Option #2 apply only when the on-board jumpers are configured accordingly. By default, only Default Jumper Setting supply voltage and current (in bold) need to be considered. For details, see On-Board Jumper Options section on previous page.

Optical Characteristics

Values for Brightness shown below are based on the recommended initialization provided on page 12.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Optimal Viewing Angles	Top	φY+	-	-	85	-	°
	Bottom	φY-		-	85	-	°
	Left	θX-		-	85	-	°
	Right	θX+		-	85	-	°
Contrast Ratio		C_r	-	>10,000:1	-	-	-
Response Time	Rise	T_R	-	-	15	-	ns
	Fall	T_F	-	-	15	-	ns
Brightness		L_V	50% Checkerboard	60	80	130	cd/m^2
Lifetime		-	T_{OP} =25°C, L_V=80cd/m^2	30,000	-	-	hrs
		-	T_{OP} =25°C, L_V=60cd/m^2	50,000	-	-	hrs

Note: Lifetime at typical temperature is based on accelerated high-temperature operation. Lifetime is tested at average 50% pixels on and is rated as Hours until **Half-Brightness**. To extend the life of the display, lower values may be used for the contrast setting registers – see below table of commands for details.

Controller Information

Built-in SSD1322 controller.
For details, view full datasheet at http://www.newhavendisplay.com/app_notes/SSD1322.pdf

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Table of Commands

Instruction	Code										Description	RESET value
	D/C	HEX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Enable Grayscale Table	0	**00**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	Enable the Grayscale table settings. (see command 0xB8)	
Set Column Address	0 1 1	**15** **A[6:0]** **B[6:0]**	**0** ***** *****	**0** **A6** **B6**	**0** **A5** **B5**	**1** **A4** **B4**	**0** **A3** **B3**	**1** **A2** **B2**	**0** **A1** **B1**	**1** **A0** **B0**	Set column start and end address A[6:0]: Column start address. Range: 0-119d B[6:0]: Column end address. Range: 0-119d	 0 119d
Write RAM Command	0	**5C**	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	Enable MCU to write Data into RAM	
Read RAM Command	0	**5D**	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**1**	Enable MCU to read Data from RAM	
Set Row Address	0 1 1	**75** **A[6:0]** **B[6:0]**	**0** ***** *****	**1** **A6** **B6**	**1** **A5** **B5**	**1** **A4** **B4**	**0** **A3** **B3**	**1** **A2** **B2**	**0** **A1** **B1**	**1** **A0** **B0**	Set row start and end address A[6:0]: Row start address. Range: 0-127d B[6:0]: Row end address. Range: 0-127d	 0 127d
Set Re-map	0 1 1	**A0** **A[5:0]** **B[4]**	**1** **0** *****	**0** **0** *****	**1** **A5** **0**	**0** **A4** **B4**	**0** **0** **0**	**0** **A2** **0**	**0** **A1** **0**	**0** **A0** **1**	A[0] = 0; Horizontal Address Increment A[0] = 1; Vertical Address Increment A[1] = 0; Disable Column Address remap A[1] = 1; Enable Column Address remap A[2] = 0; Disable Nibble remap A[2] = 1; Enable Nibble remap A[4] = 0; Scan from COM0 to COM[N-1] A[4] = 1; Scan from COM[N-1] to COM0 A[5] = 0; Disable COM split Odd/Even A[5] = 1; Enable COM split Odd/Even B[4] = 0; Disable Dual COM mode B[4] = 1; Enable Dual COM mode Note: A[5] must be 0 if B[4] is 1.	0 0 0 0 0 0
Set Display Start Line	0 1	**A1** **A[6:0]**	**1** *****	**0** **A6**	**1** **A5**	**0** **A4**	**0** **A3**	**0** **A2**	**0** **A1**	**1** **A0**	Set display RAM display start line register from 0-127.	0
Set Display Offset	0 1	**A2** **A[6:0]**	**1** *****	**0** **A6**	**1** **A5**	**0** **A4**	**0** **A3**	**0** **A2**	**1** **A1**	**0** **A0**	Set vertical shift by COM from 0~127.	0
Display Mode	0	**A4~A7**	**1**	**0**	**1**	**0**	**0**	**X2**	**X1**	**X0**	0xA4 = Entire display OFF 0xA5 = Entire display ON, all pixels Grayscale level 15 0xA6 = Normal display 0xA7 = Inverse display	0xA6
Enable Partial Display	0 1 1	**A8** **A[6:0]** **B[6:0]**	**1** **0** **0**	**0** **A6** **B6**	**1** **A5** **B5**	**0** **A4** **B4**	**1** **A3** **B3**	**0** **A2** **B2**	**0** **A1** **B1**	**0** **A0** **B0**	Turns ON partial mode. A[6:0] = Address of start row B[6:0] = Address of end row (B[6:0] > A[6:0])	
Exit Partial Display	0	**A9**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	Exit Partial Display mode	

Function Selection	0 1	**AB** **A[0]**	**1** **0**	**0** **0**	**1** **0**	**0** **0**	**1** **0**	**0** **0**	**1** **0**	**1** **A0**	A[0] = 0; External VDD A[0] = 1; Internal VDD regulator	1
Set Sleep Mode ON/OFF	0	**AE~AF**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**X0**	0xAE = Sleep Mode ON (display OFF) 0xAF = Sleep Mode OFF (display ON)	
Set Phase Length	0 1	**B1** **A[7:0]**	**1** **A7**	**0** **A6**	**1** **A5**	**1** **A4**	**0** **A3**	**0** **A2**	**0** **A1**	**1** **A0**	A[3:0] = P1. Phase 1 period of 5-31 DCLK clocks A[7:4] = P2. Phase 2 period of 3-15 DCLK clocks	9 7
Set Display Clock Divide Ratio / Oscillator Frequency	0 1	**B3** **A[7:0]**	**1** **A7**	**0** **A6**	**1** **A5**	**1** **A4**	**0** **A3**	**0** **A2**	**1** **A1**	**1** **A0**	A[3:0] = 0000; divide by 1 A[3:0] = 0001; divide by 2 A[3:0] = 0010; divide by 4 A[3:0] = 0011; divide by 8 A[3:0] = 0100; divide by 16 A[3:0] = 0101; divide by 32 A[3:0] = 0110; divide by 64 A[3:0] = 0111; divide by 128 A[3:0] = 1000; divide by 256 A[3:0] = 1001; divide by 512 A[3:0] = 1010; divide by 1024 A[3:0] >= 1011; invalid A[7:4] = Set the Oscillator Frequency. Frequency increases with the value of A[7:4]. Range 0000b~1111b.	0 1100b
VSL / Display Enhancement	0 1 1	**B4** **A[1:0]** **B[7:3]**	**1** **1** **B7**	**0** **0** **B6**	**1** **1** **B5**	**1** **0** **B4**	**0** **0** **B3**	**1** **0** **1**	**0** **A1** **0**	**0** **A0** **1**	A[1:0] = 00b; Enable external VSL A[1:0] = 10b; Internal VSL B[7:3] = 11111b; Enhanced low GS display quality B[7:3] = 10110b; Normal	 10b 10110b
Set GPIO	0 1	**B5** **A[3:0]**	**1** *	**0** *	**1** *	**1** *	**0** **A3**	**1** **A2**	**0** **A1**	**1** **A0**	A[1:0] = 00; GPIO0 input disabled A[1:0] = 01; GPIO0 input enabled A[1:0] = 10; GPIO0 output LOW A[1:0] = 11; GPIO0 output HIGH A[3:2] = 00; GPIO1 input disabled A[3:2] = 01; GPIO1 input enabled A[3:2] = 10; GPIO1 output LOW A[3:2] = 11; GPIO1 output HIGH	 10b 10b
Set Second Pre-charge Period	0 1	**B6** **A[3:0]**	**1** *	**0** *	**1** *	**1** *	**0** **A3**	**1** **A2**	**1** **A1**	**0** **A0**	Sets the second precharge period A[3:0] = DCLKs	1000b
Set Grayscale Table	0 1 1 1 1 1	**B8** **A1[7:0]** **A2[7:0]** . . .	**1** $A1_7$ $A2_7$ . . .	**0** $A1_6$ $A2_6$ . . .	**1** $A1_5$ $A2_5$ . . .	**1** $A1_4$ $A2_4$ . . .	**1** $A1_3$ $A2_3$ . . .	**0** $A1_2$ $A2_2$ . . .	**0** $A1_1$ $A2_1$ . . .	**0** $A1_0$ $A2_0$ . . .	Sets the gray scale pulse width in units of DCLK. Range 0-180d. A1[7:0] = Gamma Setting for GS1 A2[7:0] = Gamma Setting for GS2 . . .	

	1 1	**A14[7:0]** **A15[7:0]**	**$A14_7$** **$A15_7$**	**$A14_6$** **$A15_6$**	**$A14_5$** **$A15_5$**	**$A14_4$** **$A15_4$**	**$A14_3$** **$A15_3$**	**$A14_2$** **$A15_2$**	**$A14_1$** **$A15_1$**	**$A14_0$** **$A15_0$**	A14[7:0] = Gamma Setting for GS14 A15[7:0] = Gamma Setting for GS15 Note: 0 < GS1 < GS2 < GS3 … < GS14 < GS15 The setting must be followed by command 0x00.	
Select Default Linear Gray Scale Table	0	**B9**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**	Sets Linear Grayscale table GS0 pulse width = 0 GS0 pulse width = 0 GS0 pulse width = 8 GS0 pulse width = 16 . . . GS0 pulse width = 104 GS0 pulse width = 112	
Set Pre-charge Voltage	0 1	**BB** **A[4:0]**	**1** *****	**0** *****	**1** *****	**1** **A4**	**1** **A3**	**0** **A2**	**1** **A1**	**1** **A0**	Set precharge voltage level. A[4:0] = 0x00; 0.20*VCC . . A[4:0] = 0x3E; 0.60*VCC	0x17
Set VCOMH Voltage	0 1	**BE** **A[3:0]**	**1** *****	**0** *****	**1** *****	**1** *****	**1** **A3**	**1** **A2**	**1** **A1**	**0** **A0**	Sets the VCOMH voltage level A[3:0] = 0x00; 0.72*VCC . . A[3:0] = 0x04; 0.8*VCC . . A[3:0] = 0x07; 0.86*VCC	0x04
Set Contrast Control	0 1	**C1** **A[7:0]**	**1** **A7**	**1** **A6**	**0** **A5**	**0** **A4**	**0** **A3**	**0** **A2**	**0** **A1**	**1** **A0**	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases.	0x7F
Master Contrast Control	0 1	**C7** **A[3:0]**	**1** *****	**1** *****	**0** *****	**0** *****	**0** **A3**	**1** **A2**	**1** **A1**	**1** **A0**	A[3:0] = 0x00; Reduce output for all colors to 1/16 A[3:0] = 0x01; Reduce output for all colors to 2/16 . . A[3:0] = 0x0E; Reduce output for all colors to 15/16 A[3:0] = 0x0F; no change	0x0f
Set Multiplex Ratio	0 1	**CA** **A[6:0]**	**1** *****	**1** **A6**	**0** **A5**	**0** **A4**	**1** **A3**	**0** **A2**	**1** **A1**	**0** **A0**	Set MUX ratio to N+1 MUX N=A[6:0]; from 16MUX to 128MUX (0 to 14 are invalid)	127d
Set Command Lock	0 1	**FD** **A[2]**	**1** **0**	**1** **0**	**1** **0**	**1** **1**	**1** **0**	**1** **A2**	**0** **1**	**1** **0**	A[2] = 0; Unlock OLED to enable commands A[2] = 1; Lock OLED from entering commands	0x12

For detailed instruction information, view full SSD1322 datasheet here (pages 32-47):

http://www.newhavendisplay.com/app_notes/SSD1322.pdf

MPU Interface

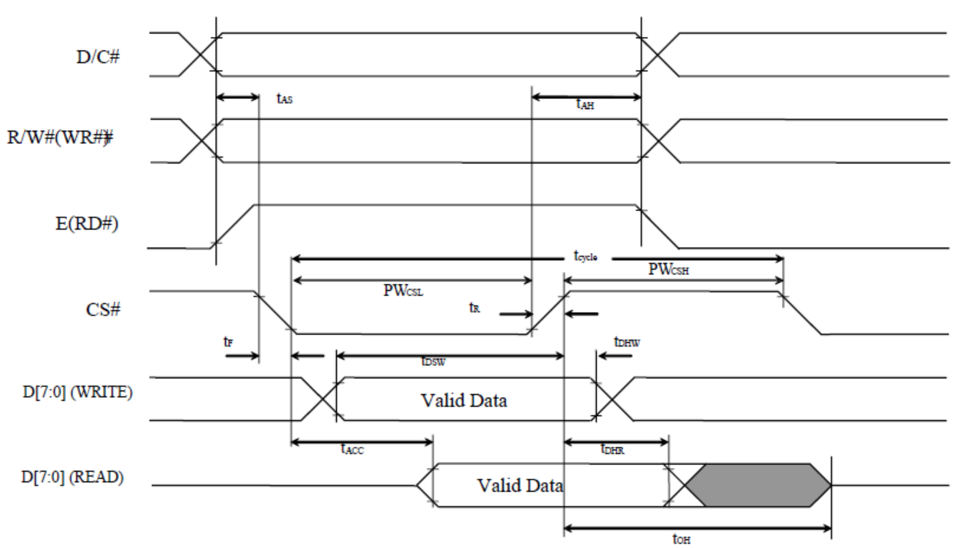
6800-MPU Parallel Interface

The parallel interface consists of 8 bi-directional data pins, R/W, D/C, E, and /CS.
A LOW on R/W indicates write operation, and HIGH on R/W indicates read operation.
A LOW on D/C indicates "Command" read or write, and HIGH on D/C indicates "Data" read or write.
The E input serves as data latch signal, while /CS is LOW. Data is latched at the falling edge of E signal.

Function	E	R/W	/CS	D/C
Write Command	↓	0	0	0
Read Status	↓	1	0	0
Write Data	↓	0	0	1
Read Data	↓	1	0	1

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



8080-MPU Parallel Interface

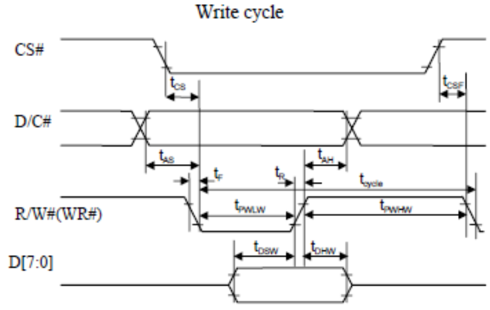
The parallel interface consists of 8 bi-directional data pins, /RD, /WR, D/C, and /CS.
A LOW on D/C indicates “Command” read or write, and HIGH on D/C indicates “Data” read or write.
A rising edge of /RS input serves as a data read latch signal while /CS is LOW.
A rising edge of /WR input serves as a data/command write latch signal while /CS is LOW.

Function	/RD	/WR	/CS	D/C
Write Command	1	↑	0	0
Read Status	↑	1	0	0
Write Data	1	↑	0	1
Read Data	↑	1	0	1

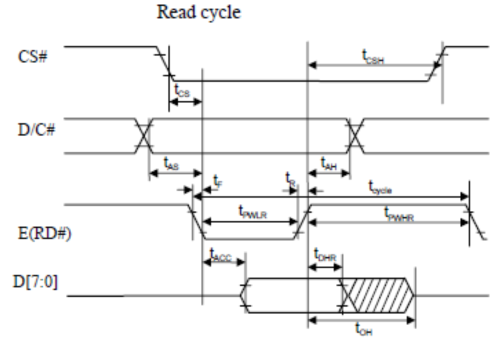
(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Write cycle



Read cycle



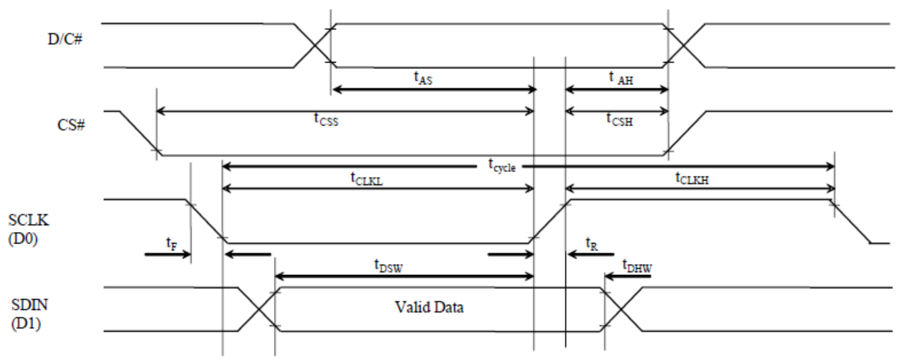
Serial Interface (4-wire)

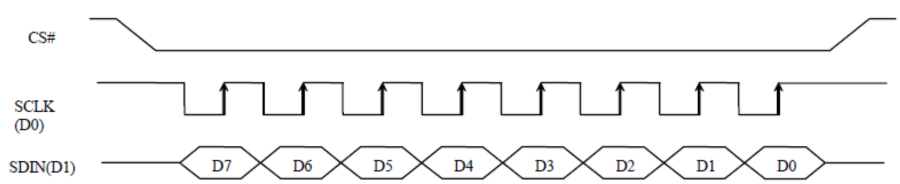
The 4-wire serial interface consists of Serial Clock (SCLK), Serial Data (SDIN), Data/Command (D/C), and Chip Select (/CS). D0 acts as SCLK and D1 acts as SDIN. D2 must be left as a No Connect
D3~D7, E, and R/W should be connected to GND.

Function	/RD	/WR	/CS	D/C	D0
Write Command	Tie LOW	Tie LOW	0	0	↑
Write Data	Tie LOW	Tie LOW	0	1	↑

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns





SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6,…D0.
D/C is sampled on every eighth clock and the data byte in the shift register is written to the GDDRAM or command register in the same clock.
Note: Read functionality is not available in serial mode.

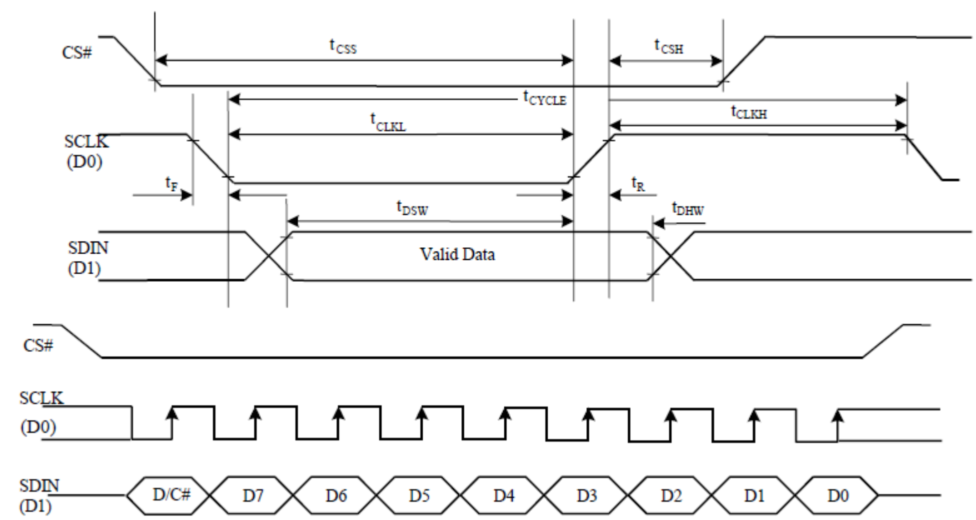
Serial Interface (3-wire)

The 3-wire serial interface consists of Serial Clock (SCLK), Serial Data In (SDIN), and Chip Select (/CS).
D0 acts as SCLK and D1 acts as SDIN. D2 must be left as a No Connect.
D3~D7, E, R/W, and D/C should be connected to Ground.

Function	/RD	/WR	/CS	D/C	D0
Write Command	Tie LOW	Tie LOW	0	Tie LOW	↑
Write Data	Tie LOW	Tie LOW	0	Tie LOW	↑

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



SDIN is shifted into an 9-bit shift register on every rising edge of SCLK in the order of D/C, D7, D6,…D0.
D/C (first bit of the sequential data) will determine if the following data byte is written to the Display Data RAM (D/C = 1) or the command register (D/C = 0).
Note: Read functionality is not available in serial mode.

For detailed timing information for each interface mode, view full SSD1322 datasheet here (pages 50-54):
http://www.newhavendisplay.com/app_notes/SSD1322.pdf

Recommended Initialization

```
void NHD12864WDY3_Init(void){
        digitalWrite(RES, LOW);         //pull /RES (pin #16) low
        delayUS(200);                   //keep /RES low for minimum 200µs
        digitalWrite(RES, HIGH);        //pull /RES high
        delayUS(200);                   //wait minimum 200µs before sending commands
        writeCommand(0xAE);             //display OFF
        writeCommand(0xB3);             //set CLK div. & OSC freq.
        writeData(0x91);
        writeCommand(0xCA);             //set MUX ratio
        writeData(0x3F);
        writeCommand(0xA2);             //set offset
        writeData(0x00);
        writeCommand(0xAB);             //function selection
        writeData(0x01);
        writeCommand(0xA0);             //set re-map
        writeData(0x16);
        writeData(0x11);
        writeCommand(0xC7);             //master contrast current
        writeData(0x0F);
        writeCommand(0xC1);             //set contrast current
        writeData(0x9F);
        writeCommand(0xB1);             //set phase length
        writeData(0xF2);
        writeCommand(0xBB);             //set pre-charge voltage
        writeData(0x1F);
        writeCommand(0xB4);             //set VSL
        writeData(0xA0);
        writeData(0xFD);
        writeCommand(0xBE);             //set VCOMH
        writeData(0x04);
        writeCommand(0xA6);             //set display mode
        writeCommand(0xAF);             //display ON
}
```

Example Software Routines

```
void setColumn(unsigned char xStart, unsigned char xEnd){
  writeCommand(0x15);       //set column (x-axis) start/end address
  writeData(xStart);        //column start; 28 is left-most column
  writeData(xEnd);          //column end; 91 is right-most column
}

void setRow(unsigned char yStart, unsigned char yEnd){
  writeCommand(0x75);       //set row (y-axis) start/end address
  writeData(yStart);        //row start; 0 is top row
  writeData(yEnd);          //row end; 63 is bottom row
}

void clearDisplay(void){
  unsigned int i;
  setColumn(28,91);         //set column (x-axis) start/end address
  setRow(0,63);             //set row (y-axis) start/end address
  writeRAM();               //single byte command (0x5C) to initiate pixel data write to GDDRAM;
  for(i=0;i<4096;i++){      // ((91-28)+1)*((63-0)+1)
   writeData(0x00);
   writeData(0x00);
  }
}

void write2Pixels(unsigned char xPos, unsigned char yPos, unsigned char pixel1, unsigned char pixel2){
  if(pixel1>=1) pixel1 = 0xFF;         //set 1st pixel value to ON
  else pixel1 = 0x00;                  //set 1st pixel value to OFF
  if(pixel2>=1) pixel2 = 0xFF;         //set 2nd pixel value to ON
  else pixel2 = 0x00;                  //set 2nd pixel value to OFF
  if(xPos>127) xPos = 127;             //boundary check (MIN xPos = 0, MAX xPos = 127)
  xPos = xPos/2;                       //account for GDDRAM address mapping
  xPos+=28;                            //account for GDDRAM address mapping
  if(yPos>63) yPos = 63;               //boundary check (MIN yPos = 0, MAX yPos = 63)
  setColumn(xPos,xPos);                //set column (x-axis) start/end address
  setRow(yPos,yPos);                   //set row (y-axis) start/end address
  writeRAM();                          //single byte command (0x5C) to initiate pixel data write to GDDRAM;
  writeData(pixel1);                   //write 1st of 2 pixels to the display
  writeData(pixel2);                   //write 2nd of 2 pixels to the display
}

void displayArray12864(const unsigned char arr[]){        //display 128x64 monochrome bitmap, horizontal pixel arrangement, 8-pixels per byte
  unsigned int i, j;
  setColumn(28,91);                    //set column (x-axis) start/end address
  setRow(0,63);                        //set row (y-axis) start/end address
  writeRAM();                          //single byte command (0x5C) to initiate pixel data write to GDDRAM;
  for(i=0;i<1024;i++){                 //translate each byte/bit into pixel data
   for(j=0;j<8;j++){
    if(((arr[i]<<j)&0x80)==0x80){
     writeData(0xFF);
    }
    else{
     writeData(0x00);
    }
   }
  }
}
```

Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	+85°C, 240hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-40°C, 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the high thermal stress for a long time.	+85°C, 240hrs	2
Low Temperature Operation	Endurance test applying the electric stress (voltage & current) and the low thermal stress for a long time.	-40°C, 240hrs	1,2
High Temperature / Humidity Storage	Endurance test applying the electric stress (voltage & current) and the high thermal with high humidity stress for a long time.	+60°C, 90% RH, 240hrs	1,2
Thermal Shock resistance	Endurance test applying the electric stress (voltage & current) during a cycle of low and high thermal stress.	-40°C, 30min -> +25°C, 5min -> +85°C, 30min = 1 cycle 100 cycles	
Vibration test	Endurance test applying vibration to simulate transportation and use.	10-22Hz, 15mm amplitude. 22-500Hz, 1.5G 30min in each of 3 directions X, Y, Z	3
Atmospheric Pressure Test	Test the endurance of the display by applying atmospheric pressure to simulate transportation by air.	115mbar, 40hrs	3
Static electricity test	Endurance test applying electric static discharge.	Air: ±8KV; 300Ω, 150pF Contact: ±4KV; 300Ω, 150pF	

Note 1: No condensation to be observed.
Note 2: Conducted after 2 hours of storage at 25°C, 0%RH.
Note 3: Test performed on product itself, not inside a container.
Evaluation Criteria:
1: Display is fully functional during operational tests and after all tests, at room temperature.
2: No observable defects.
3: Luminance >50% of initial value.
4: Current consumption within 50% of initial value