

## GENERAL DESCRIPTION

OB2365D is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

At normal load condition, it operates in fixed frequency mode. When the loading goes low, it operates in PFM mode for high power conversion efficiency. When the load is very small, the IC operates in 'Extended Burst Mode' to minimize the standby power loss. As a result, high conversion efficiency can be achieved in the whole loading range.

VCC low startup current and low operating current contribute to a reliable power on startup and low standby design with OB2365D.

OB2365D offers comprehensive protection coverage with auto-recovery including Cycle-by-Cycle current limiting, VCC under voltage lockout (UVLO) and AC Brownout protection. It also provides the protections with latched shut down including VCC over voltage protection(OVP),over load protection (OLP), over temperature protection (OTP),output over voltage protection(OVP) and short protection(SCP). Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

The tone energy at below 23KHz is minimized in the design and audio noise is eliminated during operation.

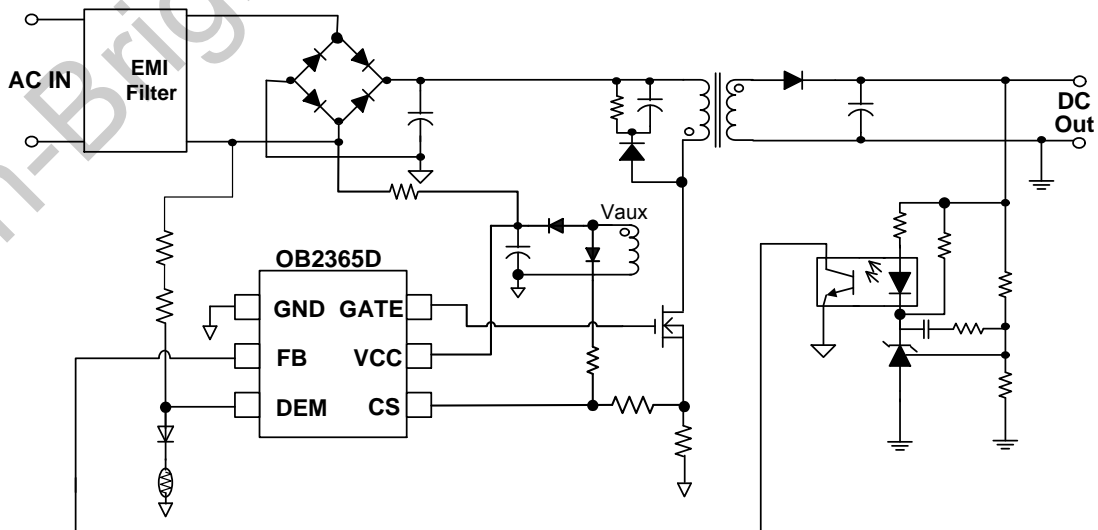
OB2365D is offered in SOT23-6 package.

## APPLICATIONS

Offline AC/DC flyback converter for

- General power supply
- Power Adapter

## TYPICAL APPLICATION

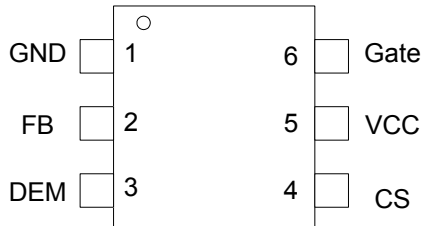


## FEATURES

- Power on soft start reducing MOSFET Vds stress
- Multi-Mode Operation
  - 120K clamping frequency @Peak load in low line voltage
  - 65KHz fixed frequency @ Heavy Load in low line voltage
  - Burst Mode @ Light Load & No Load
- Frequency shuffling for EMI
- Extended burst mode control for improved efficiency and low standby power design
- Audio noise free operation
- Comprehensive protection coverage
  - VCC Under Voltage Lockout with hysteresis (UVLO)
  - VCC Over Voltage Protection (VCC OVP) with latch mode
  - Cycle-by-cycle over current threshold setting for constant output power limiting over universal input voltage range
  - Over Current Protection (OCP) with latch mode
  - Peak load Protection with latch mode
  - External Over Temperature Protection(OTP) with latch mode
  - Brownout protection with auto-recovery
  - Adjust Over Voltage Protection(OVP) through CS pin with latch mode
  - Output SCP Protection with latch mode
  - Output diode short protection with auto-recovery

### GENERAL INFORMATION

#### Pin Configuration



#### Ordering Information

| Part Number | Description                  |
|-------------|------------------------------|
| OB2365DMP   | SOT23-6, Halogen-free in T&R |

#### Package Dissipation Rating

| Package | R $\theta$ JA(°C/W) |
|---------|---------------------|
| SOT23-6 | 200                 |

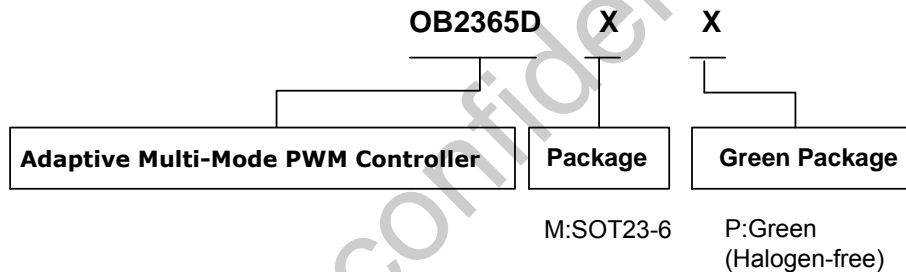
#### Recommended operating condition

| Symbol | Parameter          | Range     |
|--------|--------------------|-----------|
| VCC    | VCC Supply Voltage | 12 to 26V |

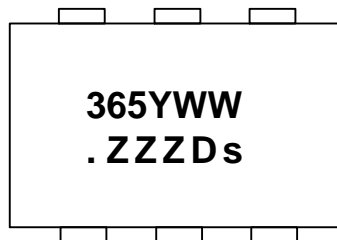
#### Absolute Maximum Ratings

| Parameter   | Value         |
|---|---------------|
| VCC DC Supply Voltage                                 | 30V           |
| FB Input Voltage                                      | -0.7 to 7V    |
| CS Input Voltage                                      | -0.7 to 7V    |
| DEM Input Voltage                                     | -0.7 to 7V    |
| Min/Max Operating Junction Temperature T <sub>J</sub> | -40 to 150 °C |
| Min/Max Storage Temperature T <sub>stg</sub>          | -55 to 150 °C |
| Lead Temperature (Soldering, 10secs)                  | 260 °C        |

**Note:** Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



#### Marking Information

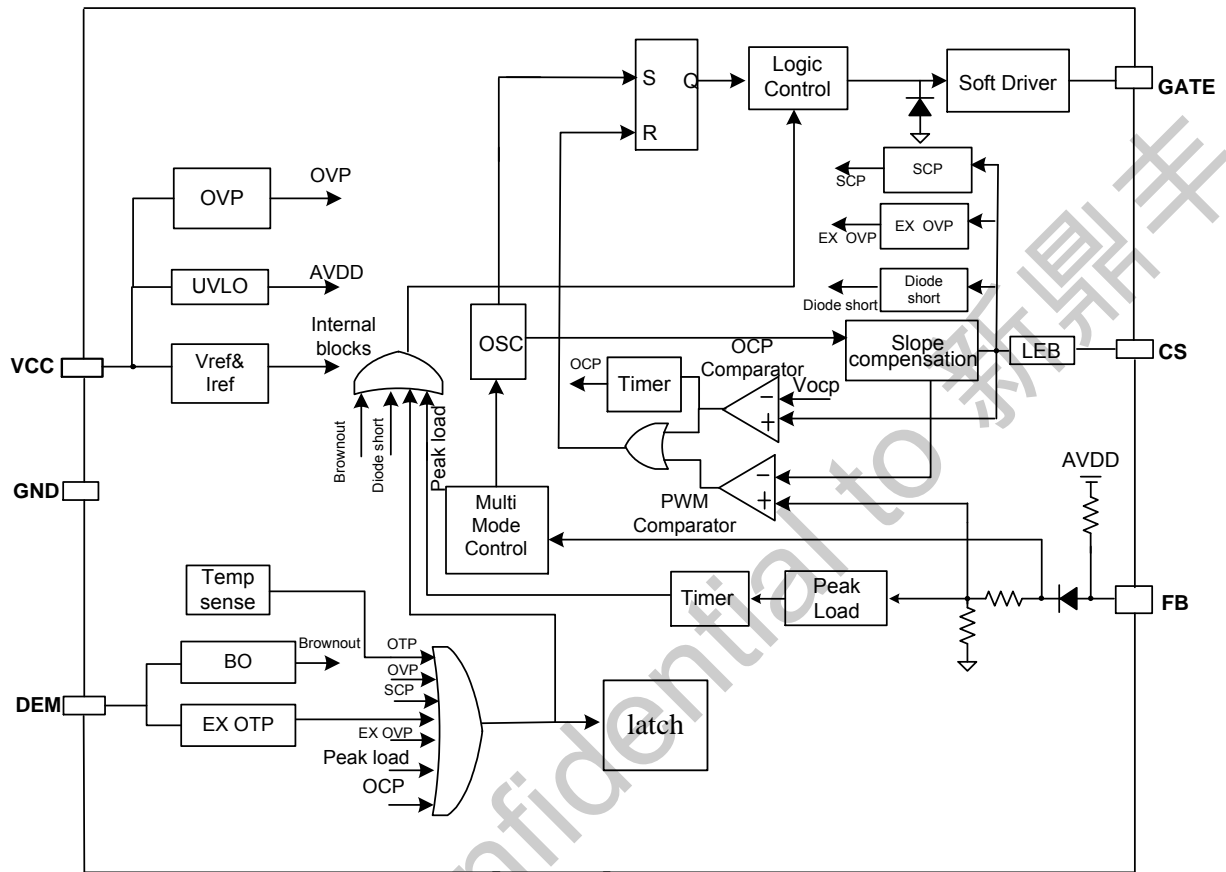


Y: Year Code  
 WW: Week Code(01-52)  
 ZZZ: Lot code  
 D: Character code  
 s: Internal code

**TERMINAL ASSIGNMENTS**

| Pin Name | I/O | Description   |
|----------|-----|---|
| VCC      | P   | Power Supply  |
| CS       | I   | Current sense input. This pin is also connected to an auxiliary winding of the PWM transformer through a resistor and a diode for OVP/SCP protection.                                 |
| Gate     | O   | Totem-pole gate driver output for power MOSFET  |
| GND      | P   | Ground  |
| DEM      | I   | Multiple functions pin. Connecting a diode and a NTC resistor to ground for OTP detection. Connecting two resistors to AC(L or N Line) can adjust Brown-in/Brown-out trigger voltage. |
| FB       | I   | Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin CS.   |

**FUNCTIONAL BLOCK DIAGRAM**



**ELECTRICAL CHARACTERISTICS**

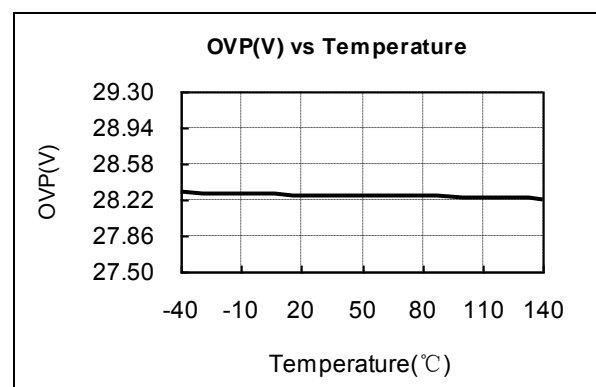
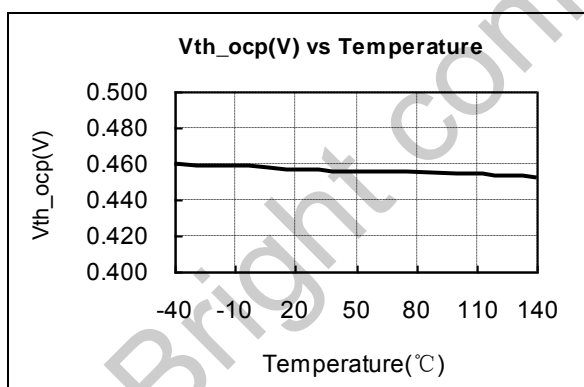
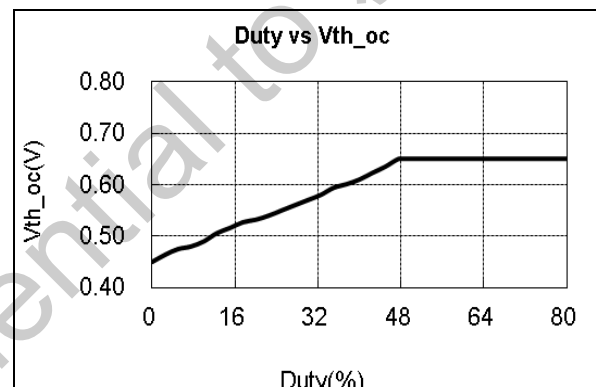
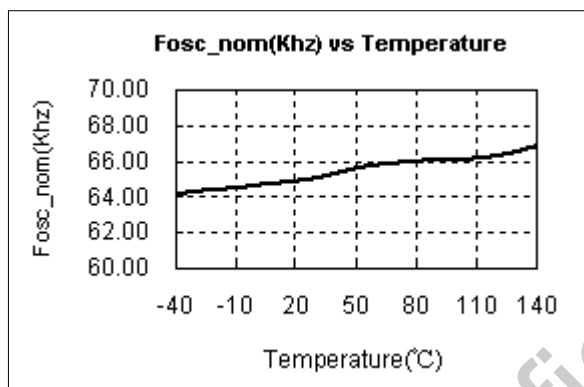
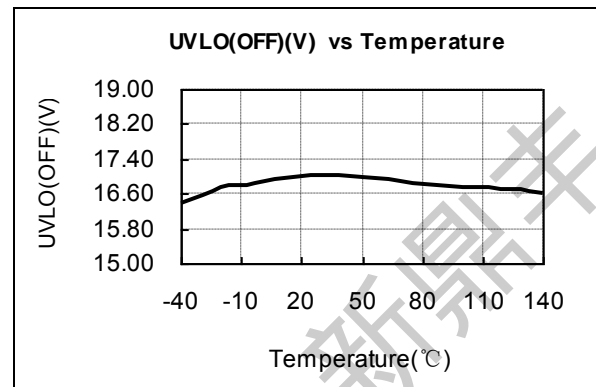
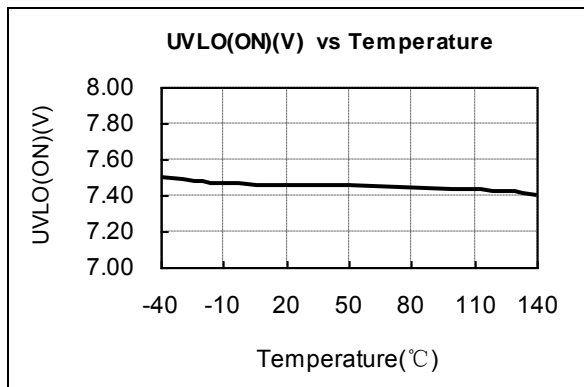
 (T<sub>A</sub> = 25°C, V<sub>CC</sub>=18V, unless otherwise noted)

| Symbol                                | Parameter  | Test Conditions  | Min | Typ. | Max  | Unit       |
|---------------------------------------|--|--|-----|------|------|------------|
| <b>Supply Voltage (VDD)</b>           |  |  |     |      |      |            |
| I <sub>startup</sub>                  | VCC Start up Current   | VCC=UVLO(OFF)-1V, measure leakage current into VCC                     |     | 2    | 5    | uA         |
| I <sub>VCC_Operation</sub>            | Operation Current  | VDD=18V,CS=4V, FB=3.5V,measure I(VCC)                                  |     | 2    | 3    | mA         |
| I <sub>VCC_Burst</sub>                | Burst Current  | CS=0V,FB=0.5V, measure I(VCC)  |     | 0.3  | 0.5  | mA         |
| UVLO(ON)                              | VCC Under Voltage Lockout Enter                                  |  | 7.0 | 7.5  | 8.0  | V          |
| UVLO(OFF)                             | VCC Under Voltage Lockout Exit (Recovery)                        |  | 16  | 17   | 18   | V          |
| V <sub>pull-up</sub>                  | Pull-up PMOS active  |  |     | 10   |      | V          |
| OVP                                   | VCC Over Voltage Protection threshold voltage                    | FB=3V, CS=0V. Slowly ramp VCC, until no gate switching.                |     | 28   | 29.5 | V          |
| V <sub>latch_release</sub>            | Latch release voltage  |  |     | 5    |      | V          |
| <b>Feedback Input Section(FB Pin)</b> |  |  |     |      |      |            |
| V <sub>FB_Open</sub>                  | V <sub>FB</sub> Open Loop Voltage                                |  |     | 5.1  |      | V          |
| A <sub>vcs</sub>                      | PWM input gain $\Delta V_{FB}/\Delta V_{CS}$                     |  |     | 3.3  |      | V/V        |
| Maximum duty cycle                    | Max duty cycle @ VCC=18V,VFB=3V,VCS=0V                           |  | 75  | 80   | 85   | %          |
| V <sub>ref_green</sub>                | The threshold enter green mode                                   |  |     |      |      | V          |
| V <sub>ref_burst_H</sub>              | The threshold exits burst mode                                   |  |     | 1.55 |      | V          |
| V <sub>ref_burst_L</sub>              | The threshold enters burst mode                                  |  |     | 1.45 |      | V          |
| I <sub>FB_Short</sub>                 | FB pin short circuit current                                     | Short FB pin to GND and measure current                                |     | 0.16 |      | mA         |
| V <sub>TH_PK</sub>                    | Peak load, threshold voltage                                     |  |     | 4.4  |      | V          |
| T <sub>d_PK</sub>                     | Peak load, debounce Time   |  |     | 72   |      | ms         |
| Z <sub>FB_IN</sub>                    | Input Impedance  |  |     | 30   |      | K $\Omega$ |
| <b>Current Sense Input(CS Pin)</b>    |  |  |     |      |      |            |
| SST_CS                                | Soft start time for CS peak                                      |  |     | 2.5  |      | ms         |
| T <sub>blanking</sub>                 | Leading edge blanking time                                       |  |     | 330  |      | ns         |
| T <sub>d_OC</sub>                     | Over Current Detection and Control Delay                         | From Over Current Occurs till the Gate driver output start to turn off |     | 80   |      | ns         |
| V <sub>TH_OC</sub>                    | Internal Current Limiting Threshold Voltage with zero duty cycle |  |     | 0.45 |      | V          |
| V <sub>TH_OC_Clamp</sub>              | OCP CS voltage clamber   |  |     | 0.65 |      | V          |
| T <sub>d_OCP</sub>                    | OCP debounce time  |  |     | 100  |      | ms         |
| V <sub>TH_PK_CS_Clamp</sub>           | PK load CS voltage clamber                                       |  |     | 0.85 |      | V          |
| V <sub>TH_OVP</sub>                   | CS pin output OVP threshold                                      |  |     | 0.36 |      | V          |
| TD_OVP                                | Output OVP debounce time   | FB > V <sub>ref_burst_H</sub>  |     | 7    |      | cycle      |
| V <sub>TH_cs_sample</sub>             | CS pin output voltage high/low                                   |  |     | 100  |      | mV         |

|                            |  |                   |      |      |      |       |
|----------------------------|--|-------------------|------|------|------|-------|
|                            | threshold  |                   |      |      |      |       |
| V <sub>TH_scp</sub>        | SCP threshold<br>(Startup blanking 6mS)                        |                   | 90   |      |      | mV    |
| TD_SCP                     | Output SCP debounce time                                       | FB > Vref_burst_H | 7    |      |      | cycle |
| TD_off_sample              | Toff CS pin sampling delay time                                |                   | 2.5  |      |      | uS    |
| <b>DEM pin</b>             |  |                   |      |      |      |       |
| I <sub>brown-in</sub>      | Brown-in threshold current                                     |                   | 10.5 | 11.5 | 12.5 | uA    |
| I <sub>brown-out</sub>     | Brown-out threshold current                                    |                   | 9    | 10   | 11   | uA    |
| T <sub>d_BO</sub>          | Brown-out protection,<br>Debounce Time                         |                   |      | 56   |      | ms    |
| V <sub>th_otp</sub>        | Voltage threshold for<br>adjustable output OTP                 |                   | 0.80 | 0.85 | 0.90 | V     |
| T <sub>d_otp</sub>         | External OTP debounce time                                     |                   |      | 30   |      | cycle |
| Clk_dem                    | Brownout and OTP detection<br>clock                            |                   |      | 32   |      | K     |
| <b>In-chip OTP</b>         |  |                   |      |      |      |       |
| OTP enter                  |  |                   |      | 150  |      | °C    |
| OTP exit                   |  |                   |      | 120  |      | °C    |
| <b>Oscillator</b>          |  |                   |      |      |      |       |
| F <sub>osc_nom</sub>       | Oscillation frequency in CCM<br>mode                           | VDD=15V,FB=3V,    |      | 65   |      | KHz   |
| Δf <sub>OSC_nom</sub>      | Oscillation frequency jittering                                |                   |      | ±7   |      | %     |
| F <sub>osc_clamp_PK</sub>  | Clamp oscillation frequency in<br>Peak load mode with 48% duty | VDD=15V,FB=4.5V   |      | 120  |      | KHz   |
| Δf <sub>OSC_clamp_PK</sub> | Min clamp oscillation frequency<br>jittering                   |                   |      | ±7   |      | %     |
| F <sub>shuffling</sub>     | Shuffling frequency  |                   |      | 240  |      | Hz    |
| Δf <sub>Temp</sub>         | Frequency Temperature<br>Stability                             |                   |      | 1    |      | %     |
| Δf <sub>VCC</sub>          | Frequency Voltage Stability                                    |                   |      | 1    |      | %     |
| F <sub>Burst</sub>         | Burst Mode Switch Frequency                                    |                   |      | 24   |      | KHz   |
| <b>Gate driver</b>         |  |                   |      |      |      |       |
| V <sub>OL</sub>            | Output low level @ VDD=18V,<br>I <sub>o</sub> =5mA             |                   |      |      | 1    | V     |
| V <sub>OH</sub>            | Output high level @ VCC=18V,<br>I <sub>o</sub> =20mA           |                   | 6    |      |      | V     |
| V <sub>clamping</sub>      | Output clamp voltage   |                   |      | 11.5 |      | V     |
| T <sub>r</sub>             | Output rising time 1.2V ~ 10.0V<br>@ CL=2000pF                 |                   |      | 250  |      | ns    |
| T <sub>f</sub>             | Output falling time 10.0V ~ 1.2V<br>@ CL=2000pF                |                   |      | 60   |      | ns    |

### CHARACTERIZATION PLOTS

VDD = 18V, TA = 25°C condition applies if not otherwise noted.



### OPERATION DESCRIPTION

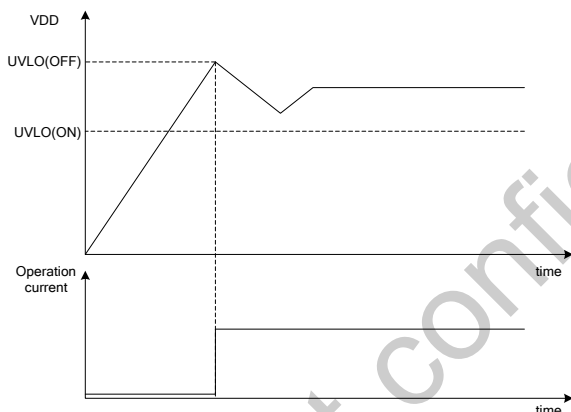
OB2365D is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications. The 'extended burst mode' control greatly reduces the standby power consumption and helps the design easier to meet the international power conservation requirements.

#### Startup Current and Start up Control

Startup current of OB2365D is designed to be very low so that VCC could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

#### Operating Current

The Operating current of OB2365D is low at 2mA (typical). Good efficiency is achieved with OB2365D low operation current together with the 'extended burst mode' control features.



#### Soft Start

OB2365D features an internal 2.5ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VCC reaches UVLO(OFF), the CS peak voltage is gradually increased from 0.05V to the maximum level. Every restart up is followed by a soft start.

#### Multi Mode Operation for High Efficiency

OB2365D is a high performance current mode PWM controller. The controller changes the mode of operation according to line voltage and load conditions.

At normal operating conditions ( $V_{G2} < V_{FB} < V_{ocp}$ ), the system operates in fixed frequency mode.

At light load conditions ( $V_{G1} < V_{FB} < V_{G2}$ ), the system operates in PFM (pulse frequency modulation) mode for high power conversion efficiency. Generally, in flyback converter, the

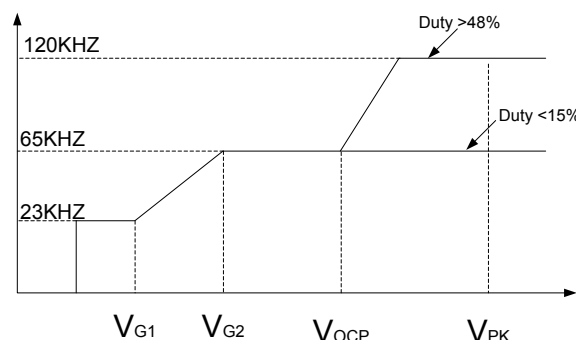
decreasing of load results in voltage level decreasing at FB pin. The controller monitors the voltage level at FB and control the switching frequency. That is, when load decreases, In such way, a smooth frequency fold-back is realized and high power conversion efficiency is achieved.

At no load or very light load conditions ( $V_{FB} < V_{G1}$ ), the system operates in On-Bright's proprietary "extended burst mode". In the extended burst mode, the switching frequency at below 23KHz is minimized to avoid audio noise during operation.

#### Oscillator Operation

During the full load power operation, OB2365D operates at a 65KHz (typical) fixed frequency mode. The efficiency and system cost is controlled at an optimal level. In over power mode, frequency is increased from 65KHz (typical) to 120KHz (typical). The maximum frequency is limited to 65KHz when the PWM duty is lower than 15%.

At light load levels, OB2365D enters the light load mode, where the output current is reduced. The switching losses are reduced by lowering the switching frequency.



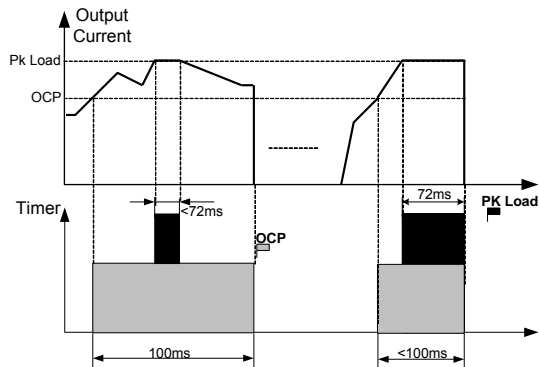
#### Two level OCP Controls

In order to meet peak current output requirement, OB2365D sets up two levels OCP protection thresholds. The two thresholds correspond to the normal OCP protection and peak power protection respectively, and these two threshold values are internally compensated. When primary side inductor current exceeds the OCP threshold, OCP timer will begin counting. After 100ms (typical), OCP protection occurs.

When primary side inductor current exceeds the peak power threshold, over peak power timer will begin counting. After 72ms (typical), peak load protection occurs.

OCP and peak power protection are mutually independent and do not affect each.





### Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB2365D current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

### Internal Synchronized Slope Compensation

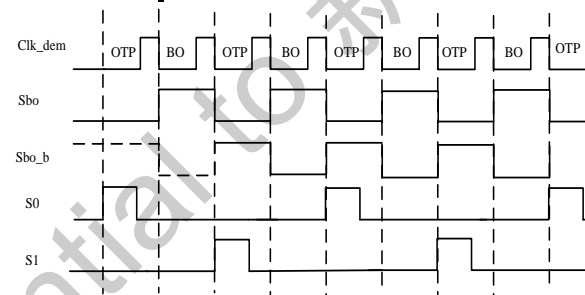
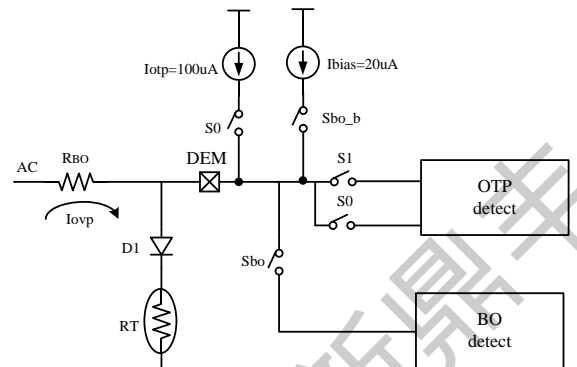
Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

### Driver

The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

### Multiple Functions of Brown-in/Brown-out and External OTP



On-Bright proprietary dual function of external OTP and Brown-in/Brown-out provides feasible and accurate detection of external OTP through NTC resistor and Brown-in/Brown-out. The dual function is realized through time-division technology as shown in the figure.

RBO: The resistor connected from DEM to AC input.

RT: The resistor connected from DEM to ground.

When system starts up, if  $I_{AUX} < I_{brown\_in}$ , Brown-in auto-recovery protection is triggered. When the system enters the normal operation mode, if  $I_{AUX} < I_{brown\_out}$ , Brown-out auto-recovery protection is triggered after 56ms debounce.

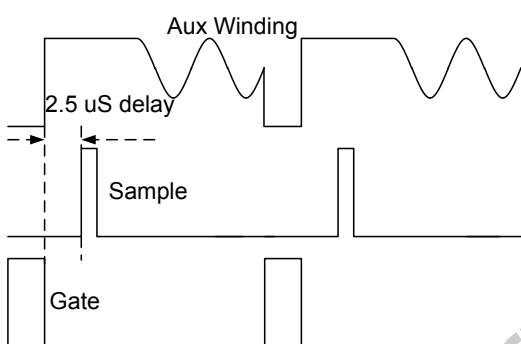
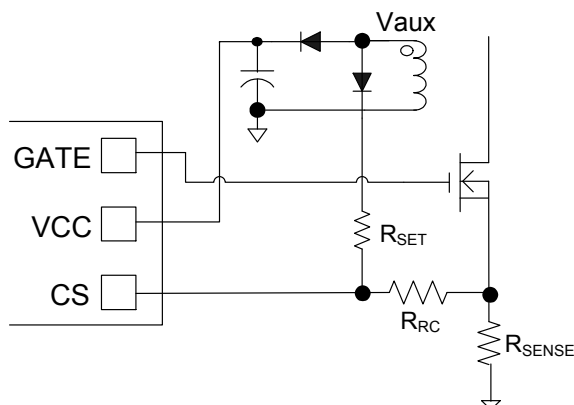
For external OTP detection, when switch control signal  $S0\_b = "1"$ , about 20uA (typical) current flows out from DEM pin. When switch control signal  $S0 = "1"$ , about 120uA (typical) current flows out from DEM pin. The DEM pin voltage difference  $\Delta V_{otp}$  at phase  $S0$  and  $S1$  phase is

$$\text{equal to } \Delta V_{otp} = \frac{RT \cdot ROVP}{ROVP + RT} \cdot 100\mu A \cdot$$

When  $\Delta V_{otp} < 0.85V$ , external OTP latched protection is triggered after 30 cycles debounce.

### Output Over Voltage Protection

An output over voltage protection is implemented in the OB2365D by sensing the auxiliary voltage:



The auxiliary winding voltage is a well-defined replica of the output voltage. The OVP works by sampling the plateau voltage at CS pin during the flyback phase. OB2365D can sample this flat voltage level after a delay time to perform over temperature protection. This delay time is used to

ignore the voltage ringing from leakage inductance of PWM transformer.

The sampling voltage level is compared with internal threshold voltage 0.36V. If the sampling voltage exceeds the OVP trip level, an internal counter starts counting subsequent OVP events. If OVP events are detected in consecutive 7 cycle, the controller assumes a true OVP and the system enters into latch mode.

If the sampling voltage is smaller than 90mV(typical), the internal counter starts counting subsequent SCP events more than 8 cycles, and the same time FB open>6mS & VCC<9.8V, then trigger SCP protection with latch.

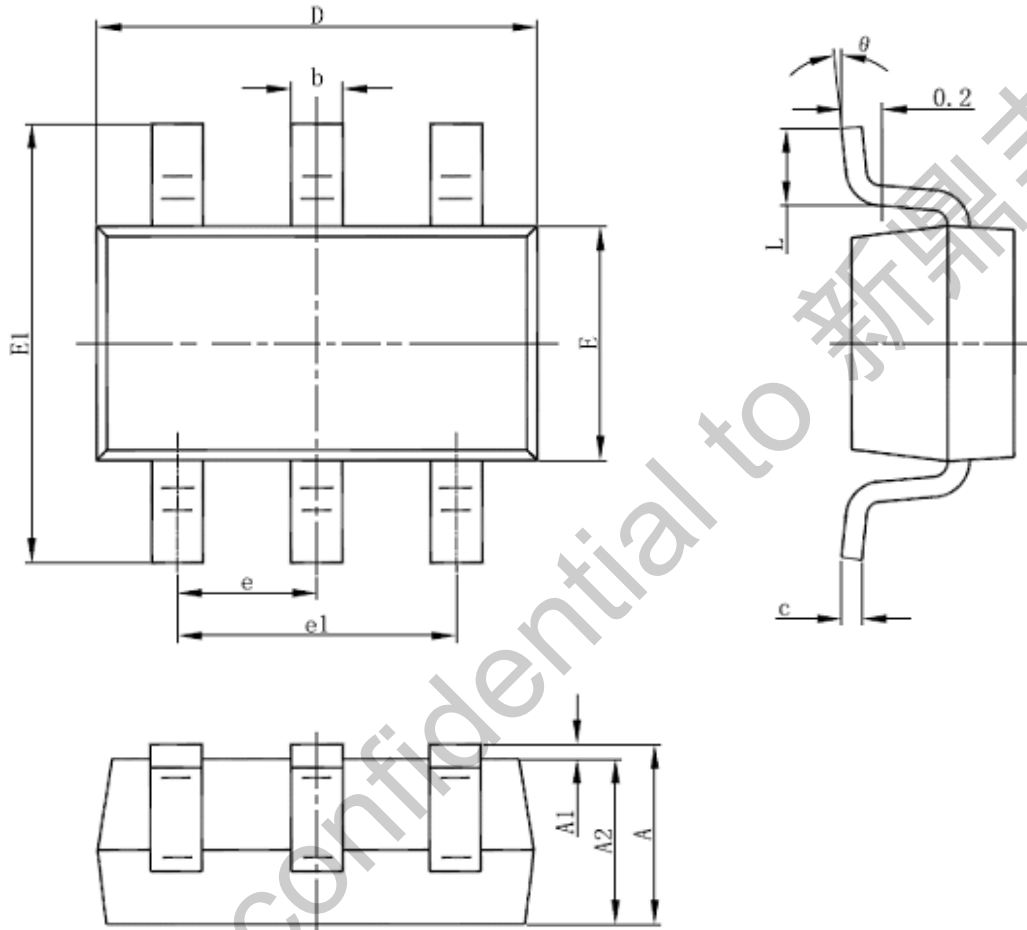
### Protection Controls

Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Under Voltage Lockout on VDD (UVLO), brownout protection and latched shut down features including over load protection (OLP), Over Temperature Protection (OTP), output SCP, VCC and output Over Voltage Protection (OVP).

With On-Bright proprietary technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

At overload condition when FB input voltage exceeds power limit threshold value for more than Td\_OLP, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below Vlatch\_release.

**PACKAGE MECHANICAL DATA**



| Symbol | Dimensions In Millimeters |       | Dimensions In Inches |       |
|--------|---------------------------|-------|----------------------|-------|
|        | Min                       | Max   | Min                  | Max   |
| A      | 1.000                     | 1.450 | 0.039                | 0.057 |
| A1     | 0.000                     | 0.150 | 0.000                | 0.006 |
| A2     | 0.900                     | 1.300 | 0.035                | 0.051 |
| b      | 0.300                     | 0.500 | 0.012                | 0.020 |
| c      | 0.080                     | 0.220 | 0.003                | 0.009 |
| D      | 2.800                     | 3.020 | 0.110                | 0.119 |
| E      | 1.500                     | 1.726 | 0.059                | 0.068 |
| E1     | 2.600                     | 3.000 | 0.102                | 0.118 |
| e      | 0.950 (BSC)               |       | 0.037 (BSC)          |       |
| e1     | 1.800                     | 2.000 | 0.071                | 0.079 |
| L      | 0.300                     | 0.600 | 0.012                | 0.024 |
| θ      | 0°                        | 8°    | 0°                   | 8°    |

## **IMPORTANT NOTICE**

### **RIGHT TO MAKE CHANGES**

On-Bright Electronics Corp. reserves the right to make corrections, modifications, enhancements, improvements and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

### **WARRANTY INFORMATION**

On-Bright Electronics Corp. warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with its standard warranty. Testing and other quality control techniques are used to the extent it deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

On-Bright Electronics Corp. assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using On-Bright's components, data sheet and application notes. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

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### **MILITARY**

On-Bright Electronics Corp.'s products are not designed for use in military applications. On-Bright Electronics Corp. will not be held liable for any damages or claims resulting from the use of its products in military applications.