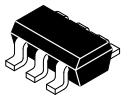
CM1231-02SO

2, 4 and 8-Channel Low-Capacitance ESD Protection Array

ON Semiconductor®

www.onsemi.com



SOT23−6
SO SUFFIX
CASE 527AJ

Product Description

The CM1231−02SO is specifically designed for next generation deep submicron ASIC protection. These devices are ideal for protecting systems with high data and clock rates and for circuits requiring low capacitive loading such as USB 2.0.

The CM1231−02SO incorporates dual stage ESD architecture which offers dramatically higher system level ESD protection compared with traditional single clamp designs. In addition, the CM1231−02SO provides a controlled filter roll−off for even greater spurious EMI suppression and signal integrity.

The CM1231−02SO protects against ESD pulses up to ±12 kV contact on the “OUT” pins per the IEC 61000−4−2 standard.

The device also features easily routed “pass−through” differential pinouts in a 6−lead SOT23 package.

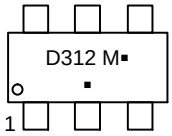
Features

- Two Channels of ESD Protection
- Exceeds ESD Protection to IEC61000−4−2 Level 4:
  - ±12 kV Contact Discharge (OUT Pins)
- Two−Stage Matched Clamp Architecture
- Matching−of−Series Resistor (R) of ±10 mΩ Typical
- Flow−Through Routing for High−Speed Signal Integrity
- Differential Channel Input Capacitance Matching of 0.02 pF Typical
- Improved Powered ASIC Latchup Protection
- Dramatic Improvement in ESD Protection vs. Best in Class Single−Stage Diode Arrays
  - 40% Reduction in Peak Clamping Voltage
  - 40% Reduction in Peak Residual Current
- Withstands over 1000 ESD Strikes*
- Available in a SOT23−6 Package
- These Devices are Pb−Free and are RoHS Compliant

Applications

- USB Devices Data Port Protection
- General High−Speed Data Line ESD Protection

MARKING DIAGRAM



D312 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
CM1231−02SO	SOT23−6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*Standard test condition is IEC61000−4−2 level 4 test circuit with each (A_{OUT}/B_{OUT}) pin subjected to ±12 kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run.

ELECTRICAL SCHEMATIC

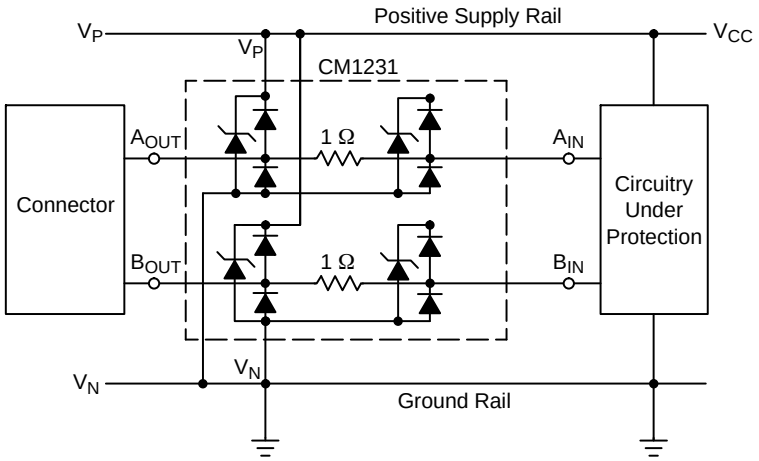
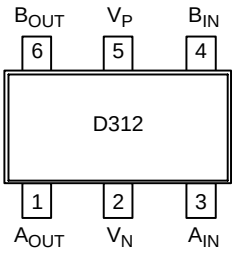


Table 1. PIN DESCRIPTIONS

Pin	Name	Description
1	A_{OUT}	Bidirectional clamp to Connector (Outside the system)
2	V_N	Ground return to Shield
3	A_{IN}	Bidirectional clamp to ASIC (Inside the system)
4	B_{IN}	Bidirectional clamp to ASIC (Inside the system)
5	V_P	Bias voltage (optional)
6	B_{OUT}	Bidirectional clamp to Connector (Outside the system)

PACKAGE / PINOUT DIAGRAMS



SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Supply Voltage (V_P)	6.0	V
Diode Forward DC Current (A_{OUT}/B_{OUT} Side)	8.0	mA
Continuous Current through Signal Pins (IN to OUT) 1000 hours	125	mA
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C
DC Voltage at any channel input	(V_N − 0.5) to (V_P + 0.5)	V
Package Power Rating (SOT23−6)	225	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_P	Operating Supply Voltage			5	5.5	V
I_{CC5}	Operating Supply Current	V_P = 5 V			1	μA
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 8 mA, T_A = 25°C	 0.60 0.60	 0.80 0.80	 0.95 0.95	V
V_{ESD}	ESD Protection, Contact Discharge per IEC 61000−4−2 Standard OUT−to−V_N Contact IN−to−V_N Contact	T_A = 25°C	 ±12 ±4			kV
I_{RES}	Residual ESD Peak Current on RDUP (Resistance of Device Under Protection)	IEC 61000−4−2 8 kV RDUP = 5 Ω, T_A = 25°C		2.3		A
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	I_{PP} = 1 A, T_A = 25°C, t_P = 8/20 μs, Zap at OUT, Measure at IN		 +9 –1.4		V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	I_{PP} = 1 A, T_A = 25°C, t_P = 8/20 μs, Zap at OUT, Measure at IN		 0.4 0.3		Ω
C_{OUT}	OUT Capacitance	f = 1 MHz, V_P = 5.0 V, V_{IN} = 2.5 V, V_{OSC} = 30 mV (Note 2)		1.5		pF
ΔC_{OUT}	Channel to Channel Capacitance Match	f = 1 MHz, V_P = 5.0 V, V_{IN} = 2.5 V, V_{OSC} = 30 mV		0.02		pF
R_S	Series Resistance			1		Ω
ΔR_S	Channel to Channel Resistance Match			±10	±30	mΩ

1. All parameters specified at T_A = –40°C to +85°C unless otherwise noted.
2. Capacitance measured from OUT to V_N with IN floating.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

SINGLE AND DUAL CLAMP ESD PROTECTION

The following sections describe the standard single clamp ESD protection device and the dual clamp ESD protection architecture of the CM1231−02SO.

Single Clamp ESD Protection

Conceptually, an ESD protection device performs the following actions upon a strike of ESD discharge into the protected ASIC (see Figure 1).

1. When an ESD potential is applied to the system under test (contact or air−discharge), Kirchoff's Current Law (KCL) dictates that the Electrical Overstress (EOS) currents will immediately divide throughout the circuit, based on the dynamic impedance of each path
2. Ideally, the classic shunt ESD clamp will switch within 1 ns to a low−impedance path and return the majority of the EOS current to the chassis shield/reference ground. In actuality, if the ESD component's response time (t_{CLAMP}) is slower than the ASIC it is protecting, or if the Dynamic Resistance (R_{DYN}) is not significantly lower than the ASIC's I/O cell circuitry, then the ASIC will have to absorb a large amount of the EOS energy, and may be more likely to fail.
3. Subsequent to the ESD/EOS event, both devices must immediately return to their original specifications, ready for an additional strike. Any deterioration in parasitics or clamping capability should be considered a failure, as it can affect signal integrity or subsequent protection capability (this is known as "multi−strike" capability.)

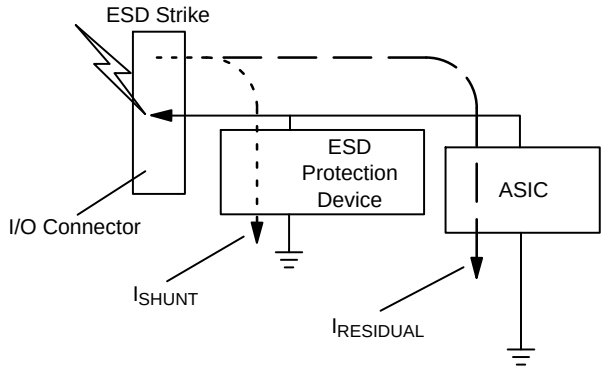


Figure 1. Single Clamp ESD Protection Block Diagram

Dual Clamp ESD Protection

In the CM1231−02SO dual clamp architecture, the first stage begins clamping immediately, as it does in the single clamp case. The dramatically reduced I_{RES} current from stage one passes through the 1 Ω series element and then gradually feeds into the stage two ESD device (see Figure 2). The series inductive and resistive elements further limit the current into the second stage, and greatly attenuate the resultant peak incident pulse presented at the ASIC side of the device.

This disconnection between the outside node and the inside ASIC node allows the stage one clamps to turn on and remain in the shunt mode before the ASIC begins to shunt the reduced residual pulse. This gives the advantage to the ESD component in the current division equation, and dramatically reduces the residual energy that the ASIC must dissipate.

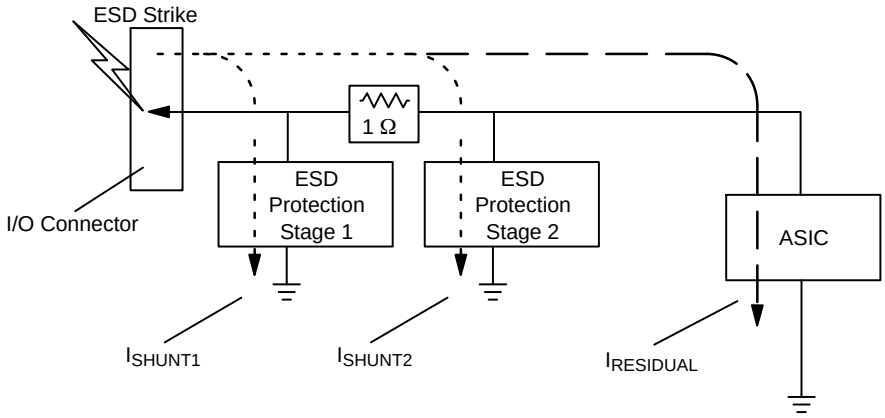


Figure 2. Dual Clamp ESD Protection Block Diagram

CM1231−02SO ARCHITECTURE OVERVIEW

The two−stage per channel matched clamp architecture with isolated clamp rails features a series element to radically reduce the residual ESD current (I_{RES}) that enters the ASIC under protection (see Figure 3). From stage 1 to stage 2, the signal lines go through matched dual 1 Ω resistors.

The function of the series element (dual 1 Ω resistors for the CM1231−02SO) is to optimize the operation of the stage two diodes to reduce the final I_{RES} current to a minimum while maintaining an acceptable insertion impedance that is negligible for the associated signaling levels.

Each stage consists of a traditional low−cap Dual Rail Clamp structure which steer the positive or negative ESD current pulse to either the positive (V_P) or negative (V_N) supply rail.

A zener diode is embedded between V_P and V_N, offering two advantages. First, it protects the V_{CC} rail against ESD strikes. Second, it eliminates the need for an additional bypass capacitor to shunt the positive ESD strikes to ground.

The CM1231−02SO therefore replaces as many as seven discrete components, while taking advantage of precision internal component matching for improved signal integrity, which is not otherwise possible with discrete components at the system level.

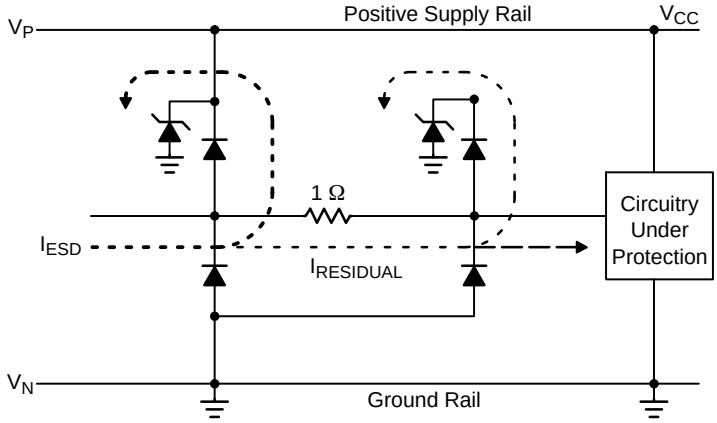


Figure 3. CM1231−02SO Block Diagram (I_{ESD} Flow During a Positive Strike)

Advantages of the CM1231−02SO Dual Stage ESD Protection Architecture

Figure 4 illustrates a single stage ESD protection device. The inductor element represents the parasitic inductance arising from the bond wire and the PCB trace leading to the ESD protection diodes.

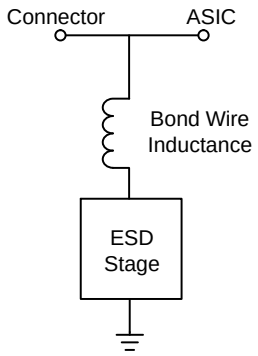


Figure 4. Single Stage ESD Protection Model

Figure 5 illustrates one of the two CM1231−02SO channels. Similarly, the inductor elements represent the parasitic inductance arising from the bond wire and PCB traces leading to the ESD protection diodes as well.

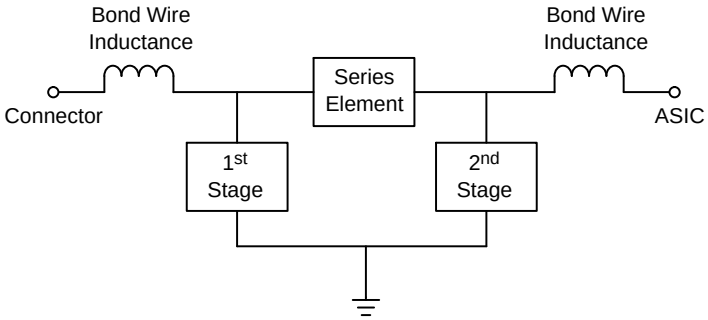


Figure 5. CM1231−02SO Dual Stage ESD Protection Model

CM1231−02SO Inductor Elements

In the CM1231−02SO dual stage architecture, the inductor elements and ESD protection diodes interact differently compared to the single stage model.

In the single stage model, the inductive element presents high impedance at high frequency, i.e. during an ESD strike. The impedance increases the resistance of the conduction path leading to the ESD protection element. This limits the speed that the ESD pulse can discharge through the single stage protection element.

The inductance elements are in series to the conduction path leading to the protected device. The elements actually help to limit the current and voltage striking the protected device.

The reactance of the series and the inductor elements in the second stage forces more of the ESD strike current to be shunted through the first stage. At the same time the voltage drop across series element helps to lower the clamping voltage at the protected terminal.

The inductor elements also tune the impedance of the stage by cancelling the capacitive load presented by the ESD diodes to the signal line. This improves the signal integrity and makes the ESD protection stages more transparent to the high bandwidth data signals passing through the channel.

The innovative architecture turns the disadvantages of the parasitic inductive elements into useful components that help to limit the ESD current strike to the protected device and also improves the signal integrity of the system by balancing the capacitive loading effects of the ESD diodes.

GRAPHICAL COMPARISON AND TEST SETUP

The following graphs (see Figure 6, Figure 7 and Figure 8) show that the CM1231−02SO (dual stage ESD protector) lowers the peak voltage and clamping voltage by 40% across a wide range of loading conditions in comparison to a standard single stage device. This data was derived using the test setups shown in Figure 9 and Figure 10.

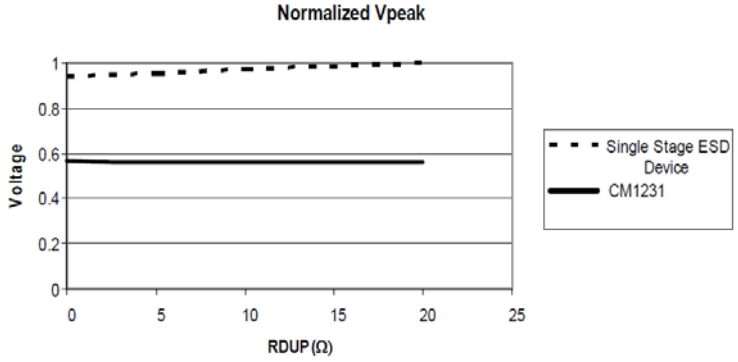


Figure 6. IEC 61000−4−2 Vpeak vs. Loading (RDUP*)

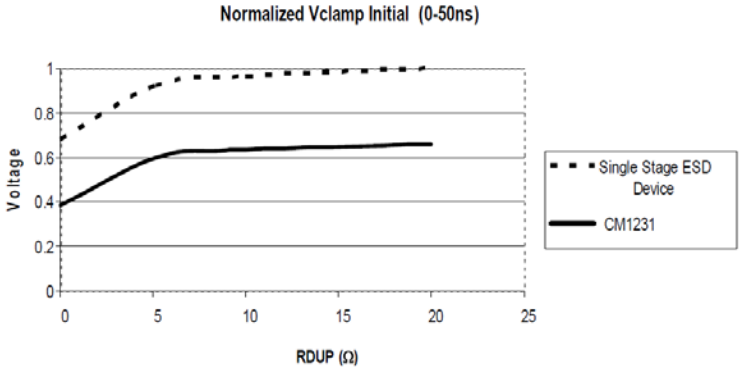


Figure 7. IEC 61000−4−2 Vclamp vs. Loading (RDUP*)

*RDUP indicates the amount of Resistance (load) supplied to the Device Under Protection (DUP) through a variable resistor.

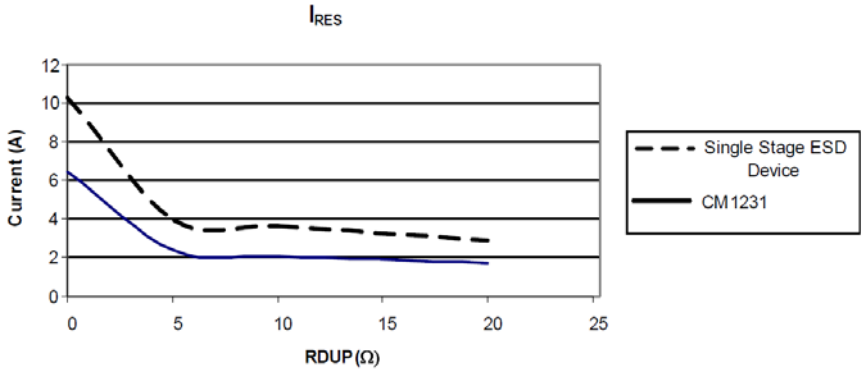


Figure 8. IEC 61000−4−2 I_{RES} (Residual ESD Peak Current) vs. Loading (RDUP)

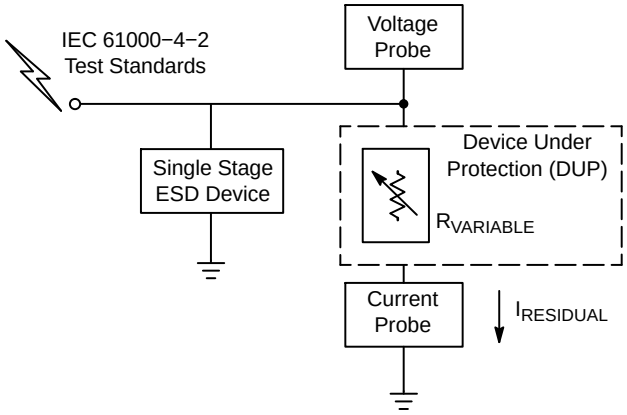


Figure 9. Single Stage ESD Device Test Setup

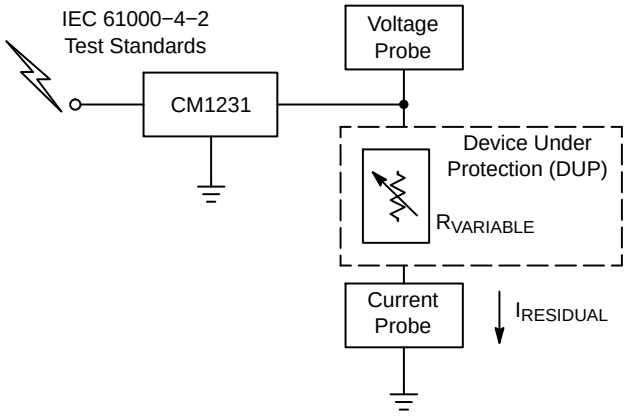


Figure 10. CM1231−02SO Test Setup

PERFORMANCE INFORMATION

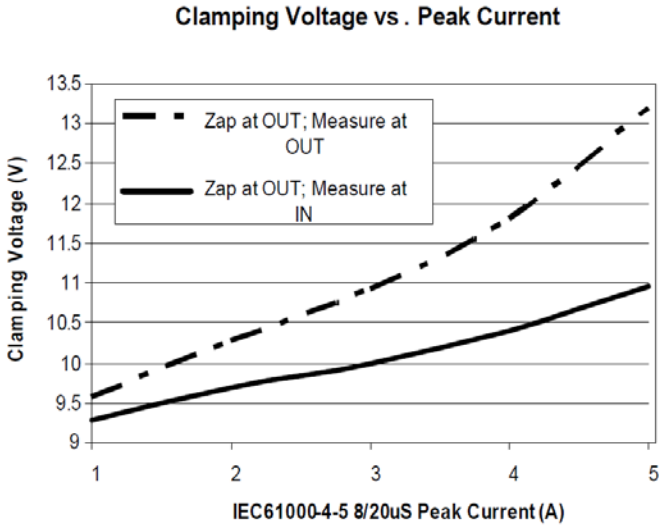


Figure 11. Clamping Voltage vs. Peak Current

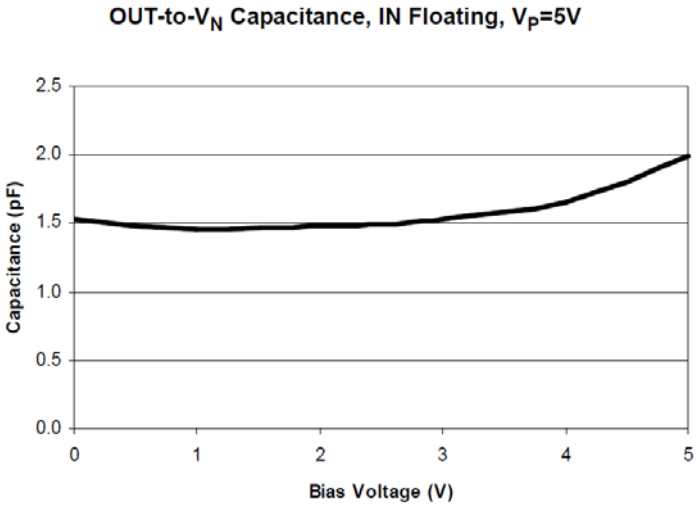


Figure 12. Capacitance vs. Bias Voltage

PERFORMANCE INFORMATION (Cont‘d)

Typical Filter Performance (Nominal Conditions unless Specified Otherwise, 0 V DC bias, 50 Ω Environment)

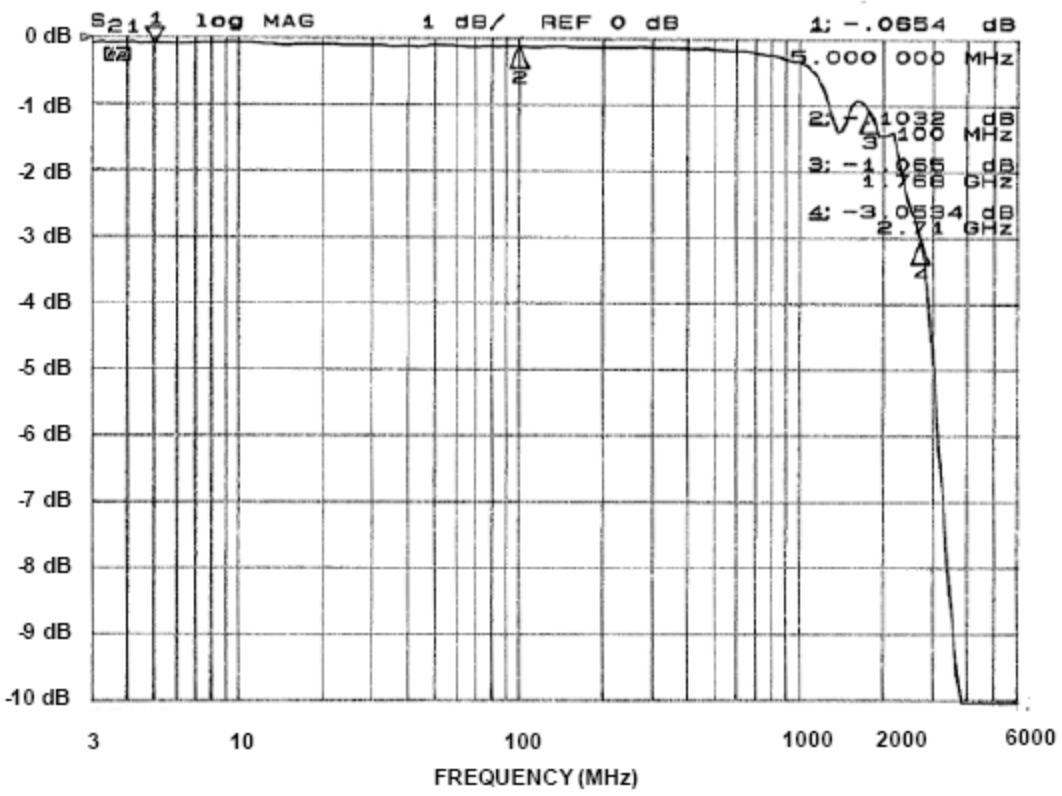


Figure 13. Typical Single−Ended S21 Plot (1 dB/div, 3 MHz to 6 GHz)

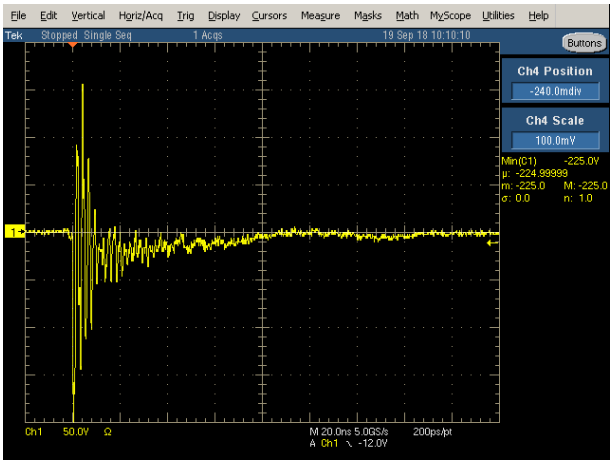


Figure 14. Negative 12 kV IEC

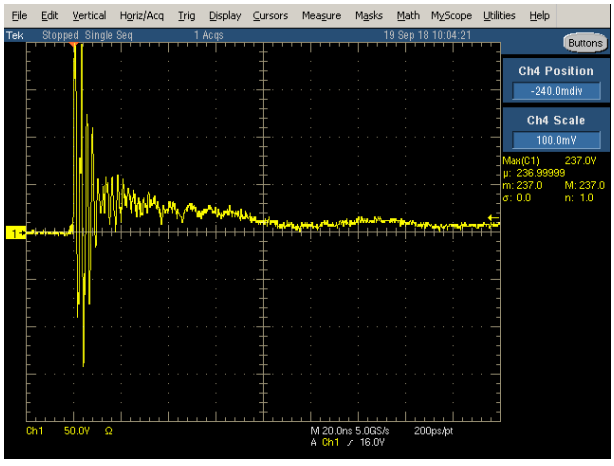


Figure 15. Positive 12 kV IEC

APPLICATION INFORMATION

CM1231−02SO Application and Guidelines

The CM1231−02SO has an integrated zener diode between V_P and V_N (for each of the two stages). This greatly reduces the effect of supply rail inductance L_2 on V_{CL} by clamping V_P at the breakdown voltage of the zener diode. However, for the lowest possible V_{CL}, especially when V_P is biased at a voltage significantly below the zener breakdown voltage, it is recommended that a 0.22 μF ceramic chip capacitor be connected between V_P and the ground plane.

With the CM1231−02SO, this additional bypass capacitor is generally not required.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

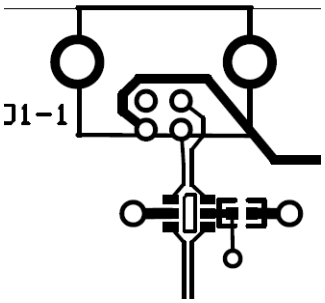


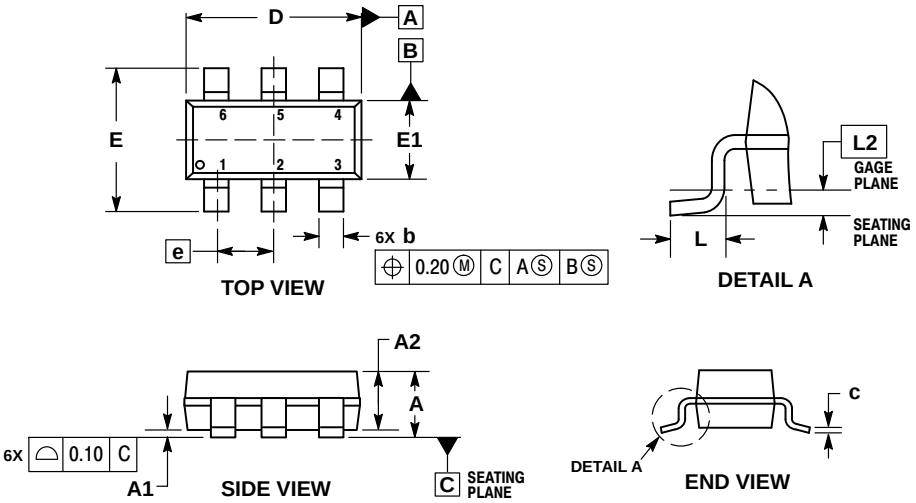
Figure 16. Typical Layout with Optional V_P Cap Footprint

Additional Information

See also ON Semiconductor Application Note, “Design Considerations for ESD Protection,” in the Applications section.

PACKAGE DIMENSIONS

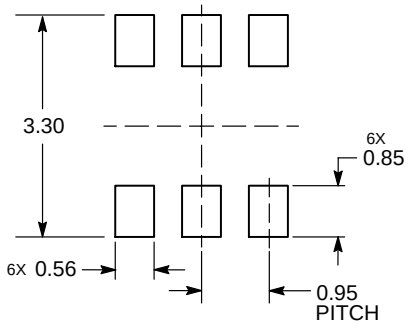
SOT−23, 6 Lead
CASE 527AJ
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.20	0.50
c	0.08	0.26
D	2.70	3.00
E	2.50	3.10
E1	1.30	1.80
e	0.95 BSC	
L	0.20	0.60
L2	0.25 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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