EVAL-CN0369SDPZ User Guide
UG-806

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the EVAL-CN0369SDPZ

FEATURES

- Self contained evaluation board including
  - ADF4002 PLL frequency synthesizer
  - AD8065 operational amplifier
  - HMC512 VCO 9.6 GHz to 10.8 GHz, with $f_{OUT}/2$
- Ultralow noise voltage regulators: ADP151 and ADM7150
- USB interface
- ADF4002 Integer-N software allows control of synthesizer functions from PC

ONLINE RESOURCES

- Documents Needed
  - ADF4002 data sheet
  - AD8065 data sheet
  - HMC512 data sheet
  - ADL5801 data sheet
  - ADF4355-2 data sheet
  - EV-ADF4355-2SD1Z user guide
- Required Software
  - ADF4002 Integer-N software
  - EV-ADF4355-2SD1Z evaluation software
- Design and Integration Files
  - Schematics, Layout Files, Bill of Materials

EQUIPMENT NEEDED

- A standard PC running Windows® XP, Windows Vista (32-bit), or Windows 7 with a USB port
- EVAL-CN0369SDPZ circuit evaluation board
- ADL5801-EVALZ circuit evaluation board
- EV-ADF4355-2SD1Z circuit evaluation board
- 2 EVAL-SDP-CS1Z evaluation boards
- A 400 MHz low pass filter
- A 100 MHz low pass filter
- 5.5 V, 5 V, and 12 V power supplies
- A signal source, such as the R&S® SMA100A signal generator
- A second signal source, such as the R&S SMA100A signal generator or a 100 MHz, low noise crystal
- A spectrum analyzer, such as the R&S FSUP signal source analyzer

GENERAL DESCRIPTION

The EVAL-CN0369SDPZ is the evaluation board described in CN-0369 and is shown in Figure 1. It contains the ADF4002 synthesizer, the AD8065 operational amplifier, HMC512 voltage controlled oscillator (VCO), and ultralow noise low dropout regulators (LDOs). Users can program the evaluation board using the ADF4002 Integer-N software. A USB cable is included with the evaluation board to connect to a PC USB port.

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REVISION HISTORY

12/2016—Revision 0: Initial Version

EVAL-CN0369SDPZ EVALUATION BOARD SETUP

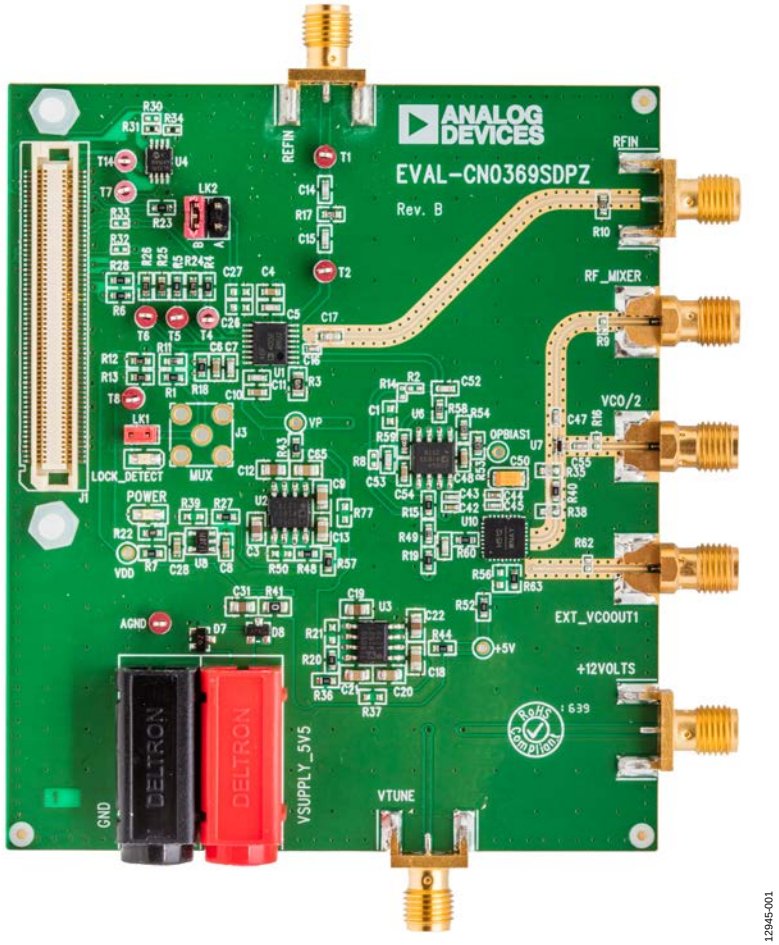

Figure 1.

EVALUATION BOARD HARDWARE

TRANSATION LOOP SYNTHESIZER

The translation loop synthesizer (also known as an offset loop) as the name implies, translates the lower 100 MHz reference frequency of the ADF4002 phase locked loop (PLL) up to a higher frequency range of 5.0 GHz to 5.4 GHz, as determined by the frequency of the local oscillator (LO). Figure 2 shows a translation loop evaluation setup using the EVAL-CN0369SDPZ.

POWER SUPPLIES

The user must apply 5.5 V to the VSUPPLY_5V5 power connectors (4 mm banana connectors) and +12 V to the SMA connector labeled +12VOLTS. The POWER on-board LED indicates when the EVAL-CN0369SDPZ is powered.

JUMPERS

Table 1 shows the required positions for Jumper LK1 and Jumper LK2 for normal operation.

Table 1. Jumper Positions

Jumper	Position
LK1	Inserted
LK2	B—normal operation
	A—hardware power-down

Jumper LK1 inserted enables the LOCK DETECT on-board LED.

RF OUTPUTS

The radio frequency (RF) output (VCO/2) and the fundamental VCO output (EXT_VCOOUT1) are ac-coupled to VCO/2 and EXT_VCOOUT1 SMA connectors, respectively. Set the RF output coupling to the spectrum analyzer must be set to 50 Ω.

ACTIVE LOOP FILTER AND CHARGE PUMP CURRENT

The default active loop filter is set to 1.1 MHz. Using a charge pump setting of 5 mA is recommended.

REFERENCE SOURCE AND FINE TUNING

An external reference using the REFIN SMA is the default reference source and fine tuning for the EVAL-CN0369SDPZ, provided by the ADF4355-2. To evaluate the EVAL-CN0369SDPZ, initially program the EV-ADF4355-2SD1Z to generate 100 MHz RF output frequency. Achieve fine tuning of the translation loop by changing the EV-ADF4355-2SD1Z output frequency incrementally. A loop bandwidth of 100 kHz is recommended to allow the ADF4355-2 to provide the fine tuning required. Insert a low pass filter between the RFOUTB+ SMA connector of the EV-ADF4355-2SD1Z and the REFIN SMA connector of the EVAL-CN0369SDPZ to filter the harmonics created by the output dividers. Terminate the unused RFOUTB– SMA connector on the EV-ADF4355-2SD1Z in 50 Ω.

The RFOUTBx SMA connector gives higher output power in comparison to RFOUTAx for lower output frequencies as it uses a higher value of pull-up inductor. Refer to the EV-ADF4355-2SD1Z user guide for details on evaluation board set-up and programming.

RFIN AND RF_MIXER AND COURSE TUNING

The ADL5801-EVALZ mixer evaluation board and a low noise signal generator provides the translation loop coarse tuning requirement.

Connect the low noise signal generator to the LO input of the ADL5801-EVALZ. Connect the RF_MIXER SMA connector from the EVAL-CN0369SDPZ to the RF input of the ADL5801-EVALZ. Connect the intermediate frequency (IF) output of the ADL5801-EVALZ to the RFIN SMA connector of the EVAL-CN0369SDPZ via a 400 MHz low pass filter. Consult the ADL5801 data sheet for details on using and connecting the ADL5801-EVALZ evaluation board.

Refer to the CN-0369 for a block diagram of the test setup of the EVAL-CN0369SDPZ, EV-ADF4355-2SD1Z, and ADL5801-EVALZ.

To evaluate the EVAL-CN0369SDPZ, initially program the signal generator to output 5.2 GHz with a power level of 0 dBm. Achieve coarse tuning of the translation loop by changing the output of the signal generator in increments of 100 MHz from 5.3 GHz to 4.9 GHz.

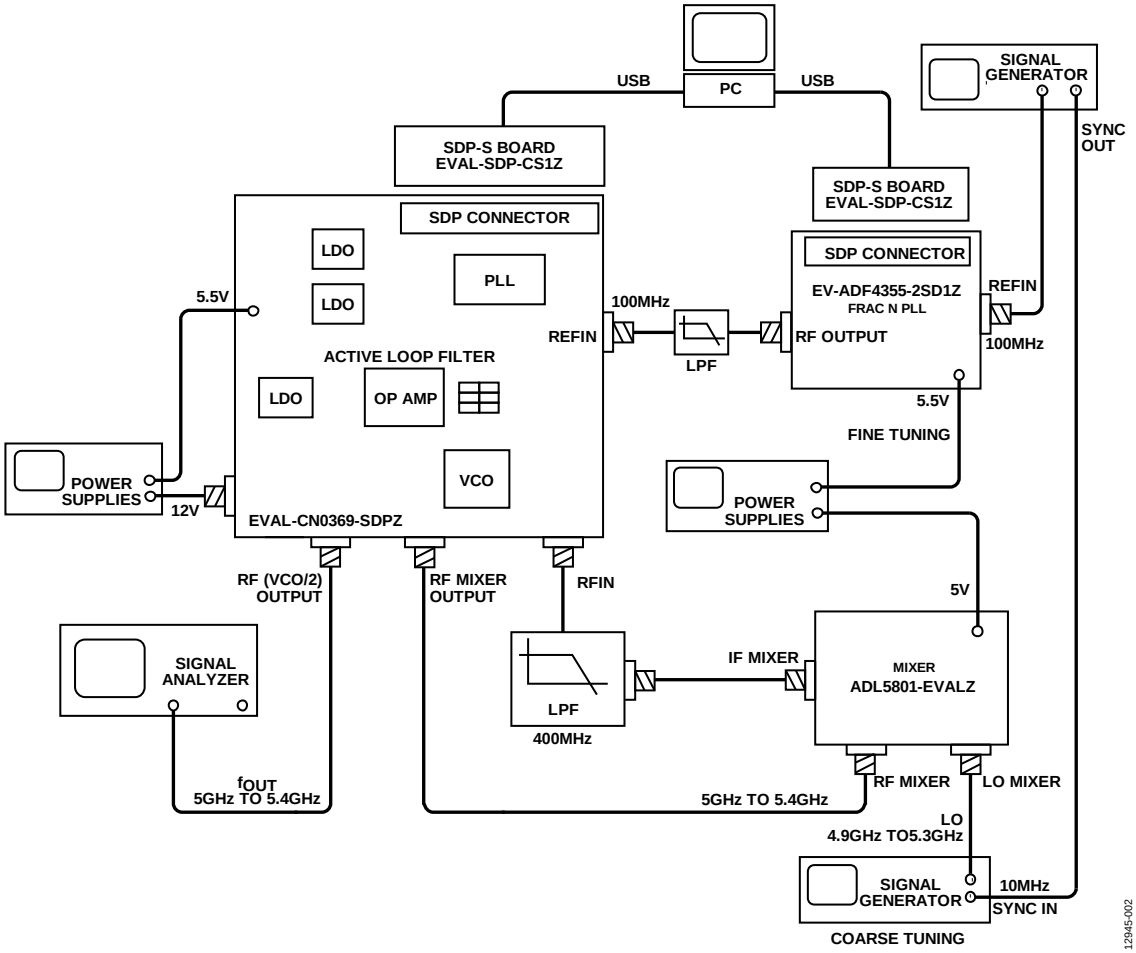

Figure 2. Translation Loop Evaluation Setup using the EVAL-CN0369SDPZ

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

The control software for EVAL-CN0369SDPZ uses the standard Integer-N programming software. For more details on the installation and use of the Integer-N programming software, consult the UG-476 user guide and the UG-161 user guide.

After installing the software, run the software by clicking the **Analog Devices Int-N PLL Software** file on the desktop or in the **Start** menu. The software main window opens (see Figure 3).

Confirm **SDP Board connected** displays in the bottom left corner of the window. Otherwise, the software has no connection to the evaluation board. In this case, check that the cable connection and USB drivers are correctly installed.

In the **Main Controls** tab (see Figure 4), program the **RF VCO Output Freq** to **100 MHz**, the **PFD Frequency** to **100 MHz**, the **Charge Pump Setting 1** and **Charge Pump Setting 2** to **5.0 mA**, and the **Phase Detector Polarity** to **Negative**.

Double-click on the **ANALOG DEVICES** logo to enable additional test modes. In the **Testmodes** drop down menu, select **Force Charge Pump Down** and update all registers (see Figure 4). Check that the VCO/2 output is free running at approximately 5.47 GHz.

Again, in the **Testmodes** drop down menu, select **Normal operation, 2.9 ns ABPW** and update all registers (see Figure 4). Check that the VCO/2 output is locked at 5.3 GHz. See Figure 5 for a phase noise plot at 5.3 GHz.

The translation loop cannot distinguish between the need for a ±ve change in VCO output frequency, therefore it is necessary to tune the loop in one direction only, hence the need to manually force the VCO output frequency to 5.47 GHz (top of tuning range), before operating in normal operation. Coarse tuning of the translation loop can then be performed by the local oscillator input to the mixer, and finely tuned by the reference input to the EVAL-CN0369SDPZ. Tuning must always be in one direction, for example, in this user guide, the VCO frequency is always tuned from the top of the VCO tuning range to the required frequency.

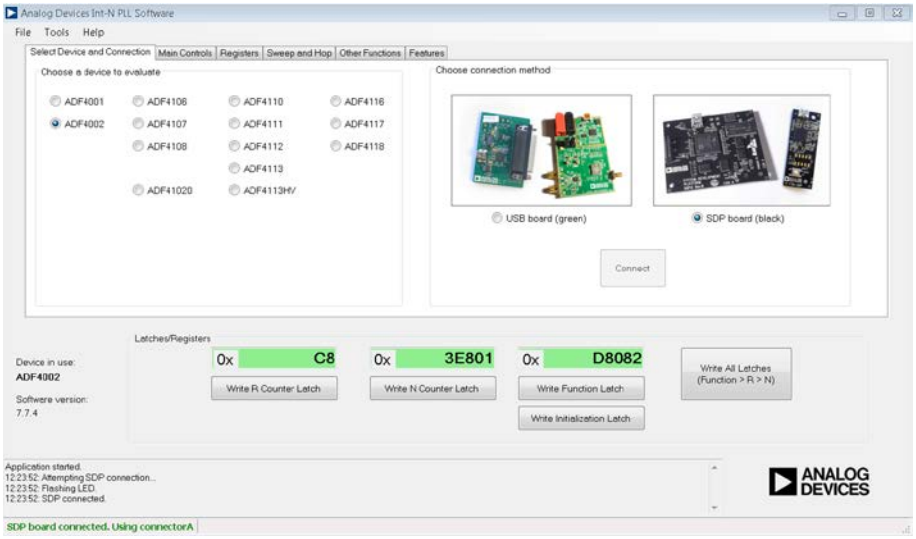

Figure 3. ***Select Device and Connection*** *Tab*

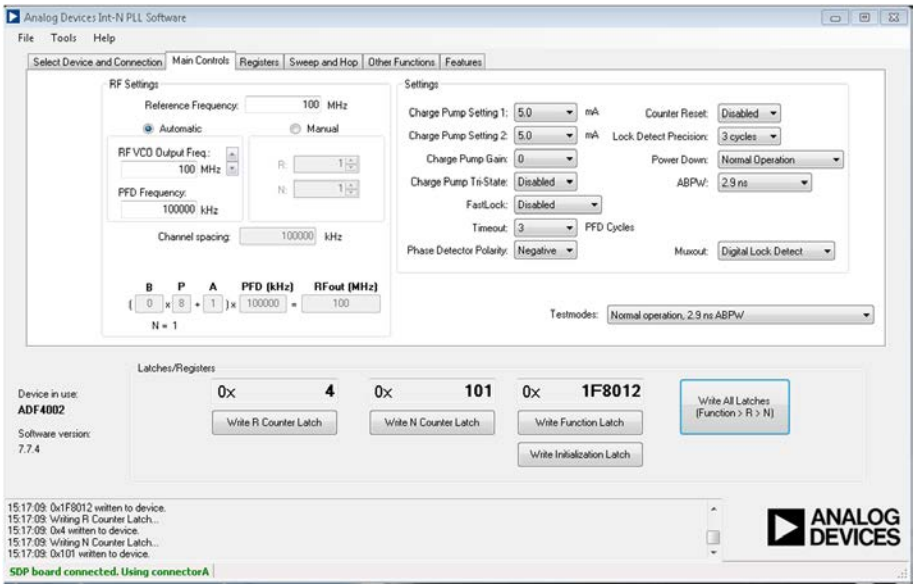

*Figure 4. **Main Controls** Tab*

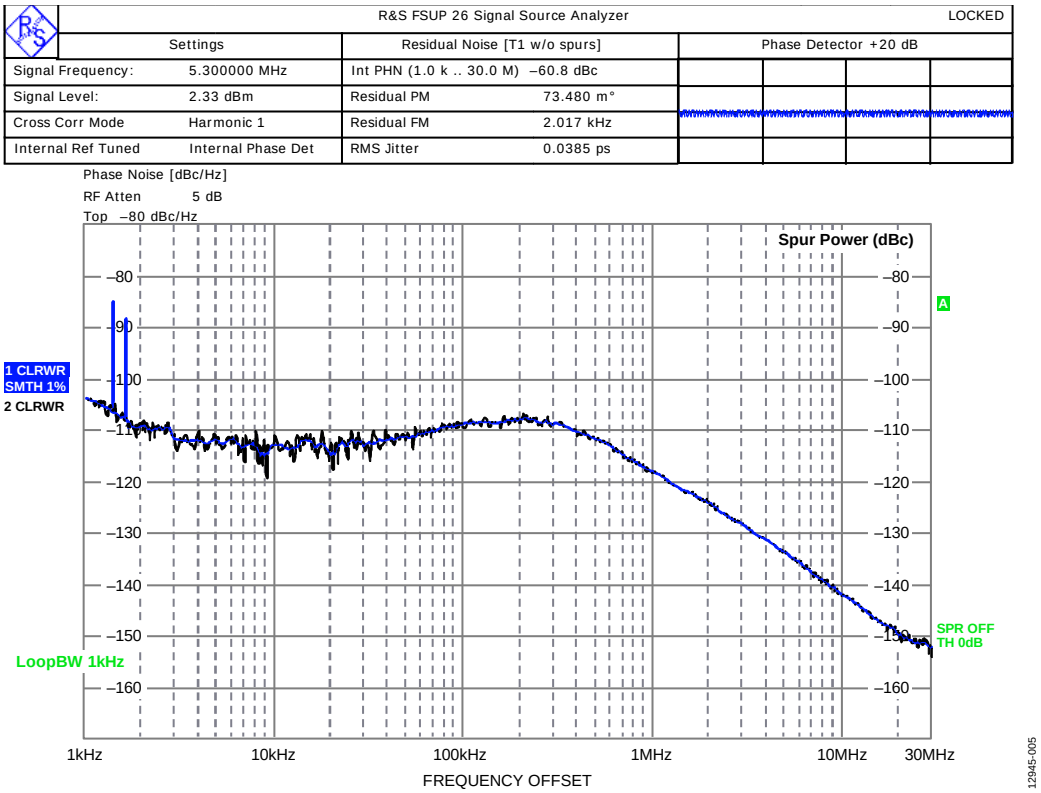

Figure 5. Translation Loop Output Frequency (f_{OUT}) Phase Noise Plot

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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