NXP Semiconductors
Data Sheet: Technical Data

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T2081

QorIQ T2081 Data Sheet

Features

- 4 e6500 cores built on Power Architecture® technology sharing a 2 MB L2 cache
- 512 KB CoreNet platform cache (CPC)
- Hierarchical interconnect fabric
  - CoreNet fabric supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet end-points
  - Queue Manager (QMan) fabric supporting packet-level queue management and quality of service scheduling
- One 32-/64-bit DDR3 SDRAM memory controller
  - DDR3 and DDR3L with ECC and interleaving support
  - Memory pre-fetch engine
- Data Path Acceleration Architecture (DPAA) incorporating acceleration for the following functions:
  - Packet parsing, classification, and distribution (Frame Manager 1.1)
  - Queue management for scheduling, packet sequencing, and congestion management (Queue Manager 1.1)
  - Hardware buffer management for buffer allocation and de-allocation (Buffer Manager 1.1)
  - Cryptography Acceleration (SEC 5.2)
  - RegEx Pattern Matching Acceleration (PME 2.1)
  - Decompression/Compression Acceleration (DCE 1.0)
- 8 SerDes lanes at up to 10 GHz
- 6 Ethernet interfaces, supporting combinations of:
  - Up to two 10 Gbps Ethernet MACs
  - Up to six 1 Gbps Ethernet MACs
  - Up to two 2.5Gbps Ethernet MACs
  - IEEE Std 1588™ support
- High-speed peripheral interfaces
  - Four PCI Express controllers (two support PCIe 2.0 and two support PCIe 3.0)
- Additional peripheral interfaces
  - Two high-speed USB 2.0 controllers with integrated PHY
  - Enhanced secure digital host controller (SD/MMC/eMMC)
  - Enhanced Serial peripheral interface (eSPI)
  - Four I2C controllers
  - Four 2-pin UARTs or two 4-pin UARTs
  - Integrated flash controller supporting NAND and NOR flash
- Three 8-channel DMA engines
- 780 FC-PBGA package, 23 mm x 23 mm, 0.8mm pitch

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1 Overview

The T2081 QorIQ integrated multicore communications processor combines 4 dual-threaded cores built on Power Architecture® technology with high-performance data path acceleration and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and military/aerospace applications.

This chip can be used for combined control, data path, and application layer processing in routers, switches, gateways, and general-purpose embedded computing systems. Its high level of integration offers significant performance benefits compared to multiple discrete devices, while also simplifying board design.

This figure shows the block diagram of the chip.

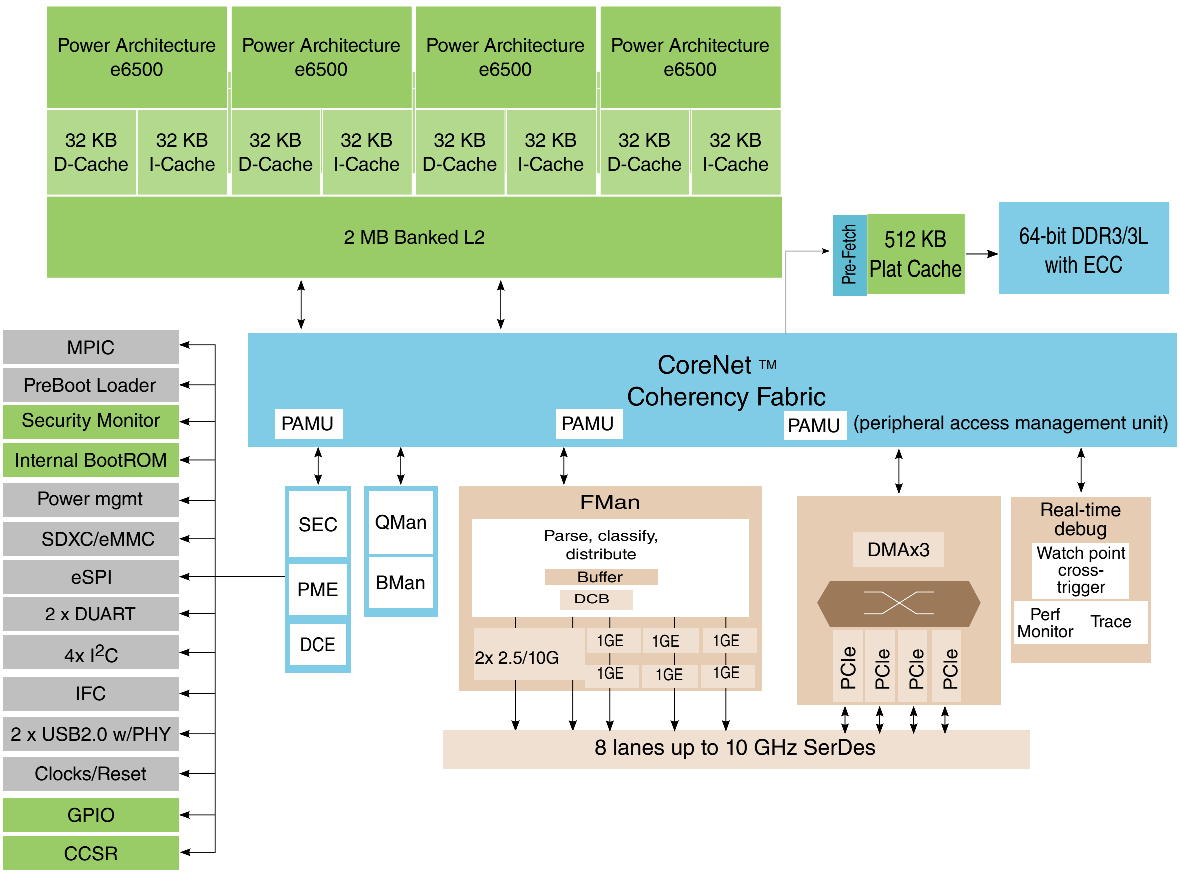


Figure 1. Block diagram

2 Pin assignments

2.1 784 ball layout diagrams

This figure shows the complete view of the T2081 ball map diagram. Figure 3, Figure 4, Figure 5, and Figure 6 show quadrant views.

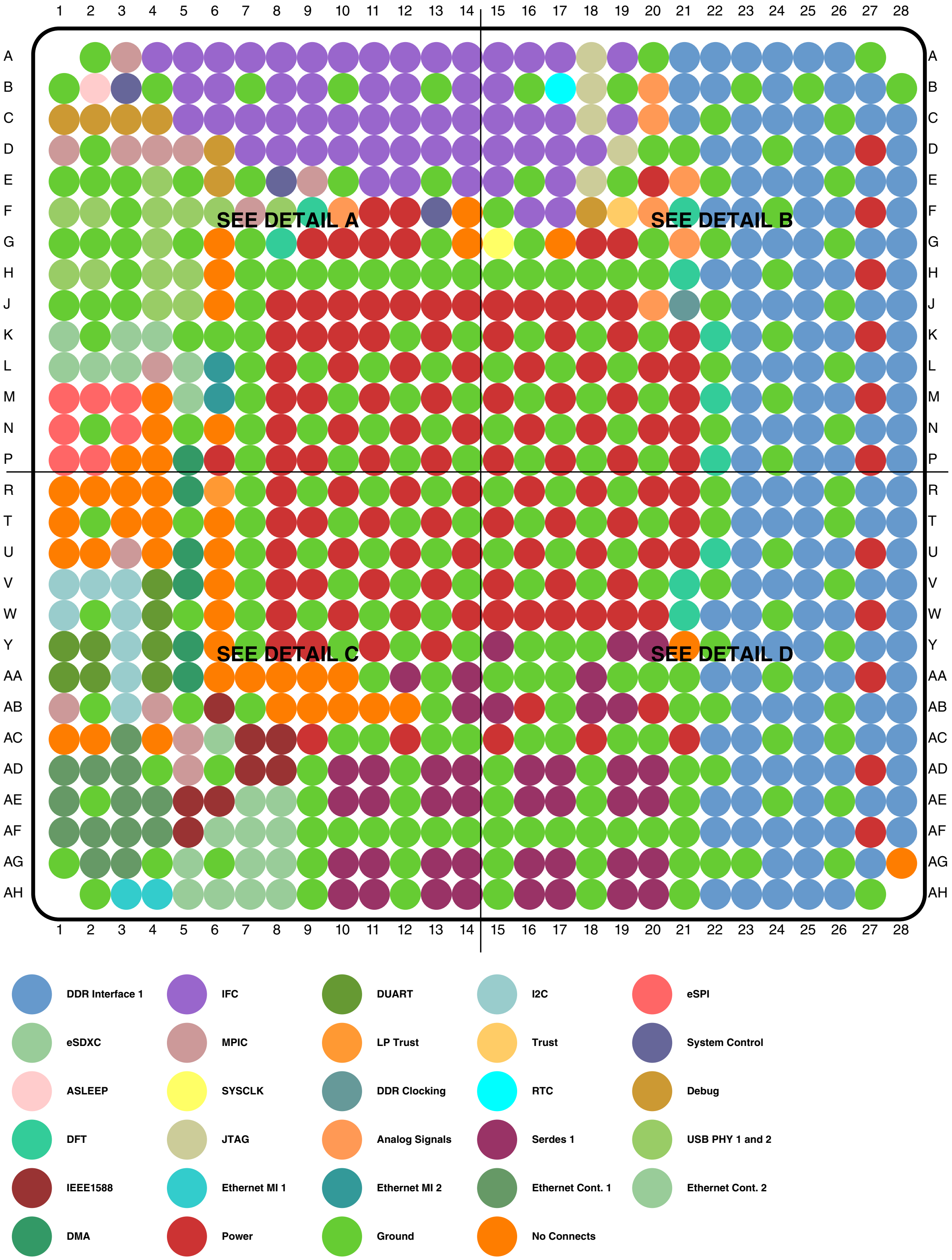


Figure 2. Complete BGA Map for the T2081

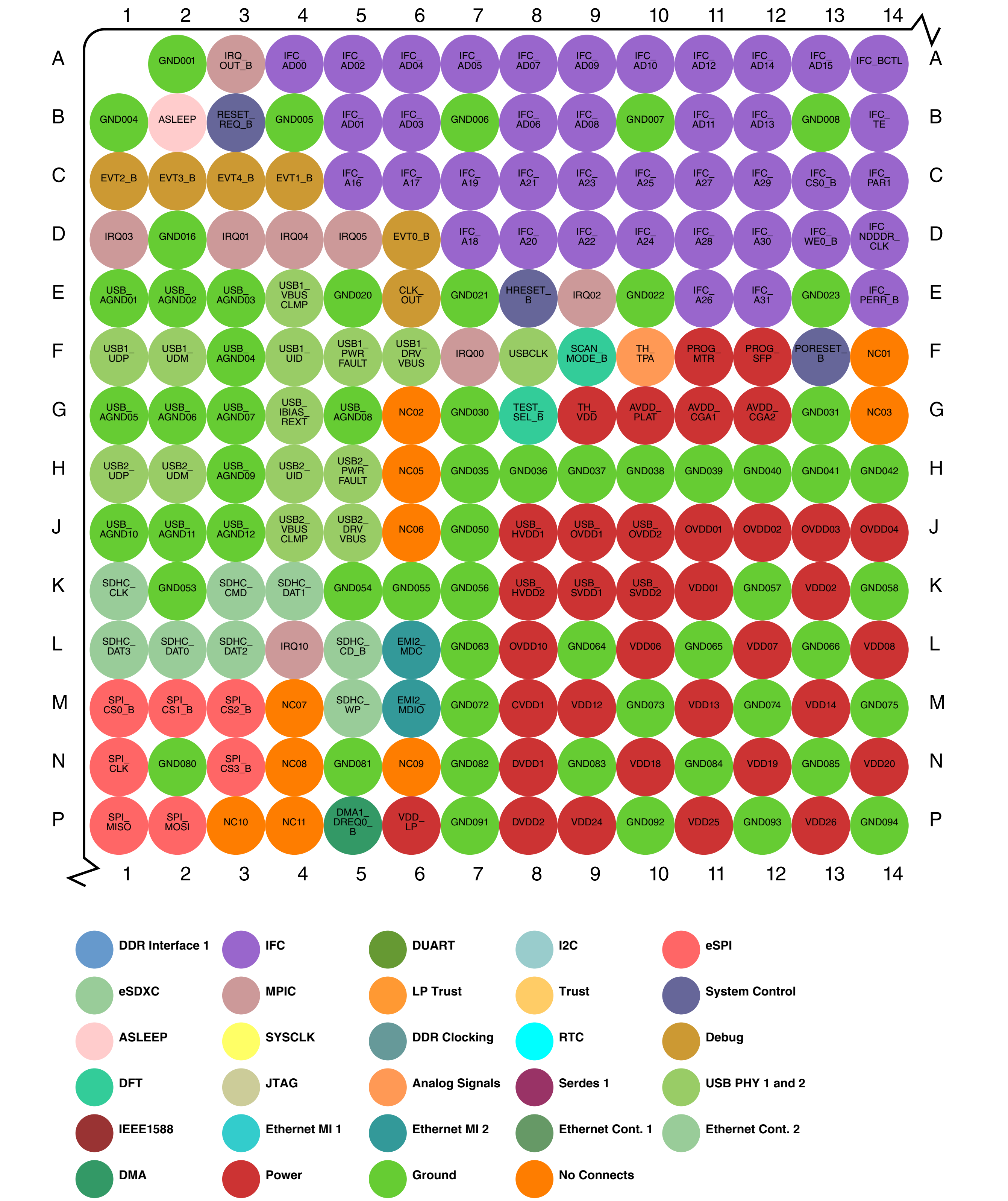


Figure 3. Detail A

	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
A	IFC_RB1_B	IFC_NDDQS	IFC_CLK0	TDI	IFC_CLK1	GND002	D1_MDQ05	D1_MDQ01	D1_MDQS0_B	D1_MDQS0	D1_MDQ07	D1_MDQ02	GND003		A
B	IFC_RB0_B	GND009	RTC	TMS	GND010	FA_ANALOG_PIN	D1_MDQ04	D1_MDM0	GND011	D1_MDQ06	GND012	D1_MDQ03	D1_MDQ14	GND013	B
C	IFC_PAR0	IFC_CS3_B	IFC_CS5_B	TDO	IFC_CS7_B	FA_ANALOG_G_V	D1_MDQ00	GND014	D1_MDQ08	D1_MDQ09	D1_MDM1	GND015	D1_MCKE0	D1_MCKE1	C
D	IFC_OE_B	IFC_CS2_B	IFC_AVD	IFC_CS6_B	TRST_B	GND017	GND018	D1_MDQ12	D1_MDQ13	GND019	D1_MDQS1_B	D1_MDQS1	G1VDD01	D1_MA15	D
E	IFC_CS1_B	GND024	IFC_CS4_B	TCK	GND025	AVDD_D1	TD1_ANODE	GND026	D1_MDQ16	D1_MDQ17	D1_MDQ15	GND027	D1_MA14	D1_MBA2	E
F	GND028	IFC_CLE	IFC_WP0_B	CKSTP_OUT_B	TMP_DETECT_B	D1_MVREF	TEST_OUT1	D1_MDQ20	D1_MDM2	GND029	D1_MDQ10	D1_MDQ11	G1VDD02	D1_MAPAR_ERR_B	F
G	SYSCLK	GND032	NC04	FA_VL	SENSE_VDD	SENSE_GND	TD1_CATHODE	GND033	D1_MDQS2_B	D1_MDQS2	D1_MDQ28	GND034	D1_MA09	D1_MA12	G
H	GND043	GND044	GND045	GND046	GND047	GND048	TEST_OUT0	D1_MDQ21	D1_MDQ22	GND049	D1_MDQ29	D1_MDQ24	G1VDD03	D1_MA11	H
J	OVDD05	OVDD06	OVDD07	OVDD08	OVDD09	D1_TPA	DDRCLK	GND051	D1_MDQ18	D1_MDQ23	D1_MDQ25	GND052	D1_MA08	D1_MA07	J
K	VDD03	GND059	VDD04	GND060	VDD05	GND061	G1VDD04	TEST_OUT4	D1_MDQ19	GND062	D1_MDQS3_B	D1_MDM3	G1VDD05	D1_MA06	K
L	GND067	VDD09	GND068	VDD10	GND069	VDD11	G1VDD06	GND070	D1_MECC4	D1_MECC0	D1_MDQS3	GND071	D1_MA04	D1_MA05	L
M	VDD15	GND076	VDD16	GND077	VDD17	GND078	G1VDD07	TEST_OUT5	D1_MECC5	GND079	D1_MDQ31	D1_MDQ30	G1VDD08	D1_MA03	M
N	GND086	VDD21	GND087	VDD22	GND088	VDD23	G1VDD09	GND089	D1_MECC1	D1_MDM8	D1_MDQ27	GND090	D1_MA02	D1_MA01	N
P	VDD27	GND095	VDD28	GND096	VDD29	GND097	G1VDD10	TEST_OUT7	D1_MDQS8_B	GND098	D1_MDQ36	D1_MDQ26	G1VDD11	D1_MDIC0	P
	15	16	17	18	19	20	21	22	23	24	25	26	27	28	

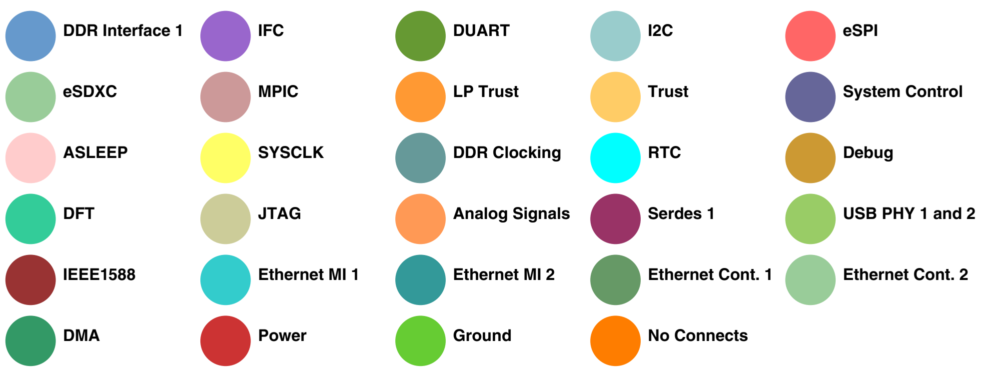


Figure 4. Detail B

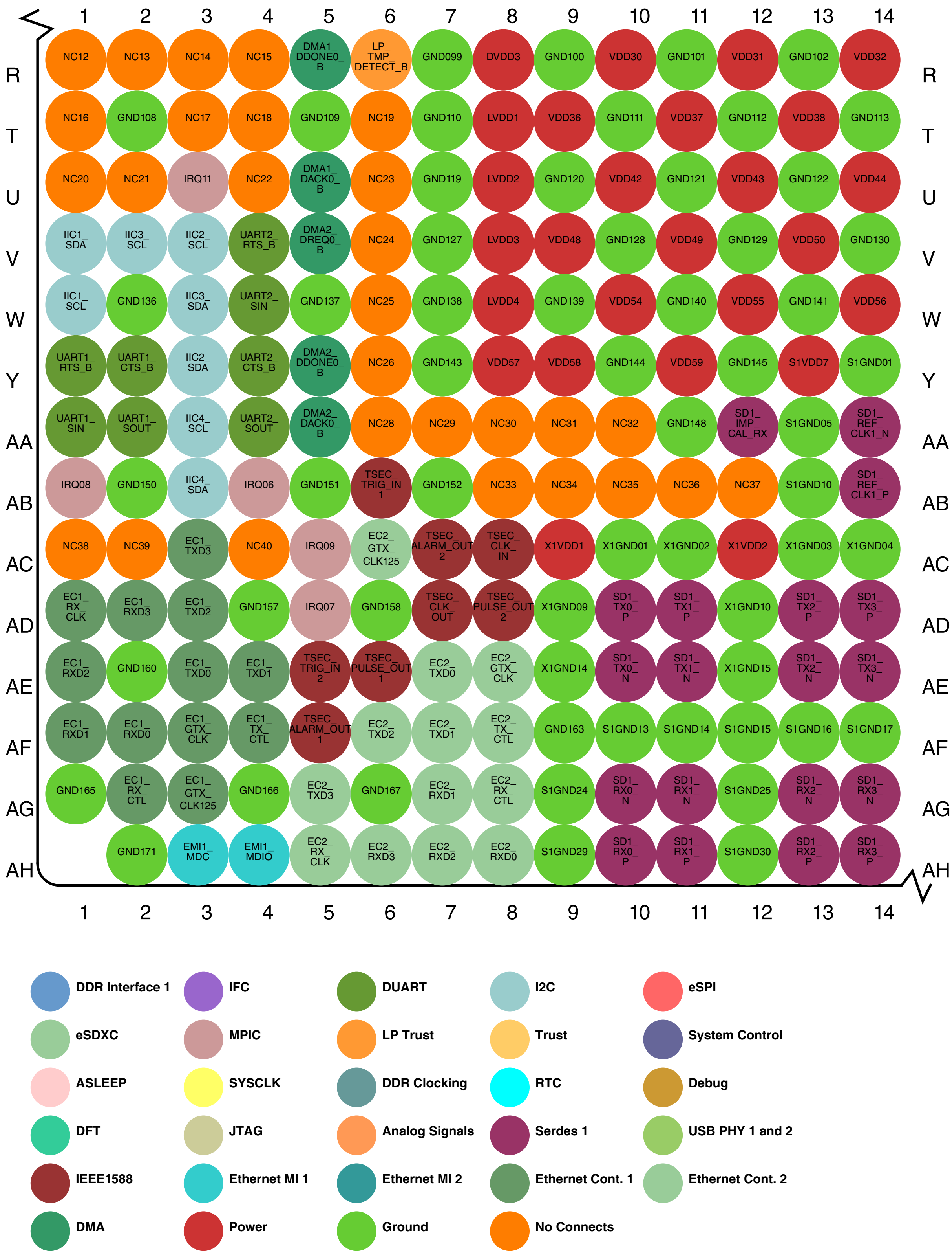


Figure 5. Detail C

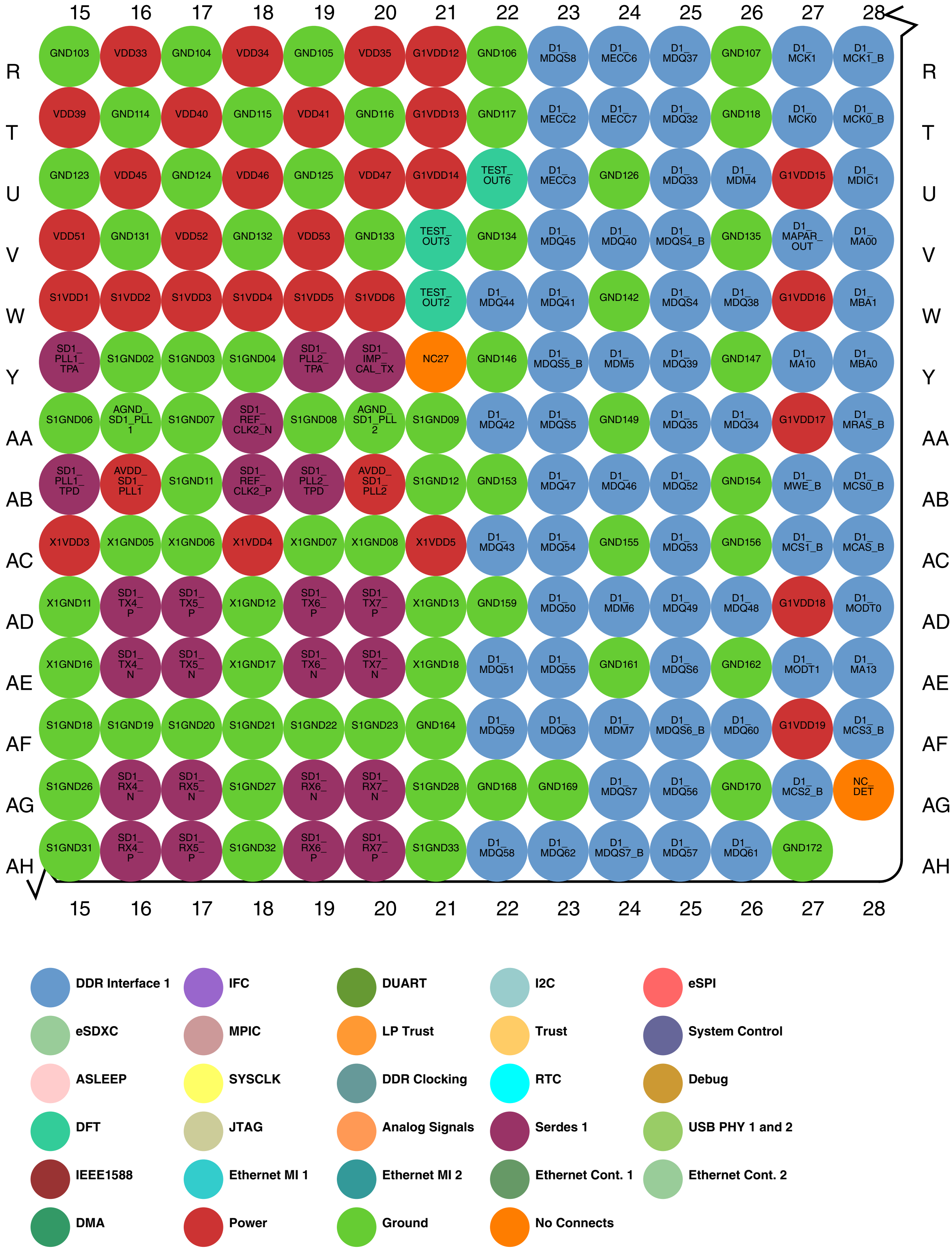


Figure 6. Detail D

2.2 Pinout list

This table provides the pinout listing for the T2081 by bus. Primary functions are **bolded** in the table.

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
D1_MA00	Address	V28	O	$G1V_{DD}$	---
D1_MA01	Address	N28	O	$G1V_{DD}$	---
D1_MA02	Address	N27	O	$G1V_{DD}$	---
D1_MA03	Address	M28	O	$G1V_{DD}$	---
D1_MA04	Address	L27	O	$G1V_{DD}$	---
D1_MA05	Address	L28	O	$G1V_{DD}$	---
D1_MA06	Address	K28	O	$G1V_{DD}$	---
D1_MA07	Address	J28	O	$G1V_{DD}$	---
D1_MA08	Address	J27	O	$G1V_{DD}$	---
D1_MA09	Address	G27	O	$G1V_{DD}$	---
D1_MA10	Address	Y27	O	$G1V_{DD}$	---
D1_MA11	Address	H28	O	$G1V_{DD}$	---
D1_MA12	Address	G28	O	$G1V_{DD}$	---
D1_MA13	Address	AE28	O	$G1V_{DD}$	---
D1_MA14	Address	E27	O	$G1V_{DD}$	---
D1_MA15	Address	D28	O	$G1V_{DD}$	---
D1_MAPAR_ERR_B	Address Parity Error	F28	I	$G1V_{DD}$	1, 6
D1_MAPAR_OUT	Address Parity Out	V27	O	$G1V_{DD}$	---
D1_MBA0	Bank Select	Y28	O	$G1V_{DD}$	---
D1_MBA1	Bank Select	W28	O	$G1V_{DD}$	---
D1_MBA2	Bank Select	E28	O	$G1V_{DD}$	---
D1_MCAS_B	Column Address Strobe	AC28	O	$G1V_{DD}$	---
D1_MCK0	Clock	T27	O	$G1V_{DD}$	---
D1_MCK0_B	Clock Complement	T28	O	$G1V_{DD}$	---
D1_MCK1	Clock	R27	O	$G1V_{DD}$	---
D1_MCK1_B	Clock Complement	R28	O	$G1V_{DD}$	---
D1_MCKE0	Clock Enable	C27	O	$G1V_{DD}$	2
D1_MCKE1	Clock Enable	C28	O	$G1V_{DD}$	2
D1_MCS0_B	Chip Select	AB28	O	$G1V_{DD}$	---
D1_MCS1_B	Chip Select	AC27	O	$G1V_{DD}$	---
D1_MCS2_B	Chip Select	AG27	O	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MCS3_B	Chip Select	AF28	O	$G1V_{DD}$	---
D1_MDIC0	Driver Impedence Calibration	P28	IO	$G1V_{DD}$	3
D1_MDIC1	Driver Impedence Calibration	U28	IO	$G1V_{DD}$	3
D1_MDM0	Data Mask	B22	O	$G1V_{DD}$	---
D1_MDM1	Data Mask	C25	O	$G1V_{DD}$	---
D1_MDM2	Data Mask	F23	O	$G1V_{DD}$	---
D1_MDM3	Data Mask	K26	O	$G1V_{DD}$	---
D1_MDM4	Data Mask	U26	O	$G1V_{DD}$	---
D1_MDM5	Data Mask	Y24	O	$G1V_{DD}$	---
D1_MDM6	Data Mask	AD24	O	$G1V_{DD}$	---
D1_MDM7	Data Mask	AF24	O	$G1V_{DD}$	---
D1_MDM8	Data Mask	N24	O	$G1V_{DD}$	---
D1_MDQ00	Data	C21	IO	$G1V_{DD}$	---
D1_MDQ01	Data	A22	IO	$G1V_{DD}$	---
D1_MDQ02	Data	A26	IO	$G1V_{DD}$	---
D1_MDQ03	Data	B26	IO	$G1V_{DD}$	---
D1_MDQ04	Data	B21	IO	$G1V_{DD}$	---
D1_MDQ05	Data	A21	IO	$G1V_{DD}$	---
D1_MDQ06	Data	B24	IO	$G1V_{DD}$	---
D1_MDQ07	Data	A25	IO	$G1V_{DD}$	---
D1_MDQ08	Data	C23	IO	$G1V_{DD}$	---
D1_MDQ09	Data	C24	IO	$G1V_{DD}$	---
D1_MDQ10	Data	F25	IO	$G1V_{DD}$	---
D1_MDQ11	Data	F26	IO	$G1V_{DD}$	---
D1_MDQ12	Data	D22	IO	$G1V_{DD}$	---
D1_MDQ13	Data	D23	IO	$G1V_{DD}$	---
D1_MDQ14	Data	B27	IO	$G1V_{DD}$	---
D1_MDQ15	Data	E25	IO	$G1V_{DD}$	---
D1_MDQ16	Data	E23	IO	$G1V_{DD}$	---
D1_MDQ17	Data	E24	IO	$G1V_{DD}$	---
D1_MDQ18	Data	J23	IO	$G1V_{DD}$	---
D1_MDQ19	Data	K23	IO	$G1V_{DD}$	---
D1_MDQ20	Data	F22	IO	$G1V_{DD}$	---
D1_MDQ21	Data	H22	IO	$G1V_{DD}$	---
D1_MDQ22	Data	H23	IO	$G1V_{DD}$	---
D1_MDQ23	Data	J24	IO	$G1V_{DD}$	---
D1_MDQ24	Data	H26	IO	$G1V_{DD}$	---
D1_MDQ25	Data	J25	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ26	Data	P26	IO	$G1V_{DD}$	---
D1_MDQ27	Data	N25	IO	$G1V_{DD}$	---
D1_MDQ28	Data	G25	IO	$G1V_{DD}$	---
D1_MDQ29	Data	H25	IO	$G1V_{DD}$	---
D1_MDQ30	Data	M26	IO	$G1V_{DD}$	---
D1_MDQ31	Data	M25	IO	$G1V_{DD}$	---
D1_MDQ32	Data	T25	IO	$G1V_{DD}$	---
D1_MDQ33	Data	U25	IO	$G1V_{DD}$	---
D1_MDQ34	Data	AA26	IO	$G1V_{DD}$	---
D1_MDQ35	Data	AA25	IO	$G1V_{DD}$	---
D1_MDQ36	Data	P25	IO	$G1V_{DD}$	---
D1_MDQ37	Data	R25	IO	$G1V_{DD}$	---
D1_MDQ38	Data	W26	IO	$G1V_{DD}$	---
D1_MDQ39	Data	Y25	IO	$G1V_{DD}$	---
D1_MDQ40	Data	V24	IO	$G1V_{DD}$	---
D1_MDQ41	Data	W23	IO	$G1V_{DD}$	---
D1_MDQ42	Data	AA22	IO	$G1V_{DD}$	---
D1_MDQ43	Data	AC22	IO	$G1V_{DD}$	---
D1_MDQ44	Data	W22	IO	$G1V_{DD}$	---
D1_MDQ45	Data	V23	IO	$G1V_{DD}$	---
D1_MDQ46	Data	AB24	IO	$G1V_{DD}$	---
D1_MDQ47	Data	AB23	IO	$G1V_{DD}$	---
D1_MDQ48	Data	AD26	IO	$G1V_{DD}$	---
D1_MDQ49	Data	AD25	IO	$G1V_{DD}$	---
D1_MDQ50	Data	AD23	IO	$G1V_{DD}$	---
D1_MDQ51	Data	AE22	IO	$G1V_{DD}$	---
D1_MDQ52	Data	AB25	IO	$G1V_{DD}$	---
D1_MDQ53	Data	AC25	IO	$G1V_{DD}$	---
D1_MDQ54	Data	AC23	IO	$G1V_{DD}$	---
D1_MDQ55	Data	AE23	IO	$G1V_{DD}$	---
D1_MDQ56	Data	AG25	IO	$G1V_{DD}$	---
D1_MDQ57	Data	AH25	IO	$G1V_{DD}$	---
D1_MDQ58	Data	AH22	IO	$G1V_{DD}$	---
D1_MDQ59	Data	AF22	IO	$G1V_{DD}$	---
D1_MDQ60	Data	AF26	IO	$G1V_{DD}$	---
D1_MDQ61	Data	AH26	IO	$G1V_{DD}$	---
D1_MDQ62	Data	AH23	IO	$G1V_{DD}$	---
D1_MDQ63	Data	AF23	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQS0	Data Strobe	A24	IO	$G1V_{DD}$	---
D1_MDQS0_B	Data Strobe	A23	IO	$G1V_{DD}$	---
D1_MDQS1	Data Strobe	D26	IO	$G1V_{DD}$	---
D1_MDQS1_B	Data Strobe	D25	IO	$G1V_{DD}$	---
D1_MDQS2	Data Strobe	G24	IO	$G1V_{DD}$	---
D1_MDQS2_B	Data Strobe	G23	IO	$G1V_{DD}$	---
D1_MDQS3	Data Strobe	L25	IO	$G1V_{DD}$	---
D1_MDQS3_B	Data Strobe	K25	IO	$G1V_{DD}$	---
D1_MDQS4	Data Strobe	W25	IO	$G1V_{DD}$	---
D1_MDQS4_B	Data Strobe	V25	IO	$G1V_{DD}$	---
D1_MDQS5	Data Strobe	AA23	IO	$G1V_{DD}$	---
D1_MDQS5_B	Data Strobe	Y23	IO	$G1V_{DD}$	---
D1_MDQS6	Data Strobe	AE25	IO	$G1V_{DD}$	---
D1_MDQS6_B	Data Strobe	AF25	IO	$G1V_{DD}$	---
D1_MDQS7	Data Strobe	AG24	IO	$G1V_{DD}$	---
D1_MDQS7_B	Data Strobe	AH24	IO	$G1V_{DD}$	---
D1_MDQS8	Data Strobe	R23	IO	$G1V_{DD}$	---
D1_MDQS8_B	Data Strobe	P23	IO	$G1V_{DD}$	---
D1_MECC0	Error Correcting Code	L24	IO	$G1V_{DD}$	---
D1_MECC1	Error Correcting Code	N23	IO	$G1V_{DD}$	---
D1_MECC2	Error Correcting Code	T23	IO	$G1V_{DD}$	---
D1_MECC3	Error Correcting Code	U23	IO	$G1V_{DD}$	---
D1_MECC4	Error Correcting Code	L23	IO	$G1V_{DD}$	---
D1_MECC5	Error Correcting Code	M23	IO	$G1V_{DD}$	---
D1_MECC6	Error Correcting Code	R24	IO	$G1V_{DD}$	---
D1_MECC7	Error Correcting Code	T24	IO	$G1V_{DD}$	---
D1_MODT0	On Die Termination	AD28	O	$G1V_{DD}$	2
D1_MODT1	On Die Termination	AE27	O	$G1V_{DD}$	2
D1_MRAS_B	Row Address Strobe	AA28	O	$G1V_{DD}$	---
D1_MWE_B	Write Enable	AB27	O	$G1V_{DD}$	---
Integrated Flash Controller					
IFC_A16	IFC Address	C5	O	OV_{DD}	1, 5
IFC_A17	IFC Address	C6	O	OV_{DD}	1, 5
IFC_A18	IFC Address	D7	O	OV_{DD}	1, 5
IFC_A19	IFC Address	C7	O	OV_{DD}	1, 5
IFC_A20	IFC Address	D8	O	OV_{DD}	1, 5
IFC_A21/cfg_dram_type	IFC Address	C8	O	OV_{DD}	1, 4
IFC_A22	IFC Address	D9	O	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_A23	IFC Address	C9	O	OV_{DD}	1
IFC_A24	IFC Address	D10	O	OV_{DD}	1
IFC_A25/GPIO2_25/ IFC_WP1_B	IFC Address	C10	O	OV_{DD}	1
IFC_A26/GPIO2_26/ IFC_WP2_B	IFC Address	E11	O	OV_{DD}	1
IFC_A27/GPIO2_27/ IFC_WP3_B	IFC Address	C11	O	OV_{DD}	1
IFC_A28/GPIO2_28	IFC Address	D11	O	OV_{DD}	1
IFC_A29/GPIO2_29/ IFC_RB2_B	IFC Address	C12	O	OV_{DD}	1
IFC_A30/GPIO2_30/ IFC_RB3_B	IFC Address	D12	O	OV_{DD}	1
IFC_A31/GPIO2_31/ IFC_RB4_B	IFC Address	E12	O	OV_{DD}	1
IFC_AD00/cfg_gpinput0	IFC Address / Data	A4	IO	OV_{DD}	4
IFC_AD01/cfg_gpinput1	IFC Address / Data	B5	IO	OV_{DD}	4
IFC_AD02/cfg_gpinput2	IFC Address / Data	A5	IO	OV_{DD}	4
IFC_AD03/cfg_gpinput3	IFC Address / Data	B6	IO	OV_{DD}	4
IFC_AD04/cfg_gpinput4	IFC Address / Data	A6	IO	OV_{DD}	4
IFC_AD05/cfg_gpinput5	IFC Address / Data	A7	IO	OV_{DD}	4
IFC_AD06/cfg_gpinput6	IFC Address / Data	B8	IO	OV_{DD}	4
IFC_AD07/cfg_gpinput7	IFC Address / Data	A8	IO	OV_{DD}	4
IFC_AD08/cfg_rcw_src0	IFC Address / Data	B9	IO	OV_{DD}	4
IFC_AD09/cfg_rcw_src1	IFC Address / Data	A9	IO	OV_{DD}	4
IFC_AD10/cfg_rcw_src2	IFC Address / Data	A10	IO	OV_{DD}	4
IFC_AD11/cfg_rcw_src3	IFC Address / Data	B11	IO	OV_{DD}	4
IFC_AD12/cfg_rcw_src4	IFC Address / Data	A11	IO	OV_{DD}	4
IFC_AD13/cfg_rcw_src5	IFC Address / Data	B12	IO	OV_{DD}	4
IFC_AD14/cfg_rcw_src6	IFC Address / Data	A12	IO	OV_{DD}	4
IFC_AD15/cfg_rcw_src7	IFC Address / Data	A13	IO	OV_{DD}	4
IFC_AVD	IFC Address Valid	D17	O	OV_{DD}	1, 5
IFC_BCTL	IFC Buffer control	A14	O	OV_{DD}	2
IFC_CLE/cfg_rcw_src8	IFC Command Latch Enable / Write Enable	F16	O	OV_{DD}	1, 4
IFC_CLK0	IFC Clock	A17	O	OV_{DD}	2
IFC_CLK1	IFC Clock	A19	O	OV_{DD}	2
IFC_CS0_B	IFC Chip Select	C13	O	OV_{DD}	1, 6
IFC_CS1_B/GPIO2_10	IFC Chip Select	E15	O	OV_{DD}	1, 6
IFC_CS2_B/GPIO2_11	IFC Chip Select	D16	O	OV_{DD}	1, 6

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_CS3_B/GPIO2_12	IFC Chip Select	C16	O	OV_{DD}	1, 6
IFC_CS4_B/GPIO1_09	IFC Chip Select	E17	O	OV_{DD}	1, 6
IFC_CS5_B/GPIO1_10	IFC Chip Select	C17	O	OV_{DD}	1, 6
IFC_CS6_B/GPIO1_11	IFC Chip Select	D18	O	OV_{DD}	1, 6
IFC_CS7_B/GPIO1_12	IFC Chip Select	C19	O	OV_{DD}	1, 6
IFC_NDDDR_CLK	IFC NAND DDR Clock	D14	O	OV_{DD}	2
IFC_NDDQS	IFC DQS Strobe	A16	IO	OV_{DD}	---
IFC_OE_B	IFC Output Enable	D15	O	OV_{DD}	1, 5
IFC_PAR0/GPIO2_13	IFC Address & Data Parity	C15	IO	OV_{DD}	---
IFC_PAR1/GPIO2_14	IFC Address & Data Parity	C14	IO	OV_{DD}	---
IFC_PERR_B/GPIO2_15	IFC Parity Error	E14	I	OV_{DD}	1
IFC_RB0_B	IFC Ready / Busy CS0	B15	I	OV_{DD}	8
IFC_RB1_B	IFC Ready / Busy CS1	A15	I	OV_{DD}	8
IFC_RB2_B/**IFC_A29**/ GPIO2_29	IFC Ready / Busy CS 2	C12	I	OV_{DD}	1
IFC_RB3_B/**IFC_A30**/ GPIO2_30	IFC Ready / Busy CS 3	D12	I	OV_{DD}	1
IFC_RB4_B/**IFC_A31**/ GPIO2_31	IFC Ready / Busy CS 4	E12	I	OV_{DD}	1
IFC_TE/cfg_ifc_te	IFC External Transceiver Enable	B14	O	OV_{DD}	1, 4
IFC_WE0_B	IFC Write Enable	D13	O	OV_{DD}	1, 5
IFC_WP0_B	IFC Write Protect	F17	O	OV_{DD}	1, 5
IFC_WP1_B/**IFC_A25**/ GPIO2_25	IFC Write Protect	C10	O	OV_{DD}	1
IFC_WP2_B/**IFC_A26**/ GPIO2_26	IFC Write Protect	E11	O	OV_{DD}	1
IFC_WP3_B/**IFC_A27**/ GPIO2_27	IFC Write Protect	C11	O	OV_{DD}	1
DUART					
UART1_CTS_B/GPIO1_21/ UART3_SIN	Clear To Send	Y2	I	DV_{DD}	1
UART1_RTS_B/GPIO1_19/ UART3_SOUT	Ready to Send	Y1	O	DV_{DD}	1
UART1_SIN/GPIO1_17	Receive Data	AA1	I	DV_{DD}	1
UART1_SOUT/GPIO1_15	Transmit Data	AA2	O	DV_{DD}	1
UART2_CTS_B/GPIO1_22/ UART4_SIN	Clear To Send	Y4	I	DV_{DD}	1
UART2_RTS_B/GPIO1_20/ UART4_SOUT	Ready to Send	V4	O	DV_{DD}	1
UART2_SIN/GPIO1_18	Receive Data	W4	I	DV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
UART2_SOUT/GPIO1_16	Transmit Data	AA4	O	DV_{DD}	1
UART3_SIN/**UART1_CTS_B**/ GPIO1_21	Receive Data	Y2	I	DV_{DD}	1
UART3_SOUT/ **UART1_RTS_B**/GPIO1_19	Transmit Data	Y1	O	DV_{DD}	1
UART4_SIN/**UART2_CTS_B**/ GPIO1_22	Receive Data	Y4	I	DV_{DD}	1
UART4_SOUT/ **UART2_RTS_B**/GPIO1_20	Transmit Data	V4	O	DV_{DD}	1
I2C					
IIC1_SCL	Serial Clock (supports PBL)	W1	IO	DV_{DD}	7, 8
IIC1_SDA	Serial Data (supports PBL)	V1	IO	DV_{DD}	7, 8
IIC2_SCL	Serial Clock	V3	IO	DV_{DD}	7, 8
IIC2_SDA	Serial Data	Y3	IO	DV_{DD}	7, 8
IIC3_SCL/GPIO4_00	Serial Clock	V2	IO	DV_{DD}	7, 8
IIC3_SDA/GPIO4_01	Serial Data	W3	IO	DV_{DD}	7, 8
IIC4_SCL/GPIO4_02/EVT5_B	Serial Clock	AA3	IO	DV_{DD}	7, 8
IIC4_SDA/GPIO4_03/EVT6_B	Serial Data	AB3	IO	DV_{DD}	7, 8
eSPI Interface					
SPI_CLK	SPI Clock	N1	O	CV_{DD}	1
SPI_CS0_B/GPIO2_00/ SDHC_DAT4	SPI Chip Select	M1	O	CV_{DD}	1, 18
SPI_CS1_B/GPIO2_01/ SDHC_DAT5	SPI Chip Select	M2	O	CV_{DD}	1, 18
SPI_CS2_B/GPIO2_02/ SDHC_DAT6	SPI Chip Select	M3	O	CV_{DD}	1, 18
SPI_CS3_B/GPIO2_03/ SDHC_DAT7/ SDHC_CLK_SYNC_OUT	SPI Chip Select	N3	O	CV_{DD}	1, 18
SPI_MISO	Master In Slave Out	P1	I	CV_{DD}	1
SPI_MOSI	Master Out Slave In	P2	IO	CV_{DD}	---
eSDHC					
SDHC_CD_B/GPIO4_24	SDHC Card Detect	L5	I	OV_{DD}	1
SDHC_CLK/GPIO2_09	Host to Card Clock	K1	IO	OV_{DD}	---
SDHC_CLK_SYNC_IN/**IRQ10**/ GPIO1_30	IN	L4	I	CV_{DD}	1
SDHC_CLK_SYNC_OUT/ **SPI_CS3_B**/GPIO2_03/ SDHC_DAT7	OUT	N3	O	OV_{DD}	1
SDHC_CMD/GPIO2_04	Command/Response	K3	IO	OV_{DD}	18
SDHC_DAT0/GPIO2_05	Data	L2	IO	OV_{DD}	18

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SDHC_DAT1/GPIO2_06	Data	K4	IO	OV_{DD}	18
SDHC_DAT2/GPIO2_07	Data	L3	IO	OV_{DD}	18
SDHC_DAT3/GPIO2_08	Data	L1	IO	OV_{DD}	18
SDHC_DAT4/**SPI_CS0_B**/ GPIO2_00	Data	M1	IO	CV_{DD}	---
SDHC_DAT5/**SPI_CS1_B**/ GPIO2_01	Data	M2	IO	CV_{DD}	---
SDHC_DAT6/**SPI_CS2_B**/ GPIO2_02	Data	M3	IO	CV_{DD}	---
SDHC_DAT7/**SPI_CS3_B**/ GPIO2_03/ SDHC_CLK_SYNC_OUT	Data	N3	IO	CV_{DD}	---
SDHC_WP/GPIO4_25	SDHC Write Protect	M5	I	OV_{DD}	1
Programmable Interrupt Controller					
IRQ00	External Interrupt	F7	I	OV_{DD}	1
IRQ01	External Interrupt	D3	I	OV_{DD}	1
IRQ02	External Interrupt	E9	I	OV_{DD}	1
IRQ03/GPIO1_23	External Interrupt	D1	I	OV_{DD}	1
IRQ04/GPIO1_24	External Interrupt	D4	I	OV_{DD}	1
IRQ05/GPIO1_25	External Interrupt	D5	I	OV_{DD}	1
IRQ06/GPIO1_26	External Interrupt	AB4	I	LV_{DD}	1
IRQ07/GPIO1_27	External Interrupt	AD5	I	LV_{DD}	1
IRQ08/GPIO1_28	External Interrupt	AB1	I	LV_{DD}	1
IRQ09/GPIO1_29	External Interrupt	AC5	I	LV_{DD}	1
IRQ10/GPIO1_30/ SDHC_CLK_SYNC_IN	External Interrupt	L4	I	CV_{DD}	1
IRQ11/GPIO1_31	External Interrupt	U3	I	DV_{DD}	1
IRQ_OUT_B/EVT9_B	Interrupt Output	A3	O	OV_{DD}	1, 6, 7
LP Trust					
LP_TMP_DETECT_B	Low Power Tamper Detect	R6	I	V_{DD}_LP	---
Trust					
TMP_DETECT_B	Tamper Detect	F19	I	OV_{DD}	1
System Control					
HRESET_B	Hard Reset	E8	IO	OV_{DD}	6, 7
PORESET_B	Power On Reset	F13	I	OV_{DD}	---
RESET_REQ_B	Reset Request (POR or Hard)	B3	O	OV_{DD}	1, 5
Power Management					
ASLEEP/GPIO1_13/ cfg_xvdd_sel	Asleep	B2	O	OV_{DD}	1, 5
SYSCLK					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SYSCLK	System Clock	G15	I	OV_{DD}	---
		DDR Clocking			
DDRCLK	DDR Controller Clock	J21	I	OV_{DD}	---
		RTC			
RTC/GPIO1_14	Real Time Clock	B17	I	OV_{DD}	1
		Debug			
CKSTP_OUT_B	Checkstop Out	F18	O	OV_{DD}	1, 6, 7
CLK_OUT	Clock Out	E6	O	OV_{DD}	2
EVT0_B	Event 0	D6	IO	OV_{DD}	9
EVT1_B	Event 1	C4	IO	OV_{DD}	---
EVT2_B	Event 2	C1	IO	OV_{DD}	---
EVT3_B	Event 3	C2	IO	OV_{DD}	---
EVT4_B	Event 4	C3	IO	OV_{DD}	---
EVT5_B/**IIC4_SCL**/GPIO4_02	Event 5	AA3	IO	DV_{DD}	---
EVT6_B/**IIC4_SDA**/GPIO4_03	Event 6	AB3	IO	DV_{DD}	---
EVT7_B/**DMA2_DACK0_B**/ GPIO4_08	Event 7	AA5	IO	DV_{DD}	---
EVT8_B/**DMA2_DDONE0_B**/ GPIO4_09	Event 8	Y5	IO	DV_{DD}	---
EVT9_B/**IRQ_OUT_B**	Event 9	A3	IO	OV_{DD}	---
		DFT			
SCAN_MODE_B	Reserved	F9	I	OV_{DD}	10
TEST_OUT0	Test Output	H21	O	$G1V_{DD}$	2
TEST_OUT1	Test Output	F21	O	$G1V_{DD}$	2
TEST_OUT2	Test Output	W21	O	$G1V_{DD}$	---
TEST_OUT3	Test Output	V21	O	$G1V_{DD}$	---
TEST_OUT4	Test Output	K22	O	$G1V_{DD}$	---
TEST_OUT5	Test Output	M22	O	$G1V_{DD}$	---
TEST_OUT6	Test Output	U22	O	$G1V_{DD}$	2
TEST_OUT7	Test Output	P22	O	$G1V_{DD}$	2
TEST_SEL_B	Reserved	G8	I	OV_{DD}	10
		JTAG			
TCK	Test Clock	E18	I	OV_{DD}	---
TDI	Test Data In	A18	I	OV_{DD}	9
TDO	Test Data Out	C18	O	OV_{DD}	2
TMS	Test Mode Select	B18	I	OV_{DD}	9
TRST_B	Test Reset	D19	I	OV_{DD}	9
		Analog Signals			

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MVREF	SSTL Reference Voltage	F20	IO	$G1V_{DD}/2$	---
D1_TPA	DDR Controller 1 Test Point Analog	J20	IO	-	12
FA_ANALOG_G_V	Reserved	C20	IO	-	15
FA_ANALOG_PIN	Reserved	B20	IO	-	15
TD1_ANODE	Thermal diode anode	E21	IO	Internal Diode	17
TD1_CATHODE	Thermal diode cathode	G21	IO	Internal Diode	17
TH_TPA	Thermal Test Point Analog	F10	-	-	12
Serdes 1					
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	AA12	I	$S1V_{DD}$	11
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	Y20	I	$X1V_{DD}$	16
SD1_PLL1_TPA	Reserved for internal use only	Y15	O	AVDD_SD1_PLL1	12
SD1_PLL1_TPD	Reserved for internal use only	AB15	O	$X1V_{DD}$	12
SD1_PLL2_TPA	Reserved for internal use only	Y19	O	AVDD_SD1_PLL2	12
SD1_PLL2_TPD	Reserved for internal use only	AB19	O	$X1V_{DD}$	12
SD1_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AA14	I	$S1V_{DD}$	---
SD1_REF_CLK1_P	SerDes PLL 1 Reference Clock	AB14	I	$S1V_{DD}$	---
SD1_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AA18	I	$S1V_{DD}$	---
SD1_REF_CLK2_P	SerDes PLL 2 Reference Clock	AB18	I	$S1V_{DD}$	---
SD1_RX0_N	SerDes Receive Data (negative)	AG10	I	$S1V_{DD}$	---
SD1_RX0_P	SerDes Receive Data (positive)	AH10	I	$S1V_{DD}$	---
SD1_RX1_N	SerDes Receive Data (negative)	AG11	I	$S1V_{DD}$	---
SD1_RX1_P	SerDes Receive Data (positive)	AH11	I	$S1V_{DD}$	---
SD1_RX2_N	SerDes Receive Data (negative)	AG13	I	$S1V_{DD}$	---
SD1_RX2_P	SerDes Receive Data (positive)	AH13	I	$S1V_{DD}$	---
SD1_RX3_N	SerDes Receive Data (negative)	AG14	I	$S1V_{DD}$	---
SD1_RX3_P	SerDes Receive Data (positive)	AH14	I	$S1V_{DD}$	---
SD1_RX4_N	SerDes Receive Data (negative)	AG16	I	$S1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD1_RX4_P	SerDes Receive Data (positive)	AH16	I	$S1V_{DD}$	---
SD1_RX5_N	SerDes Receive Data (negative)	AG17	I	$S1V_{DD}$	---
SD1_RX5_P	SerDes Receive Data (positive)	AH17	I	$S1V_{DD}$	---
SD1_RX6_N	SerDes Receive Data (negative)	AG19	I	$S1V_{DD}$	---
SD1_RX6_P	SerDes Receive Data (positive)	AH19	I	$S1V_{DD}$	---
SD1_RX7_N	SerDes Receive Data (negative)	AG20	I	$S1V_{DD}$	---
SD1_RX7_P	SerDes Receive Data (positive)	AH20	I	$S1V_{DD}$	---
SD1_TX0_N	SerDes Transmit Data (negative)	AE10	O	$X1V_{DD}$	---
SD1_TX0_P	SerDes Transmit Data (positive)	AD10	O	$X1V_{DD}$	---
SD1_TX1_N	SerDes Transmit Data (negative)	AE11	O	$X1V_{DD}$	---
SD1_TX1_P	SerDes Transmit Data (positive)	AD11	O	$X1V_{DD}$	---
SD1_TX2_N	SerDes Transmit Data (negative)	AE13	O	$X1V_{DD}$	---
SD1_TX2_P	SerDes Transmit Data (positive)	AD13	O	$X1V_{DD}$	---
SD1_TX3_N	SerDes Transmit Data (negative)	AE14	O	$X1V_{DD}$	---
SD1_TX3_P	SerDes Transmit Data (positive)	AD14	O	$X1V_{DD}$	---
SD1_TX4_N	SerDes Transmit Data (negative)	AE16	O	$X1V_{DD}$	---
SD1_TX4_P	SerDes Transmit Data (positive)	AD16	O	$X1V_{DD}$	---
SD1_TX5_N	SerDes Transmit Data (negative)	AE17	O	$X1V_{DD}$	---
SD1_TX5_P	SerDes Transmit Data (positive)	AD17	O	$X1V_{DD}$	---
SD1_TX6_N	SerDes Transmit Data (negative)	AE19	O	$X1V_{DD}$	---
SD1_TX6_P	SerDes Transmit Data (positive)	AD19	O	$X1V_{DD}$	---
SD1_TX7_N	SerDes Transmit Data (negative)	AE20	O	$X1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD1_TX7_P	SerDes Transmit Data (positive)	AD20	O	$X1V_{DD}$	---
		USB PHY 1 & 2			
USB1_DRVVBUS	USB PHY Digital signal - Drive VBUS	F6	O	USB_HV_{DD}	---
USB1_PWRFAULT	USB PHY Digital signal - Power Fault	F5	I	USB_HV_{DD}	---
USB1_UDM	USB PHY Data Minus	F2	IO	USB_HV_{DD}	---
USB1_UDP	USB PHY Data Plus	F1	IO	USB_HV_{DD}	---
USB1_UID	USB PHY ID Detect	F4	I	USB_OV_{DD}	---
USB1_VBUSCLMP	USB PHY VBUS	E4	I	USB_HV_{DD}	---
USB2_DRVVBUS	USB PHY Digital signal - Drive VBUS	J5	O	USB_HV_{DD}	---
USB2_PWRFAULT	USB PHY Digital signal - Power Fault	H5	I	USB_HV_{DD}	---
USB2_UDM	USB PHY Data Minus	H2	IO	USB_HV_{DD}	---
USB2_UDP	USB PHY Data Plus	H1	IO	USB_HV_{DD}	---
USB2_UID	USB PHY ID Detect	H4	I	USB_OV_{DD}	---
USB2_VBUSCLMP	USB PHY VBUS	J4	I	USB_HV_{DD}	---
USBCLK	USB PHY Clock In	F8	I	OV_{DD}	---
USB_IBIAS_REXT	USB PHY Impedance Calibration	G4	IO	USB_OV_{DD}	19
		IEEE1588			
TSEC_1588_ALARM_OUT1/ GPIO3_03	Alarm Out 1	AF5	O	LV_{DD}	1
TSEC_1588_ALARM_OUT2/ GPIO3_04	Alarm Out 2	AC7	O	LV_{DD}	1
TSEC_1588_CLK_IN/ GPIO3_00	Clock In	AC8	I	LV_{DD}	1
TSEC_1588_CLK_OUT/ GPIO3_05	Clock Out	AD7	O	LV_{DD}	1
TSEC_1588_PULSE_OUT1/ GPIO3_06	Pulse Out 1	AE6	O	LV_{DD}	1
TSEC_1588_PULSE_OUT2/ GPIO3_07	Pulse Out 2	AD8	O	LV_{DD}	1
TSEC_1588_TRIG_IN1/ GPIO3_01	Trigger In 1	AB6	I	LV_{DD}	1
TSEC_1588_TRIG_IN2/ GPIO3_02	Trigger In 2	AE5	I	LV_{DD}	1
		Ethernet Management Interface 1			
EMI1_MDC	Management Data Clock	AH3	O	LV_{DD}	---
EMI1_MDIO	Management Data In/Out	AH4	IO	LV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
Ethernet Management Interface 2					
EMI2_MDC	Management Data Clock (1.2V open drain)	L6	O	OV_{DD}	7, 13
EMI2_MDIO	Management Data In/Out (1.2V open drain)	M6	IO	OV_{DD}	7, 13
Ethernet Controller (RGMII) 1					
EC1_GTX_CLK/GPIO3_16	Transmit Clock Out	AF3	O	LV_{DD}	1
EC1_GTX_CLK125/GPIO3_17	Reference Clock	AG3	I	LV_{DD}	1
EC1_RXD0/GPIO3_21	Receive Data	AF2	I	LV_{DD}	1
EC1_RXD1/GPIO3_20	Receive Data	AF1	I	LV_{DD}	1
EC1_RXD2/GPIO3_19	Receive Data	AE1	I	LV_{DD}	1
EC1_RXD3/GPIO3_18	Receive Data	AD2	I	LV_{DD}	1
EC1_RX_CLK/GPIO3_23	Receive Clock	AD1	I	LV_{DD}	1
EC1_RX_CTL/GPIO3_22	Receive Data Valid	AG2	I	LV_{DD}	1
EC1_TXD0/GPIO3_14	Transmit Data	AE3	O	LV_{DD}	1
EC1_TXD1/GPIO3_13	Transmit Data	AE4	O	LV_{DD}	1
EC1_TXD2/GPIO3_12	Transmit Data	AD3	O	LV_{DD}	1
EC1_TXD3/GPIO3_11	Transmit Data	AC3	O	LV_{DD}	1
EC1_TX_CTL/GPIO3_15	Transmit Enable	AF4	O	LV_{DD}	1, 14
Ethernet Controller (RGMII) 2					
EC2_GTX_CLK/GPIO4_28	Transmit Clock Out	AE8	O	LV_{DD}	1
EC2_GTX_CLK125/GPIO4_29	Reference Clock	AC6	I	LV_{DD}	1
EC2_RXD0/GPIO3_31	Receive Data	AH8	I	LV_{DD}	1
EC2_RXD1/GPIO3_30	Receive Data	AG7	I	LV_{DD}	1
EC2_RXD2/GPIO3_29	Receive Data	AH7	I	LV_{DD}	1
EC2_RXD3/GPIO3_28	Receive Data	AH6	I	LV_{DD}	1
EC2_RX_CLK/GPIO4_31	Receive Clock	AH5	I	LV_{DD}	1
EC2_RX_CTL/GPIO4_30	Receive Data Valid	AG8	I	LV_{DD}	1
EC2_TXD0/GPIO3_27	Transmit Data	AE7	O	LV_{DD}	1
EC2_TXD1/GPIO3_26	Transmit Data	AF7	O	LV_{DD}	1
EC2_TXD2/GPIO3_25	Transmit Data	AF6	O	LV_{DD}	1
EC2_TXD3/GPIO3_24	Transmit Data	AG5	O	LV_{DD}	1
EC2_TX_CTL/GPIO4_27	Transmit Enable	AF8	O	LV_{DD}	1, 14
DMA					
DMA1_DACK0_B/GPIO4_05	DMA1 channel 0 acknowledge	U5	O	DV_{DD}	1
DMA1_DDONE0_B/GPIO4_06	DMA1 channel 0 done	R5	O	DV_{DD}	1
DMA1_DREQ0_B/GPIO4_04	DMA1 channel 0 request	P5	I	DV_{DD}	1
DMA2_DACK0_B/GPIO4_08/ EVT7_B	DMA2 channel 0 acknowledge	AA5	O	DV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DMA2_DDONE0_B/ GPIO4_09/EVT8_B	DMA2 channel 0 done	Y5	O	DV_{DD}	1
DMA2_DREQ0_B/GPIO4_07	DMA2 channel 0 request	V5	I	DV_{DD}	1
Power-On-Reset Configuration					
cfg_dram_type/**IFC_A21**	Power-On-Reset Configuration Signal	C8	I	OV_{DD}	1, 4
cfg_gpinput0/**IFC_AD00**	Power-On-Reset Configuration Signal	A4	I	OV_{DD}	1, 4
cfg_gpinput1/**IFC_AD01**	Power-On-Reset Configuration Signal	B5	I	OV_{DD}	1, 4
cfg_gpinput2/**IFC_AD02**	Power-On-Reset Configuration Signal	A5	I	OV_{DD}	1, 4
cfg_gpinput3/**IFC_AD03**	Power-On-Reset Configuration Signal	B6	I	OV_{DD}	1, 4
cfg_gpinput4/**IFC_AD04**	Power-On-Reset Configuration Signal	A6	I	OV_{DD}	1, 4
cfg_gpinput5/**IFC_AD05**	Power-On-Reset Configuration Signal	A7	I	OV_{DD}	1, 4
cfg_gpinput6/**IFC_AD06**	Power-On-Reset Configuration Signal	B8	I	OV_{DD}	1, 4
cfg_gpinput7/**IFC_AD07**	Power-On-Reset Configuration Signal	A8	I	OV_{DD}	1, 4
cfg_ifc_te/**IFC_TE**	Power-On-Reset Configuration Signal	B14	I	OV_{DD}	1, 4
cfg_rcw_src0/**IFC_AD08**	Power-On-Reset Configuration Signal	B9	I	OV_{DD}	1, 4
cfg_rcw_src1/**IFC_AD09**	Power-On-Reset Configuration Signal	A9	I	OV_{DD}	1, 4
cfg_rcw_src2/**IFC_AD10**	Power-On-Reset Configuration Signal	A10	I	OV_{DD}	1, 4
cfg_rcw_src3/**IFC_AD11**	Power-On-Reset Configuration Signal	B11	I	OV_{DD}	1, 4
cfg_rcw_src4/**IFC_AD12**	Power-On-Reset Configuration Signal	A11	I	OV_{DD}	1, 4
cfg_rcw_src5/**IFC_AD13**	Power-On-Reset Configuration Signal	B12	I	OV_{DD}	1, 4
cfg_rcw_src6/**IFC_AD14**	Power-On-Reset Configuration Signal	A12	I	OV_{DD}	1, 4
cfg_rcw_src7/**IFC_AD15**	Power-On-Reset Configuration Signal	A13	I	OV_{DD}	1, 4
cfg_rcw_src8/**IFC_CLE**	Power-On-Reset Configuration Signal	F16	I	OV_{DD}	1, 4
cfg_xvdd_sel/**ASLEEP**/ GPIO1_13	Power-On-Reset Configuration Signal	B2	I	OV_{DD}	1, 5, 5

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
General Purpose Input/Output					
GPIO1_09/**IFC_CS4_B**	General Purpose Input/Output	E17	IO	OV_{DD}	---
GPIO1_10/**IFC_CS5_B**	General Purpose Input/Output	C17	IO	OV_{DD}	---
GPIO1_11/**IFC_CS6_B**	General Purpose Input/Output	D18	IO	OV_{DD}	---
GPIO1_12/**IFC_CS7_B**	General Purpose Input/Output	C19	IO	OV_{DD}	---
GPIO1_13/**ASLEEP**/ cfg_xvdd_sel	General Purpose Input/Output	B2	O	OV_{DD}	1, 5, 5
GPIO1_14/**RTC**	General Purpose Input/Output	B17	IO	OV_{DD}	---
GPIO1_15/**UART1_SOUT**	General Purpose Input/Output	AA2	IO	DV_{DD}	---
GPIO1_16/**UART2_SOUT**	General Purpose Input/Output	AA4	IO	DV_{DD}	---
GPIO1_17/**UART1_SIN**	General Purpose Input/Output	AA1	IO	DV_{DD}	---
GPIO1_18/**UART2_SIN**	General Purpose Input/Output	W4	IO	DV_{DD}	---
GPIO1_19/**UART1_RTS_B**/ UART3_SOUT	General Purpose Input/Output	Y1	IO	DV_{DD}	---
GPIO1_20/**UART2_RTS_B**/ UART4_SOUT	General Purpose Input/Output	V4	IO	DV_{DD}	---
GPIO1_21/**UART1_CTS_B**/ UART3_SIN	General Purpose Input/Output	Y2	IO	DV_{DD}	---
GPIO1_22/**UART2_CTS_B**/ UART4_SIN	General Purpose Input/Output	Y4	IO	DV_{DD}	---
GPIO1_23/**IRQ03**	General Purpose Input/Output	D1	IO	OV_{DD}	---
GPIO1_24/**IRQ04**	General Purpose Input/Output	D4	IO	OV_{DD}	---
GPIO1_25/**IRQ05**	General Purpose Input/Output	D5	IO	OV_{DD}	---
GPIO1_26/**IRQ06**	General Purpose Input/Output	AB4	IO	LV_{DD}	---
GPIO1_27/**IRQ07**	General Purpose Input/Output	AD5	IO	LV_{DD}	---
GPIO1_28/**IRQ08**	General Purpose Input/Output	AB1	IO	LV_{DD}	---
GPIO1_29/**IRQ09**	General Purpose Input/Output	AC5	IO	LV_{DD}	---
GPIO1_30/**IRQ10**/ SDHC_CLK_SYNC_IN	General Purpose Input/Output	L4	IO	CV_{DD}	---
GPIO1_31/**IRQ11**	General Purpose Input/Output	U3	IO	DV_{DD}	---
GPIO2_00/**SPI_CS0_B**/ SDHC_DAT4	General Purpose Input/Output	M1	IO	CV_{DD}	---
GPIO2_01/**SPI_CS1_B**/ SDHC_DAT5	General Purpose Input/Output	M2	IO	CV_{DD}	---
GPIO2_02/**SPI_CS2_B**/ SDHC_DAT6	General Purpose Input/Output	M3	IO	CV_{DD}	---
GPIO2_03/**SPI_CS3_B**/ SDHC_DAT7/ SDHC_CLK_SYNC_OUT	General Purpose Input/Output	N3	IO	CV_{DD}	---
GPIO2_04/**SDHC_CMD**	General Purpose Input/Output	K3	IO	OV_{DD}	---
GPIO2_05/**SDHC_DAT0**	General Purpose Input/Output	L2	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO2_06/**SDHC_DAT1**	General Purpose Input/Output	K4	IO	OV_{DD}	---
GPIO2_07/**SDHC_DAT2**	General Purpose Input/Output	L3	IO	OV_{DD}	---
GPIO2_08/**SDHC_DAT3**	General Purpose Input/Output	L1	IO	OV_{DD}	---
GPIO2_09/**SDHC_CLK**	General Purpose Input/Output	K1	IO	OV_{DD}	---
GPIO2_10/**IFC_CS1_B**	General Purpose Input/Output	E15	IO	OV_{DD}	---
GPIO2_11/**IFC_CS2_B**	General Purpose Input/Output	D16	IO	OV_{DD}	---
GPIO2_12/**IFC_CS3_B**	General Purpose Input/Output	C16	IO	OV_{DD}	---
GPIO2_13/**IFC_PAR0**	General Purpose Input/Output	C15	IO	OV_{DD}	---
GPIO2_14/**IFC_PAR1**	General Purpose Input/Output	C14	IO	OV_{DD}	---
GPIO2_15/**IFC_PERR_B**	General Purpose Input/Output	E14	IO	OV_{DD}	---
GPIO2_25/**IFC_A25**/ IFC_WP1_B	General Purpose Input/Output	C10	IO	OV_{DD}	---
GPIO2_26/**IFC_A26**/ IFC_WP2_B	General Purpose Input/Output	E11	IO	OV_{DD}	---
GPIO2_27/**IFC_A27**/ IFC_WP3_B	General Purpose Input/Output	C11	IO	OV_{DD}	---
GPIO2_28/**IFC_A28**	General Purpose Input/Output	D11	IO	OV_{DD}	---
GPIO2_29/**IFC_A29**/ IFC_RB2_B	General Purpose Input/Output	C12	IO	OV_{DD}	---
GPIO2_30/**IFC_A30**/ IFC_RB3_B	General Purpose Input/Output	D12	IO	OV_{DD}	---
GPIO2_31/**IFC_A31**/ IFC_RB4_B	General Purpose Input/Output	E12	IO	OV_{DD}	---
GPIO3_00/ **TSEC_1588_CLK_IN**	General Purpose Input/Output	AC8	IO	LV_{DD}	---
GPIO3_01/ **TSEC_1588_TRIG_IN1**	General Purpose Input/Output	AB6	IO	LV_{DD}	---
GPIO3_02/ **TSEC_1588_TRIG_IN2**	General Purpose Input/Output	AE5	IO	LV_{DD}	---
GPIO3_03/ **TSEC_1588_ALARM_OUT1**	General Purpose Input/Output	AF5	IO	LV_{DD}	---
GPIO3_04/ **TSEC_1588_ALARM_OUT2**	General Purpose Input/Output	AC7	IO	LV_{DD}	---
GPIO3_05/ **TSEC_1588_CLK_OUT**	General Purpose Input/Output	AD7	IO	LV_{DD}	---
GPIO3_06/ **TSEC_1588_PULSE_OUT1**	General Purpose Input/Output	AE6	IO	LV_{DD}	---
GPIO3_07/ **TSEC_1588_PULSE_OUT2**	General Purpose Input/Output	AD8	IO	LV_{DD}	---
GPIO3_11/**EC1_TXD3**	General Purpose Input/Output	AC3	IO	LV_{DD}	---
GPIO3_12/**EC1_TXD2**	General Purpose Input/Output	AD3	IO	LV_{DD}	---
GPIO3_13/**EC1_TXD1**	General Purpose Input/Output	AE4	IO	LV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO3_14/**EC1_TXD0**	General Purpose Input/Output	AE3	IO	LV_{DD}	---
GPIO3_15/**EC1_TX_CTL**	General Purpose Input/Output	AF4	IO	LV_{DD}	---
GPIO3_16/**EC1_GTX_CLK**	General Purpose Input/Output	AF3	IO	LV_{DD}	---
GPIO3_17/**EC1_GTX_CLK125**	General Purpose Input/Output	AG3	IO	LV_{DD}	---
GPIO3_18/**EC1_RXD3**	General Purpose Input/Output	AD2	IO	LV_{DD}	---
GPIO3_19/**EC1_RXD2**	General Purpose Input/Output	AE1	IO	LV_{DD}	---
GPIO3_20/**EC1_RXD1**	General Purpose Input/Output	AF1	IO	LV_{DD}	---
GPIO3_21/**EC1_RXD0**	General Purpose Input/Output	AF2	IO	LV_{DD}	---
GPIO3_22/**EC1_RX_CTL**	General Purpose Input/Output	AG2	IO	LV_{DD}	---
GPIO3_23/**EC1_RX_CLK**	General Purpose Input/Output	AD1	IO	LV_{DD}	---
GPIO3_24/**EC2_TXD3**	General Purpose Input/Output	AG5	IO	LV_{DD}	---
GPIO3_25/**EC2_TXD2**	General Purpose Input/Output	AF6	IO	LV_{DD}	---
GPIO3_26/**EC2_TXD1**	General Purpose Input/Output	AF7	IO	LV_{DD}	---
GPIO3_27/**EC2_TXD0**	General Purpose Input/Output	AE7	IO	LV_{DD}	---
GPIO3_28/**EC2_RXD3**	General Purpose Input/Output	AH6	IO	LV_{DD}	---
GPIO3_29/**EC2_RXD2**	General Purpose Input/Output	AH7	IO	LV_{DD}	---
GPIO3_30/**EC2_RXD1**	General Purpose Input/Output	AG7	IO	LV_{DD}	---
GPIO3_31/**EC2_RXD0**	General Purpose Input/Output	AH8	IO	LV_{DD}	---
GPIO4_00/**IIC3_SCL**	General Purpose Input/Output	V2	IO	DV_{DD}	---
GPIO4_01/**IIC3_SDA**	General Purpose Input/Output	W3	IO	DV_{DD}	---
GPIO4_02/**IIC4_SCL**/EVT5_B	General Purpose Input/Output	AA3	IO	DV_{DD}	---
GPIO4_03/**IIC4_SDA**/EVT6_B	General Purpose Input/Output	AB3	IO	DV_{DD}	---
GPIO4_04/**DMA1_DREQ0_B**	General Purpose Input/Output	P5	IO	DV_{DD}	---
GPIO4_05/**DMA1_DACK0_B**	General Purpose Input/Output	U5	IO	DV_{DD}	---
GPIO4_06/**DMA1_DDONE0_B**	General Purpose Input/Output	R5	IO	DV_{DD}	---
GPIO4_07/**DMA2_DREQ0_B**	General Purpose Input/Output	V5	IO	DV_{DD}	---
GPIO4_08/**DMA2_DACK0_B**/EVT7_B	General Purpose Input/Output	AA5	IO	DV_{DD}	---
GPIO4_09/**DMA2_DDONE0_B**/EVT8_B	General Purpose Input/Output	Y5	IO	DV_{DD}	---
GPIO4_24/**SDHC_CD_B**	General Purpose Input/Output	L5	IO	OV_{DD}	---
GPIO4_25/**SDHC_WP**	General Purpose Input/Output	M5	IO	OV_{DD}	---
GPIO4_27/**EC2_TX_CTL**	General Purpose Input/Output	AF8	IO	LV_{DD}	---
GPIO4_28/**EC2_GTX_CLK**	General Purpose Input/Output	AE8	IO	LV_{DD}	---
GPIO4_29/**EC2_GTX_CLK125**	General Purpose Input/Output	AC6	IO	LV_{DD}	---
GPIO4_30/**EC2_RX_CTL**	General Purpose Input/Output	AG8	IO	LV_{DD}	---
GPIO4_31/**EC2_RX_CLK**	General Purpose Input/Output	AH5	IO	LV_{DD}	---
Power and Ground Signals					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND001	GND	A2	---	---	---
GND002	GND	A20	---	---	---
GND003	GND	A27	---	---	---
GND004	GND	B1	---	---	---
GND005	GND	B4	---	---	---
GND006	GND	B7	---	---	---
GND007	GND	B10	---	---	---
GND008	GND	B13	---	---	---
GND009	GND	B16	---	---	---
GND010	GND	B19	---	---	---
GND011	GND	B23	---	---	---
GND012	GND	B25	---	---	---
GND013	GND	B28	---	---	---
GND014	GND	C22	---	---	---
GND015	GND	C26	---	---	---
GND016	GND	D2	---	---	---
GND017	GND	D20	---	---	---
GND018	GND	D21	---	---	---
GND019	GND	D24	---	---	---
GND020	GND	E5	---	---	---
GND021	GND	E7	---	---	---
GND022	GND	E10	---	---	---
GND023	GND	E13	---	---	---
GND024	GND	E16	---	---	---
GND025	GND	E19	---	---	---
GND026	GND	E22	---	---	---
GND027	GND	E26	---	---	---
GND028	GND	F15	---	---	---
GND029	GND	F24	---	---	---
GND030	GND	G7	---	---	---
GND031	GND	G13	---	---	---
GND032	GND	G16	---	---	---
GND033	GND	G22	---	---	---
GND034	GND	G26	---	---	---
GND035	GND	H7	---	---	---
GND036	GND	H8	---	---	---
GND037	GND	H9	---	---	---
GND038	GND	H10	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND039	GND	H11	---	---	---
GND040	GND	H12	---	---	---
GND041	GND	H13	---	---	---
GND042	GND	H14	---	---	---
GND043	GND	H15	---	---	---
GND044	GND	H16	---	---	---
GND045	GND	H17	---	---	---
GND046	GND	H18	---	---	---
GND047	GND	H19	---	---	---
GND048	GND	H20	---	---	---
GND049	GND	H24	---	---	---
GND050	GND	J7	---	---	---
GND051	GND	J22	---	---	---
GND052	GND	J26	---	---	---
GND053	GND	K2	---	---	---
GND054	GND	K5	---	---	---
GND055	GND	K6	---	---	---
GND056	GND	K7	---	---	---
GND057	GND	K12	---	---	---
GND058	GND	K14	---	---	---
GND059	GND	K16	---	---	---
GND060	GND	K18	---	---	---
GND061	GND	K20	---	---	---
GND062	GND	K24	---	---	---
GND063	GND	L7	---	---	---
GND064	GND	L9	---	---	---
GND065	GND	L11	---	---	---
GND066	GND	L13	---	---	---
GND067	GND	L15	---	---	---
GND068	GND	L17	---	---	---
GND069	GND	L19	---	---	---
GND070	GND	L22	---	---	---
GND071	GND	L26	---	---	---
GND072	GND	M7	---	---	---
GND073	GND	M10	---	---	---
GND074	GND	M12	---	---	---
GND075	GND	M14	---	---	---
GND076	GND	M16	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND077	GND	M18	---	---	---
GND078	GND	M20	---	---	---
GND079	GND	M24	---	---	---
GND080	GND	N2	---	---	---
GND081	GND	N5	---	---	---
GND082	GND	N7	---	---	---
GND083	GND	N9	---	---	---
GND084	GND	N11	---	---	---
GND085	GND	N13	---	---	---
GND086	GND	N15	---	---	---
GND087	GND	N17	---	---	---
GND088	GND	N19	---	---	---
GND089	GND	N22	---	---	---
GND090	GND	N26	---	---	---
GND091	GND	P7	---	---	---
GND092	GND	P10	---	---	---
GND093	GND	P12	---	---	---
GND094	GND	P14	---	---	---
GND095	GND	P16	---	---	---
GND096	GND	P18	---	---	---
GND097	GND	P20	---	---	---
GND098	GND	P24	---	---	---
GND099	GND	R7	---	---	---
GND100	GND	R9	---	---	---
GND101	GND	R11	---	---	---
GND102	GND	R13	---	---	---
GND103	GND	R15	---	---	---
GND104	GND	R17	---	---	---
GND105	GND	R19	---	---	---
GND106	GND	R22	---	---	---
GND107	GND	R26	---	---	---
GND108	GND	T2	---	---	---
GND109	GND	T5	---	---	---
GND110	GND	T7	---	---	---
GND111	GND	T10	---	---	---
GND112	GND	T12	---	---	---
GND113	GND	T14	---	---	---
GND114	GND	T16	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND115	GND	T18	---	---	---
GND116	GND	T20	---	---	---
GND117	GND	T22	---	---	---
GND118	GND	T26	---	---	---
GND119	GND	U7	---	---	---
GND120	GND	U9	---	---	---
GND121	GND	U11	---	---	---
GND122	GND	U13	---	---	---
GND123	GND	U15	---	---	---
GND124	GND	U17	---	---	---
GND125	GND	U19	---	---	---
GND126	GND	U24	---	---	---
GND127	GND	V7	---	---	---
GND128	GND	V10	---	---	---
GND129	GND	V12	---	---	---
GND130	GND	V14	---	---	---
GND131	GND	V16	---	---	---
GND132	GND	V18	---	---	---
GND133	GND	V20	---	---	---
GND134	GND	V22	---	---	---
GND135	GND	V26	---	---	---
GND136	GND	W2	---	---	---
GND137	GND	W5	---	---	---
GND138	GND	W7	---	---	---
GND139	GND	W9	---	---	---
GND140	GND	W11	---	---	---
GND141	GND	W13	---	---	---
GND142	GND	W24	---	---	---
GND143	GND	Y7	---	---	---
GND144	GND	Y10	---	---	---
GND145	GND	Y12	---	---	---
GND146	GND	Y22	---	---	---
GND147	GND	Y26	---	---	---
GND148	GND	AA11	---	---	---
GND149	GND	AA24	---	---	---
GND150	GND	AB2	---	---	---
GND151	GND	AB5	---	---	---
GND152	GND	AB7	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND153	GND	AB22	---	---	---
GND154	GND	AB26	---	---	---
GND155	GND	AC24	---	---	---
GND156	GND	AC26	---	---	---
GND157	GND	AD4	---	---	---
GND158	GND	AD6	---	---	---
GND159	GND	AD22	---	---	---
GND160	GND	AE2	---	---	---
GND161	GND	AE24	---	---	---
GND162	GND	AE26	---	---	---
GND163	GND	AF9	---	---	---
GND164	GND	AF21	---	---	---
GND165	GND	AG1	---	---	---
GND166	GND	AG4	---	---	---
GND167	GND	AG6	---	---	---
GND168	GND	AG22	---	---	---
GND169	GND	AG23	---	---	---
GND170	GND	AG26	---	---	---
GND171	GND	AH2	---	---	---
GND172	GND	AH27	---	---	---
USB_AGND01	USB PHY Transceiver GND	E1	---	---	---
USB_AGND02	USB PHY Transceiver GND	E2	---	---	---
USB_AGND03	USB PHY Transceiver GND	E3	---	---	---
USB_AGND04	USB PHY Transceiver GND	F3	---	---	---
USB_AGND05	USB PHY Transceiver GND	G1	---	---	---
USB_AGND06	USB PHY Transceiver GND	G2	---	---	---
USB_AGND07	USB PHY Transceiver GND	G3	---	---	---
USB_AGND08	USB PHY Transceiver GND	G5	---	---	---
USB_AGND09	USB PHY Transceiver GND	H3	---	---	---
USB_AGND10	USB PHY Transceiver GND	J1	---	---	---
USB_AGND11	USB PHY Transceiver GND	J2	---	---	---
USB_AGND12	USB PHY Transceiver GND	J3	---	---	---
X1GND01	Serdes1 transceiver GND	AC10	---	---	---
X1GND02	Serdes1 transceiver GND	AC11	---	---	---
X1GND03	Serdes1 transceiver GND	AC13	---	---	---
X1GND04	Serdes1 transceiver GND	AC14	---	---	---
X1GND05	Serdes1 transceiver GND	AC16	---	---	---
X1GND06	Serdes1 transceiver GND	AC17	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
X1GND07	Serdes1 transceiver GND	AC19	---	---	---
X1GND08	Serdes1 transceiver GND	AC20	---	---	---
X1GND09	Serdes1 transceiver GND	AD9	---	---	---
X1GND10	Serdes1 transceiver GND	AD12	---	---	---
X1GND11	Serdes1 transceiver GND	AD15	---	---	---
X1GND12	Serdes1 transceiver GND	AD18	---	---	---
X1GND13	Serdes1 transceiver GND	AD21	---	---	---
X1GND14	Serdes1 transceiver GND	AE9	---	---	---
X1GND15	Serdes1 transceiver GND	AE12	---	---	---
X1GND16	Serdes1 transceiver GND	AE15	---	---	---
X1GND17	Serdes1 transceiver GND	AE18	---	---	---
X1GND18	Serdes1 transceiver GND	AE21	---	---	---
S1GND01	Serdes core logic GND	Y14	---	---	---
S1GND02	Serdes core logic GND	Y16	---	---	---
S1GND03	Serdes core logic GND	Y17	---	---	---
S1GND04	Serdes core logic GND	Y18	---	---	---
S1GND05	Serdes core logic GND	AA13	---	---	---
S1GND06	Serdes core logic GND	AA15	---	---	---
S1GND07	Serdes core logic GND	AA17	---	---	---
S1GND08	Serdes core logic GND	AA19	---	---	---
S1GND09	Serdes core logic GND	AA21	---	---	---
S1GND10	Serdes core logic GND	AB13	---	---	---
S1GND11	Serdes core logic GND	AB17	---	---	---
S1GND12	Serdes core logic GND	AB21	---	---	---
S1GND13	Serdes core logic GND	AF10	---	---	---
S1GND14	Serdes core logic GND	AF11	---	---	---
S1GND15	Serdes core logic GND	AF12	---	---	---
S1GND16	Serdes core logic GND	AF13	---	---	---
S1GND17	Serdes core logic GND	AF14	---	---	---
S1GND18	Serdes core logic GND	AF15	---	---	---
S1GND19	Serdes core logic GND	AF16	---	---	---
S1GND20	Serdes core logic GND	AF17	---	---	---
S1GND21	Serdes core logic GND	AF18	---	---	---
S1GND22	Serdes core logic GND	AF19	---	---	---
S1GND23	Serdes core logic GND	AF20	---	---	---
S1GND24	Serdes core logic GND	AG9	---	---	---
S1GND25	Serdes core logic GND	AG12	---	---	---
S1GND26	Serdes core logic GND	AG15	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
S1GND27	Serdes core logic GND	AG18	---	---	---
S1GND28	Serdes core logic GND	AG21	---	---	---
S1GND29	Serdes core logic GND	AH9	---	---	---
S1GND30	Serdes core logic GND	AH12	---	---	---
S1GND31	Serdes core logic GND	AH15	---	---	---
S1GND32	Serdes core logic GND	AH18	---	---	---
S1GND33	Serdes core logic GND	AH21	---	---	---
AGND_SD1_PLL1	Serdes 1 PLL 1 GND	AA16	---	---	---
AGND_SD1_PLL2	Serdes 1 PLL 2 GND	AA20	---	---	---
SENSEGND	GND Sense pin	G20	---	---	---
OVDD01	General I/O supply	J11	---	OV_{DD}	---
OVDD02	General I/O supply	J12	---	OV_{DD}	---
OVDD03	General I/O supply	J13	---	OV_{DD}	---
OVDD04	General I/O supply	J14	---	OV_{DD}	---
OVDD05	General I/O supply	J15	---	OV_{DD}	---
OVDD06	General I/O supply	J16	---	OV_{DD}	---
OVDD07	General I/O supply	J17	---	OV_{DD}	---
OVDD08	General I/O supply	J18	---	OV_{DD}	---
OVDD09	General I/O supply	J19	---	OV_{DD}	---
OVDD10	General I/O supply	L8	---	OV_{DD}	---
DVDD1	UART/I2C/DMA supply	N8	---	DV_{DD}	---
DVDD2	UART/I2C/DMA supply	P8	---	DV_{DD}	---
DVDD3	UART/I2C/DMA supply	R8	---	DV_{DD}	---
CVDD	eSPI supply	M8	---	CV_{DD}	---
LVDD1	Ethernet controllers (RGMII), EMI2 and GPIO supply	T8	---	LV_{DD}	---
LVDD2	Ethernet controllers (RGMII), EMI2 and GPIO supply	U8	---	LV_{DD}	---
LVDD3	Ethernet controllers (RGMII), EMI2 and GPIO supply	V8	---	LV_{DD}	---
LVDD4	Ethernet controllers (RGMII), EMI2 and GPIO supply	W8	---	LV_{DD}	---
G1VDD01	DDR supply	D27	---	$G1V_{DD}$	---
G1VDD02	DDR supply	F27	---	$G1V_{DD}$	---
G1VDD03	DDR supply	H27	---	$G1V_{DD}$	---
G1VDD04	DDR supply	K21	---	$G1V_{DD}$	---
G1VDD05	DDR supply	K27	---	$G1V_{DD}$	---
G1VDD06	DDR supply	L21	---	$G1V_{DD}$	---
G1VDD07	DDR supply	M21	---	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD08	DDR supply	M27	---	$G1V_{DD}$	---
G1VDD09	DDR supply	N21	---	$G1V_{DD}$	---
G1VDD10	DDR supply	P21	---	$G1V_{DD}$	---
G1VDD11	DDR supply	P27	---	$G1V_{DD}$	---
G1VDD12	DDR supply	R21	---	$G1V_{DD}$	---
G1VDD13	DDR supply	T21	---	$G1V_{DD}$	---
G1VDD14	DDR supply	U21	---	$G1V_{DD}$	---
G1VDD15	DDR supply	U27	---	$G1V_{DD}$	---
G1VDD16	DDR supply	W27	---	$G1V_{DD}$	---
G1VDD17	DDR supply	AA27	---	$G1V_{DD}$	---
G1VDD18	DDR supply	AD27	---	$G1V_{DD}$	---
G1VDD19	DDR supply	AF27	---	$G1V_{DD}$	---
S1VDD1	SerDes1 core logic supply	W15	---	$S1V_{DD}$	---
S1VDD2	SerDes1 core logic supply	W16	---	$S1V_{DD}$	---
S1VDD3	SerDes1 core logic supply	W17	---	$S1V_{DD}$	---
S1VDD4	SerDes1 core logic supply	W18	---	$S1V_{DD}$	---
S1VDD5	SerDes1 core logic supply	W19	---	$S1V_{DD}$	---
S1VDD6	SerDes1 core logic supply	W20	---	$S1V_{DD}$	---
S1VDD7	SerDes1 core logic supply	Y13	---	$S1V_{DD}$	---
X1VDD1	SerDes1 transceiver supply	AC9	---	$X1V_{DD}$	---
X1VDD2	SerDes1 transceiver supply	AC12	---	$X1V_{DD}$	---
X1VDD3	SerDes1 transceiver supply	AC15	---	$X1V_{DD}$	---
X1VDD4	SerDes1 transceiver supply	AC18	---	$X1V_{DD}$	---
X1VDD5	SerDes1 transceiver supply	AC21	---	$X1V_{DD}$	---
FA_VL	Reserved for internal use only	G18	---	FA_VL	15
PROG_MTR	Reserved for internal use only	F11	---	PROG_MTR	15
PROG_SFP	Security Fuse Programming Override supply	F12	---	PROG_SFP	---
TH_VDD	Thermal Monitor Unit supply	G9	---	TH_V_{DD}	---
VDD01	Supply for cores and platform	K11	---	V_{DD}	---
VDD02	Supply for cores and platform	K13	---	V_{DD}	---
VDD03	Supply for cores and platform	K15	---	V_{DD}	---
VDD04	Supply for cores and platform	K17	---	V_{DD}	---
VDD05	Supply for cores and platform	K19	---	V_{DD}	---
VDD06	Supply for cores and platform	L10	---	V_{DD}	---
VDD07	Supply for cores and platform	L12	---	V_{DD}	---
VDD08	Supply for cores and platform	L14	---	V_{DD}	---
VDD09	Supply for cores and platform	L16	---	V_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD10	Supply for cores and platform	L18	---	V_{DD}	---
VDD11	Supply for cores and platform	L20	---	V_{DD}	---
VDD12	Supply for cores and platform	M9	---	V_{DD}	---
VDD13	Supply for cores and platform	M11	---	V_{DD}	---
VDD14	Supply for cores and platform	M13	---	V_{DD}	---
VDD15	Supply for cores and platform	M15	---	V_{DD}	---
VDD16	Supply for cores and platform	M17	---	V_{DD}	---
VDD17	Supply for cores and platform	M19	---	V_{DD}	---
VDD18	Supply for cores and platform	N10	---	V_{DD}	---
VDD19	Supply for cores and platform	N12	---	V_{DD}	---
VDD20	Supply for cores and platform	N14	---	V_{DD}	---
VDD21	Supply for cores and platform	N16	---	V_{DD}	---
VDD22	Supply for cores and platform	N18	---	V_{DD}	---
VDD23	Supply for cores and platform	N20	---	V_{DD}	---
VDD24	Supply for cores and platform	P9	---	V_{DD}	---
VDD25	Supply for cores and platform	P11	---	V_{DD}	---
VDD26	Supply for cores and platform	P13	---	V_{DD}	---
VDD27	Supply for cores and platform	P15	---	V_{DD}	---
VDD28	Supply for cores and platform	P17	---	V_{DD}	---
VDD29	Supply for cores and platform	P19	---	V_{DD}	---
VDD30	Supply for cores and platform	R10	---	V_{DD}	---
VDD31	Supply for cores and platform	R12	---	V_{DD}	---
VDD32	Supply for cores and platform	R14	---	V_{DD}	---
VDD33	Supply for cores and platform	R16	---	V_{DD}	---
VDD34	Supply for cores and platform	R18	---	V_{DD}	---
VDD35	Supply for cores and platform	R20	---	V_{DD}	---
VDD36	Supply for cores and platform	T9	---	V_{DD}	---
VDD37	Supply for cores and platform	T11	---	V_{DD}	---
VDD38	Supply for cores and platform	T13	---	V_{DD}	---
VDD39	Supply for cores and platform	T15	---	V_{DD}	---
VDD40	Supply for cores and platform	T17	---	V_{DD}	---
VDD41	Supply for cores and platform	T19	---	V_{DD}	---
VDD42	Supply for cores and platform	U10	---	V_{DD}	---
VDD43	Supply for cores and platform	U12	---	V_{DD}	---
VDD44	Supply for cores and platform	U14	---	V_{DD}	---
VDD45	Supply for cores and platform	U16	---	V_{DD}	---
VDD46	Supply for cores and platform	U18	---	V_{DD}	---
VDD47	Supply for cores and platform	U20	---	V_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD48	Supply for cores and platform	V9	---	V_{DD}	---
VDD49	Supply for cores and platform	V11	---	V_{DD}	---
VDD50	Supply for cores and platform	V13	---	V_{DD}	---
VDD51	Supply for cores and platform	V15	---	V_{DD}	---
VDD52	Supply for cores and platform	V17	---	V_{DD}	---
VDD53	Supply for cores and platform	V19	---	V_{DD}	---
VDD54	Supply for cores and platform	W10	---	V_{DD}	---
VDD55	Supply for cores and platform	W12	---	V_{DD}	---
VDD56	Supply for cores and platform	W14	---	V_{DD}	---
VDD57	Supply for cores and platform	Y8	---	V_{DD}	---
VDD58	Supply for cores and platform	Y9	---	V_{DD}	---
VDD59	Supply for cores and platform	Y11	---	V_{DD}	---
VDD_LP	Low Power Security Monitor supply	P6	---	V_{DD}_LP	---
AVDD_CGA1	e6500 Cluster Group A PLL1 supply	G11	---	AVDD_CGA1	---
AVDD_CGA2	e6500 Cluster Group A PLL2 supply	G12	---	AVDD_CGA2	---
AVDD_PLAT	Platform PLL supply	G10	---	AVDD_PLAT	---
AVDD_D1	DDR1 PLL supply	E20	---	AVDD_D1	---
AVDD_SD1_PLL1	SerDes 1 PLL 1 supply	AB16	---	AVDD_SD1_PLL1	---
AVDD_SD1_PLL2	SerDes 1 PLL 2 supply	AB20	---	AVDD_SD1_PLL2	---
SENSEVDD	Vdd Sense pin	G19	---	SENSEVDD	---
USB_HVDD1	USB PHY Transceiver 3.3V Supply	J8	---	USB_HV_{DD}	---
USB_HVDD2	USB PHY Transceiver 3.3V Supply	K8	---	USB_HV_{DD}	---
USB_OVDD1	USB PHY Transceiver 1.8V Supply	J9	---	USB_OV_{DD}	---
USB_OVDD2	USB PHY Transceiver 1.8V Supply	J10	---	USB_OV_{DD}	---
USB_SVDD1	USB PHY Analog 1.0V Supply	K9	---	USB_SV_{DD}	---
USB_SVDD2	USB PHY Analog 1.0V Supply	K10	---	USB_SV_{DD}	---
No Connection Pins					
NC01	No Connection	F14	---	---	12
NC02	No Connection	G6	---	---	12
NC03	No Connection	G14	---	---	12
NC04	No Connection	G17	---	---	12
NC05	No Connection	H6	---	---	12
NC06	No Connection	J6	---	---	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
NC07	No Connection	M4	---	---	12
NC08	No Connection	N4	---	---	12
NC09	No Connection	N6	---	---	12
NC10	No Connection	P3	---	---	12
NC11	No Connection	P4	---	---	12
NC12	No Connection	R1	---	---	12
NC13	No Connection	R2	---	---	12
NC14	No Connection	R3	---	---	12
NC15	No Connection	R4	---	---	12
NC16	No Connection	T1	---	---	12
NC17	No Connection	T3	---	---	12
NC18	No Connection	T4	---	---	12
NC19	No Connection	T6	---	---	12
NC20	No Connection	U1	---	---	12
NC21	No Connection	U2	---	---	12
NC22	No Connection	U4	---	---	12
NC23	No Connection	U6	---	---	12
NC24	No Connection	V6	---	---	12
NC25	No Connection	W6	---	---	12
NC26	No Connection	Y6	---	---	12
NC27	No Connection	Y21	---	---	12
NC28	No Connection	AA6	---	---	12
NC29	No Connection	AA7	---	---	12
NC30	No Connection	AA8	---	---	12
NC31	No Connection	AA9	---	---	12
NC32	No Connection	AA10	---	---	12
NC33	No Connection	AB8	---	---	12
NC34	No Connection	AB9	---	---	12
NC35	No Connection	AB10	---	---	12
NC36	No Connection	AB11	---	---	12
NC37	No Connection	AB12	---	---	12
NC38	No Connection	AC1	---	---	12
NC39	No Connection	AC2	---	---	12
NC40	No Connection	AC4	---	---	12
NC_DET	No Connection	AG28	---	---	12

1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.

2. This output is actively driven during reset rather than being tri-stated during reset.

3. MDIC[0] is grounded through a 187 Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through a 187 Ω precision 1% resistor. For either full or half driver strength calibration of DDR I/Os, use the same MDIC resistor value of 187 Ω. Memory controller register setting can be used to determine automatic calibration is done to full or half drive strength. These pins are used for automatic calibration of the DDR3/DDR3L I/Os. The MDIC[0:1] pins must be connected to 187 Ω precision 1% resistors.

4. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the device is in its reset state. This pull-up is designed to be overpowered by an external 4.7 kΩ resistor. If the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.

5. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.

6. Recommend that a weak pull-up resistor (4.7 kΩ) be placed on this pin to the respective power supply.

7. This pin is an open-drain signal.

8. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.

9. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.

10. This is a test signal for factory use only and must be pulled up (100 Ω to 1 kΩ) to the respective power supply for normal operation.

11. This pin requires a 200 Ω pull-up to respective power supply.

12. Do not connect. This pin should be left floating.

13. These pins must be pulled up to 1.2 V through a 180 Ω ± 1% resistor for MDC and a 330 Ω ± 1% resistor for MDIO.

14. This pin requires an external 1 kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

15. Must be pulled to ground (GND).

16. This pin requires a 698 Ω pull-up to respective power supply.

17. This pin should be tied to ground if the diode is not utilized for temperature monitoring.

18. If used as an SDHC signal, pull up 10 kΩ to 100 kΩ to the respective I/O supply.

19. New board designs should leave a placeholder for a parallel series resistor and capacitor filter to be used in very close proximity to the USB_IBAIS_REXT pin of NXP QorIQ chips. When needed, this allows for flexibility in populating them, which helps avoid board-coupled noise to this pin. A 100 nF low-ESL SMD ceramic chip capacitor in series with a 100 Ω SMD resistor performs the needed filtration with slight variations that suit each board case.

Warning

See **"Connection Recommendations"** for additional details on properly connecting these pins for specific applications.

3 Electrical characteristics

This section provides the AC and DC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings.

Table 2. Absolute maximum ratings[1]

Characteristic	Symbol	Max Value	Unit	Notes
Core and platform supply voltage	V_{DD}	-0.3 to 1.1	V	2
PLL supply voltage (core, platform, DDR)	AV_{DD}_CGA1	-0.3 to 1.98	V	—

Table continues on the next page...

Table 2. Absolute maximum ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Notes
		AV_{DD}_CGA2 AV_{DD}_PLAT AV_{DD}_D1			
PLL supply voltage (SerDes, filtered from $X1V_{DD}$)		AV_{DD}_SD1_PLL1	-0.3 to 1.48	V	—
Fuse programming override supply		PROG_SFP	-0.3 to 1.98	V	—
Thermal monitor unit supply		TH_V_{DD}	-0.3 to 1.98	V	—
eSHDC, MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage		OV_{DD}	-0.3 to 1.98	V	—
eSPI		CV_{DD}	-0.3 to 2.75 -0.3 to 1.98	V	—
DMA, DUART, I^2C I/O voltage		DV_{DD}	-0.3 to 2.75 -0.3 to 1.98	V	—
DDR3 and DDR3L DRAM I/O voltage		$G1V_{DD}$	-0.3 to 1.65 -0.3 to 1.45	V	—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers		$S1V_{DD}$	-0.3 to 1.1	V	—
Pad power supply for SerDes transmitters		$X1V_{DD}$	-0.3 to 1.45	V	
Ethernet I/O, Ethernet management interface 1 (EMI1) 1588, GPIO I/O voltage		LV_{DD}	-0.3 to 2.75 -0.3 to 1.98	V	—
Ethernet management interface 2 (EMI2) I/O voltage		—	-0.3 to 1.32	V	4
USB PHY Transceiver supply voltage		USB_HV_{DD}	-0.3 to 3.63	V	—
		USB_OV_{DD}	-0.3 to 1.98	V	—
USB PHY Analog supply voltage		USB_SV_{DD}	-0.3 to 1.1	V	—
Low Power Security Monitor supply		V_{DD_LP}	-0.3 to 1.1	V	—
Input voltage	DDR3 and DDR3L DRAM signals	MV_{IN}	-0.3 to (GV_{DD} + 0.3)	V	5
	DDR3 and DDR3L DRAM reference	$D1\_MV_{REF}$	-0.3 to (GV_{DD}/2+ 0.3)	V	6
	Ethernet signals (except EMI2)	LV_{IN}	-0.3 to (LV_{DD} + 0.3)	V	6, 7
	eSHDC, MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG signals	OV_{IN}	-0.3 to (OV_{DD} + 0.3)	V	6, 8
	eSPI	CV_{IN}	-0.3 to (CV_{DD} + 0.3)	V	6, 8
	DMA, DUART, I^2C signals	DV_{IN}	-0.3 to (DV_{DD} + 0.3)	V	8, 9
	SerDes signals	SV_{IN}	-0.4 to (SV_{DD} + 0.3)	V	6
	USB PHY Transceiver signals	USB_HV_{IN}	-0.3 to (USB_HV_{DD} + 0.3)	V	6
		USB_OV_{IN}	-0.3 to (USB_OV_{DD} + 0.3)	V	6
	Ethernet management interface 2 signals	-	-0.3 to (1.2 + 0.3)	V	—
Storage temperature range		T_{STG}	-55 to 150	°C	—

Table continues on the next page...

Table 2. Absolute maximum ratings[1] (continued)

Characteristic	Symbol	Max Value	Unit	Notes

Notes:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.

4. Ethernet MII management interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels.

5. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

6. (C, S,G,L,O,D)V_{IN}, USBn_V_{IN}_3P3, USBn_V_{IN}_1P8 and D1_MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

7. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

8. **Caution:** CV_{IN} and OV_{IN} must not exceed CV_{DD} and OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

9. **Caution:** DV_{IN} must not exceed DV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this chip.

NOTE

The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 3. Recommended operating conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Core and platform supply voltage	At initial start-up	V_{DD}	1.025 ± 30 mV	V	1, 2, 3, 7
	During normal operation		VID ± 30 mV	V	1, 2, 3, 7
PLL supply voltage (core, platform, DDR)		AV_{DD}_CGA1 AV_{DD}_CGA2 AV_{DD}_PLAT AV_{DD}_D1	1.8 V ± 90 mV	V	8
PLL supply voltage (SerDes, filtered from $X1V_{DD}$)		AV_{DD}_SD1_PLLn (n = 1 or 2)	1.35 V ± 67 mV	V	—

Table continues on the next page...

Table 3. Recommended operating conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Fuse programming override supply		PROG_SFP	1.80 V ± 90 mV	V	4
Thermal monitor unit supply		TH_V_{DD}	1.8 V ± 90 mV	V	—
eSHDC, MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage		OV_{DD}	1.8 V ± 90 mV	V	—
eSPI		CV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
DMA, DUART, I²C I/O voltage		DV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
DDR DRAM I/O voltage	DDR3	$G1V_{DD}$	1.5 V ± 75 mV	V	—
	DDR3L		1.35 V ± 67 mV		
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers		$S1V_{DD}$	1.0 V + 50 mV 1.0 V - 30 mV	V	—
Pad power supply for SerDes transmitters		$X1V_{DD}$	1.35 V ± 67 mV	V	—
Ethernet , Ethernet management interface 1 (EMI1), 1588, GPIO I/O voltage		LV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	5
Ethernet management interface 2 (EMI2) I/O voltage		—	1.2 V ± 60 mV	V	—
USB PHY Transceiver supply voltage		USB_HV_{DD}	3.3 V ± 165 mV	V	—
		USB_OV_{DD}	1.8 V ± 90 mV	V	—
USB PHY Analog supply voltage	At initial start-up	USB_SV_{DD}	1.025 ± 30 mV	V	1, 3
	During normal operation		VID ± 30 mV		
Low Power Security Monitor supply		V_{DD_LP}	1.0 V ± 50 mV	V	—
Input voltage	DDR3 and DDR3L DRAM signals	MV_{IN}	GND to GV_{DD}	V	—
	DDR3 and DDR3L DRAM reference	$D1\_MV_{REF}$	$GV_{DD}/2$ ± 1%	V	—
	Ethernet signals (except EMI2), USB, 1588, GPIO signals	LV_{IN}	GND to LV_{DD}	V	—
	eSHDC, MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	—
	eSPI	CV_{IN}	GND to CV_{DD}	V	—
	DMA, DUART, I²C signals	DV_{IN}	GND to DV_{DD}	V	—
	SerDes signals	SV_{IN}	GND to SV_{DD}	V	—
	USB PHY Transceiver signals	USB_HV_{IN}	GND to USB_HV_{DD}	V	—
		USB_OV_{IN}	GND to USB_OV_{DD}	V	—
	Ethernet management interface 2 (EMI2) signals	—	GND to 1.2V	V	6
Operating temperature range	Normal operation	T_A, T_J	T_A = 0 (min) to T_J = 105(max)	°C	—
	Extended Temperature	T_A,	T_A = -40 (min) to	°C	—

Table continues on the next page...

Table 3. Recommended operating conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
		T_J	T_J = 105(max)		
	Secure boot fuse programming	T_A, T_J	T_A = 0 (min) to T_J = 70 (max)	°C	4

Notes:

1. See Voltage ID (VID) controllable supply and Core and platform supply voltage filtering for additional information.

2. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.

3. Operation at 1.1 V is allowable for up to 25 ms at initial power on.

4. PROG_SFP must be supplied 1.80 V and the chip must operate in the specified fuse programming temperature range (0 - 70°C) only during secure boot fuse programming. For all other operating conditions, PROG_SFP must be tied to GND, subject to the power sequencing constraints shown in Power sequencing.

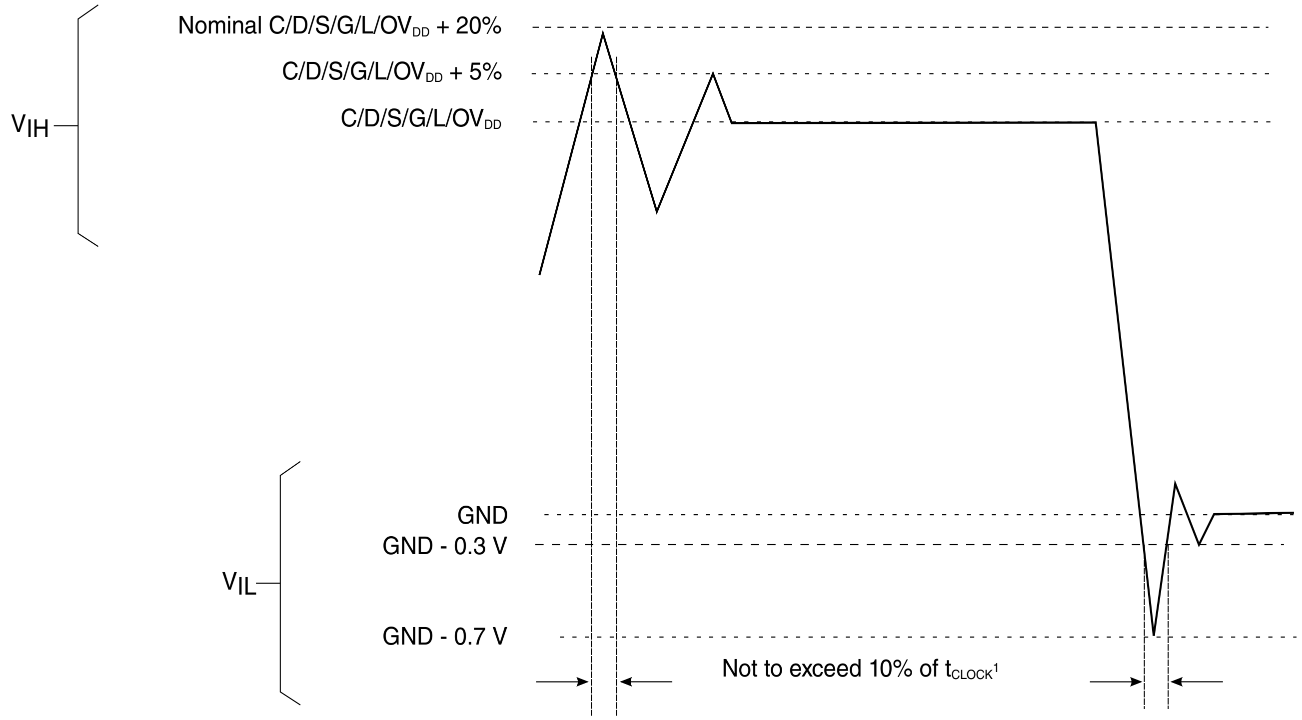
5. Selecting RGMII limits to LV_{DD} = 2.5 V.

6. Ethernet MII management interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels.

7. Voltage ID (VID) operating range is between 0.975 to 1.025V. Regulator selection should be based on Vout range of at least 0.9 to 1.1 V, with resolution of 12.5 mV or better.

8. Keep the filter close to the pin. Voltage and tolerance for AV_{DD} is defined at the input of the PLL supply filter and not the pin of AV_{DD}.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Note:

t_{CLOCK} refers to the clock period associated with the respective interface:
For I[2]C ODV_{DD}, t_{CLOCK} references SYSCLK.
For DDR GV_{DD}, t_{CLOCK} references Dn_MCLK.
For eSPI OCV_{DD}, t_{CLOCK} references SPI_CLK.
For JTAG OV_{DD}, t_{CLOCK} references TCK.
For SerDes SV_{DD}, t_{CLOCK} references SD_REF_CLK.
For Ethernet LV_{DD}, t_{CLOCK} references ECn_GTX_CLK125.

Figure 7. Overshoot/Undershoot voltage for CV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}/SV_{DD}/DV_{DD}

The core and platform voltages must always be provided at nominal VID. See Table 3 for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. DV_{DD}, OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied D1_MV_{REF} signal (nominally set to GV_{DD}/2) as is appropriate for the SSTL_1.35/SSTL_1.5 electrical signaling standard. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

3.1.3 Output driver characteristics

This chip provides information on the characteristics of the output driver strengths.

NOTE

These values are preliminary estimates.

Table 4. Output drive capability

Driver type	Output impedance (Ω)			Supply Voltage	Notes
	Minimum[2]	Typical	Maximum[3]		
DDR3 signal	—	18 (full-strength mode) 27 (half-strength mode)	—	$G1V_{DD}$ = 1.5 V	1
DDR3L signal	—	18 (full-strength mode) 27 (half-strength mode)	—	$G1V_{DD}$ = 1.35 V	1
Ethernet signals	45	—	90	$L1V_{DD}$ / LV_{DD} = 3.3 V	—
	40	—	90	$L1V_{DD}$ / LV_{DD} = 2.5 V	
	40	—	75	$L1V_{DD}$ / LV_{DD} = 1.8 V	
MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage	23	—	51	OV_{DD}, $O1V_{DD}$ = 1.8 V	—
DUART, DMA, MPIC, QE, TDM, I^2C, DIU	45	—	90	DV_{DD} = 3.3 V	—
	40	—	90	DV_{DD} = 2.5 V	
	40	—	75	DV_{DD} = 1.8 V	
eSPI, SDHC_WP, SDHC_CD	45	—	90	CV_{DD} = 3.3 V	—
	40	—	75	CV_{DD} = 1.8 V	
eSDHC	45	—	90	EV_{DD} = 3.3 V	—
	40	—	75	EV_{DD} = 1.8 V	

Notes:

1. The drive strength of the DDR3 or DDR3L interface in half-strength mode is at T_j = 105 °C and at $G1V_{DD}$ (min).
2. Estimated number based on best case processed device.
3. Estimated number based on worst case processed device.

3.2 Power sequencing

The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation. For power up, these requirements are as follows:

1. Bring up V_{DD}, $S1V_{DD}$, USB_SV_{DD}, V_{DD}_LP, USB_HV_{DD}, LV_{DD}, DV_{DD}, CV_{DD}, USB_OV_{DD}, OV_{DD}, TH_V_{DD}, AV_{DD} (cores, platform, DDR), $G1V_{DD}$, $X1V_{DD}$, and AV_{DD}_ SD1_PLLn. Drive PROG_SFP = GND.
    - PORESET_B input must be driven asserted and held during this step.

Power supplies in step 1 have no ordering requirement with respect to one another except for the USB power supplies per the following note.

NOTE

a. USB_SV_{DD} supply must ramp before or after the USB_HV_{DD} and USB_OV_{DD} supplies have ramped. The supply set that ramp first must reach 90% of its final value before a supply from the other set can be ramped up.
b. USB_HV_{DD} and USB_OV_{DD} supplies among themselves are sequence independent.
c. USB_HV_{DD} rise time (10% to 90%) has a minimum of 100 us.

2. Negate PORESET_B input as long as the required assertion/hold time has been met per Table 19.
3. For secure boot fuse programming, use the following steps:
   a. After negation of PORESET_B, drive PROG_SFP = 1.80 V after a required minimum delay per Table 5.
   b. After fuse programming is completed, it is required to return PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 5. See Security fuse processor, for additional details.

Warning

No activity other than that required for secure boot fuse programming is permitted while PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while PROG_SFP = GND.

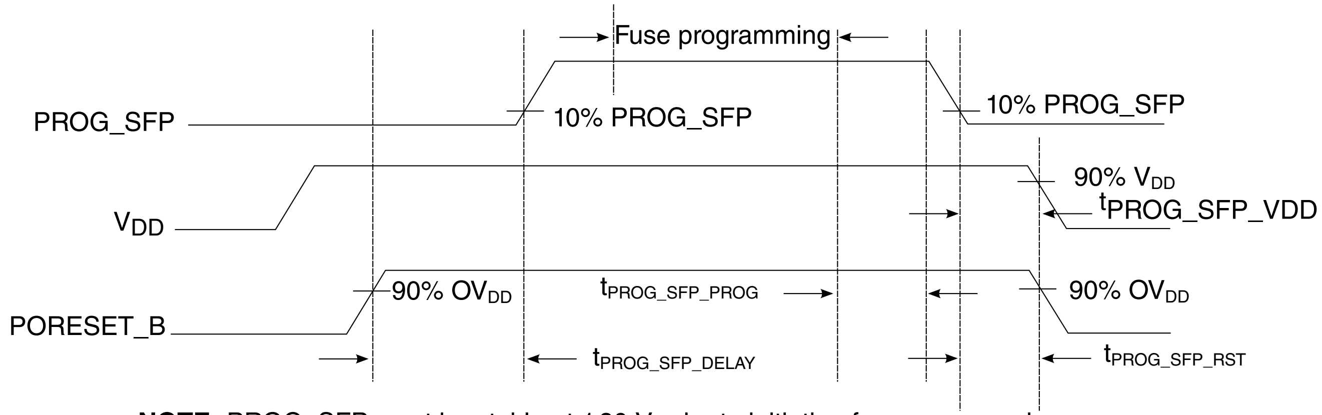
From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} supplies, there will be a brief period as the V_{DD} powers up that the I/Os associated with that I/O supply may go from being tri-stated to an indeterminate state (either driven to a logic one or zero) and extra current may be drawn by the device.

Only 300,000 POR cycles are permitted per lifetime of a device. Note that this value is based on design estimates and is preliminary.

If using Trust Architecture Security Monitor battery-backed features, prior to V_{DD} ramping up to the 0.5 V level, ensure that OV_{DD} is ramped to the recommended operational voltage and SYSCLK is running. The clock should have a minimum frequency of 800 Hz and a maximum frequency no greater than the supported system clock frequency for the device.

All supplies must be at their stable values within 400 ms.

This figure provides the PROG_SFP timing diagram.



NOTE: PROG_SFP must be stable at 1.80 V prior to initiating fuse programming.

Figure 8. PROG_SFP timing diagram

This table provides information on the power-down and power-up sequence parameters for PROG_SFP.

Table 5. PROG_SFP timing [5]

Driver type	Min	Max	Unit	Notes
$t_{PROG\_SFP\_DELAY}$	100	—	SYSCLKs	1
$t_{PROG\_SFP\_PROG}$	0	—	μs	2
$t_{PROG\_SFP\_VDD}$	0	—	μs	3
$t_{PROG\_SFP\_RST}$	0	—	μs	4

Notes:

1. Delay required from the deassertion of PORESET_B to driving PROG_SFP ramp up. Delay measured from PORESET_B deassertion at 90% OV_{DD} to 10% PROG_SFP ramp up.

2. Delay required from fuse programming finished to PROG_SFP ramp down start. Fuse programming must complete while PROG_SFP is stable at 1.80 V. No activity other than that required for secure boot fuse programming is permitted while PROG_SFP driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while PROG_SFP = GND. After fuse programming is completed, it is required to return PROG_SFP = GND.

3. Delay required from PROG_SFP ramp down complete to V_{DD} ramp down start. PROG_SFP must be grounded to minimum 10% PROG_SFP before V_{DD} is at 90% V_{DD}.

4. Delay required from PROG_SFP ramp down complete to PORESET_B assertion. PROG_SFP must be grounded to minimum 10% PROG_SFP before PORESET_B assertion reaches 90% OV_{DD}.

5. Only two secure boot fuse programming events are permitted per lifetime of a device.

3.3 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Power sequencing, it is required that PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 5.

NOTE

All input signals, including I/Os that are configured as inputs, driven into the chip need to monotonically increase/decrease through entire rise/fall durations.

3.4 Power characteristics

This table shows the power dissipations of the V_{DD} and $S1V_{DD}$ supply for various operating platform clock frequencies versus the core and DDR clock frequencies when Altivec power is gated off. See the e6500 core reference manual, section 8.6.1, "Altivec power down—software controlled entry" for details on how to place Altivec in low power state.

Table 6. T2081 power dissipation with Altivec power-gated off[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	FMan freq (MHz)	V_{DD}[8] (V)	$S1V_{DD}$ (V)	Junction temperature (°C)	Core and platform power[1] (W)	V_{DD} power (W)	$S1V_{DD}$ power (W)	Notes
Typical	1800 (low-power version)	600	2133	700	VID	1.0	65	12.5	11.9	0.6	2, 3, 9
Thermal							105	18.4	17.8	0.6	4, 5, 9
Maximum								20.6	20.0	0.6	5, 6, 7, 9
Typical	1800 (standard version)	600	1867	700	VID	1.0	65	12.6	12.0	0.6	2, 3
Thermal							105	20.6	20.0	0.6	4, 5
Maximum								22.8	22.2	0.6	5, 6, 7
Typical	1533 (low-power version)	600	2133	700	VID	1.0	65	11.5	10.9	0.6	2, 3, 9
Thermal							105	14.9	14.3	0.6	4, 5, 9
Maximum								16.8	16.2	0.6	5, 6, 7, 9

Table continues on the next page...

Table 6. T2081 power dissipation with Altivec power-gated off[1] (continued)

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	FMan freq (MHz)	V_{DD}[8] (V)	$S1V_{DD}$ (V)	Junction temperature (°C)	Core and platform power[1] (W)	V_{DD} power (W)	$S1V_{DD}$ power (W)	Notes
Typical	1533 (standard version)	600	1867	700	VID	1.0	65	11.5	10.9	0.6	2, 3
Thermal							105	16.7	16.1	0.6	4, 5
Maximum								18.6	18.0	0.6	5, 6, 7
Typical	1200 (low-power version)	533	1600	600	VID	1.0	65	10.0	9.4	0.6	2, 3, 9
Thermal							105	12.0	11.4	0.6	4, 5, 9
Maximum								13.4	12.8	0.6	5, 6, 7, 9
Typical	1200 (standard version)	533	1600	600	VID	1.0	65	10.0	9.4	0.6	2, 3
Thermal							105	13.3	12.7	0.6	4, 5
Maximum								14.7	14.1	0.6	5, 6, 7

Notes:

1. Combined power of V_{DD} and $S1V_{DD}$ with platform at power-on reset default state, the DDR controller and all SerDes banks active. Does not include I/O power and Altivec is power-gated off.
2. Typical power assumes Dhrystone running with activity factor of 70% (on all cores) and is executing DMA on the platform with 100% activity factor.
3. Typical power based on nominal, processed device.
4. Thermal power assumes Dhrystone running with activity factor of 70% (on all cores) and executing DMA on the platform at 100% activity factor.
5. Thermal and maximum power are based on worst-case processed device.
6. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and is executing DMA on the platform at 115% activity factor.
7. Maximum power provided for power supply design sizing.
8. Voltage ID (VID) operating range is between 0.975 V to 1.025 V.
9. The difference between low-power and standard is shown in the product part number. The low-power version part numbers end in "T1B", "P1B", and "QLB".

This table shows the power dissipation of the V_{DD} and SnV_{DD} supply for various operating platform clock frequencies versus the core and DDR clock frequencies when Altivec power is gated on. See the e6500 core reference manual, section 8.6.4, "Altivec power up—software-controlled entry" for details on how to enable Altivec.

Table 7. T2081 power dissipation with Altivec power-gated on[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	FMan freq (MHz)	V_{DD}[8] (V)	$S1V_{DD}$ (V)	Junction temperature (°C)	Core and platform power[1] (W)	V_{DD} power (W)	$S1V_{DD}$ power (W)	Notes
Typical	1800	600	2133	700	VID	1.0	65	13.4	12.8	0.6	2, 3, 9

Table continues on the next page...

Table 7. T2081 power dissipation with Altivec power-gated on[1] (continued)

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	FMan freq (MHz)	V_{DD}[8] (V)	$S1V_{DD}$ (V)	Junction temperature (ºC)	Core and platform power[1] (W)	V_{DD} power (W)	$S1V_{DD}$ power (W)	Notes
Thermal	(low-power version)						105	19.7	19.1	0.6	4, 5, 9
Maximum								21.8	21.2	0.6	5, 6, 7, 9
Typical	1800 (standard version)	600	1867	700	VID	1.0	65	13.5	12.9	0.6	2, 3
Thermal							105	21.9	21.3	0.6	4, 5
Maximum								24.0	23.4	0.6	5, 6, 7
Typical	1533 (low-power version)	600	2133	700	VID	1.0	65	12.3	11.7	0.6	2, 3, 9
Thermal							105	15.8	15.2	0.6	4, 5, 9
Maximum								17.6	17.0	0.6	5, 6, 7, 9
Typical	1533 (standard version)	600	1867	700	VID	1.0	65	12.3	11.7	0.6	2, 3
Thermal							105	17.7	17.1	0.6	4, 5
Maximum								19.5	18.9	0.6	5, 6, 7
Typical	1200 (low-power version)	533	1600	600	VID	1.0	65	10.6	10.0	0.6	2, 3, 9
Thermal							105	12.7	12.1	0.6	4, 5, 9
Maximum								14.0	13.4	0.6	5, 6, 7, 9
Typical	1200 (standard version)	533	1600	600	VID	1.0	65	10.6	10.0	0.6	2, 3
Thermal							105	14.1	13.5	0.6	4, 5
Maximum								15.4	14.8	0.6	5, 6, 7

Notes:

1. Combined power of V_{DD} and $S1V_{DD}$ with platform at power-on reset default state, the DDR controller and all SerDes banks active. Does not include I/O power and Altivec is power-gated off.

2. Typical power assumes Dhrystone running with activity factor of 70% (on all cores) and is executing DMA on the platform with 100% activity factor.

3. Typical power based on nominal, processed device.

4. Thermal power assumes Dhrystone running with activity factor of 70% (on all cores) and executing DMA on the platform at 100% activity factor.

5. Thermal and maximum power are based on worst-case processed device.

6. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and is executing DMA on the platform at 115% activity factor.

7. Maximum power provided for power supply design sizing.

8. Voltage ID (VID) operating range is between 0.975 V to 1.025 V.

9. The difference between low-power and standard is shown in the product part number. The low-power version part numbers end in "T1B", "P1B", and "QLB".

This table provides all the estimated I/O power supply values based on preliminary measurements.

Table 8. T2081 I/O power dissipation

I/O Power supply		Parameter	Typical (mW)	Maximum (mW)	Notes
LVCMOS	OV_{DD} 1.8 V	—	50	60	1, 3, 4, 6
LVCMOS	CV_{DD} 1.8 V	—	40	70	
LVCMOS	CV_{DD} 2.5 V	—	50	80	
LVCMOS	LV_{DD} 1.8 V	—	230	360	
LVCMOS	LV_{DD} 2.5 V	—	310	440	
LVCMOS	DV_{DD} 1.8 V	—	50	90	
LVCMOS	DV_{DD} 2.5 V	—	70	130	
DDR I/O	GV_{DD} 1.5 V	2133 MT/s	1144	2200	1, 2, 5, 6
DDR I/O	GV_{DD} 1.35 V	1867 MT/s	840	1610	
DDR I/O	GV_{DD} 1.5 V	1867 MT/s	1030	1990	
DDR I/O	GV_{DD} 1.35 V	1600 MT/s	720	1380	
DDR I/O	GV_{DD} 1.5 V	1600 MT/s	890	1700	
USB_PHY	USB_OV_{DD} 1.8 V	—	40	60	1, 6
USB_PHY	USB_HV_{DD} 3.3 V	—	100	110	
USB_SV_{DD}	USB_SV_{DD}	—	7	7	
PLL core and system	AVDD_CGA*, AVDD_PLAT	—	20	20	1, 6
PLL DDR	AVDD_D1	—	30	40	
PLL LYNX	AVDD_SRDS*	—	50	50	
SerDes, 1.35 V	XV_{DD} SGMII	1x 1.25 G-baud	50	60	1, 6, 7
SerDes, 1.35 V	XV_{DD}	2x 1.25 G-baud	70	90	
SerDes, 1.35 V	XV_{DD}	4x 1.25 G-baud	130	140	
SerDes, 1.35 V	XV_{DD}	8x 1.25 G-baud	230	240	
SerDes, 1.35 V	XV_{DD}	1x 3.125 G-baud	50	60	
SerDes, 1.35 V	XV_{DD}	2x 3.125 G-baud	80	90	
SerDes, 1.35 V	XV_{DD}	4x 3.125 G-baud	140	150	
SerDes, 1.35 V	XV_{DD} SATA	1x 3 G-baud	50	60	
SerDes, 1.35 V	XV_{DD}	2x 3 G-baud	70	80	
SerDes, 1.35 V	XV_{DD} SRIO	1x 2.5 G-baud	50	60	
SerDes, 1.35 V	XV_{DD}	2x 2.5 G-baud	80	90	
SerDes, 1.35 V	XV_{DD}	4x 2.5 G-baud	140	150	
SerDes, 1.35 V	XV_{DD}	1x 3.125 G-baud	50	60	
SerDes, 1.35 V	XV_{DD}	2x 3.125 G-baud	80	90	
SerDes, 1.35 V	XV_{DD}	4x 3.125 G-baud	140	150	
SerDes, 1.35 V	XV_{DD}	1x 5 G-baud	50	70	
SerDes, 1.35 V	XV_{DD}	2x 5 G-baud	90	100	
SerDes, 1.35 V	XV_{DD}	4x 5 G-baud	150	160	
SerDes, 1.35 V	XV_{DD} PEX2.0	1x 5 G-baud	50	70	
SerDes, 1.35 V	XV_{DD}	2x 5 G-baud	90	100	
SerDes, 1.35 V	XV_{DD}	4x 5 G-baud	150	160	

Table continues on the next page...

Table 8. T2081 I/O power dissipation (continued)

I/O Power supply		Parameter	Typical (mW)	Maximum (mW)	Notes
SerDes, 1.35 V	XV_{DD}	8x 5 G-baud	280	290	
SerDes, 1.35 V	XV_{DD} PEX3.0	1x 8 G-baud	60	70	
SerDes, 1.35 V	XV_{DD}	2x 8 G-baud	100	110	
SerDes, 1.35 V	XV_{DD}	4x 8 G-baud	170	190	
SerDes, 1.35 V	XV_{DD} XFI	1x 10 G-baud	60	70	
SerDes, 1.35 V	XV_{DD}	2x 10 G-baud	100	110	
SerDes, 1.35 V	XV_{DD}	4x 10 G-baud	170	190	
Fuse Programming Override	PROG_SFG	—	—	173	1, 8
Thermal Monitor Unit	TH_V_{DD}	—	—	18	1

Notes:

1. The maximum values are dependent on actual use case such as what application, external components used, environmental conditions such as temperature voltage and frequency. This is not intended to be the maximum guaranteed power. Expect different results depending on the use case. The maximum values are estimated and they are based on simulations at 105 °C junction temperature.

2. Typical DDR power numbers are based on one 2-rank DIMM with 40% utilization.

3. Assuming 15 pF total capacitance load.

4. GPIOs are supported on 1.8 V and 2.5 V rails as specified in the hardware specification.

5. Maximum DDR power numbers are based on one 2-rank DIMM with 100% utilization.

6. The typical values are estimates and based on simulations at nominal recommended voltage for the I/O power supply and assuming at 65° C junction temperature.

7. The total power numbers of XV_{DD} is dependent on customer application use case. This table lists all the SerDes configurations possible for the device. To get the XV_{DD} power numbers, the user should add the combined lanes to match to the total SerDes Lanes used, not simply multiply the power numbers by the number of lanes.

8. The max power requirement is during programming. No active power beyond leakage levels should be drawn and the supply must be grounded when not programming.

This table shows the preliminary power dissipation on the V_{DD_LP} supply for the T2081 at allowable voltage levels.

Table 9. V_{DD_LP} Power Dissipation

Supply	Maximum	Unit	Notes
V_{DD_LP} (T2081 on, 65C)	1.5	mW	1
V_{DD_LP} (T2081 off, 65C)	360	uW	2
V_{DD_LP} (T2081 off, 40C)	132	uW	2

Notes:

1. V_{DD_LP} = 1.0 V, T_J = 65 °C

2. When T2081 is off, V_{DD_LP} may be supplied by battery power to retain the Zeroizable Master Key and other Trust Architecture state. Board should implement a PMIC which switches V_{DD_LP} to battery when SoC powered down. See T2080 Reference Manual Trust Architecture chapter for more information.

Table 10. T2081 Rev 1.1 single core/single cluster low-power mode power savings, 1.0 V 105°C[1,2,3]

Mode	Core Frequency = 1.8 GHz	Core Frequency = 1.533 GHz	Core Frequency = 1.2 GHz	Units	Comments	Notes
PH10	0.96	0.82	0.64	Watts	Savings realized moving from PH00 to PH10 state, single core	1, 2, 4
PH15	0.27	0.23	0.19	Watts	Savings realized moving from PH10 to PH15 state, single core	1, 4, 5
PH20	0.37	0.35	0.34	Watts	Savings realized moving from PH15 to PH20 state, single core	1, 4
PCL10	0.95	0.91	0.73	Watts	Savings realized moving from PH20 to PCL10 state, single cluster	1
LPM20	0.90	0.82	0.72	Watts	Savings realized moving from PCL10 to LPM20 state	1
LPM40	0.60	0.49	0.35	Watts	Savings realized moving from LPM20 to LPM40 state, single cluster	1

Notes:

1. Power for V_{DD} only.

2. Typical power assumes Dhrystone running (PH00 state) with 70% activity factor.

3. Typical power based on nominal process distribution for this device.

4. PH10, PH15, PH20 power savings with one core. Maximum savings would be *n* times, where *n* is the number of used cores.

5. Require both threads of the core to enter the same low-power mode.

3.5 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

Table 11. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/DV_{DD}/ $G1V_{DD}$/ $S1V_{DD}$/$X1V_{DD}$/LV_{DD}, all core and platform V_{DD} supplies, $D1\_MV_{REF}$, all AV_{DD}, and CV_{DD} supplies.)	—	25	V/ms	1, 2
Required ramp rate for PROG_SFP	—	25	V/ms	1, 2

Notes:

1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.

2. Over full recommended operating temperature range (see Table 3).

3.6 Input clocks

3.6.1 System clock (SYSCLK) timing specifications

This section provides the system clock DC and AC timing specifications.

3.6.1.1 System clock DC timing specifications

This table provides the system clock (SYSCLK) DC specifications.

Table 12. SYSCLK DC electrical characteristics[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	—	V	1
Input low voltage	V_{IL}	—	—	0.6	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (OV_{IN}= 0 V or OV_{IN} = OV_{DD})	I_{IN}	-50	—	+50	μA	2

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended operating conditions.
3. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 3.

3.6.1.2 System clock AC timing specifications

This table provides the system clock (SYSCLK) AC timing specifications.

Table 13. SYSCLK AC timing specifications[5]

Parameter/condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	66	—	133.3	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	7.5	—	15	ns	1, 2
SYSCLK duty cycle	t_{KHK} / t_{SYSCLK}	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK jitter phase noise at -56 dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 1.8 V OV_{DD}	ΔV_{AC}	0.6 x OV_{DD}	—	1 x OV_{DD}	V	6

Notes:

Table 13. SYSCLK AC timing specifications[5]

Parameter/condition	Symbol	Min	Typ	Max	Unit	Notes
1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency do not exceed their respective maximum or minimum operating frequencies. 2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$. 3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}. 4. Phase noise is calculated as FFT of TIE jitter. 5. At recommended operating conditions with OV_{DD} = 1.8V, see Table 3. 6. AC swing measured relative to half OV_{DD} or V_{IH} and V_{IL} have equal absolute offset from $OV_{DD}/2$, So, Swing = $(V_{IH}-V_{IL})/OV_{DD}$ and ΔVAC = Swing x OV_{DD}.						

3.6.2 Spread-spectrum sources

Spread-spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the chip is compatible with spread-spectrum sources if the recommendations listed in this table are observed.

Table 14. Spread-spectrum clock source recommendations[1]

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	2, 3
Notes: 1. At recommended operating conditions with OVDD = 1.8 V, see Table 3. 2. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 13. 3. Maximum spread-spectrum frequency may not result in exceeding any maximum operating frequency of the device.				

CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should avoid violating the stated limits by using down-spreading only.

3.6.3 Real-time clock timing

The real-time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the counters of the MPIC and the time base unit of the core; there is no need for jitter specification. The minimum period of the RTC signal should be greater than or equal to 16x the period of the platform clock with a 50% duty cycle. There is no minimum RTC frequency; RTC may be grounded if not needed.

3.6.4 Gigabit Ethernet reference clock timing

This table provides the Ethernet gigabit reference clock DC specifications.

Table 15. EC*n*_GTX_CLK125 DC electrical characteristics[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	—	V	2
Input low voltage	V_{IL}	—	—	0.7	V	2
Input capacitance	C_{IN}	—	—	6	pF	—
Input current (LV_{IN} = 0 V or $LV_{IN} = LV_{DD}$)	I_{IN}	—	—	± 50	μA	3

Notes:

1. At recommended operating conditions with LV_{DD} = 2.5 V.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.

3. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.

This table provides the Ethernet gigabit reference clocks AC timing specifications.

Table 16. EC*n*_GTX_CLK125 AC timing specifications[1]

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 frequency	t_{G125}	125 - 100 ppm	125	125 + 100 ppm	MHz	—
EC*n*_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC*n*_GTX_CLK125 rise and fall time LV_{DD} = 2.5 V	t_{G125R}/t_{G125F}	—	—	0.75	ns	2
EC*n*_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	47	—	53	%	3
EC*n*_GTX_CLK125 jitter	—	—	—	± 150	ps	3

Notes:

Table 16. EC*n*_GTX_CLK125 AC timing specifications[1]

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
1. At recommended operating conditions with LV_{DD} = 2.5 V ± 125 mV.						
2. Rise and fall times for EC*n*_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V.						
3. EC*n*_GTX_CLK125 is used to generate the GTX clock for the Ethernet transmitter with 2% degradation. The ECn_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the GTX_CLK. See RGMII AC timing specifications for duty cycle for 10Base-T and 100Base-T reference clock.						

3.6.5 DDR clock timing

This section provides the DDR clock DC and AC timing specifications. DDR3L maximum supported data rate is 1866 MT/s.

3.6.5.1 DDR clock DC timing specifications

This table provides the DDR clock (DDRCLK) DC specifications.

Table 17. DDRCLK DC electrical characteristics[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	—	V	1
Input low voltage	V_{IL}	—	—	0.6	V	1
Input capacitance	C_{IN}	—	—	12	pF	—
Input current (OV_{IN}= 0 V or OV_{IN} = OV_{DD})	I_{IN}	-50	—	+ 50	μA	2
Note:						
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.						
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended operating conditions.						
3. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 3.						

3.6.5.2 DDR clock AC timing specifications

This table provides the DDR clock (DDRCLK) AC timing specifications.

Table 18. DDRCLK AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}	66.7	—	133.3	MHz	1, 2
DDRCLK cycle time	t_{DDRCLK}	5	—	15	ns	1, 2
DDRCLK duty cycle	t_{KHK} / t_{DDRCLK}	40	—	60	%	2

Table continues on the next page...

Table 18. DDRCLK AC timing specifications[5] (continued)

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
DDRCLK slew rate	—	1	—	4	V/ns	3
DDRCLK peak period jitter	—	—	—	± 150	ps	—
DDRCLK jitter phase noise at -56 dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 1.8 V OV_{DD}	ΔV_{AC}	0.35 x OV_{DD}	—	0.65 x OV_{DD}	V	—

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting DDRCLK frequency do not exceed their respective maximum or minimum operating frequencies.

2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.

3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.

4. Phase noise is calculated as FFT of TIE jitter.

5. At recommended operating conditions with OV_{DD} = 1.8V, see Table 3.

3.6.6 Other input clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information about the input clock requirements of functional modules sourced external of the chip, such as SerDes, Ethernet management, eSDHC, IFC, see the specific interface section.

3.7 RESET initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table describes the AC electrical specifications for the RESET initialization timing.

Table 19. RESET Initialization timing specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of PORESET_B	1	—	ms	1
Required input assertion time of HRESET_B	32	—	SYSCLKs	2, 3
Maximum rise/fall time of HRESET_B	—	10	SYSCLK	4
Maximum rise/fall time of PORESET_B	—	1	SYSCLK	4
PLL input setup time with stable SYSCLK before HRESET_B negation	100	—	μs	—
Input setup time for POR configs with respect to negation of PORESET_B	4	—	SYSCLKs	2
Input hold time for all POR configs with respect to negation of PORESET_B	2	—	SYSCLKs	2

Table continues on the next page...

Table 19. RESET Initialization timing specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B	—	5	SYSCLKs	2

Notes:

1. PORESET_B must be driven asserted before the core and platform power supplies are powered up.
2. SYSCLK is the primary clock input for the chip.
3. The device asserts HRESET_B as an output when PORESET_B is asserted to initiate the power-on reset process. The device releases HRESET_B sometime after PORESET_B is deasserted. The exact sequencing of HRESET_B deassertion is documented in section "Power-On Reset Sequence" in the chip reference manual.
4. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

3.8 DDR3 and DDR3L SDRAM controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and the GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

NOTE

When operating at a DDR data rate greater than or equal to 1866 MT/s, only one dual-ranked module per memory controller is supported. DDR3L is not supported at a DDR data rate of 2133 MT/s.

3.8.1 DDR3 and DDR3L SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 20. DDR3 SDRAM interface DC electrical characteristics (GV_{DD} = 1.5 V)[1, 7]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREF*n*	0.49 x GV_{DD}	0.51 x GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MVREF*n* - 0.100	V	5
I/O leakage current	I_{OZ}	-50	50	μA	6

Table continues on the next page...

Table 20. DDR3 SDRAM interface DC electrical characteristics (GV_{DD} = 1.5 V)[1, 7] (continued)

Parameter	Symbol	Min	Max	Unit	Note
Notes:					
1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.					
2. MVREF*n* is expected to be equal to 0.5 x GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n* may not exceed the MVREF*n* DC level by more than ±1% of GV_{DD} (i.e. ±15 mV).					
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* - 0.04 and a max value of MVREF*n* + 0.04. V_{TT} should track variations in the DC level of MVREF*n*.					
4. The voltage regulator for MVREF*n* must meet the specifications stated in Table 22.					
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.					
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.					
7. For recommended operating conditions, see Table 3.					

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 21. DDR3L SDRAM interface DC electrical characteristics (GV_{DD} = 1.35 V)[1, 7]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREF*n*	0.49 x GV_{DD}	0.51 x GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.090	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MVREF*n* - 0.090	V	5
I/O leakage current	I_{OZ}	-100	100	μA	6
Notes:					
1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.					
2. MVREF*n* is expected to be equal to 0.5 x GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n* may not exceed the MVREF*n* DC level by more than ±1% of GV_{DD} (i.e. ±13.5 mV).					
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* - 0.04 and a max value of MVREF*n* + 0.04. V_{TT} should track variations in the DC level of MVREF*n*.					
4. The voltage regulator for MVREF*n* must meet the specifications stated in Table 22.					
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.					
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.					
7. For recommended operating conditions, see Table 3.					

This table provides the current draw characteristics for MVREF*n*.

Table 22. Current draw characteristics for MVREF*n*[1]

Parameter	Symbol	Min	Max	Unit	Notes
Current draw for DDR3 SDRAM for MVREF*n*	I_{MVREFn}	—	500	μA	—
Current draw for DDR3L SDRAM for MVREF*n*	I_{MVREFn}	—	500	μA	—
Note: 1. For recommended operating conditions, see Table 3.					

3.8.2 DDR3 and DDR3L SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR3 and DDR3L memories. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and the required GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

3.8.2.1 DDR3 and DDR3L SDRAM interface input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 or DDR3L SDRAM.

Table 23. DDR3 and DDR3L SDRAM interface input AC timing specifications[4]

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS-MDQ/MECC	t_{CISKEW}	—	—	ps	1, 3
2133 MT/s data rate		-80	80		
1866 MT/s data rate		-93	93		
1600 MT/s data rate		-112	112		
1333 MT/s data rate		-125	125		
1200 MT/s data rate		-142	142		
1066 MT/s data rate		-170	170		
Tolerated Skew for MDQS-MDQ/MECC	t_{DISKEW}	—	—	ps	2, 3
2133 MT/s data rate		-154	154		
1866 MT/s data rate		-175	175		
1600 MT/s data rate		-200	200		
1333 MT/s data rate		-250	250		
1200 MT/s data rate		-275	275		
1066 MT/s data rate		-300	300		
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.					

Table 23. DDR3 and DDR3L SDRAM interface input AC timing specifications[4]

Parameter	Symbol	Min	Max	Unit	Notes
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.					
3. 2133 MT/s is only supported for DDR3, not DDR3L.					
4. For recommended operating conditions, see Table 3.					

This figure shows the DDR3 and DDR3L SDRAM interface input timing diagram.

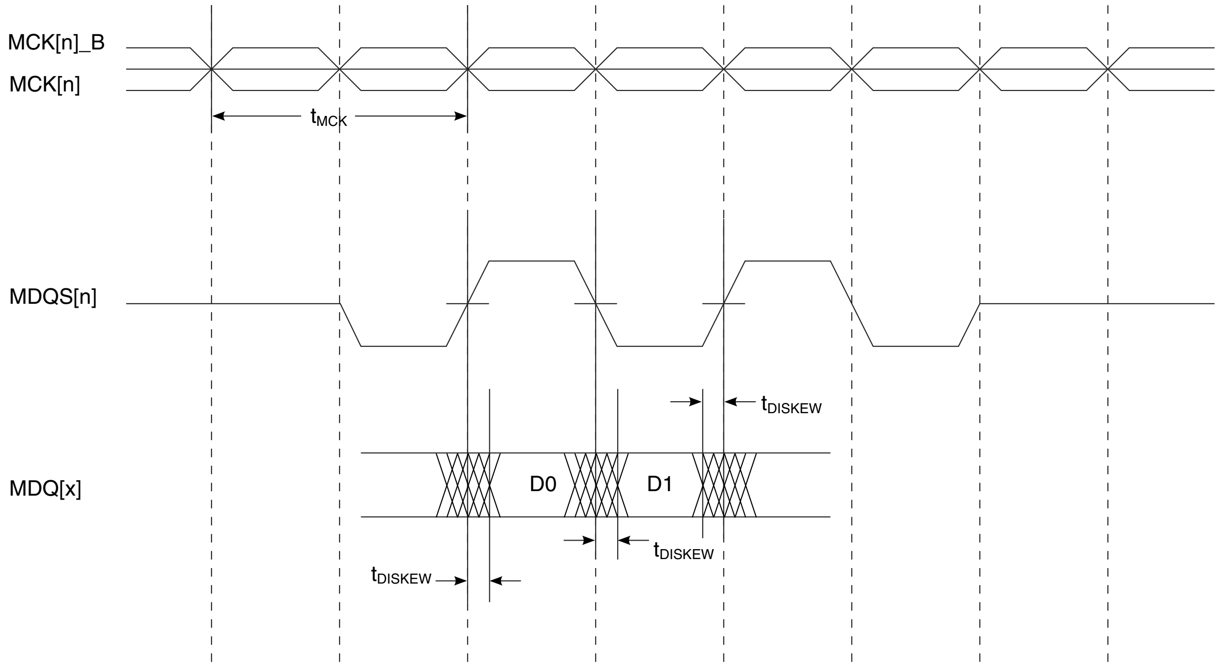


Figure 9. DDR3 and DDR3L SDRAM interface input timing diagram

3.8.2.2 DDR3 and DDR3L SDRAM interface output AC timing specifications

This table contains the output AC timing targets for the DDR3 SDRAM interface.

Table 24. DDR3 and DDR3L SDRAM interface output AC timing specifications[8]

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	0.938	2	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}	—	—	ns	3, 7
2133 MT/s data rate		0.350	—		
1866 MT/s data rate		0.410	—		
1600 MT/s data rate		0.495	—		

Table continues on the next page...

Table 24. DDR3 and DDR3L SDRAM interface output AC timing specifications[8] (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
1333 MT/s data rate		0.606	—		
1200 MT/s data rate		0.675	—		
1066 MT/s data rate		0.744	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}	—	—	ns	3, 7
2133 MT/s data rate		0.350	—		
1866 MT/s data rate		0.390	—		
1600 MT/s data rate		0.495	—		
1333 MT/s data rate		0.606	—		
1200 MT/s data rate		0.675	—		
1066 MT/s data rate		0.744	—		
MCK to MDQS Skew	t_{DDKHMH}	—	—	ns	4
> 1600 MT/s data rate		-0.150	0.150		4, 6
> 1066 MT/s data rate, ≤ 1600 MT/s data rate		-0.245	0.245		4, 6
MDQ/MECC/MDM output Data eye	$t_{DDKXDEYE}$	—	—	ns	5, 7
2133 MT/s data rate		0.320	—		
1866 MT/s data rate		0.350	—		
1600 MT/s data rate		0.400	—		
1333 MT/s data rate		0.500	—		
1200 MT/s data rate		0.550	—		
1066 MT/s data rate		0.600	—		
MDQS preamble	t_{DDKHMP}	0.9 x t_{MCK}	—	ns	—
MDQS postamble	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	—

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time.

2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.

3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MECC/MDM/MDQS.

4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the chip reference manual for a description and explanation of the timing modifications enabled by the use of these bits.

5. Available eye for data (MDQ), ECC (MECC), and data mask (MDM) outputs at the pin of the processor. Memory controller will center the strobe (MDQS) in the available data eye at the DRAM (end point) during the initialization.

6. Note that for data rates of 1200 MT/s or higher, it is required to program the start value of the DQS adjust for write leveling.

7. 2133 MT/s is only supported for DDR3, not DDR3L.

8. For recommended operating conditions, see Table 3.

NOTE

For the ADDR/CMD setup and hold specifications in Table 24, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle for data rates of 1866 MT/s or less and 9/16 applied cycle for data rates greater than 1866 MT/s. It is recommended that, during system validation, memory clocks are adjusted to best fit the particular system. design.

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

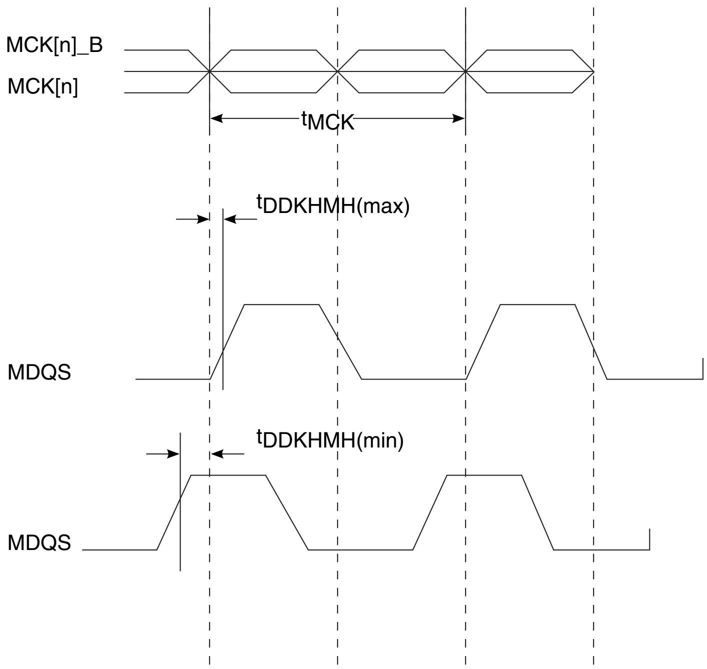


Figure 10. t_{DDKHMH} timing diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

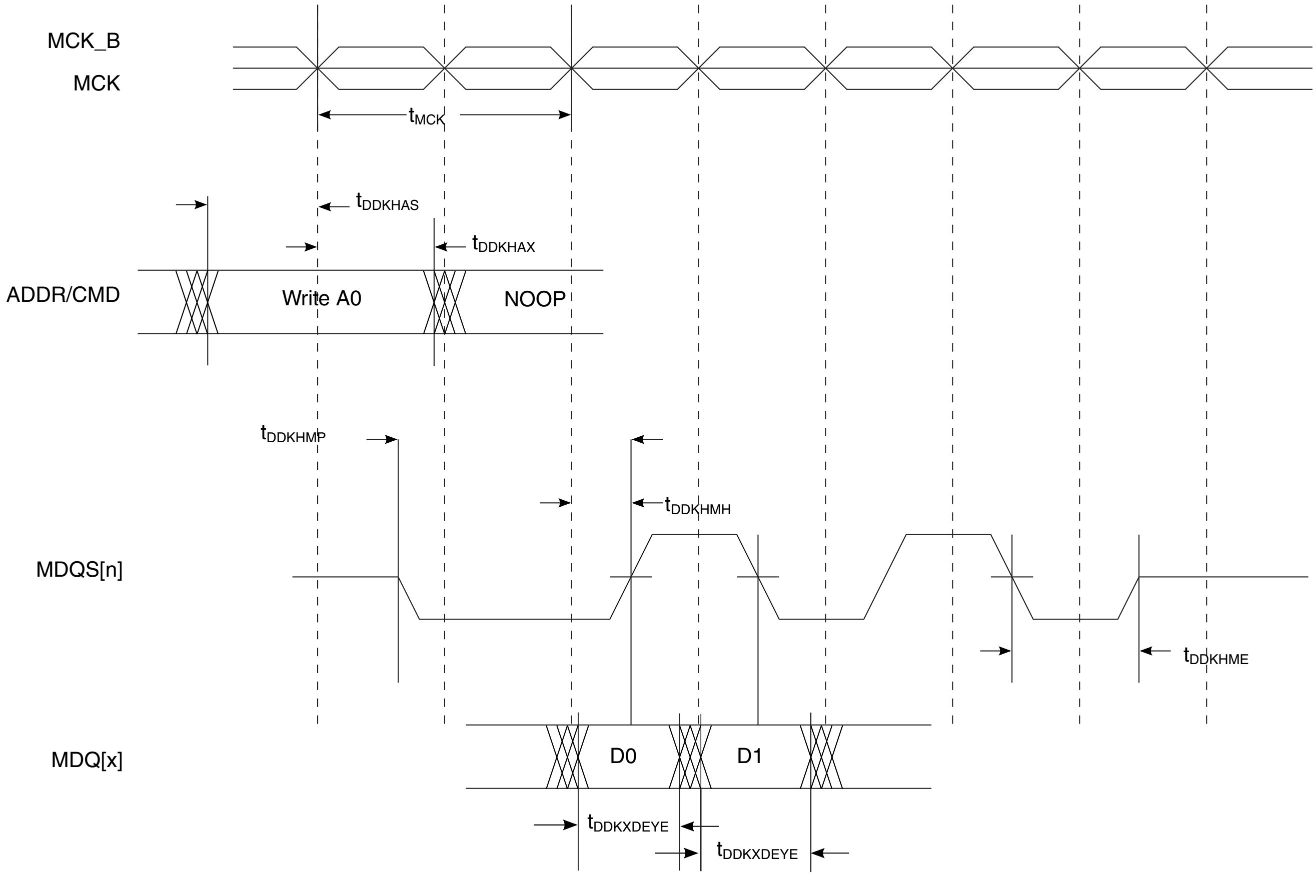


Figure 11. DDR3 and DDR3L output timing diagram

3.9 eSPI interface

This section describes the DC and AC electrical specifications for the eSPI interface.

3.9.1 eSPI DC electrical characteristics

This table provides the DC electrical characteristics for the eSPI interface operating at OV_{DD} = 2.5 V.

Table 25. eSPI DC electrical characteristics (2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	-50	+50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	—	V	—

Table continues on the next page...

Table 25. eSPI DC electrical characteristics (2.5 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output low voltage (OV_{DD} = min, I_{OL} = 1mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3.

This table provides the DC electrical characteristics for the eSPI interface operating at OV_{DD} = 1.8 V.

Table 26. eSPI DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3.

3.9.2 eSPI AC timing specifications

This table provides the eSPI input and output AC timing specifications.

Table 27. eSPI AC timing specifications[3]

Characteristic	Symbol [2]	Min	Max	Unit	Notes
SPI_MOSI output-Master data (internal clock) hold time	t_{NIKHOX}	n1 + ($t_{PLATFORM\_CLK}$ * SPMODE[HO_ADJ])	—	ns	1, 2 , 4
SPI_MOSI output-Master data (internal clock) delay	t_{NIKHOV}	—	n2 + ($t_{PLATFORM\_CLK}$ * SPMODE[HO_ADJ])	ns	1, 2 , 4
SPI_CS outputs-Master data (internal clock) hold time	$t_{NIKHOX2}$	0	—	ns	1
SPI_CS outputs-Master data (internal clock) delay	$t_{NIKHOV2}$	—	6.0	ns	1

Table continues on the next page...

Table 27. eSPI AC timing specifications[3] (continued)

Characteristic	Symbol [2]	Min	Max	Unit	Notes
SPI inputs-Master data (internal clock) input setup time	t_{NIIVKH}	3.6	—	ns	—
SPI inputs-Master data (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—
Clock-high time	t_{NIKCKH}	4	—	ns	
Clock-low time	t_{NIKCKL}	4	—	ns	—

Notes:

1. See the chip reference manual for details about the SPMODE register.

2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

3. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

4. n1 and n2 values are -1.0 and 1.0 respectively.

This figure provides the AC test load for the eSPI.

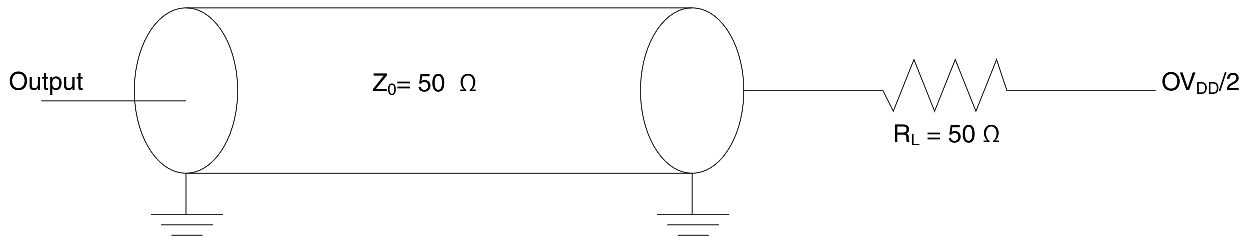


Figure 12. eSPI AC test load

This figure provides the eSPI clock output timing diagram.

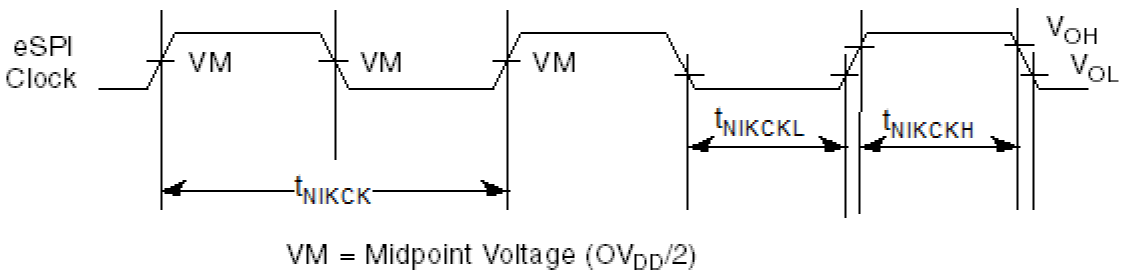


Figure 13. eSPI clock output timing diagram

This figure represents the AC timing from Table 27 in master mode (internal clock). Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI.

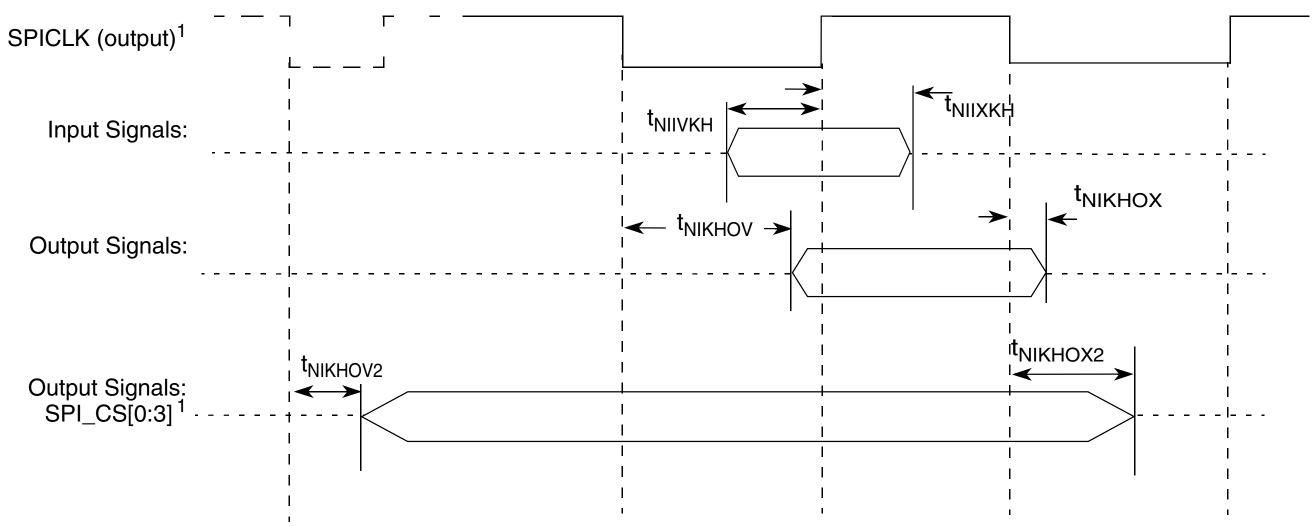


Figure 14. eSPI AC timing in master mode (internal clock) diagram

NOTE

SPICLK appears on the interface only after CS assertion.

3.10 DUART interface

This section describes the DC and AC electrical specifications for the DUART interface.

3.10.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 2.5 V.

Table 28. DUART DC electrical characteristics(2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (DV_{IN} = 0 V or DV_{IN} = DV_{DD})	I_{IN}	-50	+50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (DV_{DD} = min, I_{OL} = 1mA)	V_{OL}	—	0.4	V	—

Table continues on the next page...

Table 28. DUART DC electrical characteristics(2.5 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Notes:					
1. The min $V_{IL}$and max V_{IH} values are based on the min and max DV_{IN} respective values found in Table 3.					
2. The symbol DV_{IN} represents the input voltage of the supply. It is referenced in Recommended operating conditions.					
3. For recommended operating conditions, see Table 3.					

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 1.8 V.

Table 29. DUART DC electrical characteristics(1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (DV_{IN} = 0 V or DV_{IN} = DV_{DD})	I_{IN}	-50	+50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (DV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—
Notes:					
1. The min $V_{IL}$and max V_{IH} values are based on the min and max DV_{IN} respective values found in Table 3.					
2. The symbol DV_{IN} represents the input voltage of the supply. It is referenced in Recommended operating conditions.					
3. For recommended operating conditions, see Table 3.					

3.10.2 DUART AC electrical specifications

This table provides the AC timing parameters for the DUART interface.

Table 30. DUART AC timing specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{PLAT}/(2 x 1,048,576)	baud	1, 3
Maximum baud rate	f_{PLAT}/(2 x 16)	baud	1, 2
Notes:			
1. f_{PLAT} refers to the internal platform clock.			
2. The actual attainable baud rate is limited by the latency of interrupt processing.			
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.			

3.11 Ethernet interface, Ethernet management interface 1 and 2, IEEE Std 1588™

This section provides the AC and DC electrical characteristics for the Ethernet controller and the Ethernet management interfaces.

3.11.1 SGMII electrical specifications

See SGMII interface.

3.11.2 RGMII electrical specifications

This section discusses the electrical characteristics for the RGMII interface.

3.11.2.1 RGMII DC electrical characteristics

This table shows the DC electrical characteristics for the RGMII interface.

Table 31. RGMII DC electrical characteristics(LV_{DD} = 2.5 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.70	V	1
Input current (LV_{IN}= 0 V or LV_{IN}= LV_{DD})	I_{IH}	-50	+50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	GND - 0.3	0.40	V	—

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3.

3.11.2.2 RGMII AC timing specifications

This table presents the RGMII AC timing specifications.

Table 32. RGMII AC timing specifications (LV_{DD} = 2.5 V)[8]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	-750	0	1000	ps	7, 9
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3

Table continues on the next page...

Table 32. RGMII AC timing specifications (LV_{DD} = 2.5 V)[8] (continued)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	—
Rise time (20%-80%)	t_{RGTR}	—	—	0.75	ns	5, 6
Fall time (20%-80%)	t_{RGTF}	—	—	0.75	ns	5, 6

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).

2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.

3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.

4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

5. Applies to inputs and outputs.

6. System/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

7. The frequency of ECn_RX_CLK (input) should not exceed the frequency of ECn_GTX_CLK (output) by more than 300 ppm.

8. For recommended operating conditions, see Table 3.

9. IEEE specification mandates tSKRGT_TX = ± 0.5 ns. Per erratum A-005177, we see tSKRGT_TX has a wider output skew range from -0.75 ns to 1.00 ns, which is larger than the specification asks for. If the device cannot cope with this wide skew, use RGMII at 100 Mbps or 10 Mbps, which allows larger maximum RX skews, or terminate 1000 Mbps RGMII links with PHYs that accommodate larger RX skews. **NOTE:** MAC10 is not impacted by erratum A-005177, and it meets industry specifications.

This figure shows the RGMII AC timing and multiplexing diagrams.

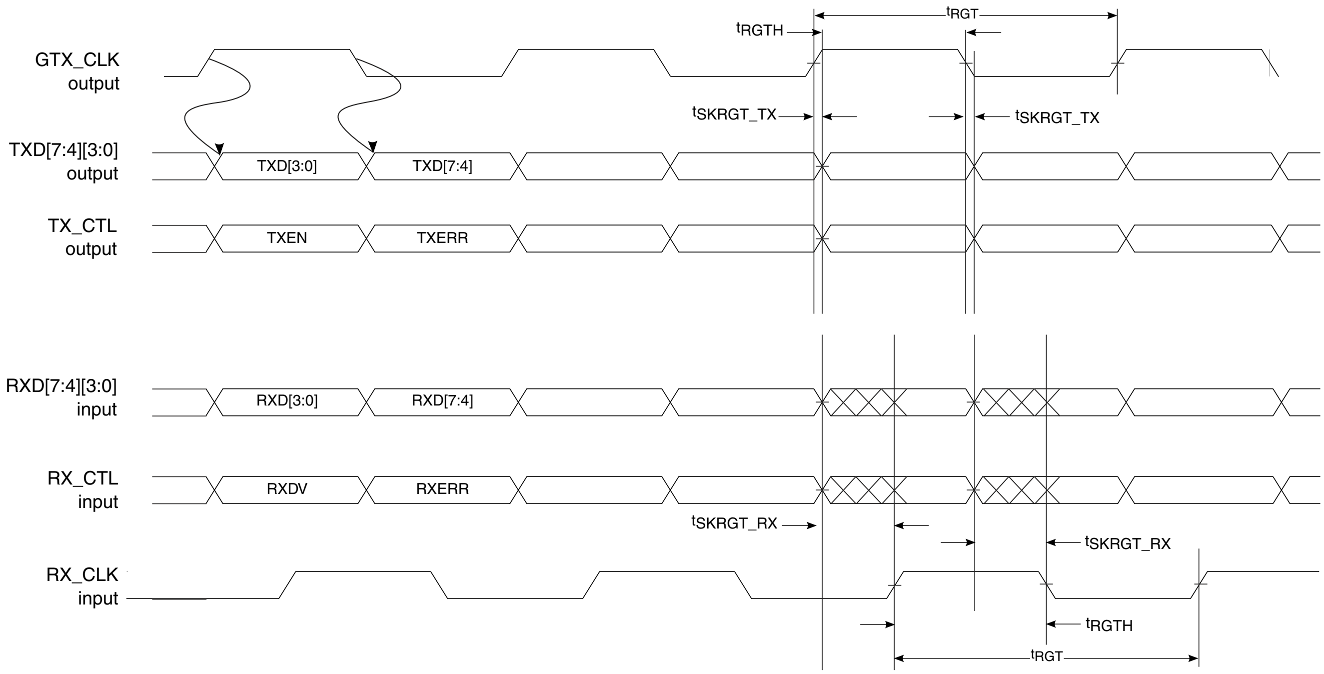


Figure 15. RGMII AC timing and multiplexing diagrams

Warning

NXP guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

3.11.3 Ethernet management interface (EMI)

This section discusses the electrical characteristics for the EMI1 and EMI2 interfaces.

Frame Manager's external GE MDIO configures external GE PHYs connected to EMI1 pins. Frame Manager's external 10GE MDIO configures external XFI PHY connected to EMI2 pins.

The EMI1 interface timing is compatible with IEEE Std 802.3™ clause 22 and EMI2 interface timing is compatible with IEEE Std 802.3™ clause 45.

3.11.3.1 Ethernet management interface 1 DC electrical characteristics

The DC electrical characteristics for EMI1_MDIO and EMI1_MDC are provided in this section.

Table 33. Ethernet management interface 1 DC electrical characteristics (LV_{DD} = 2.5 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.70	V	1
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	50	μA	2
Input low current (V_{IN} = GND)	I_{IL}	-50	—	μA	—
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	GND - 0.3	0.40	V	—

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol VIN, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3.

Table 34. Ethernet management interface 1 DC electrical characteristics (LV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.60	V	1
Input current (LV_{IN}= 0V or LV_{IN}=LV_{DD})	I_{IN}	-50	50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.40	V	—

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN}/QV_{IN} values found in Table 3.
2. The symbol VIN, in this case, represents the OV_{IN} symbol referenced in Table 3.

3.11.3.2 Ethernet management interface 2 DC electrical characteristics

Ethernet management interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. The DC electrical characteristics for EMI2_MDIO and EMI2_MDC are provided in this section.

Table 35. Ethernet management interface 2 DC electrical characteristics (1.2 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.84	—	V	—
Input low voltage	V_{IL}	—	0.36	V	—
Output low voltage (I_{OL} = 100 μA)	V_{OL}	—	0.2	V	—
Output low current (V_{OL} = 0.2 V)	I_{OL}	4	—	mA	—
Input capacitance	C_{IN}	—	10	pF	—

Notes:

1. For recommended operating conditions, see Table 3.

3.11.3.3 Ethernet management interface 1 AC electrical specifications

This table provides the Ethernet management interface 1 AC timing specifications.

Table 36. Ethernet management interface 1 AC timing specifications[5]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	(5 x t_{enet_clk}) - 3	—	(5 x t_{enet_clk}) + 3	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	8	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.

2. This parameter is dependent on the Ethernet clock frequency (MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC).

3. This parameter is dependent on the Ethernet clock frequency. The delay is equal to 5 Ethernet clock periods ± 3 ns. For example, with an Ethernet clock of 400 MHz, the min/max delay is 12.5 ns ± 3 ns.

4. t_{enet_clk} is the Ethernet clock period (Frame Manager clock period).

5. For recommended operating conditions, see Table 3.

3.11.3.4 Ethernet management interface 2 AC electrical characteristics

This table provides the Ethernet management interface 2 AC timing specifications.

Table 37. Ethernet management interface 2 AC timing specifications[5]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	2.5	—	—	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	(5 x t_{enet_clk}) - 3	—	(5 x t_{enet_clk}) + 3	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	8	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.

2. This parameter is dependent on the Ethernet clock frequency (MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC).

Table 37. Ethernet management interface 2 AC timing specifications[5]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
3. This parameter is dependent on the Ethernet clock frequency. The delay is equal to 5 Ethernet clock periods ± 3 ns. For example, with an Ethernet clock of 400 MHz, the min/max delay is 12.5 ns ± 3 ns.						
4. t_{enet_clk} is the Ethernet clock period (Frame Manager clock period).						
5. For recommended operating conditions, see Table 3.						

This figure shows the Ethernet management interface timing diagram

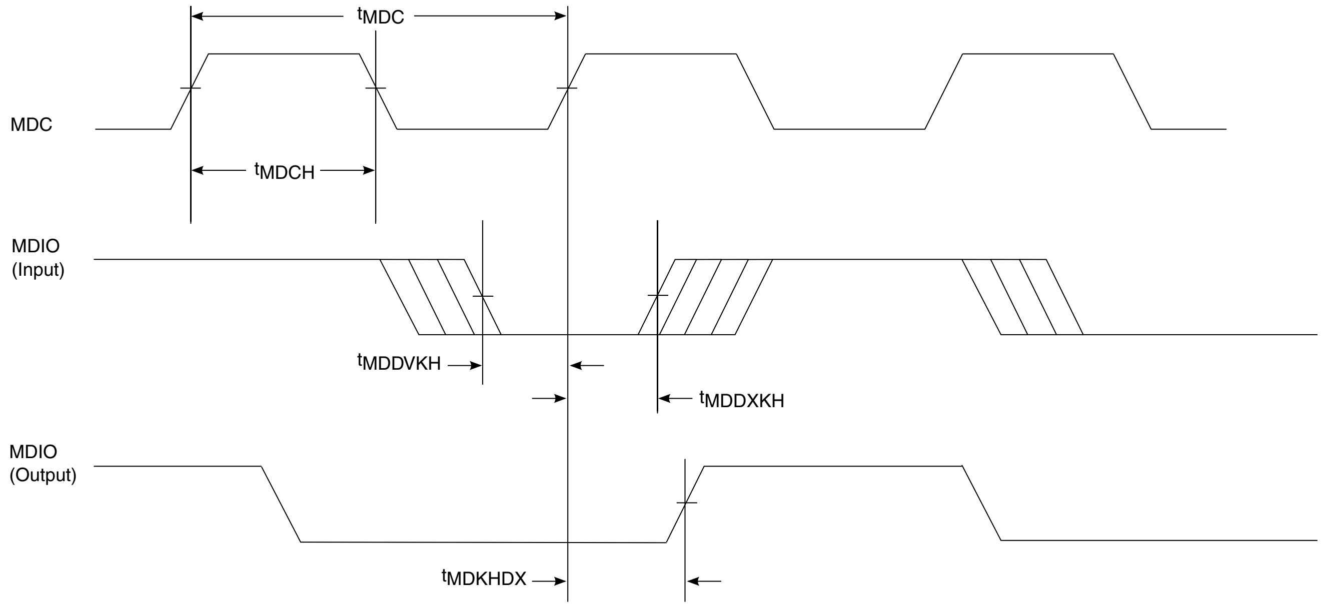


Figure 16. Ethernet management interface timing diagram

3.11.4 IEEE 1588 electrical specifications

3.11.4.1 IEEE 1588 DC electrical characteristics

This table shows IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 38. IEEE 1588 DC electrical characteristics (LV_{DD} = 2.5 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.70	V	1
Input current (LV_{IN}= 0 V or LV_{IN}= LV_{DD})	I_{IH}	-50	+50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—

Table continues on the next page...

Table 38. IEEE 1588 DC electrical characteristics (LV_{DD} = 2.5 V)[3] (continued)

Parameters	Symbol	Min	Max	Unit	Notes
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	GND - 0.3	0.40	V	—

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3.

This table shows IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 1.8 V supply.

Table 39. IEEE 1588 DC electrical characteristics (LV_{DD} = 1.8 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (LV_{IN}= 0 V or LV_{IN}= LV_{DD})	I_{IH}	-50	+50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	GND - 0.3	0.40	V	—

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3.

3.11.4.2 IEEE 1588 AC specifications

This table provides the IEEE 1588 AC timing specifications.

Table 40. IEEE 1588 AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK_IN clock period	$t_{T1588CLK}$	3.3	—	T_{RX_CLK} x 7	ns	1, 3
TSEC_1588_CLK_IN duty cycle	$t_{T1588CLKH}$/ $t_{T1588CLK}$	40	50	60	%	2
TSEC_1588_CLK_IN peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time TSEC_1588_CLK_IN (20% -80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time TSEC_1588_CLK_IN (80% -20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	5.0	—	—	ns	4
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$/ $t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT1/2, TSEC_1588_ALARM_OUT1/2	$t_{T1588OV}$	0.5	—	3.0	ns	—

Table continues on the next page...

Table 40. IEEE 1588 AC timing specifications[5] (continued)

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_TRIG_IN1/2 pulse width	$t_{T1588TRIGH}$	2 x $t_{T1588CLK\_MAX}$	—	—	ns	3

Notes:

1. T_{RX_CLK} is the maximum clock period of ethernet receiving clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.

2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.

3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns, respectively.

4. There are 3 input clock sources for 1588 i.e. TSEC_1588_CLK_IN, RTC and MAC clock / 2. When using TSEC_1588_CLK_IN, the minimum clock period is 2 x $t_{T1588CLK}$.

5. For recommended operating conditions, see Table 3.

This figure shows the data and command output AC timing diagram.

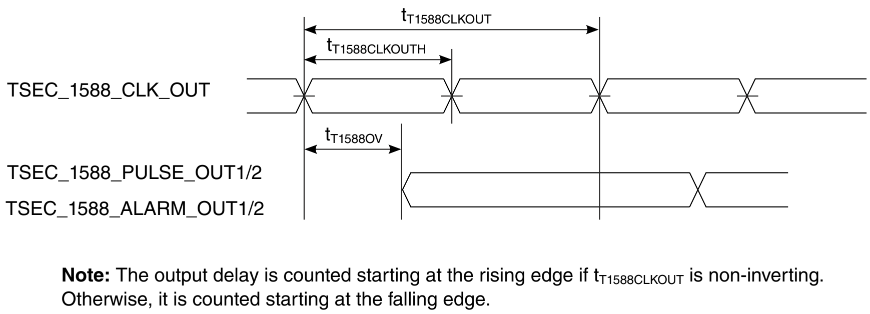


Figure 17. IEEE 1588 output AC timing

This figure shows the data and command input AC timing diagram.

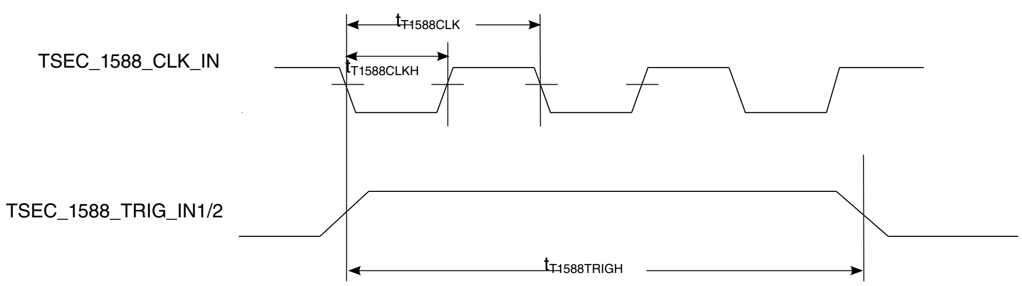


Figure 18. IEEE 1588 input AC timing

3.12 USB interface

This section provides the AC and DC electrical specifications for the USB interface.

3.12.1 USB DC electrical characteristics

This table provides the DC electrical characteristics for the USB interface at USB_HV_{DD} = 3.3 V.

Table 41. USB DC electrical characteristics (USB_HV_{DD} = 3.3 V) [3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	-	V	1, 4
Input low voltage	V_{IL}	-	0.8	V	1, 4
Input current (USB_HV_{IN} = 0 V or USB_HV_{IN}= USB_HV_{DD})	I_{IN}	-100	+100	μA	2, 4
Output high voltage (USB_HV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.8	-	V	5
Output low voltage (USB_HV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	-	0.3	V	5

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max USB_HV_{IN} values found in Table 3.

2. The symbol USB_HV_{IN}, in this case, represents the USB_HV_{IN} symbol referenced in Recommended operating conditions

3. For recommended operating conditions, see Table 3

4. These specifications only apply to the following pins: USB1_PWRFAULT, USB2_PWRFAULT, USB1_UDM (full-speed mode), USB2_UDM (full-speed mode), USB1_UDP (full-speed mode), and USB2_UDP (full-speed mode).

5. This specification only applies to USB1_DRVVBUS and USB2_DRVVBUS pins.

This table provides the DC electrical characteristics for the USBCLK at OV_{DD} = 1.8 V.

Table 42. USBCLK DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	-	±100	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended operating conditions.

3. For recommended operating conditions, see Table 3.

3.12.2 USB AC timing specifications

This section describes the AC timing specifications for the on-chip USB PHY. See Chapter 7 in the *Universal Serial Bus Revision 2.0 Specification* for more information.

This table provides the USB clock input (USBCLK) AC timing specifications.

Table 43. USBCLK AC timing specifications[1]

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
Frequency range	-	$f_{USB\_CLK\_IN}$	-	24	-	MHz	-
Rise/Fall time	Measured between 10% and 90%	t_{USRF}	-	-	6	ns	2
Clock frequency tolerance	-	t_{CLK_TOL}	-0.01	0	0.01	%	-
Reference clock duty cycle	Measured at rising edge and/or failing edge at $OV_{DD}/2$	t_{CLK_DUTY}	40	50	60	%	-
Total input jitter/time interval error	RMS value measured with a second-order, band-pass filter of 500 kHz to 4 MHz bandwidth at 10^{-12} BER	t_{CLK_PJ}	-	-	5	ps	-

Notes:

1. For recommended operating conditions, see Table 3

2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

3.13 Integrated flash controller

This section describes the DC and AC electrical specifications for the integrated flash controller.

3.13.1 Integrated flash controller DC electrical characteristics

This table provides the DC electrical characteristics for the integrated flash controller when operating at OV_{DD}= 1.8 V.

Table 44. Integrated flash controller DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	-50	+50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended operating conditions.

3. For recommended operating conditions, see Table 3.

3.13.2 Integrated flash controller AC timing

This section describes the AC timing specifications for the integrated flash controller.

3.13.2.1 Test condition

This figure provides the AC test load for the integrated flash controller.

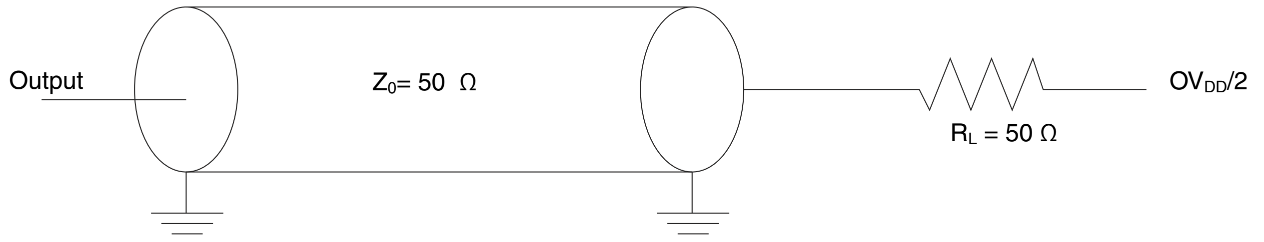


Figure 19. Integrated flash controller AC test load

3.13.2.2 Integrated flash controller AC timing specifications

All output signal timings are relative to the falling edge of any IFC_CLK. The external circuit must use the rising edge of the IFC_CLKs to latch the data.

All input timings are relative to the rising edge of IFC_CLKs.

This table describes the timing specifications of the integrated flash controller interface.

Table 45. Integrated flash controller timing specifications (OV_{DD} = 1.8 V)[5]

Parameter	Symbol[1]	Min	Max	Unit	Notes
IFC_CLK cycle time	t_{IBK}	10	-	ns	-
IFC_CLK duty cycle	t_{IBKH}/ t_{IBK}	45	55	%	-
IFC_CLK[n] skew to IFC_CLK[m]	$t_{IBKSKEW}$	-	150	ps	2
Input setup	t_{IBIVKH}	4	-	ns	-
Input hold	t_{IBIXKH}	1	-	ns	-
Output delay	t_{IBKLOV}	-	2.5	ns	-
Output hold	t_{IBKLOX}	-2	-	ns	4
IFC_CLK to output high impedance for AD	t_{IBKLOZ}	-	2	ns	3

1. All signals are measured from OV_{DD}/2 of rising/falling edge of IFC_CLK to OV_{DD}/2 of the signal in question.

2. Skew measured between different IFC_CLK signals at OV_{DD}/2.

Table 45. Integrated flash controller timing specifications (OV_{DD} = 1.8 V)[5]

Parameter	Symbol[1]	Min	Max	Unit	Notes
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.					
4. Here the negative sign means output transit happens earlier than the falling edge of IFC_CLK.					
5. For recommended operating conditions, see Table 3.					

This figure shows the AC timing diagram.

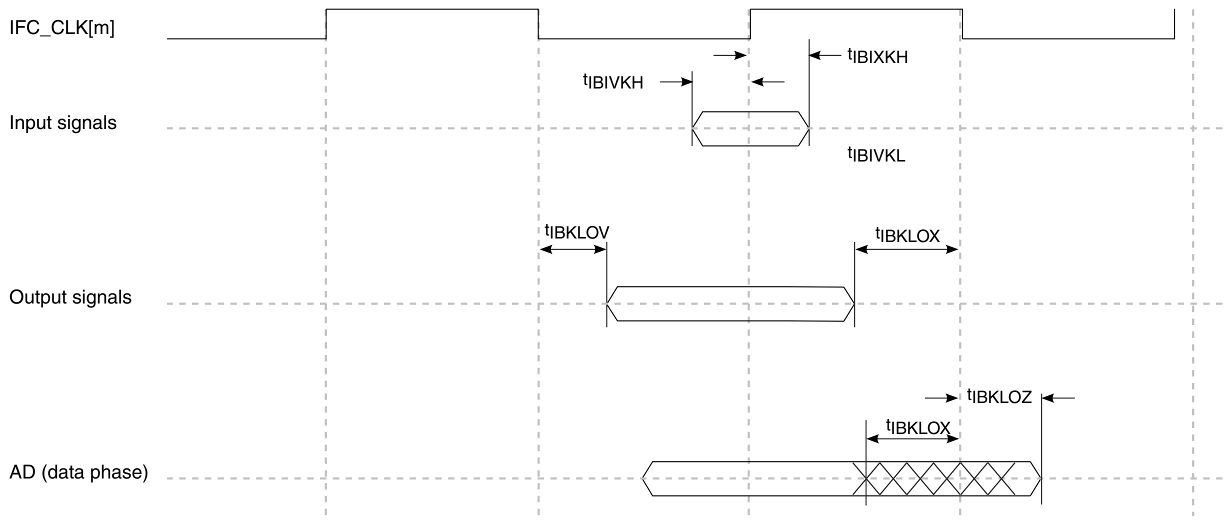


Figure 20. Integrated flash controller signals

The figure above applies to all the controllers that IFC supports.

- For input signals, the AC timing data is used directly for all controllers.
- For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay.

This figure shows how the AC timing diagram applies to GPCM. The same principle also applies to other controllers of IFC.

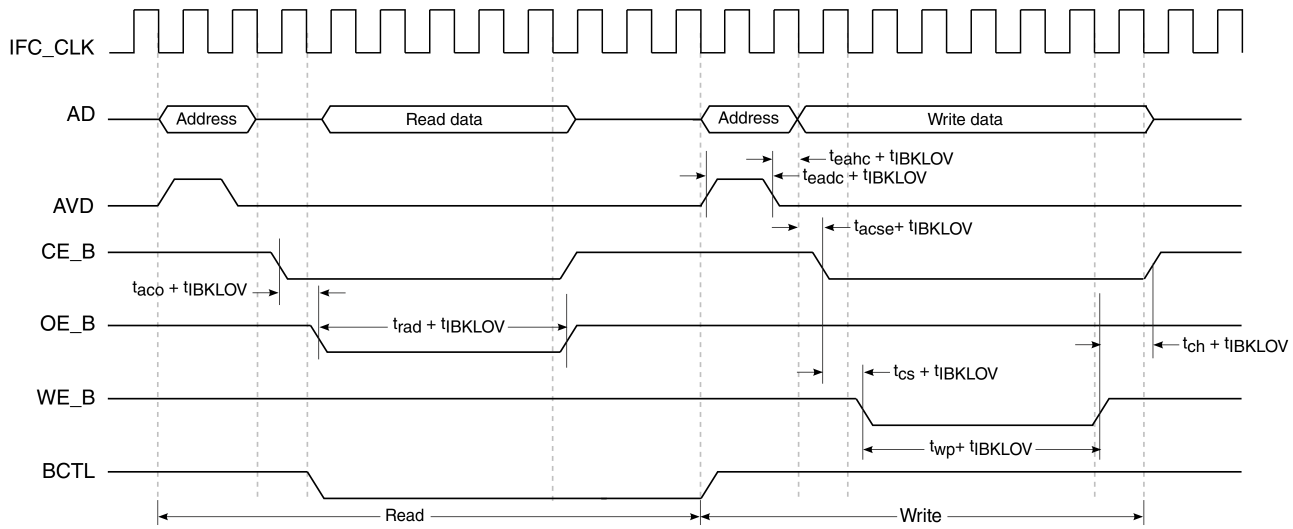


Figure 21. GPCM output timing diagram[1, 2]

Notes for figure:

1. t_{aco}, t_{rad},t_{eahc},t_{eadc}, t_{acse}, t_{cs}, t_{ch},t_{wp} are programmable. See the chip reference manual.

2. For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay.

3.14 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

3.14.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 46. eSDHC interface DC electrical characteristics (dual-voltage cards)[3]

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	-	0.7 x V_{DD}	-	V	1
Input low voltage	V_{IL}	-	-	0.2 x V_{DD}	V	1
Input/Output leakage current	I_{IN}/I_{OZ}	-	-50	50	μA	-
Output high voltage	V_{OH}	I_{OH} = -100 μA at V_{DD} min	V_{DD} - 0.2 V	-	V	-
Output low voltage	V_{OL}	I_{OL}= 100 μA at V_{DD} min	-	0.2	V	-

Table continues on the next page...

Table 46. eSDHC interface DC electrical characteristics (dual-voltage cards)[3] (continued)

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = -100 μA	V_{DD} - 0.2	-	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA	-	0.3	V	2

1. The min V_{IL} and V_{IH} values are based on the respective min and max V_{IN} values found in Table 3.
2. Open-drain mode is for MMC cards only.
3. For recommended operating conditions, see Table 3.
4. SDHC interface is powered by OV_{DD} and CV_{DD}. The V_{DD} and V_{IN} in the table above should be replaced by the respective I/O power supply.

3.14.2 eSDHC AC timing specifications

This table provides the eSDHC AC timing specifications as defined in Figure 22 and Figure 23 (OV_{DD}/CV_{DD} = 1.8 V or 3.3 V).

Table 47. eSDHC AC timing specifications (High Speed/Full Speed)[6]

Parameter		Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency	SD/SDIO (full-speed/high-speed mode)	f_{SCK}	0	25/50	MHz	2, 4
	MMC full-speed/high-speed mode			20/52		
SDHC_CLK clock low time (full-speed/high-speed mode)		t_{SCKL}	10/7	—	ns	4
SDHC_CLK clock high time (full-speed/high-speed mode)		t_{SCKH}	10/7	—	ns	4
SDHC_CLK clock rise and fall times		$t_{SCKR/}$ t_{SCKF}	—	3	ns	4
Input setup times: SDHC_CMD, SDHC_DATx to SDHC_CLK		t_{NIIVKH}	2.5	—	ns	3, 4, 5
Input hold times: SDHC_CMD, SDHC_DATx to SDHC_CLK		t_{NIIXKH}	2.5	—	ns	4, 5
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid		t_{NIKHOX}	-3	—	ns	4, 5
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid		t_{NIKHOV}	—	3	ns	4, 5

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. In full-speed mode, the clock frequency value can be 0-25 MHz for an SD/SDIO card and 0-20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0-50 MHz for an SD/SDIO card and 0-52 MHz for an MMC card.

3. To satisfy setup timing, one-way board-routing delay between Host and Card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1 ns for any high speed MMC card. For any high speed or default speed mode SD card, the one way board routing delay between Host and Card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1.5ns.

4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF.

Table 47. eSDHC AC timing specifications (High Speed/Full Speed)[6]

Parameter	Symbol[1]	Min	Max	Unit	Notes
5. The parameter values apply to both full-speed and high-speed modes.					
6. For recommended operating conditions, see Table 3.					

This figure provides the eSDHC clock input timing diagram.

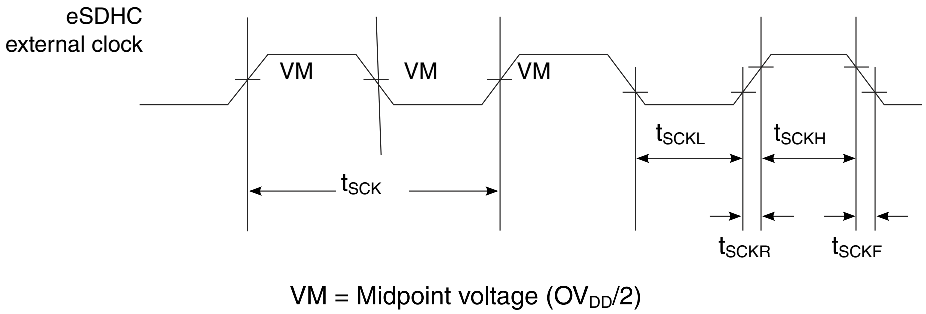


Figure 22. eSDHC clock input timing diagram

This figure provides the data and command input/output timing diagram.

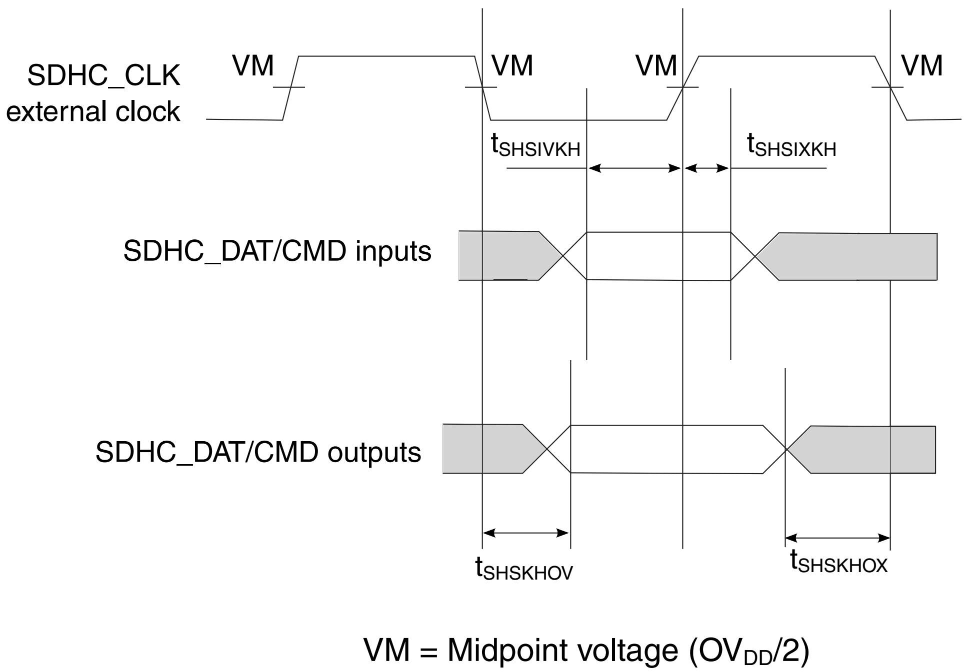


Figure 23. eSDHC data and command input/output timing diagram referenced to clock

This table provides the eSDHC AC timing specifications for eMMC HS200 mode as defined in Figure 24 (EV_{DD}/CV_{DD} = 1.8 V).

Table 48. eSDHC AC timing (eMMC HS200)

Parameter		Symbol	Min	Max	Units	Notes
SDHC_CLK clock frequency	eMMC HS200 mode	f_{SCK}	—	175	MHz	—
SDHC_CLK duty cycle		—	47	53	%	—
SDHC_CLK clock rise and fall times		t_{SCKR}/ t_{SCKF}	—	1	ns	1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	eMMC HS200 mode	t_{NIKHOX}	1.6	—	ns	—
Output delay time: SDHC_CLK to SDHC_CMD, SDHC DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	eMMC HS200 mode	t_{NIKHOV}	—	3.9	ns	—
Input data window (UI)	eMMC HS200 mode	t_{IDV}	0.475	—	Unit interval	—

Notes:

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 10$ pF.

2. For recommended operating conditions, see Table 3.

This figure provides the HS200 mode timing diagram.

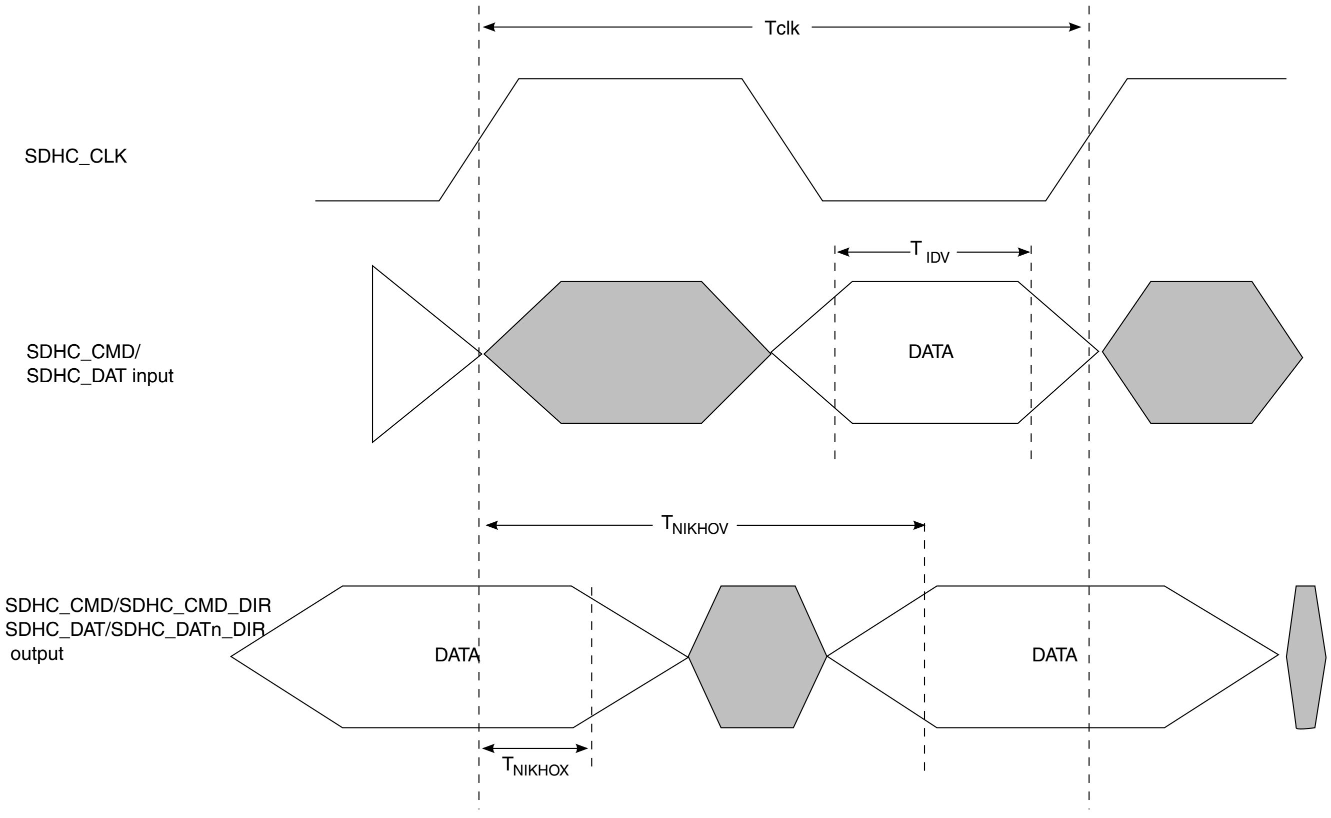


Figure 24. eMMC HS200 mode timing diagram

3.15 Multicore programmable interrupt controller (MPIC)

This section describes the DC and AC electrical specifications for the multicore programmable interrupt controller.

3.15.1 MPIC DC specifications

This figure provides the DC electrical characteristics for the MPIC interface.

Table 49. MPIC DC electrical characteristics (OV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	-50	+50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
3. For recommended operating conditions, see Table 3.

3.15.2 MPIC AC timing specifications

This table provides the MPIC input and output AC timing specifications.

Table 50. MPIC Input AC timing specifications[2]

Characteristic	Symbol	Min	Max	Unit	Notes
MPIC inputs-minimum pulse width	t_{PIWID}	3	-	SYSCLKs	1

1. MPIC inputs and outputs are asynchronous to any visible clock. MPIC outputs must be synchronized before use by any external synchronous logic. MPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.
2. For recommended operating conditions, see Table 3.

3.16 JTAG controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

3.16.1 JTAG DC electrical characteristics

This table provides the JTAG DC electrical characteristics.

Table 51. JTAG DC electrical characteristics (OV_{DD} = 1.8V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	-	-100/+50	μA	2, 4
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol found in Table 3.

3. For recommended operating conditions, see Table 3.

4. TDI, TMS, and TRST_B have internal pull-ups per the IEEE Std. 1149.1 specification.

3.16.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 25 through Figure 28.

Table 52. JTAG AC timing specifications[4]

Parameter	Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0	2	ns	—
TRST_B assert time	t_{TRST}	25	—	ns	2
Input setup times	t_{JTDVKH}	4	—	ns	5
Input hold times	t_{JTDXKH}	10	—	ns	—
Output valid times	t_{JTKLDV}			ns	3
Boundary-scan data		—	15		
TDO		—	10		

Table continues on the next page...

Table 52. JTAG AC timing specifications[4] (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Output hold times	t_{JTKLDX}	0	—	ns	3

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2.TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.

3. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

4. For recommended operating conditions, see Table 3.

5. LP_TMP_DETECT pin requires 9.5ns input setup time for the board JTAG test to go through runTESTIdle.

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

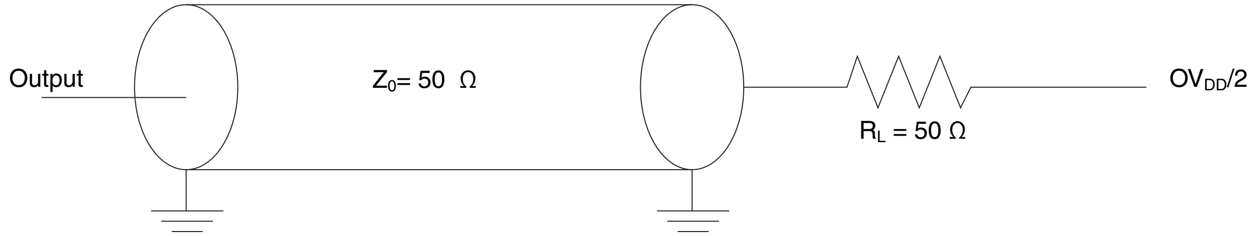


Figure 25. AC test load for the JTAG interface

This figure provides the JTAG clock input timing diagram.

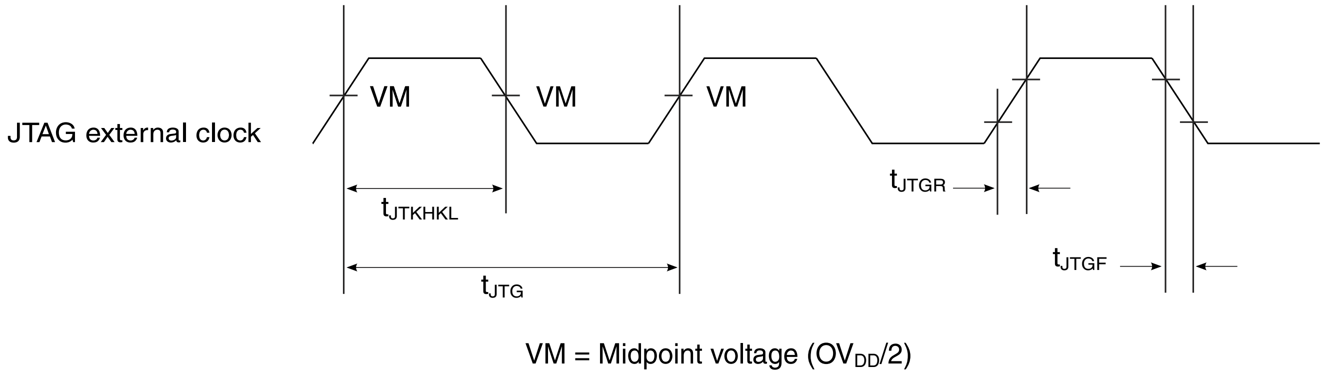


Figure 26. JTAG clock input timing diagram

This figure provides the TRST_B timing diagram.

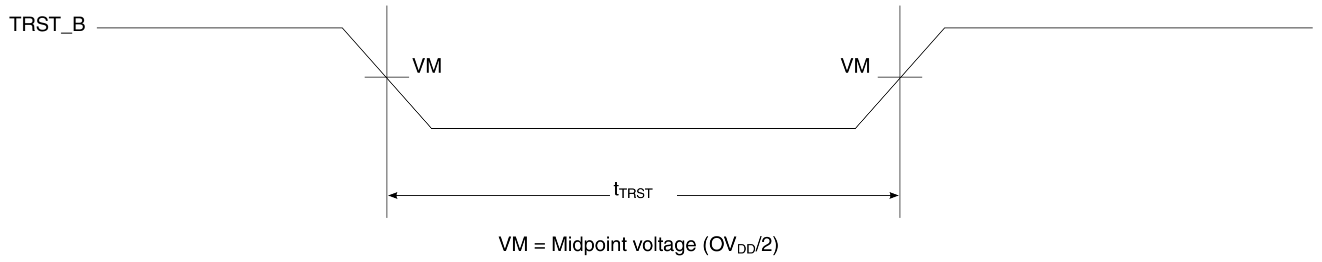


Figure 27. TRST_B timing diagram

This figure provides the boundary-scan timing diagram.

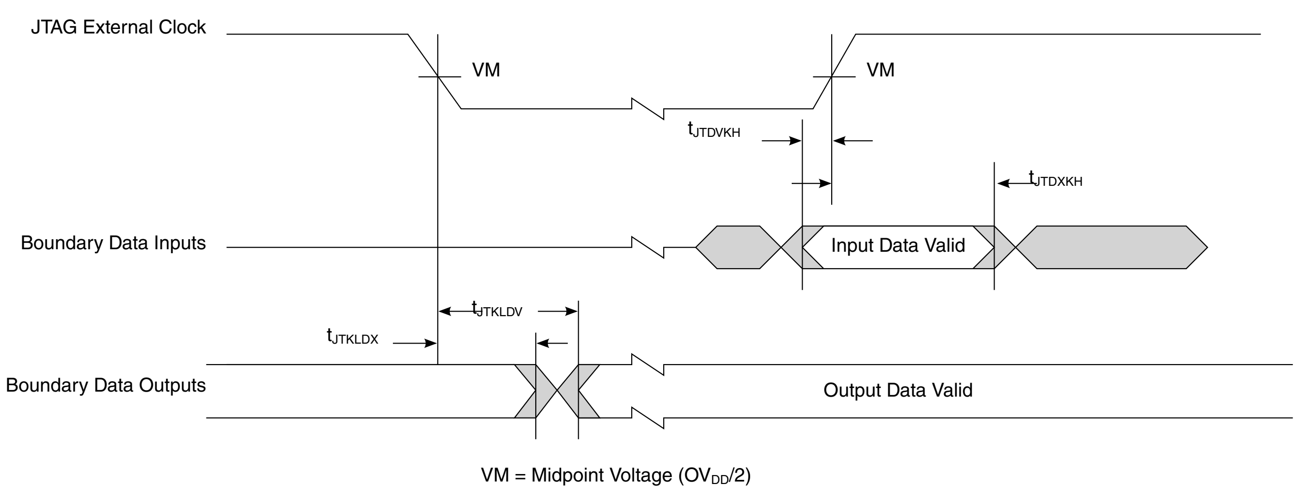


Figure 28. Boundary-scan timing diagram

3.17 I²C interface

This section describes the DC and AC electrical characteristics for the I²C interface.

3.17.1 I²C DC electrical characteristics

This table provides the DC electrical characteristics for the I²C interfaces operating at 2.5V.

Table 53. I^2C DC electrical characteristics (DV_{DD} = 2.5V)[5]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	-	V	1
Input low voltage	V_{IL}	-	0.7	V	1
Output low voltage (OV_{DD} = min, I_{OL} = 3 mA)	V_{OL}	0	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 x OV_{DD} and 0.9 x OV_{DD}(max)	I_I	-50	50	μA	4
Capacitance for each I/O pin	C_I	-	10	pF	-

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the chip reference manual for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.
5. For recommended operating conditions, see Table 3.

This table provides the DC electrical characteristics for the I^2C interfaces operating at 1.8V.

Table 54. I^2C DC electrical characteristics (DV_{DD} = 1.8V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	0	0.36	V	
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between 0.1 x OV_{DD} and 0.9 x OV_{DD}(max)	I_I	-50	50	μA	3
Capacitance for each I/O pin	C_I	-	10	pF	-

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. See the chip reference manual for information about the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.
4. For recommended operating conditions, see Table 3.

3.17.2 I^2C AC timing specifications

This table provides the AC timing parameters for the I^2C interfaces.

Table 55. I^2C AC timing specifications[5]

Parameter	Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	-	μs	-
High period of the SCL clock	t_{I2CH}	0.6	-	μs	-
Setup time for a repeated START condition	t_{I2SVKH}	0.6	-	μs	-
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	-	μs	-
Data setup time	t_{I2DVKH}	100	-	ns	-
Data input hold time:	t_{I2DXKL}			μs	3
CBUS compatible masters		-	-		
I^2C bus devices		0	-		
Data output delay time	t_{I2OVKL}	-	0.9	μs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	-	μs	-
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	-	μs	-
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 x OV_{DD}	-	V	-
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 x OV_{DD}	-	V	-
Capacitive load for each bus line	Cb	-	400	pF	-

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^2C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^2C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^2C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.

2. The requirements for I^2C frequency calculation must be followed. See *Determining the I^2C Frequency Divider Ratio for SCL* (AN2919).

3. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I^2C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the chip as transmitter, see *Determining the I^2C Frequency Divider Ratio for SCL* (AN2919).

4. The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

5. For recommended operating conditions, see Table 3.

This figure provides the AC test load for the I^2C.

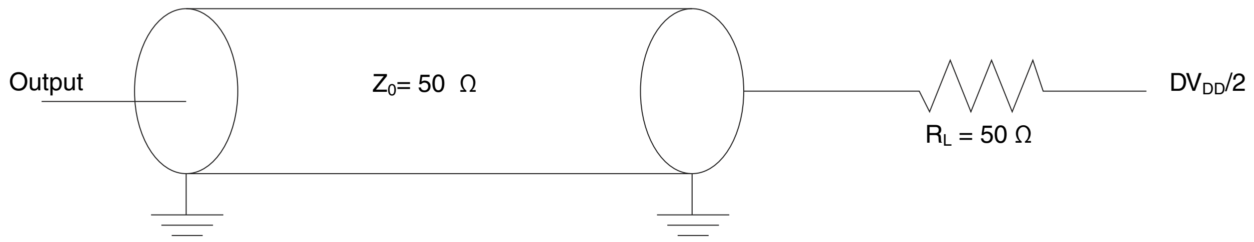


Figure 29. I²C AC test load

This figure shows the AC timing diagram for the I²C bus.

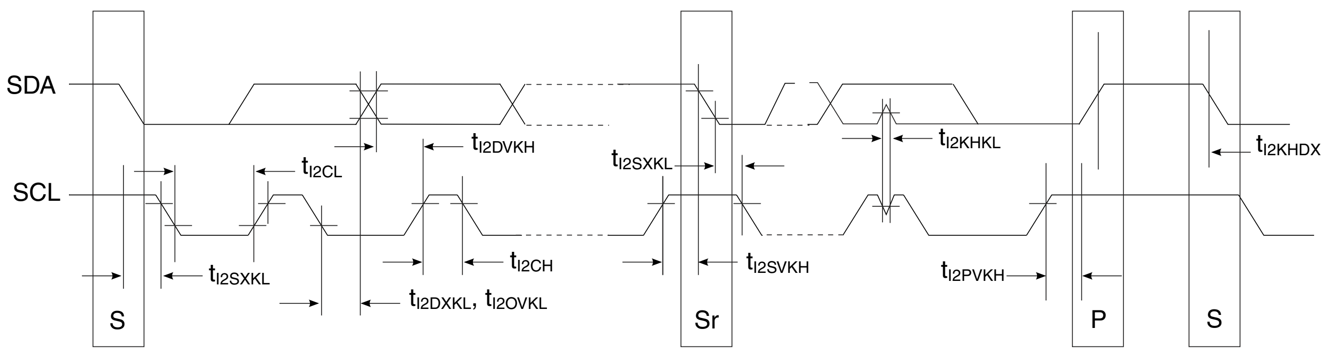


Figure 30. I²C Bus AC timing diagram

3.18 GPIO interface

This section describes the DC and AC electrical characteristics for the GPIO interface.

3.18.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for GPIO pins operating at LV_{DD} = 2.5 V.

Table 56. GPIO DC electrical characteristics (2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	-	V	1
Input low voltage	V_{IL}	-	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	-50	+50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	-	V	-

Table continues on the next page...

Table 56. GPIO DC electrical characteristics (2.5 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output low voltage (LV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	-	0.4	V	-
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3 . 2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions. 3. For recommended operating conditions, see Table 3.					

This table provides the DC electrical characteristics for GPIO pins operating at LV_{DD} or OV_{DD}= 1.8 V.

Table 57. GPIO DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = L/OV_{DD})	I_{IN}	-	±50	μA	2
Output high voltage (L/OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (L/OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-
1. The min V_{IL} and max V_{IH} values are based on the respective min and max L/OV_{IN} values found in Table 3. 2. The symbol V_{IN}, in this case, represents the L/OV_{IN} symbol referenced in Recommended operating conditions. 3. For recommended operating conditions, see Table 3.					

3.18.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

Table 58. GPIO input AC timing specifications[2]

Parameter	Symbol	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1
Notes: 1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation. 2. For recommended operating conditions, see Table 3.				

This figure provides the AC test load for the GPIO.

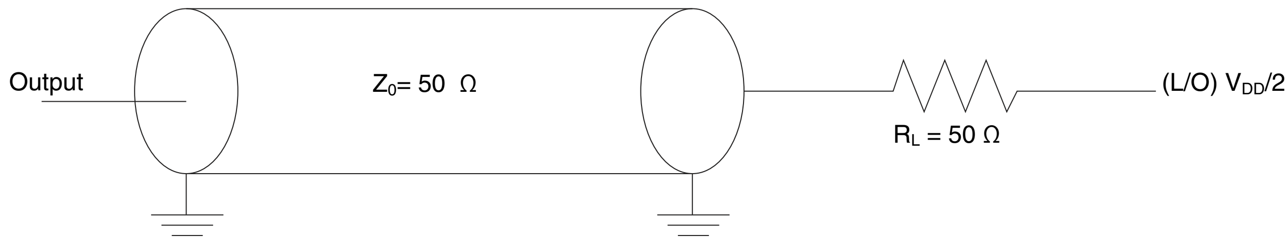


Figure 31. GPIO AC test load

3.19 High-speed serial interfaces (HSSI)

The chip features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, XFI, and SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

3.19.1 Signal terms definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n*_P and SD_TX*n*_N) or a receiver input (SD_RX*n*_P and SD_RX*n*_N). Each signal swings between A volts and B volts where A > B.

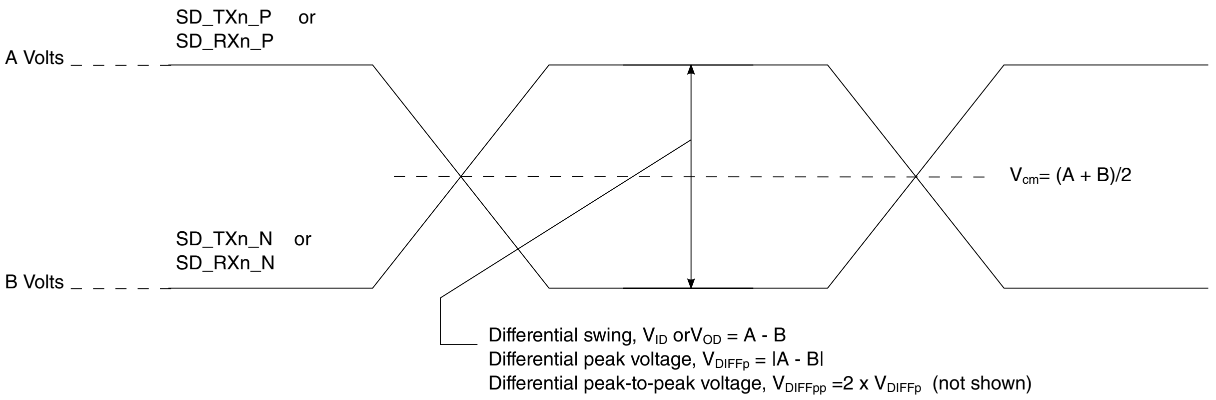


Figure 32. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing

The transmitter output signals and the receiver input signals SD_TX*n*_P, SD_TX*n*_N, SD_RX*n*_P and SD_RX*n*_N each have a peak-to-peak swing of A - B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing)

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TXn\_P} - V_{SD\_TXn\_N}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing)

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RXn\_P} - V_{SD\_RXn\_N}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_N, for example) from the non-inverting signal (SD_TX*n*_P, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 37 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TXn\_P} + V_{SD\_TXn\_N}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp\text{-}p}$) is 1000 mV p-p.

3.19.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N for SerDes 1.

SerDes 1 may be used for various combinations of the following IP blocks based on the RCW Configuration field SRDS_PRTCLn:

- SerDes 1: SGMII (1.25 and 3.125 GBaud), PEX3 (2.5, 5 and 8 GT/s), PEX4 (2.5 and 5 GT/s), XFI (10.3125 GBaud only), 1000Base-KX (3.125GBaud), 10GBase-KR (10.3125 GBaud only)

The following sections describe the SerDes reference clock requirements and provide application information.

3.19.2.1 SerDes spread-spectrum clock source recommendations

SD1_REF_CLKn_P/SD1_REF_CLKn_N are designed to work with spread-spectrum clock for PCI Express protocol only with the spreading specification defined in Table 59. When using spread-spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

The spread-spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread-spectrum supported protocols. For example, if the spread-spectrum clocking is desired on a SerDes reference clock for PCI Express and the same reference clock is used for any other protocol such as SGMII due to the SerDes lane usage mapping option, spread-spectrum clocking cannot be used at all.

Table 59. SerDes spread-spectrum clock source recommendations[1]

Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	-
Frequency spread	+0	-0.5	%	2
Notes:				
1. At recommended operating conditions. See Table 3.				
2. Only down-spreading is allowed.				

3.19.2.2 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

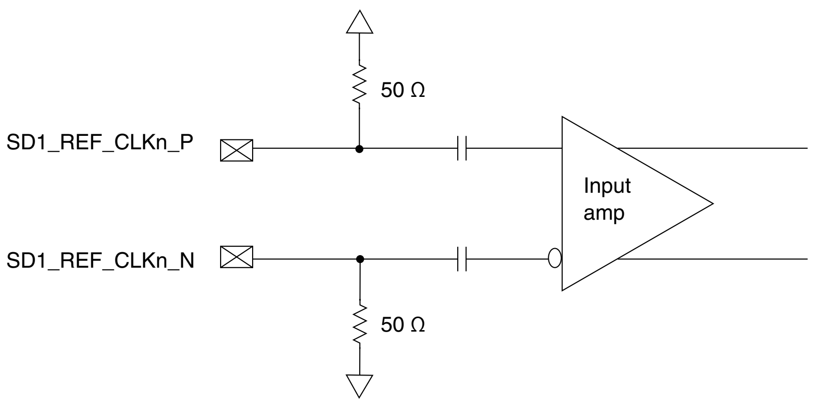


Figure 33. Receiver of SerDes reference clocks

The characteristics of the clock signals are as follows:

- The SerDes transceivers core power supply voltage requirements ($SV_{DD}n$) are as specified in Recommended operating conditions.

- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N are internally AC-coupled differential inputs as shown in Figure 33. Each differential clock input (SD1_REF_CLK*n*_P or SD1_REF_CLK*n*_N) has on-chip 50-Ω termination to SGND*n*followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND*n*. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N inputs cannot drive 50 Ω to SGND*n* DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

3.19.2.3 DC-level requirement for SerDes reference clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below.

Differential mode:

- The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

- For an external DC-coupled connection, as described in SerDes reference clock receiver characteristics, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 34 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

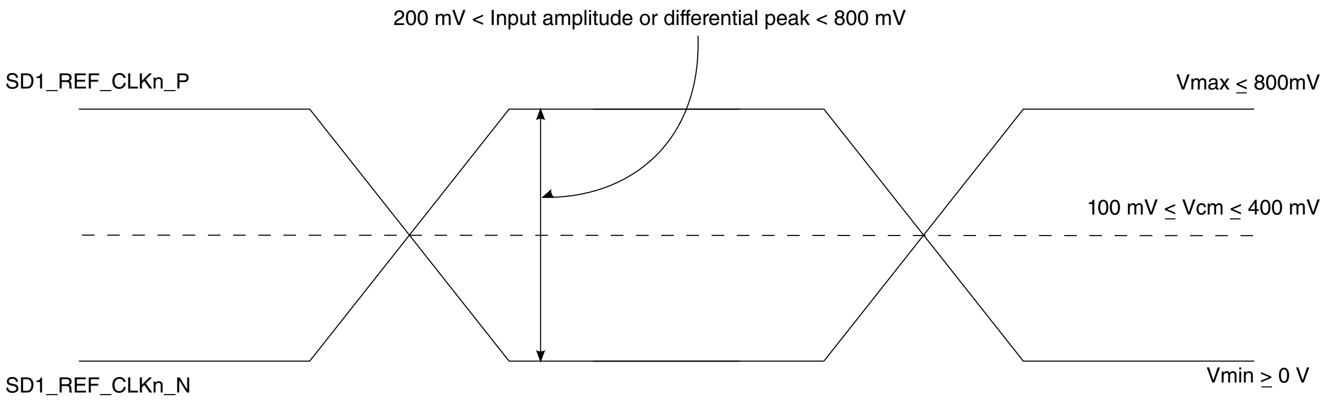


Figure 34. Differential reference clock input DC requirements (external DC-coupled)

- For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGNDn. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGNDn). Figure 35 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

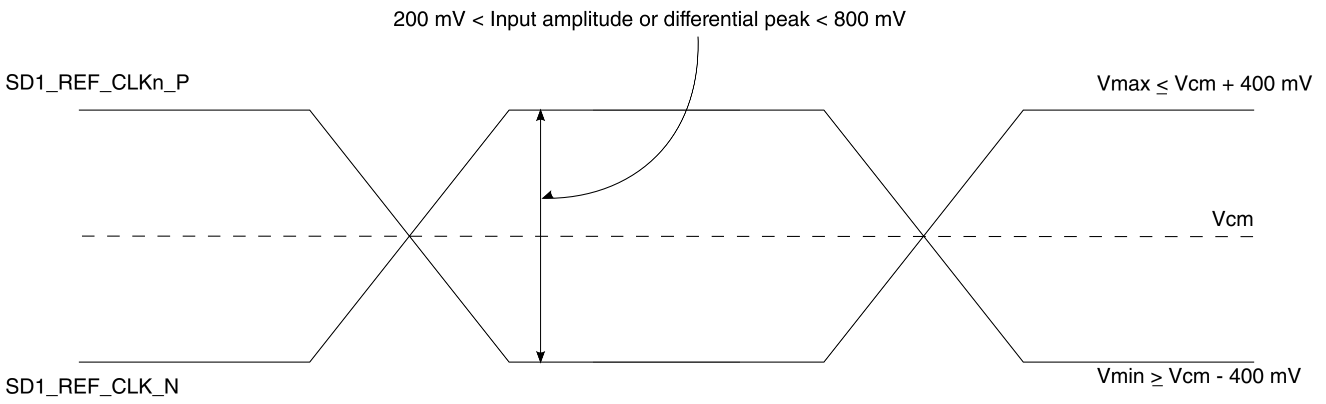


Figure 35. Differential reference clock input DC requirements (external AC-coupled)

Single-ended mode:

- The reference clock can also be single-ended. The SD1_REF_CLKn_P input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to-peak (from V_{MIN} to V_{MAX}) with SD1_REF_CLKn_N either left unconnected or tied to ground.
- The SD1_REF_CLKn_P input average voltage must be between 200 and 400 mV. Figure 36 shows the SerDes reference clock input requirement for single-ended signaling mode.
- To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SD1_REF_CLKn_N) through the same source impedance as the clock input (SD1_REF_CLKn_P) in use.

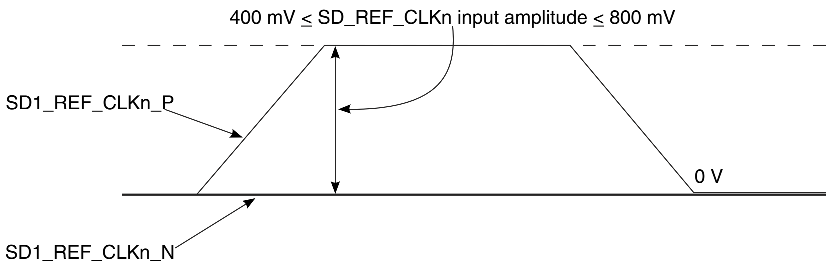


Figure 36. Single-ended reference clock input DC requirements

3.19.2.4 AC requirements for SerDes reference clocks

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates up to 8 GBaud.

This includes PCI Express (2.5, 5 and 8 GT/s), SGMII (1.25GBuad), 2.5x SGMII (3.125GBaud), and SerDes reference clocks to be guaranteed by the customer's application design.

Table 60. SD1_REF_CLKn_P/ SD1_REF_CLKn_N input clock requirements ($SV_{DD}n$ = 1.0 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLKn_P/ SD1_REF_CLKn_N frequency range	t_{CLK_REF}	-	100/125/156.25	-	MHz	2
SD1_REF_CLKn_P/ SD1_REF_CLKn_N clock frequency tolerance	t_{CLK_TOL}	-300	-	300	ppm	3
SD1_REF_CLKn_P/ SD1_REF_CLKn_N clock frequency tolerance	t_{CLK_TOL}	-100	-	100	ppm	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD1_REF_CLKn_P/ SD1_REF_CLKn_N max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	-	-	42	ps	-

Table continues on the next page...

Table 60. SD1_REF_CLKn_P/ SD1_REF_CLKn_N input clock requirements ($SV_{DD}n$ = 1.0 V)[1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLKn_P/ SD1_REF_CLKn_N total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	-	-	86	ps	6
SD1_REF_CLKn_P/ SD1_REF_CLKn_N 10 kHz to 1.5 MHz RMS jitter	$t_{REFCLK-LF-RMS}$	-	-	3	ps RMS	7
SD1_REF_CLKn_P/ SD1_REF_CLKn_N > 1.5 MHz to Nyquist RMS jitter	$t_{REFCLK-HF-RMS}$	-	-	3.1	ps RMS	7
SD1_REF_CLKn_P/ SD1_REF_CLKn_N RMS reference clock jitter	$t_{REFCLK-RMS-DC}$	-	-	1	ps RMS	8
SD1_REF_CLKn_P/ SD1_REF_CLKn_N rising/ falling edge rate	t_{CLKRR}/t_{CLKFR}	1	-	4	V/ns	9
Differential input high voltage	V_{IH}	200	-	-	mV	5
Differential input low voltage	V_{IL}	-	-	-200	mV	5
Rising edge rate (SD1_REF_CLKn_P) to falling edge rate (SD1_REF_CLKn_P) matching	Rise-Fall Matching	-	-	20	%	10, 11

Notes:

1. For recommended operating conditions, see Table 3.

2. **Caution:** Only 100, 125 and 156.25 have been tested.In-between values do not work correctly with the rest of the system.

3. For PCI Express (2.5, 5, 8 GT/s)

4. For SGMII, 2.5x SGMII

5. Measurement taken from differential waveform

6. Limits from PCI Express CEM Rev 2.0

7. For PCI Express-5 GT/s, per PCI Express base specification rev 3.0

8. For PCI-Express-8 GT/s, per PCI-Express base specification rev 3.0

9. Measured from -200 mV to +200 mV on the differential waveform (derived from SD1_REF_CLKn_P minus SD1_REF_CLKn_N). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 37.

10. Measurement taken from single-ended waveform

11. Matching applies to rising edge for SD1_REF_CLKn_P and falling edge rate for SD1_REF_CLKn_N. It is measured using a 200 mV window centered on the median cross point where SD1_REF_CLKn_P rising meets SD1_REF_CLKn_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD1_REF_CLKn_P must be compared to the fall edge rate of SD1_REF_CLKn_N, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 38.

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates greater than 8 GBaud.

This includes XFI (10.3125 GBaud) and 10GBase-KR (10.3125 GBaud), SerDes reference clocks to be guaranteed by the customer's application design.

Table 61. SD1_REF_CLKn_P/ SD1_REF_CLKn_N input clock requirements ($SV_{DD}n$ = 1.0 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLKn_P/ SD1_REF_CLKn_N frequency range	t_{CLK_REF}	-	156.25	-	MHz	2
SD1_REF_CLKn_P/ SD1_REF_CLKn_N clock frequency tolerance	t_{CLK_TOL}	-100	-	100	ppm	-
SD1_REF_CLKn_P/ SD1_REF_CLKn_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	3
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@1 kHz	-	-	-85	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@10 kHz	-	-	-108	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@100 kHz	-	-	-128	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@1 MHz	-	-	-138	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@10MHz	-	-	-138	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N random jitter (1.2 MHz to 15 MHz)	t_{CLK_RJ}	-	-	0.8	ps	-
SD1_REF_CLKn_P/ SD1_REF_CLKn_N total reference clock jitter at 10^{-12} BER (1.2 MHz to 15 MHz)	t_{CLK_TJ}	-	-	11	ps	-
SD1_REF_CLKn_P/ SD1_REF_CLKn_N spurious noise (1.2 MHz to 15 MHz)	-	-	-	-75	dBC	-

Notes:

1. For recommended operating conditions, see Table 3.

2. **Caution:** Only 156.25 have been tested. In-between values do not work correctly with the rest of the system.

3. Measurement taken from differential waveform.

4. Per XFP Spec. Rev 4.5, the Module Jitter Generation spec at XFI Optical Output is 10mUI (RMS) and 100 mUI (p-p). In the CDR mode the host is contributing 7 mUI (RMS) and 50 mUI (p-p) jitter.

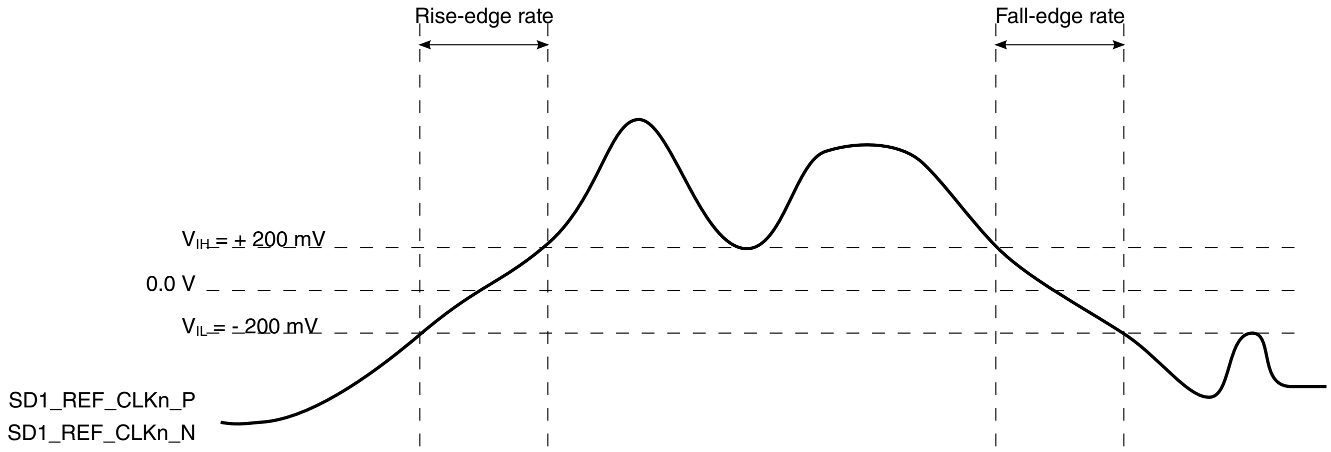


Figure 37. Differential measurement points for rise and fall time

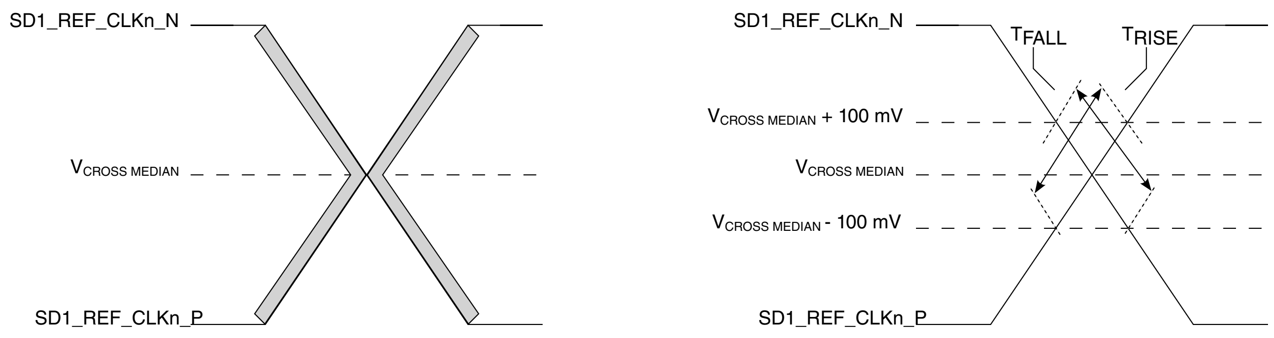


Figure 38. Single-ended measurement points for rise and fall time matching

3.19.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

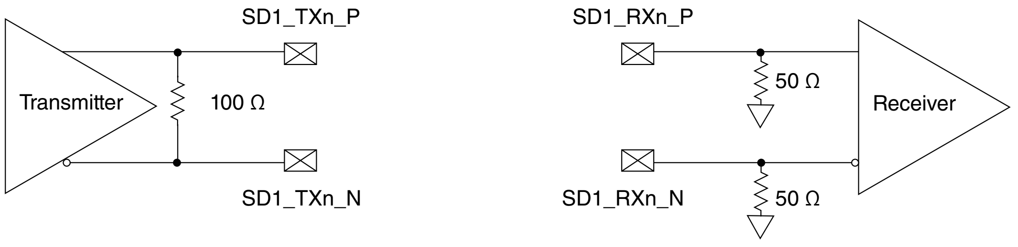


Figure 39. SerDes transmitter and receiver reference circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below based on the application usage:

- PCI Express
- SGMII interface
- XFI interface
- 10GBase-KR interface
- 1000Base-KX interface

Note that external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.19.4 PCI Express

This section describes the clocking dependencies, DC and AC electrical specifications for the PCI Express bus.

3.19.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.19.4.2 PCI Express clocking requirements for SD1_REF_CLKn_P and SD1_REF_CLKn_N

SerDes 1-2 (SD[1:2]_REF_CLK[1:2]_P and SD[1:2]_REF_CLK[1:2]_N) may be used for various SerDes PCI Express configurations based on the RCW Configuration field SRDS_PRTCL. PCI Express is not supported on SerDes 1 and 2.

NOTE

PCI Express operating in x8 mode is only supported at 2.5 and 5.0 GT/s.

For more information on these specifications, see SerDes reference clocks.

3.19.4.3 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

3.19.4.3.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 62. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p} = 2 \times \mid V_{TX-D+} - V_{TX-D-} \mid$
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low Impedance
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC Impedance during all states

Notes:

1. For recommended operating conditions, see Table 3.

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 63. PCI Express 2.0 (5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p} = 2 \times \mid V_{TX-D+} - V_{TX-D-} \mid$
Low power differential peak-to-peak output voltage	$V_{TX-DIFFp-p\_low}$	400	500	1200	mV	$V_{TX-DIFFp-p} = 2 \times \mid V_{TX-D+} - V_{TX-D-} \mid$
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Notes:

1. For recommended operating conditions, see Table 3.

This table defines the PCI Express 3.0 (8 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 64. PCI Express 3.0 (8 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Full swing transmitter voltage with no TX Eq	$V_{TX-FS-NO-EQ}$	800	-	1300	mVp-p	See Note 1.
Reduced swing transmitter voltage with no TX Eq	$V_{TX-RS-NO-EQ}$	400	-	1300	mV	See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	-
Minimum swing during EIEOS for full swing	$V_{TX-EIEOS-FS}$	250	-	-	mVp-p	See Note 2
Minimum swing during EIEOS for reduced swing	$V_{TX-EIEOS-RS}$	232	-	-	mVp-p	See Note 2
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Notes:

1. Voltage measurements for $V_{TX-FS-NO-EQ}$ and $V_{TX-RS-NO-EQ}$ are made using the 64-zeroes/64-ones pattern in the compliance pattern.

2. Voltage limits comprehend both full swing and reduced swing modes. The transmitter must reject any changes that would violate this specification. The maximum level is covered in the $V_{TX-FS-NO-EQ}$ measurement which represents the maximum peak voltage the transmitter can drive. The $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ voltage limits are imposed to guarantee the EIEOS threshold of 175 mV_{P-P} at the receiver pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel.

3. For recommended operating conditions, see Table 3.

3.19.4.4 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 65. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0 V)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX\text{-}DIFFp\text{-}p}$	120	1000	1200	mV	$V_{RX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-}\rvert$ See Note 1.
DC differential input impedance	$Z_{RX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	$Z_{RX\text{-}DC}$	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	65	-	175	mV	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-}\rvert$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.

2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.

4. For recommended operating conditions, see Table 3.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 66. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0 V)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX\text{-}DIFFp\text{-}p}$	120	1000	1200	mV	$V_{RX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-}\rvert$ See Note 1.
DC differential input impedance	$Z_{RX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	$Z_{RX\text{-}DC}$	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	65	-	175	mV	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-}\rvert$

Table continues on the next page...

Table 66. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0 V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
						Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50 Ω to GND on each pin.

2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.

4. For recommended operating conditions, see Table 3.

This table defines the DC specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 67. PCI Express 3.0 (8 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0 V)[6]

Parameter	Symbol	Min	Typ	Max	Units	Notes
DC differential input impedance	$Z_{RX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	$Z_{RX\text{-}DC}$	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Generator launch voltage	$V_{RX\text{-}LAUNCH\text{-}8G}$	-	800	-	mV	Measured at TP1 per PCI Express base spec. rev 3.0
Eye height (-20dB Channel)	$V_{RX\text{-}SV\text{-}8G}$	25	-	-	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Eye height (-12dB Channel)	$V_{RX\text{-}SV\text{-}8G}$	50	-	-	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Eye height (-3dB Channel)	$V_{RX\text{-}SV\text{-}8G}$	200	-	-	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Electrical idle detect threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	65	-	175	mV	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.

2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

Table 67. PCI Express 3.0 (8 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0 V)[6]

Parameter	Symbol	Min	Typ	Max	Units	Notes
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.						
4. $V_{RX\text{-}SV\text{-}8G}$ is tested at three different voltages to ensure the receiver device under test is capable of equalizing over a range of channel loss profiles. The "SV" in the parameter names refers to stressed voltage.						
5. $V_{RX\text{-}SV\text{-}8G}$ is referenced to TP2P and is obtained after post processing data captured at TP2.						
6. For recommended operating conditions, see Table 3.						

3.19.4.5 PCI Express AC physical layer specifications

This section contains the AC specifications for the physical layer of PCI Express on this device.

3.19.4.5.1 PCI Express AC physical layer transmitter specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 68. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	$T_{TX\text{-}EYE}$	0.75	-	-	UI	The maximum transmitter jitter can be derived as $T_{TX\text{-}MAX\text{-}JITTER} = 1 - T_{TX\text{-}EYE}$ = 0.25 UI. Does not include spread-spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	-	-	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1 and 2.

Table continues on the next page...

Table 68. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Notes:

1. Specified at the measurement point into a timing and voltage test load as shown in Figure 41 and measured over any 250 consecutive transmitter UIs.

2. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

4. For recommended operating conditions, see Table 3.

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 69. PCI Express 2.0 (5 GT/s) differential transmitter output AC specifications[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = 0.25 UI. See Note 1.
Transmitter RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	-	-	0.15	ps	-
Transmitter RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	-	3.0	-	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 2.

Notes:

1. Specified at the measurement point into a timing and voltage test load as shown in Figure 41 and measured over any 250 consecutive transmitter UIs.

2. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

3. For recommended operating conditions, see Table 3.

This table defines the PCI Express 3.0 (8 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 70. PCI Express 3.0 (8 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	124.9625	125.00	125.0375	ps	Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Transmitter uncorrelated total jitter	T_{TX-UTJ}	-	-	31.25	ps p-p	-
Transmitter uncorrelated deterministic jitter	$T_{TX-UDJ-DD}$	-	-	12	ps p-p	-
Total uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-TJ}$	-	-	24	ps p-p	See Note 1, 2
Deterministic data dependent jitter (DjDD) uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-DJDD}$	-	-	10	ps p-p	See Note 1, 2
Data dependent jitter	T_{TX-DDJ}	-	-	18	ps p-p	See Note 2
AC coupling capacitor	C_{TX}	176	-	265	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Notes:

1. PWJ parameters shall be measured after data dependent jitter (DDJ) separation.
2. Measured with optimized preset value after de-embedding to transmitter pin.
3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
4. For recommended operating conditions, see Table 3.

3.19.4.5.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 71. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.

Table continues on the next page...

Table 71. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Minimum receiver eye width	$T_{RX\text{-}EYE}$	0.4	-	-	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX\text{-}MAX\text{-}JITTER}$ = 1 - $T_{RX\text{-}EYE}$= 0.6 UI. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	-	-	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1, 2 and 3.

Notes:

1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 41 must be used as the receiver device when taking measurements. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

2. A $T_{RX\text{-}EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

3. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

4. For recommended operating conditions, see Table 3.

This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 72. PCI Express 2.0 (5 GT/s) differential receiver input AC specifications[1]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Max receiver inherent timing error	$T_{RX\text{-}TJ\text{-}CC}$	-	-	0.4	UI	The maximum inherent total timing error for common RefClk receiver architecture
Max receiver inherent deterministic timing error	$T_{RX\text{-}DJ\text{-}DD\text{-}CC}$	-	-	0.30	UI	The maximum inherent deterministic timing error for common RefClk receiver architecture

Table continues on the next page...

Table 72. PCI Express 2.0 (5 GT/s) differential receiver input AC specifications[1] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Note: 1. For recommended operating conditions, see Table 3.						

This table defines the AC specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 73. PCI Express 3.0 (8 GT/s) differential receiver input AC specifications[5]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	124.9625	125.00	125.0375	ps	Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations. See Note 1.
Eye Width at TP2P	$T_{RX\text{-}SV\text{-}8G}$	0.3	-	0.35	UI	See Note 1
Differential mode interference	$V_{RX\text{-}SV\text{-}DIFF\text{-}8G}$	14	-	-	mV	Frequency = 2.1GHz. See Note 2.
Sinusoidal Jitter at 100 MHz	$T_{RX\text{-}SV\text{-}SJ\text{-}8G}$	-	-	0.1	UI p-p	Fixed at 100 MHz. See Note 3.
Random Jitter	$T_{RX\text{-}SV\text{-}RJ\text{-}8G}$	-	-	2.0	ps RMS	Random jitter spectrally flat before filtering. See Note 4.

Note:

1. $T_{RX\text{-}SV\text{-}8G}$ is referenced to TP2P and obtained after post processing data captured at TP2. $T_{RX\text{-}SV\text{-}8G}$ includes the effects of applying the behavioral receiver model and receiver behavioral equalization.

2. $V_{RX\text{-}SV\text{-}DIFF\text{-}8G}$ voltage may need to be adjusted over a wide range for the different loss calibration channels.

3. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency as shown in Figure 40.

4. Random jitter (Rj) is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. See Figure 40 for details. Rj may be adjusted to meet the 0.3 UI value for $T_{RX\text{-}SV\text{-}8G}$.

5. For recommended operating conditions, see Table 3.

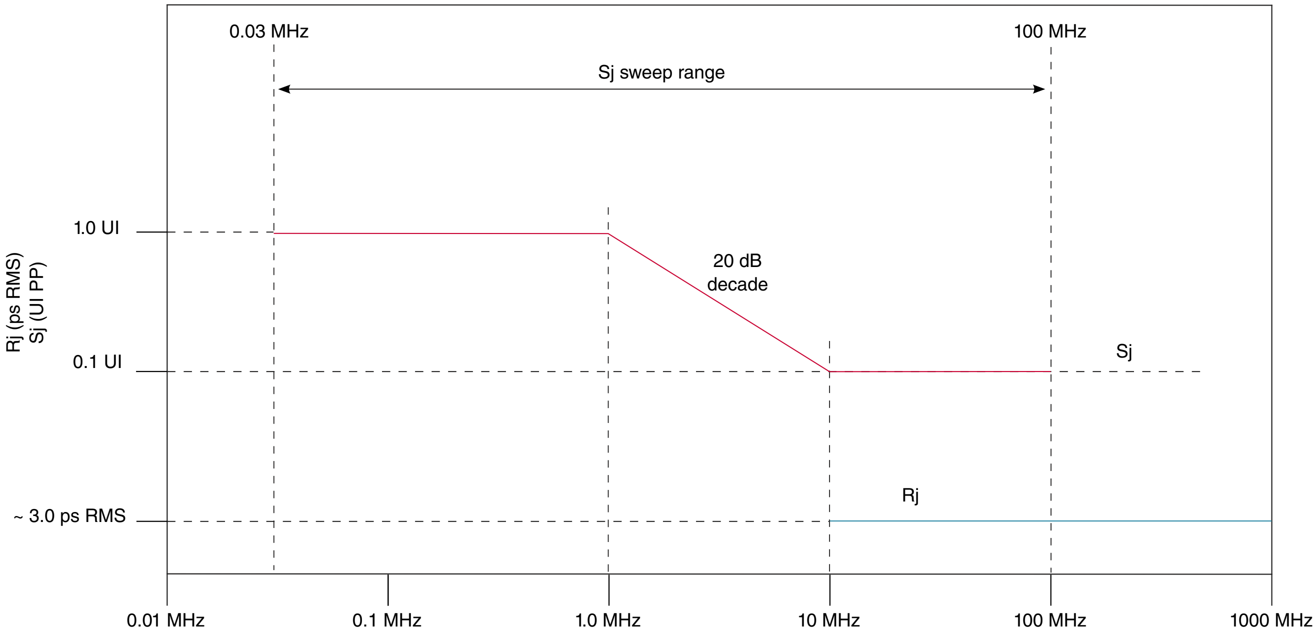


Figure 40. Swept sinusoidal jitter mask

3.19.4.6 Test and measurement load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/ board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D- package pins.

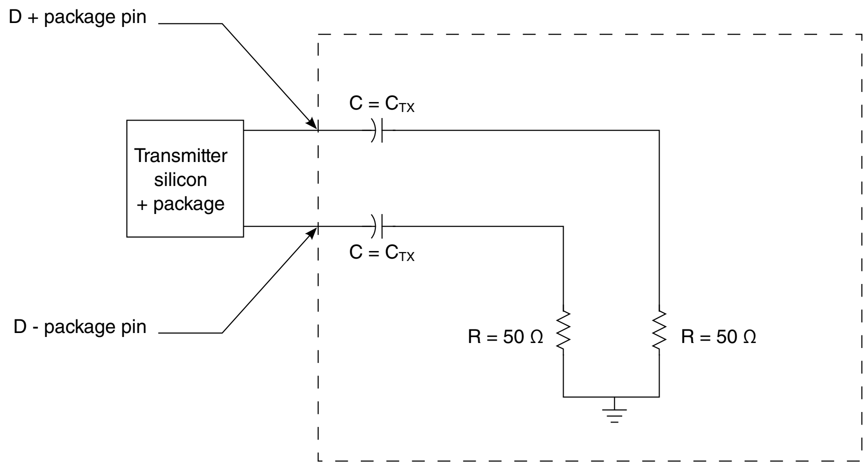


Figure 41. Test/measurement load

3.19.5 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 42, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND*n*. The reference circuit of the SerDes transmitter and receiver is shown in Figure 39 .

3.19.5.1 SGMII clocking requirements for SD1_REF_CLKn_P and SD1_REF_CLKn_N

When operating in SGMII mode, the ECn_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_Npins. SerDes 1 may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.19.5.2 SGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

3.19.5.2.1 SGMII and SGMII 2.5x transmit DC specifications

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD1_TX*n*_P and SD1_TX*n*_N)as shown in Figure 43.

Table 74. SGMII DC transmitter electrical characteristics (XV_{DD} = 1.35 V)[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	-	-	1.5 x $\lvert V_{OD} \rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD} \rvert_{-min}/2$	-	-	mV	1
Output differential voltage[2, 3] (XV_{DD-Typ} at 1.35 V)	$\lvert V_{OD} \rvert$	320	500.0	725.0	mV	-
		293.8	459.0	665.6		-
		266.9	417.0	604.7		-
		240.6	376.0	545.2		-
		213.1	333.0	482.9		-
		186.9	292.0	423.4		-
		160.0	250.0	362.5		-
Output impedance (differential)	R_O	80	100	120	Ω	-

Notes:

1. This does not align to DC-coupled SGMII.

2. $\lvert V_{OD} \rvert = \lvert V_{SD\_TXn\_P} - V_{SD\_TXn\_N} \rvert$. $\lvert V_{OD} \rvert$ is also referred to as output differential peak voltage. $V_{TX-DIFFp-p} = 2 \times \lvert V_{OD} \rvert$.

3. The $\lvert V_{OD} \rvert$ value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.35 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SD1_TXn_P and SD1_TXn_N.

4. For recommended operating conditions, see Table 3.

This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

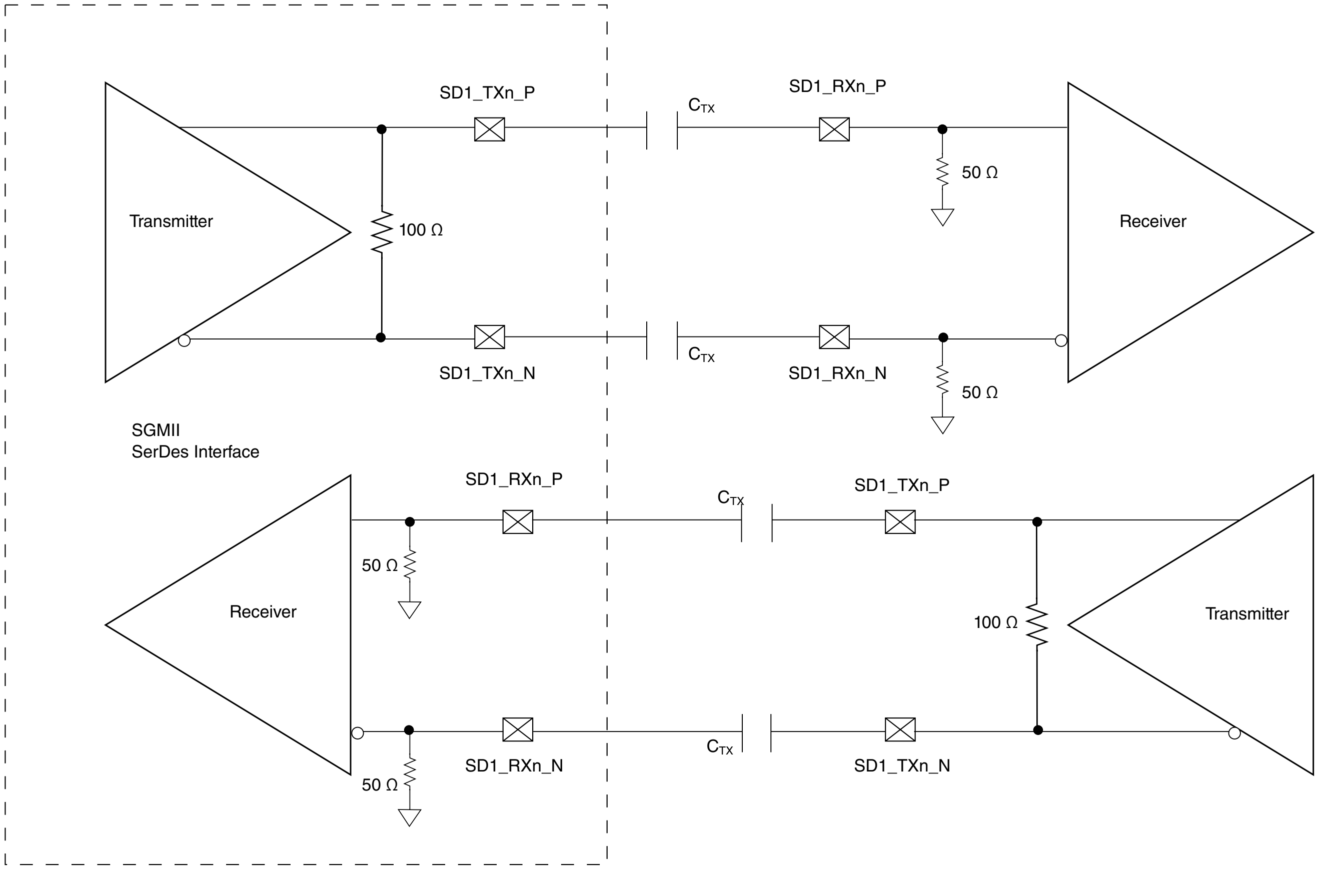


Figure 42. 4-wire AC-coupled SGMII serial link connection example

This figure shows the SGMII transmitter DC measurement circuit.

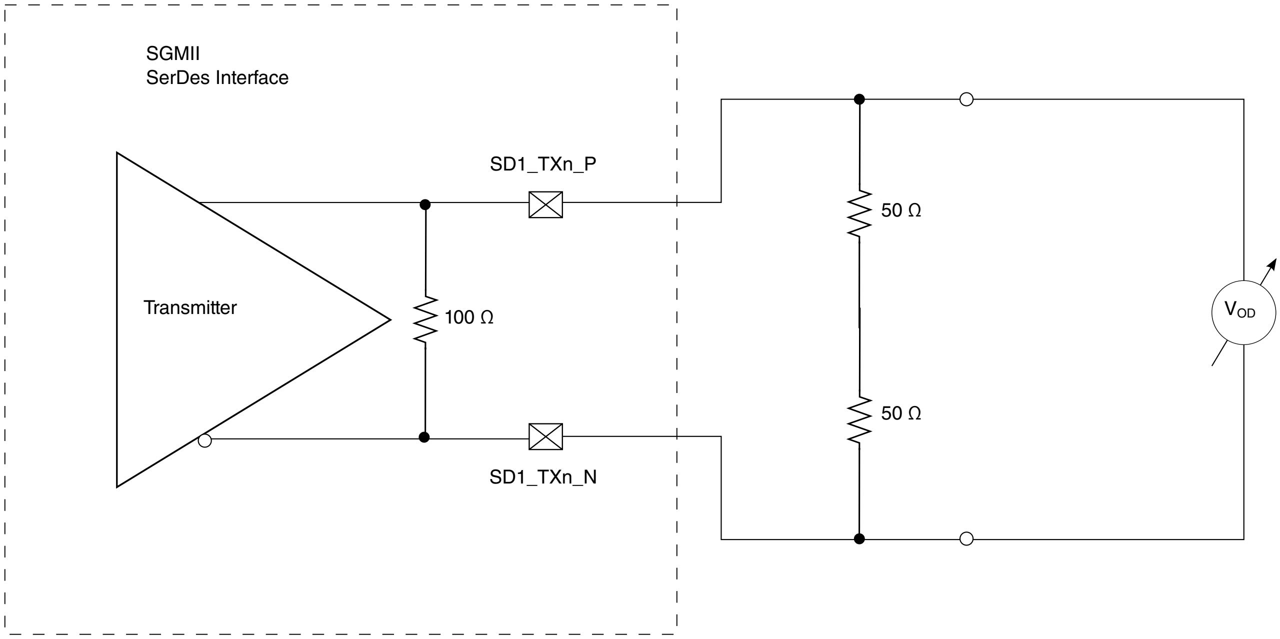


Figure 43. SGMII transmitter DC measurement circuit

This table defines the SGMII 2.5x transmitter DC electrical characteristics for 3.125 GBaud.

Table 75. SGMII 2.5x transmitter DC electrical characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$\lvert V_{OD} \rvert$	400	-	600	mV	-
Output impedance (differential)	R_O	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 3.						

3.19.5.2.2 SGMII and SGMII 2.5x DC receiver electrical characteristics

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 76. SGMII DC receiver electrical characteristics (SV_{DD} = 1.0V)[4]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC input voltage range		-	N/A			-	1
Input differential voltage	-	$V_{RX\_DIFFp-p}$	100	-	1200	mV	2
	-		175	-			
Loss of signal threshold	-	V_{LOS}	30	-	100	mV	3
	-		65	-	175		

Table continues on the next page...

Table 76. SGMII DC receiver electrical characteristics (SV_{DD} = 1.0V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver differential input impedance	Z_{RX_DIFF}	80	-	120	Ω	-

Notes:

1. Input must be externally AC coupled.

2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.

3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See PCI Express DC physical layer receiver specifications, and PCI Express AC physical layer receiver specifications, for further explanation.

4. For recommended operating conditions, see Table 3.

This table defines the SGMII 2.5x receiver DC electrical characteristics for 3.125 GBaud.

Table 77. SGMII 2.5x receiver DC timing specifications (SV_{DD} = 1.0V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX\_DIFFp-p}$	200	-	1200	mV	-
Loss of signal threshold	V_{LOS}	75	-	200	mV	-
Receiver differential input impedance	Z_{RX_DIFF}	80	-	120	Ω	-

Notes:

1. For recommended operating conditions, see Table 3.

3.19.5.3 SGMII AC timing specifications

This section discusses the AC timing specifications for the SGMII interface.

3.19.5.3.1 SGMII and SGMII 2.5x transmit AC timing specifications

This table provides the SGMII and SGMII 2.5x transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 78. SGMII transmit AC timing specifications[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	2
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5x SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1
AC coupling capacitor	C_{TX}	10	—	200	nF	3

Notes:

1. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.

Table 78. SGMII transmit AC timing specifications[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
2. See Figure 45 for single frequency sinusoidal jitter measurements.						
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.						
4. For recommended operating conditions, see Table 3.						

3.19.5.3.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD1_TX*n*_P and SD1_TX*n*_N) or at the receiver inputs (SD1_RX*n*_P and SD1_RX*n*_N) respectively, as depicted in this figure.

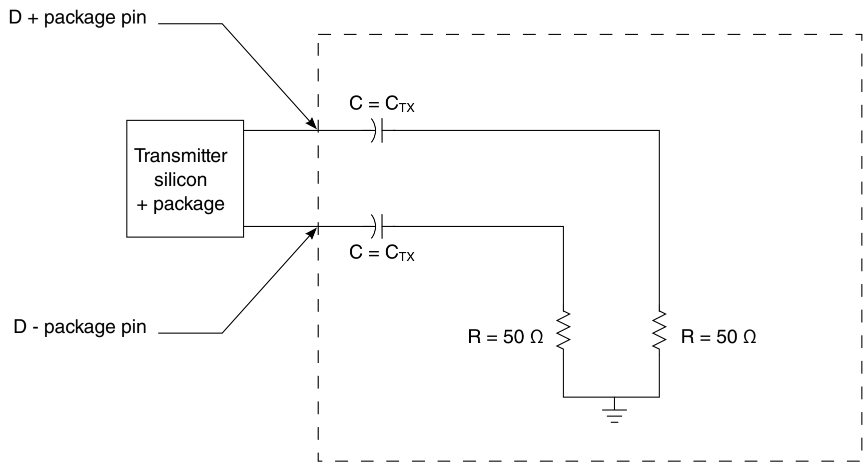


Figure 44. SGMII AC test/measurement load

3.19.5.3.3 SGMII and SGMII 2.5x receiver AC timing specification

This table provides the SGMII and SGMII 2.5x receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 79. SGMII Receive AC timing specifications[3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	—	—	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	—	—	0.55	UI p-p	1
Total jitter tolerance	J_T	—	—	0.65	UI p-p	1, 2
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5x SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1

Table continues on the next page...

Table 79. SGMII Receive AC timing specifications[3] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Notes: 1. Measured at receiver 2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 45. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects. 3. For recommended operating conditions, see Table 3.						

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of the following figure.

This figure shows the single-frequency sinusoidal jitter limits for 2.5 GBaud and 3.125 GBaud rates.

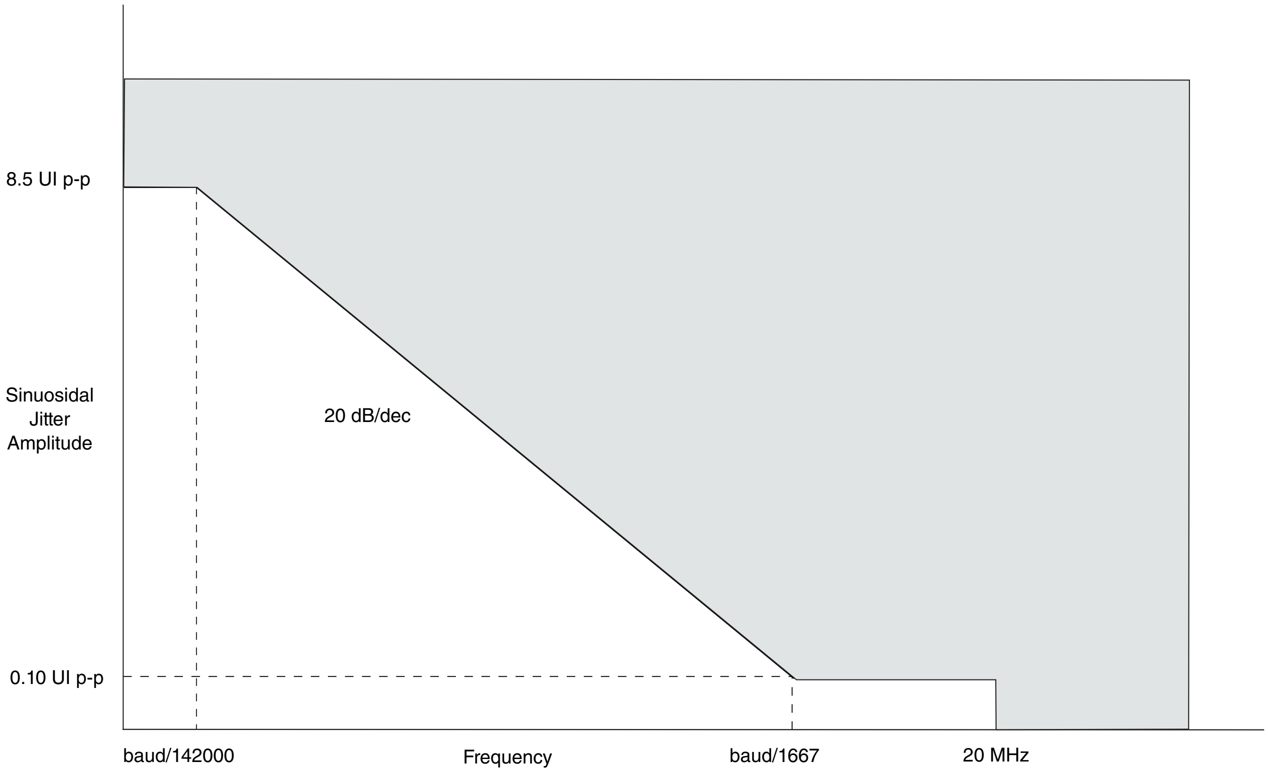


Figure 45. Single-frequency sinusoidal jitter limits

3.19.6 XFI interface

This section describes the XFI clocking requirements and its DC and AC electrical characteristics.

3.19.6.1 XFI clocking requirements for SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N

Only SerDes 1 (SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N) may be used for SerDes XFI configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.19.6.2 XFI DC electrical characteristics

This section describes the DC electrical characteristics for XFI.

3.19.6.2.1 XFI transmitter DC electrical characteristics

This table defines the XFI transmitter DC electrical characteristics.

Table 80. XFI transmitter DC electrical characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	360	-	770	mV	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-1.14 dB}$	0.6	1.1	1.6	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5 dB}$	3	3.5	4	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-4.66 dB}$	4.1	4.6	5.1	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0 dB}$	5.5	6.0	6.5	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-9.5 dB}$	9	9.5	10	dB	-
Differential resistance	T_{RD}	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 3.						

3.19.6.2.2 XFI receiver DC electrical characteristics

This table defines the XFI receiver DC electrical characteristics.

Table 81. XFI receiver DC electrical characteristics (SV_{DD} = 1.0V)[2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX-DIFF}$	110	-	1050	mV	1

Table continues on the next page...

Table 81. XFI receiver DC electrical characteristics (SV_{DD} = 1.0V)[2] (continued)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential resistance	R_{RD}	80	100	120	Ω	-
1. Measured at receiver						
2. For recommended operating conditions, see Table 3.						

3.19.6.3 XFI AC timing specifications

This section describes the AC timing specifications for XFI.

3.19.6.3.1 XFI transmitter AC timing specifications

This table defines the XFI transmitter AC timing specifications. RefClk jitter is not included.

Table 82. XFI transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100ppm	10.3125	10.3125 + 100ppm	Gb/s
Unit Interval	UI	-	96.96	-	ps
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter	T_J	-	-	0.30	UI p-p
Notes:					
1. For recommended operating conditions, see Table 3.					

3.19.6.3.2 XFI receiver AC timing specifications

This table defines the XFI receiver AC timing specifications. RefClk jitter is not included.

Table 83. XFI receiver AC timing specifications[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 - 100ppm	10.3125	10.3125 + 100ppm	Gb/s	-
Unit Interval	UI	-	96.96	-	ps	-
Total non-EQJ jitter	$T_{NON-EQJ}$	-	-	0.45	UI p-p	1
Total jitter tolerance	T_J	-	-	0.65	UI p-p	1, 2
1. The total jitter (T_J) consists of Random Jitter (R_J), Duty Cycle Distortion (DCD), Periodic Jitter (P_J), and Inter symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter (R_J), and periodic jitter (P_J). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non - EQJ = T_J - ISI = R_J + DCD + P_J						

Table 83. XFI receiver AC timing specifications[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
2. The XFI channel has a loss budget of 9.6 dB @5.5GHz. The channel loss including connector @ 5.5GHz is 6dB. The channel crosstalk and reflection margin is 3.6dB. Manual tuning of TX Equalization and amplitude will be required for performance optimization.						
3. For recommended operating conditions, see Table 3.						

This figure shows the sinusoidal jitter tolerance of XFI receiver.

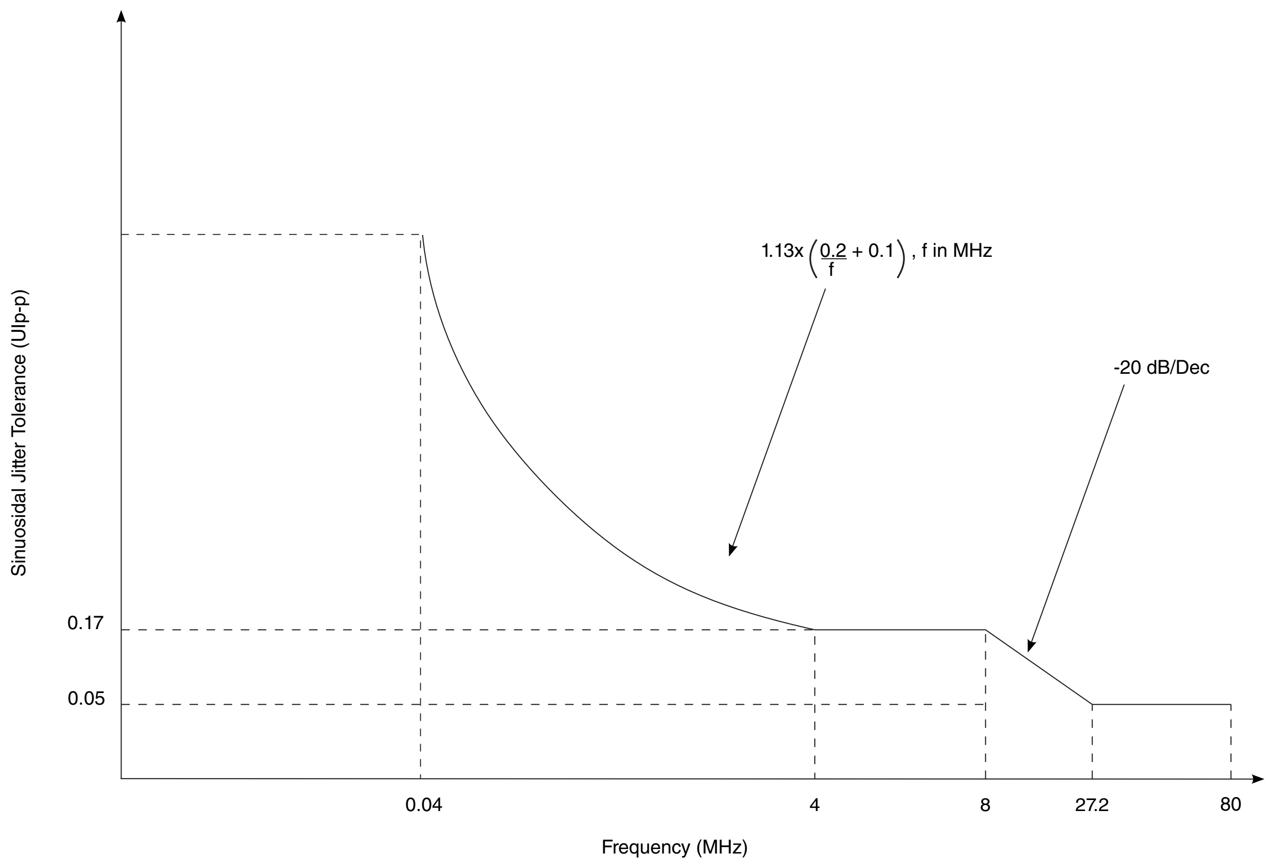


Figure 46. XFI host receiver input sinusoidal jitter tolerance

3.19.7 10GBase-KR interface

This section describes the 10GBase-KR clocking requirements and its DC and AC electrical characteristics.

3.19.7.1 10GBase-KR clocking requirements for SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B

Only SerDes 1 (SD1_REF_CLK[1:2]_Pand SD1_REF_CLK[1:2]_N) may be used for SerDes 10GBase-KR configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks .

3.19.7.2 10GBase-KR DC electrical characteristics

This section describes the DC electrical characteristics for 10GBase-KR.

3.19.7.2.1 10GBase-KR transmitter DC electrical characteristics

This table defines the 10GBase-KR transmitter DC electrical characteristics.

Table 84. 10GBaseKR transmitter DC electrical characteristics (XV_{DD} = 1.35V or 1.5V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	800	-	1200	mV	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3	3.5	4	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-9.5dB}$	9	9.5	10	dB	-
Differential resistance	T_{RD}	80	100	120	Ω	-
1. For recommended operating conditions, see Table 3.						

3.19.7.2.2 10GBase-KR receiver DC electrical characteristics

This table defines the 10GBase-KR receiver DC electrical characteristics.

Table 85. 10GBase-KR receiver DC electrical characteristics (XV_{DD} = 1.35V or 1.5V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX-DIFF}$	-	-	1200	mV	-
Differential resistance	R_{RD}	80	-	120	Ω	-
1. For recommended operating conditions, see Table 3.						

3.19.7.3 10GBase-KR AC timing specifications

This section describes the AC timing specifications for 10GBase-KR.

3.19.7.3.1 10GBase-KR transmitter AC timing specifications

This table defines the 10GBase-KR transmitter AC timing specifications. RefClk jitter is not included.

Table 86. 10GBase-KR transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	Gb/s
Uncorrelated high probability jitter/Random jitter	U_{HPJ}/R_J	-	-	0.15	UI p-p
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter	T_J	-	-	0.30	UI p-p
1. For recommended operating conditions, see Table 3.					

3.19.7.3.2 10GBase-KR receiver AC timing specifications

This table defines the 10GBase-KR receiver AC timing specifications. RefClk jitter is not included.

Table 87. 10GBase-KR receiver AC timing specifications[2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	Gb/s	-
Random jitter	R_J	-	-	0.130	UI p-p	-
Sinusodial jitter, maximum	$S_{J\text{-max}}$	-	-	0.115	UI p-p	-
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p	-
Total jitter	T_J	-	-	See Note 1	UI p-p	1
1. The total jitter (TJ) is per Interference tolerance test IEEE Standard 802.3ap-2007 specified in Annex 69A.						
2. For recommended operating conditions, see Table 3.						

3.19.8 1000Base-KX interface

This section discusses the electrical characteristics for the 1000Base-KX. Only AC-coupled operation is supported.

3.19.8.1 1000Base-KX DC electrical characteristics

3.19.8.1.1 1000Base-KX Transmitter DC Specifications

This table describes the 1000Base-KX SerDes transmitter DC specification at TP1 per IEEE Std 802.3ap-2007. Transmitter DC characteristics are measured at the transmitter outputs (SD1_TXn_P and SD1_TXn_N).

Table 88. 1000Base-KX Transmitter DC Specifications

Parameter	Symbols	Min	Typ	Max	Units	Notes
Output differential voltage	$V_{TX-DIFFp-p}$	800	-	1600	mV	1
Differential resistance	T_{RD}	80	100	120	ohm	-
Notes: 1. SRDSxLNmTECR0[AMP_RED]=00_0000. 2. For recommended operating conditions, see Table 3.						

3.19.8.1.2 1000Base-KX Receiver DC Specifications

Table below provides the 1000Base-KX receiver DC timing specifications.

Table 89. 1000Base-KX Receiver DC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Input differential voltage	$V_{RX-DIFFp-p}$	-	-	1600	mV	1
Differential resistance	T_{RDIN}	80	-	120	ohm	-
Notes: 1. For recommended operating conditions, see Table 3.						

3.19.8.2 1000Base-KX AC electrical characteristics

3.19.8.2.1 1000Base-KX Transmitter AC Specifications

Table below provides the 1000Base-KX transmitter AC specification.

Table 90. 1000Base-KX Transmitter AC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Baud Rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-

Table continues on the next page...

Table 90. 1000Base-KX Transmitter AC Specifications (continued)

Parameter	Symbols	Min	Typical	Max	Units	Notes
Uncorrelated High Probability Jitter/ Random Jitter	$T_{UHPJ}T_{RJ}$	-	-	0.15	UI p-p	-
Deterministic Jitter	T_{DJ}	-	-	0.10	UI p-p	-
Total Jitter	T_{TJ}	-	-	0.25	UI p-p	1
Notes: 1. Total jitter is specified at a BER of 10^{-12}. 2. For recommended operating conditions, see Table 3.						

3.19.8.2.2 1000Base-KX Receiver AC Specifications

Table below provides the 1000Base-KX receiver AC specification with parameters guided by IEEE Std 802.3ap-2007.

Table 91. 1000Base-KX Receiver AC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Receiver Baud Rate	R_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Random Jitter	R_{RJ}	-	-	0.15	UI p-p	1
Sinusoidal Jitter, maximum	$R_{SJ\text{-}max}$	-	-	0.10	UI p-p	2
Total Jitter	R_{TJ}	-	-	See Note 3	UI p-p	2
Notes: 1. Random jitter is specified at a BER of 10^{-12}. 2. The receiver interference tolerance level of this parameter shall be measured as described in Annex 69A of the IEEE Std 802.3ap-2007. 3. Per IEEE 802.3ap-clause 70. 4. The AC specifications do not include Refclk jitter. 5. For recommended operating conditions, see Table 3.						

4 Hardware design considerations

4.1 System clocking

This section describes the PLL configuration of the chip.

4.1.1 PLL characteristics

Characteristics of the chip's PLLs include the following:

- There are two selectable core cluster PLLs which generate a clock for each core cluster from the externally supplied SYSCLK input.
  - Core cluster 1 (cores 0-3) can select from cluster group A PLL 1 or 2 (CGA1 or 2 PLL).
  - The frequency ratio between each of the core cluster PLLs and SYSCLK is selected using the configuration bits. The frequency for each core cluster is selected using the configuration bits.
- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits.
- Cluster group A generates an asynchronous clock for eSDHC SDR mode from cluster group A PLL1 or cluster group A PLL 2.
- Cluster group A generates an asynchronous clock for FMan from the platform PLL, cluster group A PLL1 or cluster group A PLL 2.
- The DDR block PLL generates an asynchronous DDR clock from the externally supplied DDRCLK input. The frequency ratio is selected using the Memory Controller Complex PLL multiplier/ratio configuration bits.
- The one SerDes block has 2 PLLs which generate a core clock from their respective externally supplied SD1_REF_CLKn_P/SD1_REF_CLKn_N inputs. The frequency ratio is selected using the SerDes PLL RCW configuration bits as described in SerDes PLL ratio.

4.1.2 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and integrated flash controller.

Table 92. Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency				Unit	Notes
	1533 MHz		1800 MHz			
	Min	Max	Min	Max		
Core cluster group PLL frequency	1000	1533	1000	1800	MHz	1, 2
Core cluster frequency	250	1533	250	1800	MHz	2
Platform clock frequency	400	600	400	600	MHz	1, 7
Memory bus clock frequency	533	933	533	1066	MHz	1, 3, 4

Table continues on the next page...

Table 92. Processor, platform, and memory clocking specifications (continued)

Characteristic	Maximum processor core frequency				Unit	Notes
	1533 MHz		1800 MHz			
	Min	Max	Min	Max		
IFC clock frequency	—	100	—	100	MHz	5
FMan	see note 6	700	see note 6	700	MHz	6

Notes:

1. **Caution:**The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.

2. The core cluster can run at cluster group PLL/1, PLL/2, or PLL/4. For the PLL/1 case, the minimum frequency is 1000 MHz. With a minimum cluster group PLL frequency of 1000 MHz, this results in a minimum allowable core cluster frequency of 250 MHz for PLL/4.

3. The memory bus clock speed is half the DDR3/DDR3L data rate. DDR3/3L memory bus clock frequency is limited to min = 533 MHz.

4. The memory bus clock speed is dictated by its own PLL.

5. The integrated flash controller (IFC) clock speed on IFC_CLK[0:1] is determined by half of the platform clock divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information.

6. The FMan minimum frequency is 132 MHz for SGMII (1.25G), 330 MHz for SGMII (2.5G), and 330 MHz for XFI.

7. The minimum platform frequency should meet the requirements in Minimum platform frequency requirements for high-speed interfaces.

4.1.2.1 DDR clock ranges

The DDR memory controller can run only in asynchronous mode, where the memory bus is clocked with the clock provided on the DDRCLK input pin, which has its own dedicated PLL.

This table provides the clocking specifications for the memory bus.

Table 93. Memory bus clocking specifications

Characteristic	Min	Max	Unit	Notes
Memory bus clock frequency	533	1066	MHz	1, 2, 3

Notes:

1. **Caution:** The platform clock to SYSCLK ratio and core to platform clock ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform frequency do not exceed their respective maximum or minimum operating frequencies.

2. The memory bus clock refers to the chip's memory controllers' Dn_MCK[0:3] and Dn_MCK[0:3]_B output clocks, running at half of the DDR data rate.

3. The memory bus clock speed is dictated by its own PLL.

4.1.3 SerDes PLL ratio

The clock ratio between each of the two SerDes PLLs and their respective externally supplied SD1_REF_CLKn_P/SD1_REF_CLK*n*_N inputs is determined by a set of RCW Configuration fields-SRDS_PRTCL_Sn, SRDS_PLL_REF_CLK_SEL_Sn, and SRDS_DIV_*_Sn-as shown in this table.

Table 94. Valid SerDes RCW encodings and reference clocks

SerDes protocol (given lane)	Valid reference clock frequency	Legal setting for SRDS_PRTCL_Sn	Legal setting for SRDS_PLL_REF_CLK_SEL_Sn	Legal setting for SRDS_DIV_*_Sn	Notes
High-speed serial and debug interfaces					
PCI Express 2.5 GT/s (doesn't negotiate upwards)	100 MHz	Any PCIe	0b0: 100 MHz	2b10: 2.5 G	1
	125 MHz		0b1: 125 MHz		1
PCI Express 5 GT/s (can negotiate up to 5 GT/s)	100 MHz	Any PCIe	0b0: 100 MHz	2b01: 5.0 G	1
	125 MHz		0b1: 125 MHz		1
PCI Express 8 GT/s (can negotiate up to 8 GT/s)	100 MHz	Any PCIe	0b0: 100 MHz	2b00: 8.0 G	1
	125 MHz		0b1: 125 MHz		1
Networking interfaces					
SGMII (1.25 GBaud)	100 MHz	SGMII @ 1.25 GBaud	0b0: 100 MHz	Don't care	-
	125 MHz	1000Base-KX @ 1.25 GBaud	0b1: 125 MHz		-
2.5x SGMII (3.125 GBaud)	125 MHz	SGMII @ 3.125 GBaud	0b0: 125 MHz	Don't care	-
	156.25 MHz		0b1: 156.25 MHz		-
XFI (10.3125 GBaud)	156.25 MHz	XFI @ 10.3125 GBaud	0b0: 156.25 MHz	Don't care	-
10GBase-KR (10.3125GBaud)	156.25 MHz	10GBase-KR @ 10.3125 GBaud	0b0: 156.25 MHz	Don't care	-

Notes:

1. A spread-spectrum reference clock is permitted for PCI Express. However, if any other high-speed interfaces such as sRIO, SATA, or debug is used concurrently on the same SerDes bank, spread-spectrum clocking is not permitted.

4.1.4 Frequency options

This section discusses interface frequency options.

4.1.4.1 SYSCLK and platform frequency options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 95. SYSCLK and platform frequency options

Platform: SYSCLK ratio	SYSCLK (MHz)		
	66.67	100.00	133.33
	Platform frequency (MHz)[1]		
3:1			400
4:1		400	533
5:1		500	
6:1	400	600	
7:1	466		
8:1	533		
9:1	600		
Notes:			
1. Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed).			

4.1.4.2 Minimum platform frequency requirements for high-speed interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to:

$$\frac{527\text{ MHz x (PCI Express link width)}}{16}$$

Figure 47. Gen 1 PEX minimum platform frequency

$$\frac{527\text{ MHz x (PCI Express link width)}}{8}$$

Figure 48. Gen 2 PEX minimum platform frequency

$$\frac{527\text{ MHz x (PCI Express link width)}}{4}$$

Figure 49. Gen 3 PEX minimum platform frequency

See section "Link Width," in the chip reference manual for PCI Express interface width details. Note that "PCI Express link width" in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection. It refers to the widest port in use, not the combined width of the number ports in use. For instance, if two x4 PCIe Gen3 ports are in use, 527 MHz platform frequency is needed to support by using Gen 3 equation (527 x 4 / 4, not 527 x 4 x 2 / 4).

For proper serial RapidIO operation, the platform clock frequency must be greater than or equal to 525MHz.

4.2 Power supply design

4.2.1 Voltage ID (VID) controllable supply

To guarantee performance and power specifications, a specific method of selecting the optimum voltage-level must be implemented when the chip is used. As part of the chip's boot process, software must read the VID efuse values stored in the Fuse Status register (FUSESR) and then configure the external voltage regulator based on this information. This method requires a point of load voltage regulator for each chip. The V_{DD} supply should be separated from the Serdes 1.0V supply $S1V_{DD}$. It is required in order to control the V_{DD} supply only.

NOTE

During the power-on reset process, the fuse values are read and stored in the FUSESR. It is expected that the chip's boot code reads the FUSESR value very early in the boot sequence and updates the regulator accordingly.

The default voltage regulator setting that is safe for the system to boot is the recommended operating V_{DD} at initial start-up of 1.025V. It is highly recommended to select a regulator with a Vout range of at least 0.9V to 1.1V, with a resolution of 12.5mV or better, when implementing a VID solution.

The table below lists the valid VID efuse values that will be programmed at the factory for this chip.

Table 96. Fuse Status Register (DCFG_CCSR_FUSESR)

Binary value of DA_V / DA_ALT_V	V_{DD} voltage
00000	1.0250 V
00001	0.9875 V
00010	0.9750 V
10000	1.0000 V
10001	1.0125 V
10010	1.0250 V

For additional information on VID, please refer to the chip reference manual.

4.2.1.1 Options for system design

There are several widely-accepted options available to the system designer for obtaining the benefits of a VID solution. The most common option is to use the VID solution to drive a system's controllable voltage-regulators through a sideband interface such as a simple parallel bus or PMBus interface. PMbus is similar to I^2C but with extensions to improve robustness and address shortcomings of I^2C; the PMBus specification can be found at www.pmbus.org. The simple parallel bus is supported by the chip through GPIO pins and the PMBus interface is supported by an I^2C interface. Other VID solutions may be to access an FPGA/ASIC or separate power management chip through the IFC, SPI, or other chip-specific interface, where the other device then manages the voltage regulator. The method chosen for implementing the chip-specific voltage in the system is decided by the user.

4.2.1.1.1 Example 1: Regulators supporting parallel bus configuration

In this example, a user builds a VID solution using controllable regulators with a parallel bus. In this implementation, the user chooses to utilize any subset of the available GPIO pins on the chip except those noted below.

NOTE

GPIO pins that are muxed on an interface used by the application for loading RCW information are not available for VID use.

It is recommended that all GPIO pins used for VID are located in the same 32-bit GPIO IP block so that all bits can be accessed with a single read or write.

The general procedure for setting the core voltage regulator to the desired operating voltage is as follows:

1. The GPIO pins are released to high-impedance at POR. Because GPIO pins default to being inputs, they do not begin automatically driving after POR, and only work as outputs under software control.
2. The board is responsible for a default voltage regulator setting that is "safe" for the system to boot. To achieve this, the user puts pull-up and/or pull-down resistors on the GPIO pins as needed for that specific system. For the case where the regulator's interface operates at a different voltage than OV_{DD}, the chip's GPIO module can be operated in an open drain configuration.

3. There is no direct connection between the Fuse Status Register (FUSESR) and the chip's pins. As part of the chip's boot process, software must read the efuse values stored in the FUSESR and then configure the voltage regulator based on this information. The software determines the proper value for the parallel interface and writes it to the GPIO block data (GPDAT) register. It then changes the GPIO direction (GPDIR) register from input to output to drive the new value on the device pins, thus overriding the board configuration default value. Note that some regulators may require a series of writes so that the voltage is slowly stepped from its old to its new value.
4. When the voltage has stabilized, software adjusts the operating frequencies as desired.

Upon completion of configuration, some regulators may have a write-protect pin to prevent undesired data changes after configuration is complete. A single GPIO pin on the chip could be allocated for this task if desired.

4.2.1.1.2 Example 2: Regulators supporting PMBus configuration

In this example, a user builds a VID solution using controllable regulators with a PMBus interface. For the case where the regulator's interface operates at a different voltage than DV_{DD}, the chip's I^2C module can be operated in an open-drain configuration.

In this implementation, the user chooses to utilize any I^2C interface available on the chip. These regulators have a means for setting a safe, default, operating value either through strapping pins or through a default, non-volatile store.

NOTE

> If I^2C1 controller is selected, it is important that its calling address is different than the 7-bit value of 0x50h used by the pre-boot loader (PBL) for RCW and pre-boot initialization.

The general procedure for setting the core voltage regulator to the desired operating voltage is as follows:

1. The board is responsible for configuring a safe default value for the controllable regulator either through dedicated pins or its non-volatile store.
2. As part of the chip's boot process, software must read the efuse values stored in the FUSESR register and then configure the voltage regulator based on this information. The software decides on a new configuration and sends this value across the I^2C interface connected to the regulator's PMBus interface. Note that some regulators may require a series of writes so that the voltage is slowly stepped from its old to its new value.
3. When the voltage has stabilized, software adjusts the operating frequencies as desired.

Upon completion of configuration, some regulators may have a write-protect pin to prevent undesired data changes after configuration is complete. A single GPIO pin on the chip could be allocated for this task, if desired.

4.2.1.1.3 Example 3: Regulators supporting FPGA/ASIC or separate power management device configuration

In this example, a user builds a VID solution using controllable regulators that are managed by a FPGA/ASIC or a separate power-management device. In this implementation, the user chooses to utilize the IFC, eSPI or any other available chip interface to connect to the power-management device.

The general procedure for setting the core voltage regulator to the desired operating voltage is as follows:

1. The board is responsible for configuring a safe default value for the controllable regulator either through dedicated pins or its non-volatile store.
2. As part of the chip's boot process, software must read the efuse values stored in the FUSESR and then configure the voltage regulator based on this information. The software decides on a new configuration and sends this value across the IFC, eSPI, or any other interface that is used to connect to the FPGA/ASIC or separate power-management device that manages the regulator. Note that some regulators may require a series of writes so that the voltage is slowly stepped from its old to its new value.
3. When the voltage has stabilized, software adjusts the operating frequencies as desired.

Upon completion of configuration, some regulators may have a write-protect pin to prevent undesired data changes after configuration is complete. A single GPIO pin on the chip could be allocated for this task, if desired.

4.2.2 Core and platform supply voltage filtering

The V_{DD} supply is normally derived from a high current capacity linear or switching power supply which can regulate its output voltage very accurately despite changes in current demand from the chip within the regulator's relatively low bandwidth. Several bulk decoupling capacitors must be distributed around the PCB to supply transient current demand above the bandwidth of the voltage regulator.

These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

As a guideline for customers and their power regulator vendors, NXP recommends that these bulk capacitors should be chosen to maintain the positive transient power surges to less than VID + 50 mV (negative transient undershoot should comply with specification of VID - 30mV) for current steps of up to 10 A with a slew rate of 12 A/us.

These bulk decoupling capacitors will ideally supply a stable voltage for current transients into the megahertz range. Above that, see Decoupling recommendations for further decoupling recommendations.

4.2.3 PLL power supply filtering

Each of the PLLs described in System clocking is provided with power through independent power supply pins (AV_{DD}_PLAT, A_{VDD}_CGAn, A_{VDD}_CGBn and AV_{DD}_Dn and AV_{DD}_ SD1_PLLn). AV_{DD}_PLAT, A_{VDD}_CGAn, A_{VDD}_CGBn and AV_{DD}_Dn voltages must be derived directly from a 1.8 V voltage source through a low frequency filter scheme. AV_{DD}_ SD1_PLLn voltages must be derived directly from the $X1V_{DD}$ source through a low frequency filter scheme. The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 50, one for each of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced. This circuit is intended to filter noise in the PLL's resonant frequency range from a 500 kHz to 10 MHz range.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

This figure shows the PLL power supply filter circuit.

Where:

- R = 5 Ω ± 5%
- C1 = 10 μF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH
- C2 = 1.0 μF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH

NOTE

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH).

NOTE

Voltage for AV_{DD} is defined at the input of the PLL supply filter and not the pin of AV_{DD}.

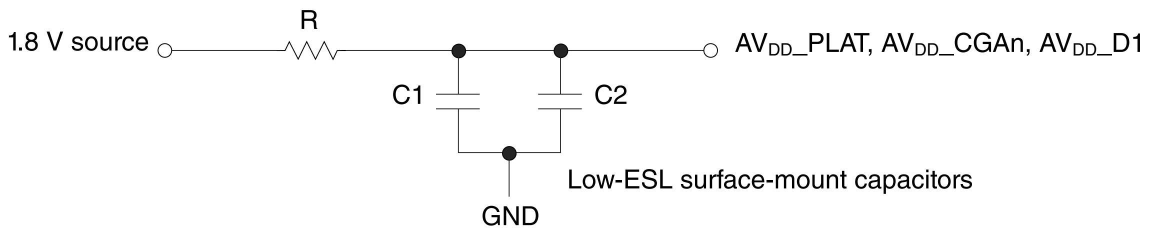


Figure 50. PLL power supply filter circuit

The AV_{DD}_ SD1_PLLn signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 51. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_ SD1_PLLn balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_ SD1_PLLn balls. The 0.003-μF capacitors closest to the balls, followed by a 4.7-μF and 47-μF capacitor, and finally the 0.33 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_ SD1_PLL*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.

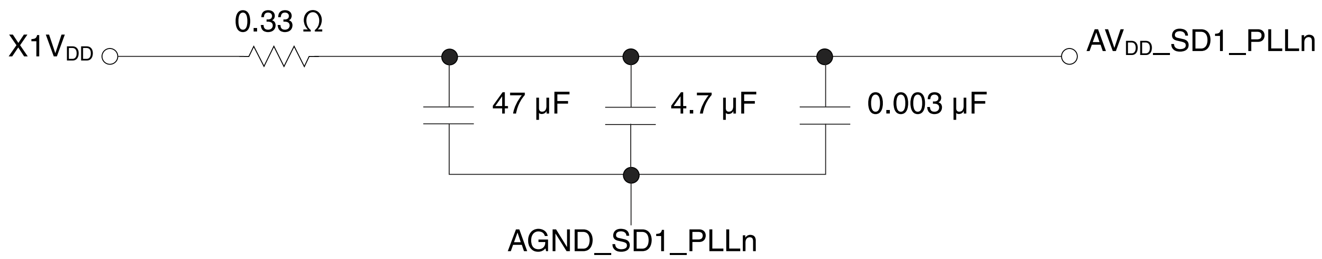


Figure 51. SerDes PLL power supply filter circuit

Note the following:

- AV_{DD}_ SD1_PLL*n* should be a filtered version of $X1V_{DD}$.
- Signals on the SerDes interface are fed from the $X1V_{DD}$ power plane.
- Voltage for AV_{DD}_ SD1_PLLn is defined at the PLL supply filter and not the pin of AV_{DD}_ SD1_PLL*n*.

- A 47-µF 0805 XR5 or XR7, 4.7-µF 0603, and 0.003-µF 0402 capacitor are recommended. The size and material type are important. A 0.33-Ω ± 1% resistor is recommended.
- There needs to be dedicated analog ground, AGND_ SD1_PLL*n* for each AV_{DD}_ SD1_PLL*n* pin up to the physical local of the filters themselves.

4.2.4 $S1V_{DD}$ power supply filtering

For initial system bring-up, the linear regulator option is highly recommended.

An example solution for $S1V_{DD}$ filtering, where $S1V_{DD}$ is sourced from a linear regulator, is illustrated in Figure 52. The component values in this example filter are system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- F1 and F2 = 120 Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

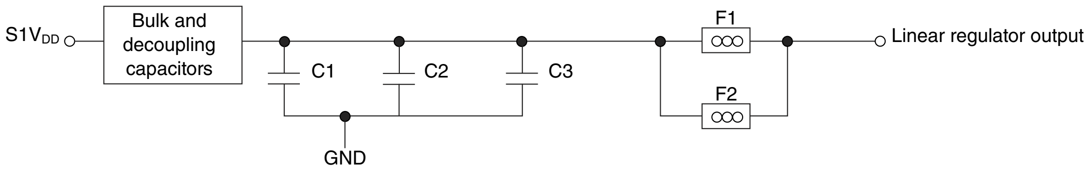


Figure 52. $S1V_{DD}$ power supply filter circuit

Note the following:

- Please refer to Power-on ramp rate, for maximum $S1V_{DD}$ power-up ramp rate.
- There needs to be enough output capacitance or a soft start feature to assure ramp rate requirement is met.
- The ferrite beads should be placed in parallel to reduce voltage droop.
- Besides a linear regulator, a low noise dedicated switching regulator can also be used. 10 mVp-p, 50kHz - 500MHz is the noise goal.

4.2.5 X1V_{DD} power supply filtering

X1V_{DD} may be supplied by a linear regulator or sourced by a filtered G1V_{DD}. Systems may design in both options to allow flexibility to address system noise dependencies. However, for initial system bring-up, the linear regulator option is highly recommended.

An example solution for X1V_{DD} filtering, where X1V_{DD} is sourced from a linear regulator, is illustrated in Figure 53. The component values in this example filter are system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- F1 and F2 = 120 Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

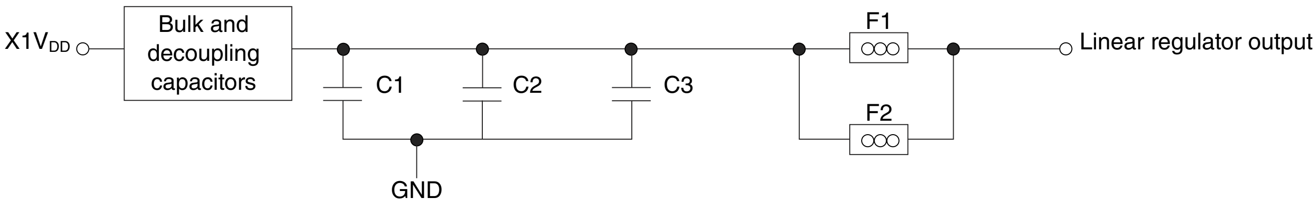


Figure 53. X1V_{DD} power supply filter circuit

Note the following:

- See Power-on ramp rate for maximum X1V_{DD} power-up ramp rate.
- There needs to be enough output capacitance or a soft-start feature to assure ramp rate requirement is met.
- The ferrite beads should be placed in parallel to reduce voltage droop.
- Besides a linear regulator, a low-noise, dedicated switching regulator can be used. 10 mVp-p, 50 kHz - 500 MHz is the noise goal.

4.2.6 USB_HV_{DD} and USB_OV_{DD} power supply filtering

USB_HV_{DD} and USB_OV_{DD} must be sourced by a filtered 3.3 V and 1.8 V voltage source using a star connection. An example solution for USB_HV_{DD} and USB_OV_{DD} filtering, where USB_HV_{DD} and USB_OV_{DD} are sourced from a 3.3 V and 1.8 V voltage source, is illustrated in the following figure. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- F1 = 120 Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

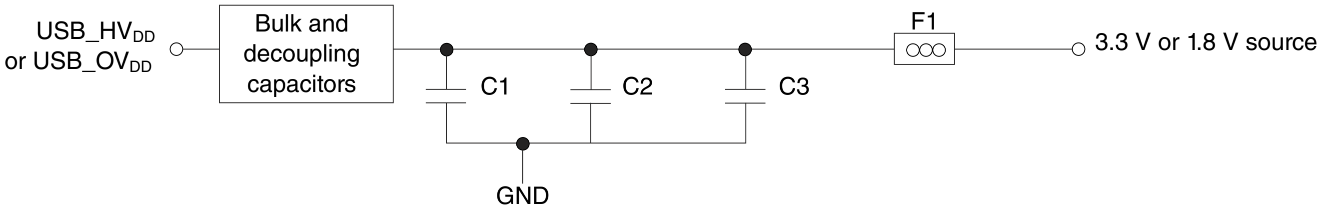


Figure 54. USB_HV$_{DD}$ and USB_OV$_{DD}$ power supply filter circuit

4.2.7 USB_SV$_{DD}$ power supply filtering

USB_SV$_{DD}$ must be sourced by a filtered V$_{DD}$ using a star connection. An example solution for USB_SV$_{DD}$ filtering, where USB_SV$_{DD}$ is sourced from V$_{DD}$, is illustrated in the following figure. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 2.2 µF ± 20%, X5R, with Low ESL (for example, Panasonic ECJ0EB0J225M)
- F1 = 120 Ω at 100-MHz 2A 25% Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

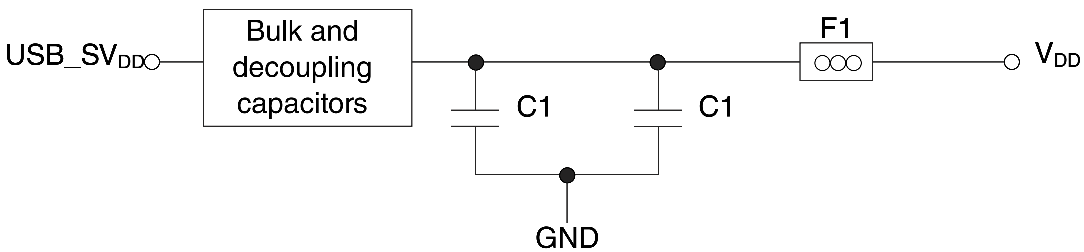


Figure 55. USB_SV$_{DD}$ power supply filter circuit

4.3 Decoupling recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, DV_{DD}, $G1V_{DD}$, and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, DV_{DD}, $G1V_{DD}$, LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

As presented in Core and platform supply voltage filtering, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and other planes (for example, OV_{DD}, DV_{DD}, $G1V_{DD}$, and LV_{DD}), to enable quick recharging of the smaller chip capacitors.

4.4 SerDes block power supply decoupling recommendations

The SerDes block requires a clean, tightly regulated source of power ($S1V_{DD}$ and $X1V_{DD}$) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

NOTE

Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

1. The board should have at least 1 x 0.1-uF SMT ceramic chip capacitor placed as close as possible to each supply ball of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
2. Between the device and any SerDes voltage regulator there should be a lower bulk capacitor for example a 10-uF, low ESR SMT tantalum or ceramic and a higher bulk

capacitor for example a 100uF - 300-uF low ESR SMT tantalum or ceramic capacitor.

4.5 Connection recommendations

The following is a list of connection recommendations:

- To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted in this document, all unused active low inputs should be tied to V_{DD}, OV_{DD}, DV_{DD}, $G1V_{DD}$, and LV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD}, OV_{DD}, DV_{DD}, $G1V_{DD}$, LV_{DD} and GND pins of the device.
- The TEST_SEL_B pin must be pulled high.
- The chip has temperature diodes on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as on Semiconductor, NCT72). Even if a temperature diode monitoring device is not utilized on production systems, being able to access these pins for debug or problem analysis can be valuable. Therefore, it is suggested to connect these pins to test points connected to ground through low value resistors, which can be removed if a temperature monitoring device is ever to be connected. The chip temperature diode specifications are as follows:
  - Operating range: 10 - 230 μA
  - Ideality factor over 13.5 - 220 μA: Temperature range 25°C - 105°C n = 1.006833 ± 0.008

4.5.1 Legacy JTAG configuration signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 57. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST_B signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST_B to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST_B during the power-on reset flow. Simply tying TRST_B to PORESET_B is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert PORESET_B or TRST_B in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 57 allows the COP port to independently assert PORESET_B or TRST_B, while ensuring that the target can drive PORESET_B as well.

The COP interface has a standard header, shown in Figure 56, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 56 is common to all known emulators.

4.5.1.1 Termination of unused signals

If the JTAG interface and COP header will not be used, NXP recommends the following connections:

- TRST_B should be tied to PORESET_B through a 0 kΩ isolation resistor so that it is asserted when the system reset signal (PORESET_B) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. NXP recommends that the COP header be designed into the system as shown in Figure 57. If this is not possible, the isolation resistor will allow future access to TRST_B in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS or TDO.

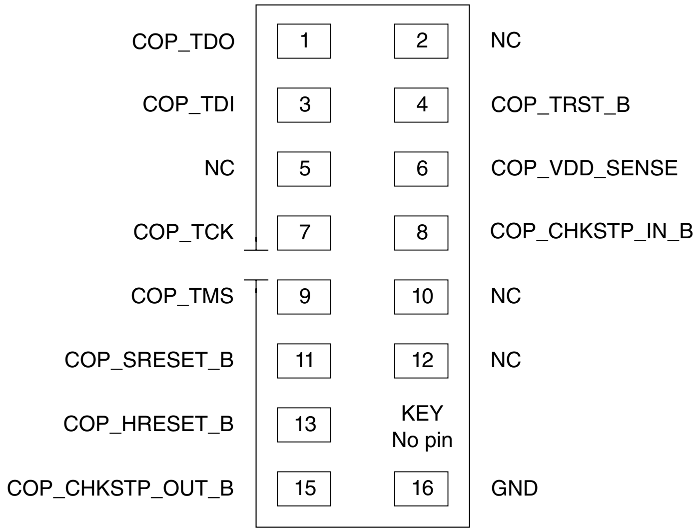
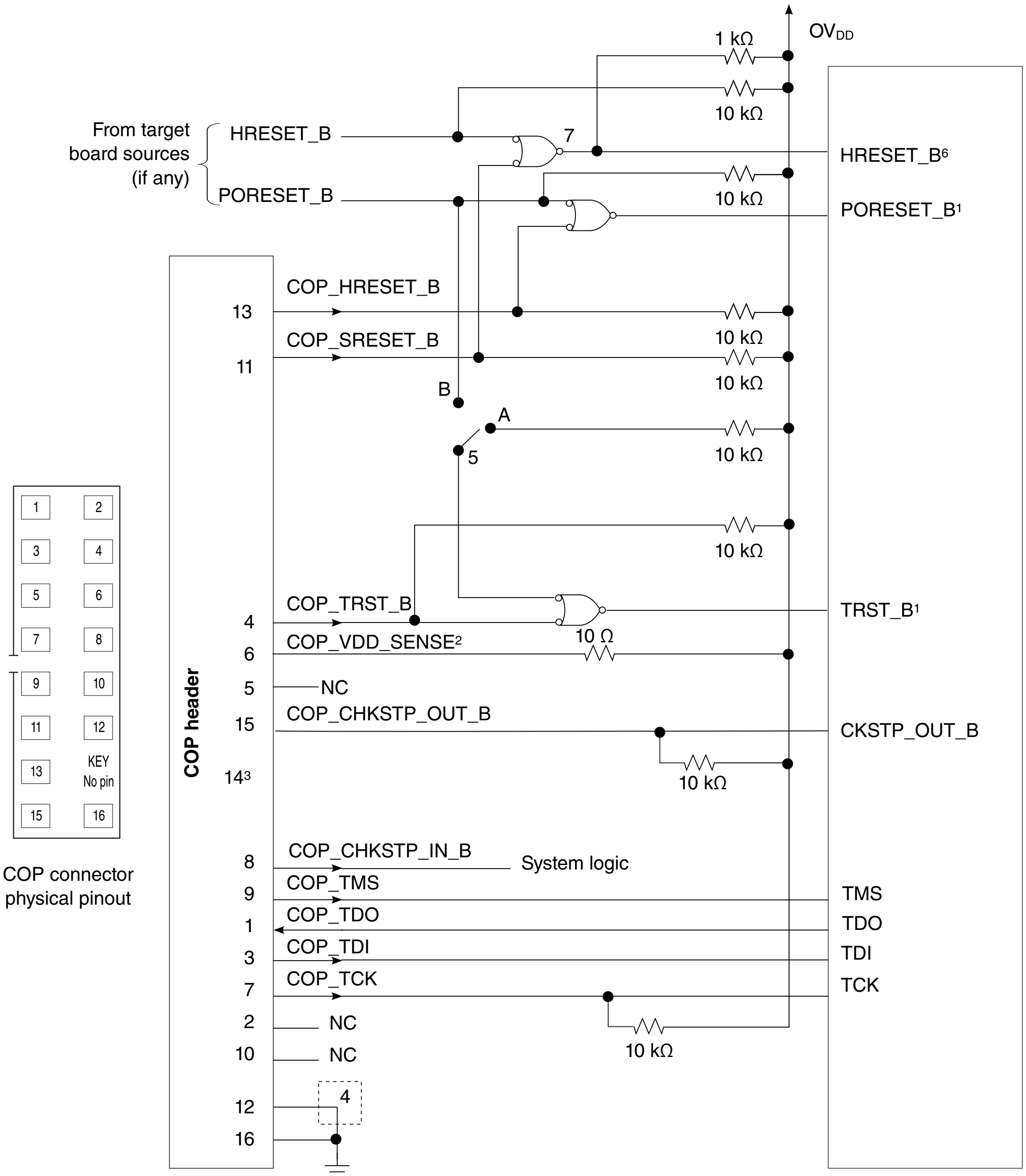


Figure 56. Legacy COP connector physical pinout



Notes:

1. The COP port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a no-connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting HRESET_B causes a hard reset on the device
7. This is an open-drain output gate.

Figure 57. Legacy JTAG interface connection

4.5.2 Guidelines for high-speed interface termination

4.5.2.1 SerDes interface entirely unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section.

Note that $S1V_{DD}$, $X1V_{DD}$ and AVDD_SD1_PLL1 must remain powered.

For AVDD_SD1_PLL*n*, it must be connected to $X1V_{DD}$ through a zero ohm resistor (instead of filter circuit shown in Figure 51).

The following pins must be left unconnected:

- SD1_TX[7:0]_P
- SD1_TX[7:0]_N

The following pins must be connected to SnGND:

- SD1_RX[7:0]_P
- SD1_RX[7:0]_N
- SD1_REF_CLK1_P, SD1_REF_CLK2_P
- SD1_REF_CLK1_N, SD1_REF_CLK2_N

The following pins must be left unconnected:

- SD1_IMP_CAL_RX
- SD1_IMP_CAL_TX

It is possible to independently disable each SerDes module by disabling all PLLs associated with it.

SerDes *n* = 1:2 is disabled as follows:

- SRDS_PLL_PD_S*n* = 2’b11 (both PLLs configured as powered down)
- SRDS_PLL_REF_CLK_SEL_S*n* = 2’b00
- SRDS_PRTCL_S*n* = 2 (no other values permitted when both PLLs are powered down

4.5.2.2 SerDes interface partly unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

Note that both $S1V_{DD}$ and $X1V_{DD}$ must remain powered.

If any of the PLLs are un-used, the corresponding AVDD_SD1_PLL*n* must be connected to $X1V_{DD}$ through a zero ohm resistor (instead of filter circuit shown in Figure 51).

The following unused pins must be left unconnected:

- SD1_TX[*n*]_P
- SD1_TX[*n*]_N

The following unused pins must be connected to SnGND:

- SD1_RX[*n*]_P
- SD1_RX[*n*]_N
- SD1_REF_CLK[1:2]_P, SD1_REF_CLK[1:2]_N (If entire SerDes 1 unused)

In the RCW configuration field SRDS_PLL_PD_S*n*, the respective bits for each unused PLL must be set to power it down. A module is disabled when both its PLLs are turned off.

After POR, if an entire SerDes module is unused, it must be powered down by clearing the SDEN fields of its corresponding PLL1 and PLL2 reset control registers (SRDS*x*PLL*n*RSTCTL).

Unused lanes must be powered down by clearing the RRST and TRST fields and setting the RX_PD and TX_PD fields in the corresponding lane's general control register (SRDS*x*LN*m*GCR0).

4.5.3 USB controller connections

This section details the hardware connections required for the USB controllers.

4.5.3.1 USB divider network

This figure shows the required divider network for the VBUS interface for the chip. Additional requirements for the external components are:

- Both resistors require 1% accuracy and a current capability of up to 1 mA. They must both have the same temperature coefficient and accuracy.
- The zener diode must have a value of 5 V–5.25 V.
- The 0.6 V diode requires an I_F = 10 mA, I_R < 500 nA and $V_{F(Max)}$ = 0.8 V. If the USB PHY does not support OTG mode, this diode can be removed from the schematic or made a DNP component.

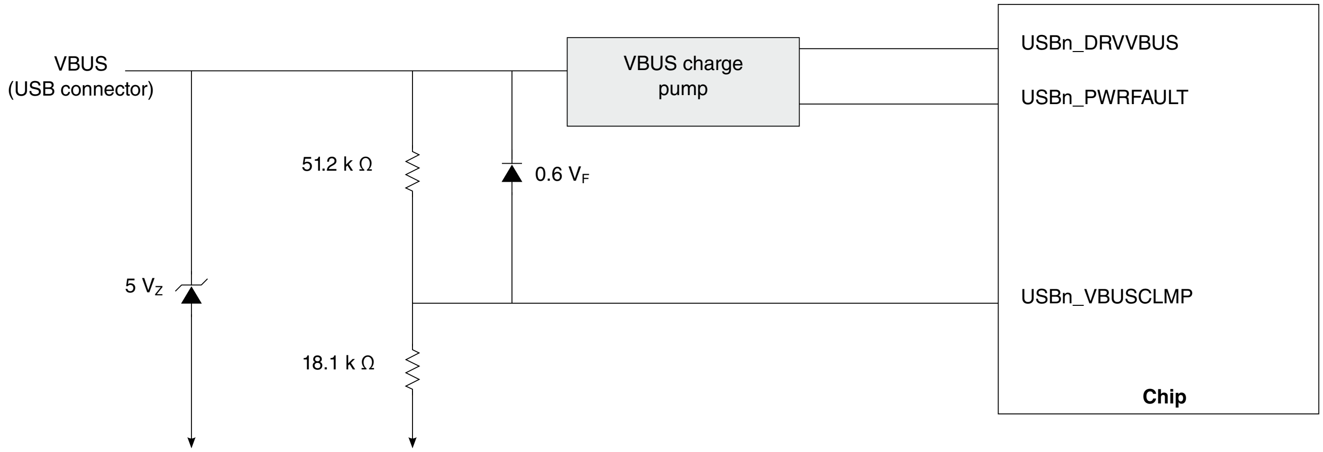


Figure 58. Divider network at VBUS

4.6 Thermal

This table shows the thermal characteristics for the chip. Note that these numbers are based on design estimates and are preliminary.

Table 97. Package thermal characteristics[1] (Rev 1.1)

Rating	Board	Symbol	Value	Unit	Notes
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	22	°C/W	2, 3
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	14	°C/W	2, 4
Junction to ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	15	°C/W	2, 3
Junction to ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	10	°C/W	2, 3
Junction to board	—	$R_{\Theta JB}$	4	°C/W	4
Junction to case top	—	$R_{\Theta JCTOP}$	0.7	°C/W	5
Junction to lid top	—	$R_{\Theta JCLID}$	0.35	°C/W	6

Notes:

1. See Thermal management information for additional details.

2. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3. Per JEDEC JESD51-3 and JESD51-6 with the board (JESD51-9) horizontal.

4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5. Junction-to-case-top at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

6. Junction-to-lid-top thermal resistance determined using the MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.

4.7 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

4.8 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 59. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 15 pounds force (67 Newton).

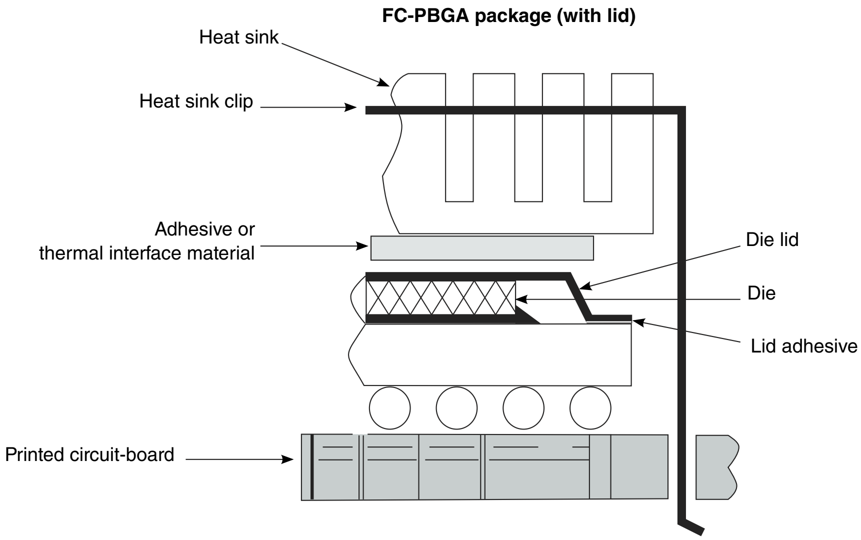


Figure 59. Package exploded, cross-sectional view-FC-PBGA (with lid) - Rev 1.1

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

For additional information regarding thermal management of lid-less flip-chip packages, refer to application note AN4871 "Assembly Handling and Thermal Solutions for Lidless Flip Chip Ball Grid Array Packages".

4.8.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

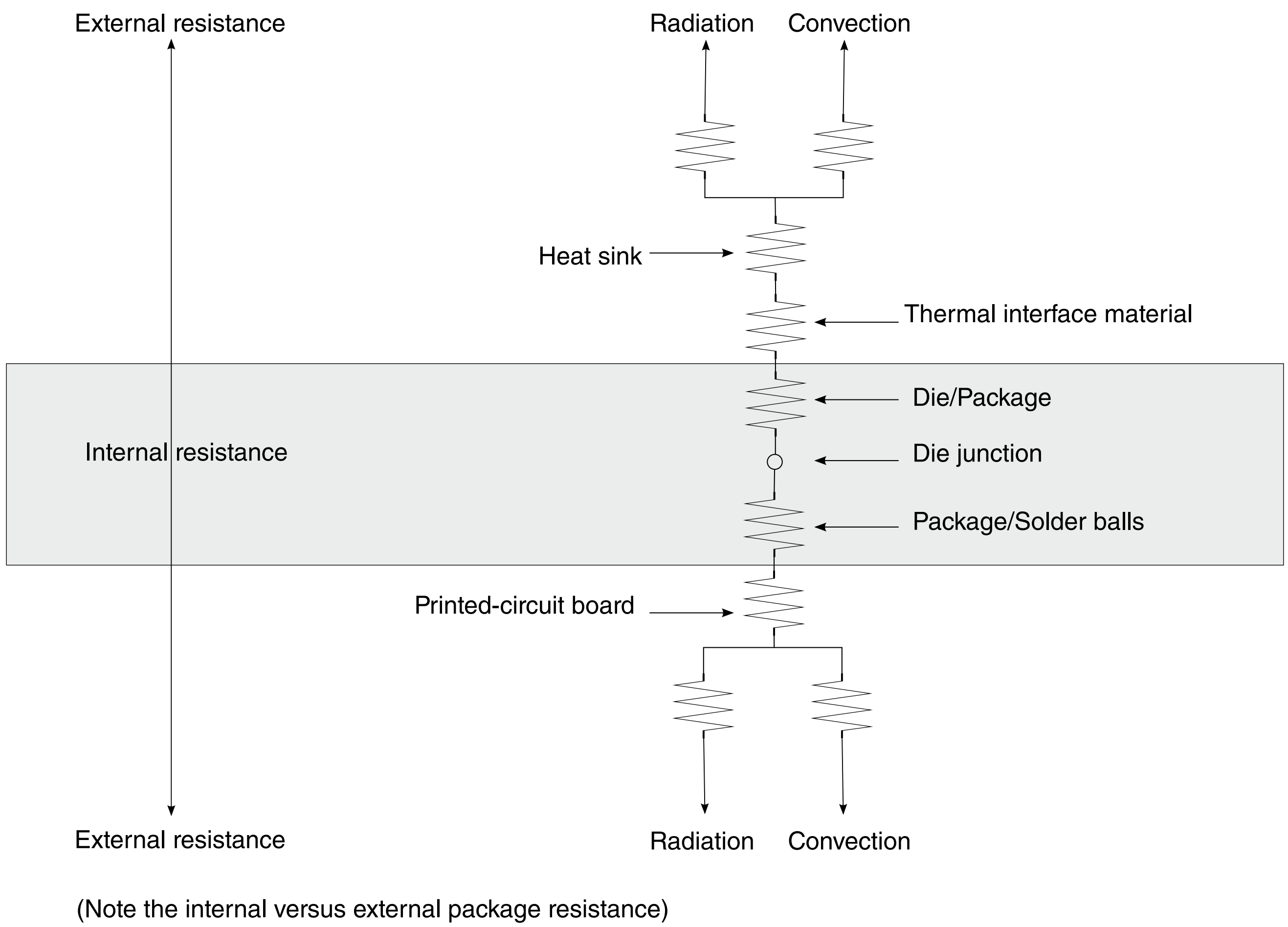


Figure 60. Package with heat sink mounted to a printed-circuit board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

4.8.2 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 59).

The system board designer can choose among several types of commercially-available thermal interface materials.

5 Package information

5.1 Package parameters for the FC-PBGA

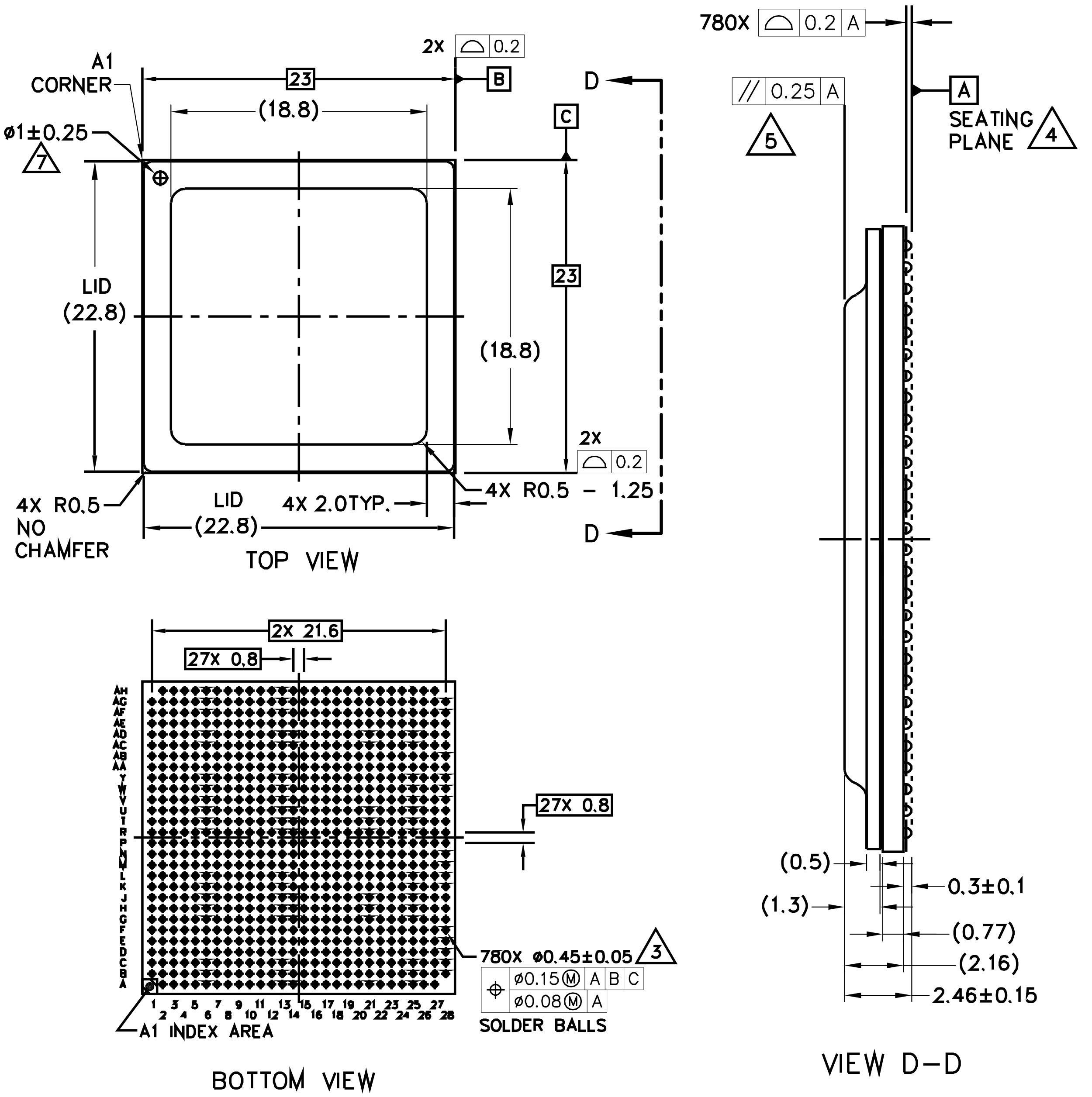
The package parameters are as provided in the following list. The package type is 23 mm x 23 mm, 780 flip-chip, plastic-ball, grid array (FC-PBGA).

Rev 1.1:

- Package outline - 23 mm x 23 mm
- Interconnects - 780
- Ball pitch - 0.8 mm
- Ball diameter (typical) - 0.45 mm
- Solder balls - 96.5% Sn, 3% Ag, 0.5% Cu
- Module height - 2.31 mm (minimum), 2.46 mm (typical), 2.61 (maximum)

5.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip for Rev 1.1 silicon.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: FCPBGA, WITH LID, 23 X 23 X 2.46 PKG, 0.8 MM PITCH, 780 I/O	DOCUMENT NO: 98ASA00854D	REV: 0
	STANDARD: NON-JEDEC	
	03 DEC 2014	

Figure 61. Mechanical dimensions of the FC-PBGA, with lid

NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

6 Security fuse processor

This chip implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.80 V to the PROG_SFP pin per Power sequencing. PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of eight fuse programming cycles. All other times PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering PROG_SFP are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

NOTE

Users not implementing the QorIQ platform's Trust Architecture features should connect PROG_SFP to GND.

7 Ordering information

Contact your local NXP sales office or regional marketing team for order information.

7.1 Part numbering nomenclature

This table provides the NXP QorIQ platform part numbering nomenclature.

Table 98. Part numbering nomenclature

pt or t	n	nn	n	x	t	e	n	c	d	r
Generation	Platform	Number of virtual cores	Derivative	Qual status	Temperature range	Encryption	Package type	CPU speed	DDR data rate	Die revision
PT = 28nm (PT=Prototype) (T=Production)	2	08 = 8 virtual cores	0-9	P = Prototype N = Qualified to industrial tier	S = Standard temp X = Extended temp	E = SEC present N = SEC not present	7 = FC-PBGA C4 and sphere Pb-free (lidless) 8 = FC-PBGA C4 and sphere Pb-free (with lid)	M = 1200 MHz P = 1533 MHz T = 1800 MHz	Q(L) = 1600 MT/s T = 1866 MT/s 1 = 2133 MT/s	A = Rev 1.0 B = Rev 1.1

7.2 Orderable part numbers addressed by this document

This table provides the NXP orderable part numbers addressed by this document for the chip.

Table 99. Orderable part numbers addressed by this document

Part number	pt or t	n	nn	n	x	t	e	n	c	d	r
T2081NSE8MQB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	S = Std temp	E = SEC present	8	M = 1200 MHz	Q = 1600 MT/s	B = Rev 1.1
T2081NSN8MQB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	S = Std temp	N = SEC not present	8	M = 1200 MHz	Q = 1600 MT/s	B = Rev 1.1
T2081NXE8MQB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	X = Ext temp	E = SEC present	8	M = 1200 MHz	Q = 1600 MT/s	B = Rev 1.1
T2081NXN8MQB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	X = Ext temp	N = SEC not present	8	M = 1200 MHz	Q = 1600 MT/s	B = Rev 1.1

Table continues on the next page...

Table 99. Orderable part numbers addressed by this document (continued)

Part number	*pt or t*	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
T2081NSE8PTB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	S = Std temp	E = SEC present	8	P = 1533 MHz	T = 1866 MT/s	B = Rev 1.1
T2081NSN8PTB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	S = Std temp	N = SEC not present	8	P = 1533 MHz	T = 1866 MT/s	B = Rev 1.1
T2081NXE8PTB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	X = Ext temp	E = SEC present	8	P = 1533 MHz	T = 1866 MT/s	B = Rev 1.1
T2081NXN8PTB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	X = Ext temp	N = SEC not present	8	P = 1533 MHz	T = 1866 MT/s	B = Rev 1.1
T2081NSE8TTB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	S = Std temp	E = SEC present	8	T = 1800 MHz	T = 1866 MT/s	B = Rev 1.1
T2081NSN8TTB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	S = Std temp	N = SEC not present	8	T = 1800 MHz	T = 1866 MT/s	B = Rev 1.1
T2081NXE8TTB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	X = Ext temp	E = SEC present	8	T = 1800 MHz	T = 1866 MT/s	B = Rev 1.1
T2081NXN8TTB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	X = Ext temp	N = SEC not present	8	T = 1800 MHz	T = 1866 MT/s	B = Rev 1.1
T2081NSE8T1B	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	S = Std temp	E = SEC present	8	T = 1800 MHz	1 = 2133 MT/s	B = Rev 1.1
T2081NSN8T1B	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	S = Std temp	N = SEC not present	8	T = 1800 MHz	1 = 2133 MT/s	B = Rev 1.1
T2081NXE8T1B	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	X = Ext temp	E = SEC present	8	T = 1800 MHz	1 = 2133 MT/s	B = Rev 1.1
T2081NXN8T1B	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	X = Ext temp	N = SEC not present	8	T = 1800 MHz	1 = 2133 MT/s	B = Rev 1.1
T2081NSE8MQLB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	S = Std temp	E = SEC present	8	M = 1200 MHz	QL = 1600 MT/s	B = Rev 1.1
T2081NSN8MQLB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	S = Std temp	N = SEC not present	8	M = 1200 MHz	QL = 1600 MT/s	B = Rev 1.1
T2081NXE8MQLB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	X = Ext temp	E = SEC present	8	M = 1200 MHz	QL = 1600 MT/s	B = Rev 1.1
T2081NXN8MQLB	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	X = Ext temp	N = SEC not present	8	M = 1200 MHz	QL = 1600 MT/s	B = Rev 1.1

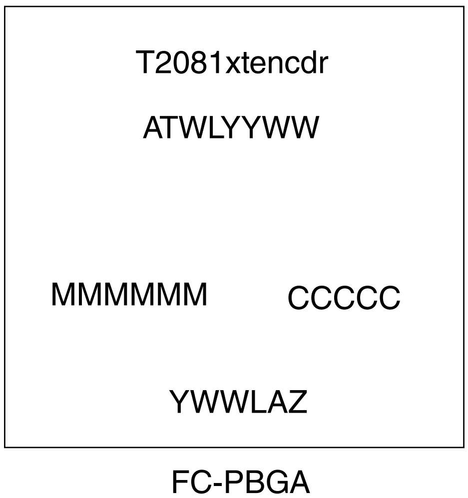
Table continues on the next page...

Table 99. Orderable part numbers addressed by this document (continued)

Part number	*pt or t*	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
T2081NSE8P1B	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	S = Std temp	E = SEC present	8	P = 1533 MHz	1 = 2133 MT/s	B = Rev 1.1
T2081NSN8P1B	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	S = Std temp	N = SEC not present	8	P = 1533 MHz	1 = 2133 MT/s	B = Rev 1.1
T2081NXE8P1B	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	X = Ext temp	E = SEC present	8	P = 1533 MHz	1 = 2133 MT/s	B = Rev 1.1
T2081NXN8P1B	T = 28nm	2	08 = 8 virtual cores	1	N = Qualified	X = Ext temp	N = SEC not present	8	P = 1533 MHz	1 = 2133 MT/s	B = Rev 1.1

7.2.1 Part marking

Parts are marked as in the example shown in this figure.



Legend:
T2081xtencdr is the orderable part number.
ATWLYYWW is the traceability code
MMMMMM is the mask number.
CCCCC is the country code.
YWWLAZ is the assembly traceability code.

Figure 62. Part marking for FC-PBGA chip

8 Revision history

This table summarizes revisions to this document.

Table 100. Revision history

Revision	Date	Description
3	03/2018	• Changed XVDD to SVDD in Figure 7 • Updated the row "AC Input Swing Limits at 1.8 V OVDD" in Table 13 • Updated the row "Input capacitance" in Table 15 • Removed the table "PLL lock times" from the section RESET initialization • Added Table 48 and Figure 24 • Updated the row "Input current (OVIN = 0 V or OVIN = OVDD)" in Table 51 • Updated note 5 in Table 92 • Changed "two fuse programming cycles" to "eight fuse programming cycles" in Security fuse processor

2	07/2016	• Updated the document title to conform with new document naming requirements.
		• In the pin list table:
		  • Revealed alternate pin SDHC_CLK_SYNC_IN on primary pin IRQ[10].
		  • Revealed alternate pin SDHC_CLK_SYNC_OUT on primary pin SPI_CS_B[3].
		• In Power sequencing, added a note for the frequency requirements when using Trust Architecture Security Monitor battery-backed features and changed the stable value from 75 ms to 400 ms.
		• In Table 6 and Table 7, added the 1533 MHz and 1200 MHz low-power numbers and added footnote 9.
		• In eSPI AC timing specifications, added a note for the master mode internal clock diagram that SPICLK appears on the interface only after CS assertion.
		• In RGMII AC timing specifications, added a note to footnote 9 that MAC10 is not impacted by erratum A-005177 and meets industry specifications.
		• In Part numbering nomenclature, added CPU speed "M = 1200 MHz".
		• In Orderable part numbers addressed by this document, added the following part numbers:
		  • T2081NSE8MQLB
		  • T2081NSN8MQLB
		  • T2081NXE8MQLB
		  • T2081NXN8MQLB
		  • T2081NSE8P1B
		  • T2081NSN8P1B
		  • T2081NXE8P1B
		  • T2081NXN8P1B

1	03/2016	• Throughout the document, removed Rev 1.0 information and the preliminary data disclaimers.
		• In Table 3, added table footnote 8.
		• Updated Table 4, "Output driver capability."
		• In Table 6 and Table 7, added the 2133 MT/s (low-power version) numbers and re-ordered the rows from largest to smallest MHz power number.
		• In Table 8 :
		  • Added rows for DDR I/O 2133 MT/s and USB_SV_{DD}.
		  • Updated the SerDes 1.35 V parameter to "4x 5 G-baud".
		• In Table 10, updated the PH10 core frequencies.
		• In Table 19, added the maximum rise/fall of PORESET_B and changed the HRESET_B max from 1 to 10.
		• In DDR3 and DDR3L SDRAM controller, added to the NOTE that DDR3L is not supported at a DDR data rate of 2133 MT/s.
		• In the tables of DDR3 and DDR3L SDRAM interface DC electrical characteristics, changed "D*n*_MV_{REF}" to "MVREF*n*".
		• In Table 20, updated the I/O leakage current min/max from -100/100 to -50/50.
		• In Table 23 and Table 24, added the 2133 MT/s data rates and added notes that only DDR3 supports 2133 MT/s.
		• In Table 32, added "10 Mbps" to note 9 as an option for RGMII if the device cannot cope with a wide skew.
		• Added Table 34, "Ethernet management interface 1 DC electrical characteristics (LV_{DD} = 1.8 V)."

Table continues on the next page...

Table 100. Revision history (continued)

Revision	Date	Description

		• In Table 37, removed "x2" from "(Frame Manager x2)" in table footnote 4.
		• In Table 39, changed the input current min and max to -50 and 50.
		• In Table 71, updated the unit interval minimum from 199.40 to 199.94.
		• Added Figure 45, "Single-frequency sinusoidal jitter limits."
		• In Table 92, updated the 1800 MHz memory bus clock frequency maximum from 933 to 1066 and, in table footnote 6, changed the XFI minimum frequency from 359 MHz to 300 MHz.
		• In Table 93, changed the maximum frequency from 933 MHz to 1066 MHz.
		• Removed the following sections:
		  • "Platform to SYSCLK PLL ratio"
		  • "Core cluster to SYSCLK PLL ratio"
		  • "Core complex PLL select"
		  • "DDR controller PLL ratios"
		  • "Frame Manager clock select"
		  • "eSDHC SDR mode clock select"
		• In Connection recommendations, changed the example from "Analog Devices, ADT7461A" to "Semiconductor, NCT72" and added the chip temperature diode specifications.
		• In Thermal management information, updated the recommended spring force maximum from 10 pounds to 15 pounds.
		• Updated Mechanical dimensions of the FC-PBGA, to include package parameters.
		• In Orderable part numbers addressed by this document, added the following part numbers:
		  • T2081NSE8T1B
		  • T2081NSN8T1B
		  • T2081NXE8T1B
		  • T2081NXN8T1B

0	01/2015	Initial release

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