

CMOS Low Voltage 4 Ω , 4-Channel Multiplexer

ADG704

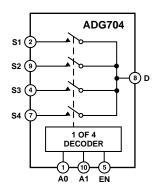
FEATURES

+1.8 V to +5.5 V Single Supply 2.5 Ω (Typ) On Resistance Low On-Resistance Flatness -3 dB Bandwidth >200 MHz Rail-to-Rail Operation 10-Lead μ SOIC Package Fast Switching Times t_{ON} 20 ns t_{OFE} 13 ns

 t_{OFF} 13 ns Typical Power Consumption (<0.01 $\mu\text{W})$ TTL/CMOS Compatible

APPLICATIONS
Battery Powered Systems
Communication Systems
Sample-and-Hold Systems
Audio Signal Routing
Data Acquisition System
Video Switching

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG704 is a CMOS analog multiplexer, comprising four single channels. This multiplexer is designed on an advanced submicron process that provides low power dissipation yet gives high switching speed, low on resistance, low leakage currents and high bandwidths.

The on resistance profile is very flat over the full analog signal range. This ensures excellent linearity and low distortion when switching audio signals. Fast switching speed also makes the part suitable for video signal switching.

The ADG704 can operate from a single supply range of +1.8 V to +5.5 V, making it ideal for use in battery powered instruments and with the new generation of DACs and ADCs from Analog Devices.

The ADG704 switches one of four inputs to a common output, D, as determined by the 3-bit binary address lines, A0, A1 and EN. A Logic "0" on the EN pin disables the device.

Each switch of the ADG704 conducts equally well in both directions when ON. The ADG704 exhibits break-before-make switching action.

The ADG704 is available in 10-lead µSOIC package.

PRODUCT HIGHLIGHTS

- 1. +1.8 V to +5.5 V Single Supply Operation.
 The ADG704 offers high performance and is fully specified and guaranteed with +3 V and +5 V supply rails.
- 2. Very Low R_{ON} (4.5 Ω Max at 5 V, 8 Ω Max at 3 V). At supply voltage of +1.8 V, R_{ON} is typically 35 Ω over the temperature range.
- 3. Low On-Resistance Flatness.
- 4. -3 dB Bandwidth Greater than 200 MHz.
- Low Power Dissipation. CMOS construction ensures low power dissipation.
- 6. Fast t_{ON}/t_{OFF}.
- 7. Break-Before-Make Switching Action.
- 8. 10-Lead μSOIC Package.

REV. A

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$\label{eq:continuous} \textbf{ADG704-SPECIFICATIONS}^{1~(V_{DD}~=~+5~V~\pm~10\%,~GND~=~0~V.~All~Specifications~-40°C~to~+85°C,~unless~otherwise~noted.)}$

	B Version -40°C to				
Parameter	+25°C	+85°C	Units	Test Conditions/Comments	
ANALOG SWITCH					
Analog Signal Range		$0~V~to~V_{\mathrm{DD}}$	V		
On-Resistance (R _{ON})	2.5		Ω typ	$V_S = 0 \text{ V to } V_{DD}, I_{DS} = -10 \text{ mA};$	
	4	4.5	Ω max	Test Circuit 1	
On-Resistance Match Between					
Channels (ΔR_{ON})		0.1	Ω typ	$V_S = 0 \text{ V to } V_{DD}, I_{DS} = -10 \text{ mA}$	
		0.4	Ω max		
On-Resistance Flatness $(R_{FLAT(ON)})$	0.75		Ω typ	$V_S = 0 \text{ V to } V_{DD}, I_{DS} = -10 \text{ mA}$	
		1.2	Ω max		
LEAKAGE CURRENTS				V _{DD} = +5.5 V	
Source OFF Leakage I _S (OFF)	±0.01		nA typ	$V_S = 4.5 \text{ V/1 V}, V_D = 1 \text{ V/4.5 V};$	
20 m 20 11 20 m mg 13 (211)	±0.1	±0.3	nA max	Test Circuit 2	
Drain OFF Leakage I _D (OFF)	±0.01	_0.5	nA typ	$V_S = 4.5 \text{ V/1 V}, V_D = 1 \text{ V/4.5 V};$	
Diam off Zouringo ip (off)	±0.1	±0.3	nA max	Test Circuit 2	
Channel ON Leakage ID, IS (ON)	±0.01		nA typ	$V_S = V_D = 4.5 \text{ V or } 1 \text{ V};$	
	±0.1	±0.3	nA max	Test Circuit 3	
DIOMENT DIDITEO					
DIGITAL INPUTS		2.4			
Input High Voltage, V _{INH}		2.4	V min		
Input Low Voltage, V _{INL}		0.8	V max		
Input Current	0.005			X7 - X7 X7	
I_{INL} or I_{INH}	0.005	±0.1	μA typ	$V_{IN} = V_{INL}$ or V_{INH}	
		±0.1	μA max		
DYNAMIC CHARACTERISTICS ²					
t_{ON}	14		ns typ	$R_L = 300 \Omega, C_L = 35 pF$	
		20	ns max	$V_S = 3 V$, Test Circuit 4	
t _{OFF}	6		ns typ	$R_L = 300 \Omega, C_L = 35 pF$	
		13	ns max	$V_S = 3 V$, Test Circuit 4	
Break-Before-Make Time Delay, t _D	8		ns typ	$R_L = 300 \Omega, C_L = 35 pF$	
		1	ns min	$V_{S1} = V_{S2} = 3 \text{ V}$, Test Circuit 5	
Charge Injection	3		pC typ	$V_S = 2 V, R_S = 0 \Omega, C_L = 1 nF;$	
				Test Circuit 6	
Off Isolation	-60		dB typ	$R_L = 50 \Omega, C_L = 5 pF, f = 10 MHz$	
	-80		dB typ	$R_L = 50 \Omega, C_L = 5 pF, f = 1 MHz;$	
				Test Circuit 7	
Channel-to-Channel Crosstalk	-62		dB typ	$R_L = 50 \Omega, C_L = 5 pF, f = 10 MHz$	
	-82		dB typ	$R_L = 50 \Omega, C_L = 5 pF, f = 1 MHz;$	
D 1 111 0 1D	200			Test Circuit 8	
Bandwidth –3 dB	200		MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$; Test Circuit 9	
C_{S} (OFF)	9		pF typ		
$C_{\rm D}$ (OFF)	37		pF typ		
$C_D, C_S(ON)$	54		pF typ		
POWER REQUIREMENTS				$V_{\rm DD} = +5.5 \text{ V}$	
-				Digital Inputs = 0 V or 5 V	
$I_{ m DD}$	0.001		μA typ		
		1.0	μA max		

Specifications subject to change without notice.

NOTES ¹Temperature ranges are as follows: B Version: -40°C to +85°C.

²Guaranteed by design, not subject to production test.

$\textbf{SPECIFICATIONS}^{1} \ (\textbf{V}_{DD} = +3 \ \textbf{V} \ \pm \ 10\%, \ \textbf{GND} = 0 \ \textbf{V}. \ \textbf{All Specifications} \ -40 ^{\circ} \textbf{C} \ \text{to} \ +85 ^{\circ} \textbf{C}, \ \textbf{unless otherwise noted.})$

	B Version -40°C to			
Parameter	+25°C	+85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V _{DD}	V	
On-Resistance (R _{ON})	4.5	5	Ω typ	$V_S = 0 \text{ V to } V_{DD}, I_{DS} = -10 \text{ mA};$
COLO		8	Ω max	Test Circuit 1
On-Resistance Match Between				
Channels (ΔR_{ON})	0.1		Ω typ	$V_{S} = 0 \text{ V to } V_{DD}, I_{DS} = -10 \text{ mA}$
(—() ₁ (/)		0.4	Ω max	.3
On-Resistance Flatness (R _{FLAT(ON)})		2.5	Ω typ	$V_{S} = 0 \text{ V to } V_{DD}, I_{DS} = -10 \text{ mA}$
			17 P	
LEAKAGE CURRENTS				$V_{\rm DD} = +3.3 \text{ V}$
Source OFF Leakage I _S (OFF)	±0.01		nA typ	$V_S = 3 \text{ V/1 V}, V_D = 1 \text{ V/3 V};$
	± 0.1	±0.3	nA max	Test Circuit 2
Drain OFF Leakage I _D (OFF)	±0.01		nA typ	$V_S = 3 \text{ V/1 V}, V_D = 1 \text{ V/3 V};$
	±0.1	±0.3	nA max	Test Circuit 2
Channel ON Leakage I _D , I _S (ON)	±0.01		nA typ	$V_S = V_D = 3 \text{ V or } 1 \text{ V};$
	±0.1	±0.3	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.0	V min	
		0.4	V max	
Input Low Voltage, V _{INL}		0.4	v IIIax	
Input Current	0.005			V - V - V
I _{INL} or I _{INH}	0.005	10.1	μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		±0.1	μA max	
DYNAMIC CHARACTERISTICS ²				
t_{ON}	16		ns typ	$R_L = 300 \Omega, C_L = 35 pF$
		24	ns max	$V_S = 2 V$, Test Circuit 4
$t_{ m OFF}$	8		ns typ	$R_{L} = 300 \Omega, C_{L} = 35 pF$
		16	ns max	$V_S = 2 V$, Test Circuit 4
Break-Before-Make Time Delay, t _D	9		ns typ	$R_L = 300 \Omega, C_L = 35 pF$
Ç. B		1	ns min	$V_{S1} = V_{S2} = 2 \text{ V}$, Test Circuit 5
Charge Injection	3		pC typ	$V_S = 1.5 \text{ V}, R_S = 0 \Omega, C_L = 1 \text{ nF};$
<i>5</i> ,			1 31	Test Circuit 6
Off Isolation	-60		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 10 MHz$
	-80		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$;
			JP	Test Circuit 7
Channel-to-Channel Crosstalk	-62		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 10 MHz$
Grammer to Grammer Grosstank	-82		dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$;
	02		ub typ	Test Circuit 8
Bandwidth –3 dB	200		MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$; Test Circuit
C _S (OFF)	9		pF typ	IL - 30 22, OL - 3 pr., Test Circuit
C _D (OFF)	37		pF typ	
C_D (ON)	54		pF typ	
	77		prityp	
POWER REQUIREMENTS				$V_{\rm DD} = +3.3 \text{ V}$
				Digital Inputs = 0 V or 3 V
$I_{ m DD}$	0.001		μA typ	
		1.0	μA max	

REV. A -3-

NOTES ¹Temperature ranges are as follows: B Version: -40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG704

ABSOLUTE MAXIMUM RATINGS¹

 $(T_A = +25^{\circ}C \text{ unless otherwise noted})$

(1 _A = 125 C unless otherwise noted)
V _{DD} to GND0.3 V to +6 V
Analog, Digital Inputs ² -0.3 V to V_{DD} +0.3 V or
30 mA, Whichever Occurs First
Continuous Current, S or D
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range
Industrial (B Version)40°C to +85°C
Storage Temperature Range65°C to +150°C
Junction Temperature +150°C
μSOIC Package, Power Dissipation
θ_{JA} Thermal Impedance
Lead Temperature, Soldering
Vapor Phase (60 sec)+215°C
Infrared (15 sec) +220°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

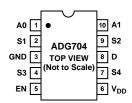
ORDERING GUIDE

Model	Temperature Range	Brand ¹	Package Option ²
ADG704BRM	−40°C to +85°C	S9B	RM-10

NOTES

¹Brand = Due to small package size, these three characters represent the part number.

PIN CONFIGURATION (10-Lead μSOIC)



TERMINOLOGY

tance as measured over the specified analog signal range. ID (OFF) Drain leakage current with the switch "OFF." Source leakage current with the switch "OFF." ID, IS (ON) Channel leakage current with the switch "ON." VD (VS) Analog voltage on terminals D, S. CS (OFF) CD (OFF) CD, CS (ON) CS (ON) CS (ON) CS (ON) CON" switch drain capacitance. OPER' switch drain capacitance. OPER' switch drain capacitance. CON" switch capacitance. Delay between applying the digital control input and the output switching off. "OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another. See Test Circuit 5. Crosstalk A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. Off Isolation A measure of unwanted signal coupling through an "OFF" switch. A measure of the glitch impulse transferred from the digital input to the analog output during switching. The frequency at which the output is attenuated by -3 dBs. On Response On Loss The voltage drop across the "ON" switch, seen on the On Response vs. Frequency plot	TERMINOLOG	GY		
Source terminal. May be an input or output. Drain terminal. May be an input or output. Logic control inputs. EN Logic control input. Cohmic resistance between D and S. Con resistance match between any two channels i.e., R _{ON} max-R _{ON} min. Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range. I _D (OFF) I _S (OFF) I _D I _S (ON) V _D V _S Cas (OFF) C _D (OFF) C _D (OFF) C _D (OFF) C _D (OFF) T _O (OFF) C _D (OFF) C _D (OFF) C _D (ON) Ton Delay between applying the digital control input and the output switching off. Coff? "Time or "ON" time measured between the 90% points of both switches, when switching from one address state to another. See Test Circuit 5. Crosstalk A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. Off Isolation A measure of unwanted signal coupling through an "OFF" switch. A measure of unwanted signal coupling through an "OFF" switch. Charge Injection A measure of unwanted signal coupling through an "OFF" switch. A measure of unwanted signal coupling through an "OFF" switch. Charge Injection A measure of unwanted signal coupling through an "OFF" switch. The frequency at which the output is attenuated by -3 dBs. On Response On Loss The frequency response of the "ON" switch, seen on the On Response vs. Frequency plot	$V_{ m DD}$	Most positive power supply potential.		
D Drain terminal. May be an input or output. A0, A1 Logic control inputs. EN Logic control input. Ohmic resistance between D and S. On resistance match between any two channels i.e., Ronmax-Ronmin. Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range. ID (OFF) Drain leakage current with the switch "OFF." IS (OFF) Source leakage current with the switch "OFF." ID, IS (ON) Channel leakage current with the switch "ON." VD (VS) Analog voltage on terminals D, S. "OFF" switch source capacitance. "OFF" switch drain capacitance. "ON" switch capacitance. Delay between applying the digital control input and the output switching off. TOFF ToPical Source in the switch of	GND	Ground (0 V) reference.		
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input and the output switching on. See Test Circuit 4. Delay between applying the digital control input and the output switching off. "OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another. See Test Circuit 5. Crosstalk A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. Off Isolation A measure of unwanted signal coupling through an "OFF" switch. Charge Injection A measure of the glitch impulse transferred from the digital input to the analog output during switching. Bandwidth The frequency at which the output is attenuated by -3 dBs. On Response On Loss The voltage drop across the "ON" switch, seen on the On Response vs. Frequency plot	C_D , C_S (ON)	"ON" switch capacitance.		
input and the output switching off. "OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another. See Test Circuit 5. Crosstalk A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. Off Isolation A measure of unwanted signal coupling through an "OFF" switch. Charge Injection A measure of the glitch impulse transferred from the digital input to the analog output during switching. Bandwidth The frequency at which the output is attenuated by -3 dBs. On Response On Loss The voltage drop across the "ON" switch, seen on the On Response vs. Frequency plot	t_{ON}	input and the output switching on. See Test		
the 90% points of both switches, when switching from one address state to another. See Test Circuit 5. Crosstalk A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. Off Isolation A measure of unwanted signal coupling through an "OFF" switch. Charge Injection A measure of the glitch impulse transferred from the digital input to the analog output during switching. Bandwidth The frequency at which the output is attenuated by –3 dBs. On Response On Loss The voltage drop across the "ON" switch, seen on the On Response vs. Frequency plot	t _{OFF}			
through from one channel to another as a result of parasitic capacitance. A measure of unwanted signal coupling through an "OFF" switch. A measure of the glitch impulse transferred from the digital input to the analog output during switching. Bandwidth The frequency at which the output is attenuated by –3 dBs. On Response On Loss The voltage drop across the "ON" switch, seen on the On Response vs. Frequency plot	t_{D}	the 90% points of both switches, when switching from one address state to another. See Test		
through an "OFF" switch. Charge Injection Bandwidth On Response On Loss through an "OFF" switch. A measure of the glitch impulse transferred from the digital input to the analog output during switching. The frequency at which the output is attenuated by –3 dBs. The frequency response of the "ON" switch. The voltage drop across the "ON" switch, seen on the On Response vs. Frequency plot	Crosstalk	through from one channel to another as a		
Injection from the digital input to the analog output during switching. Bandwidth The frequency at which the output is attenuated by -3 dBs. On Response On Loss The voltage drop across the "ON" switch, seen on the On Response vs. Frequency plot	Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.		
ated by –3 dBs. On Response On Loss The frequency response of the "ON" switch. The voltage drop across the "ON" switch, seen on the On Response vs. Frequency plot		from the digital input to the analog output		
On Loss The voltage drop across the "ON" switch, seen on the On Response vs. Frequency plot	Bandwidth			
seen on the On Response vs. Frequency plot	On Response	The frequency response of the "ON" switch.		
at very low frequencies.	On Loss	seen on the On Response vs. Frequency plot as how many dBs the signal is away from 0 dB		

Table I. Truth Table

A1	A 0	EN	ON Switch
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG704 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



 $^{{}^{2}}RM = \mu SOIC.$

Typical Performance Characteristics—ADG704

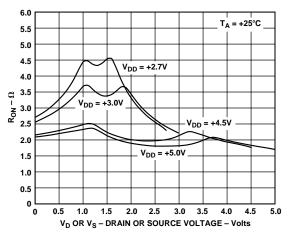


Figure 1. On Resistance as a Function of V_D (V_S) Single Supplies

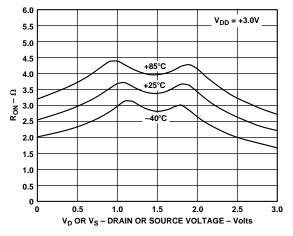


Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures; $V_{DD} = 3 \text{ V}$

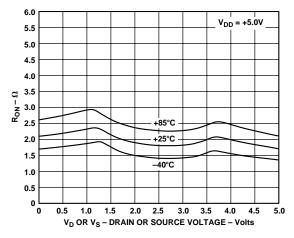


Figure 3. On Resistance as a Function of V_D (V_S) for Different Temperatures; $V_{DD} = 5 \text{ V}$

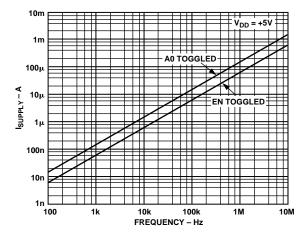


Figure 4. Supply Current vs. Input Switching Frequency

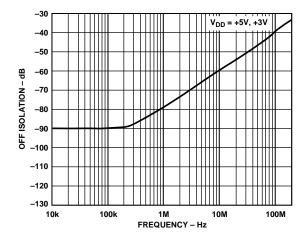


Figure 5. Off Isolation vs. Frequency

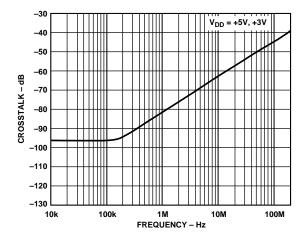


Figure 6. Crosstalk vs. Frequency

REV. A -5-

ADG704

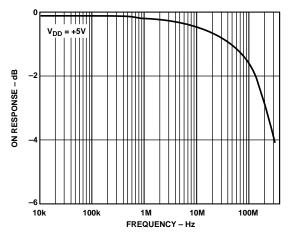


Figure 7. On Response vs. Frequency

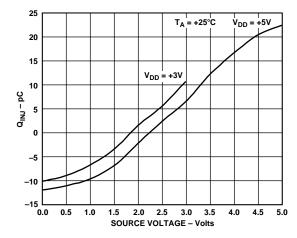


Figure 8. Charge Injection vs. Source Voltage

APPLICATIONS

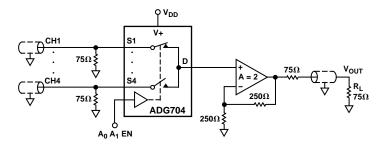
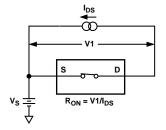


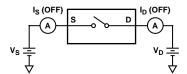
Figure 9. 4-Channel Video Multiplexing

-6-

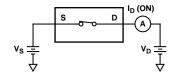
Test Circuits



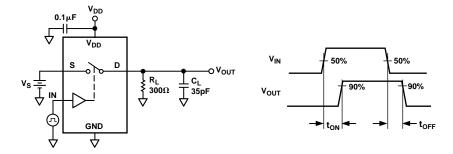
Test Circuit 1. On Resistance



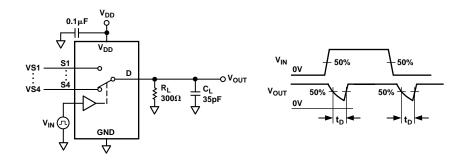
Test Circuit 2. Off Leakage



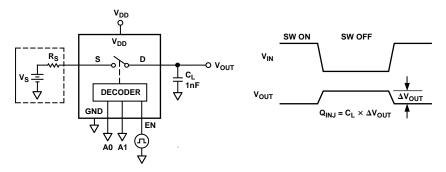
Test Circuit 3. On Leakage



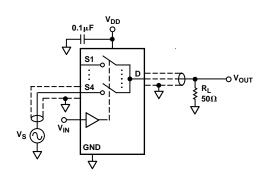
Test Circuit 4. Switching Times



Test Circuit 5. Break-Before-Make Time Delay, t_D



Test Circuit 6. Charge Injection



V_{OUT} O

V_{DD}

V_{DD}

S1

V_{DD}

R_L

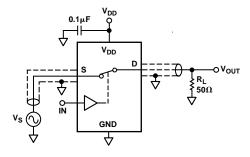
50Ω

CHANNEL-TO-CHANNEL

CROSSTALK = 20 × LOG |V_S/V_{OUT}|

Test Circuit 7. Off Isolation

Test Circuit 8. Channel-to-Channel Crosstalk



Test Circuit 9. Bandwidth

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

10-Lead μSOIC (RM-10)

