# TPS54328 4.5-V to 18-V Input, 3-A Synchronous Step-Down Converter With Eco-Mode™

## 1 Features

- D-CAP2™ Mode Enables Fast Transient Response
- Low Output Ripple and Allows Ceramic Output Capacitor
- Wide Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.76 V to 7 V
- Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications
  - 100 mΩ (High-Side) and 70 mΩ (Low-Side)
- High Efficiency, Less Than 10 µA at Shutdown
- High Initial Bandgap Reference Accuracy
- Adjustable Soft Start
- Pre-Biased Soft Start
- 700-kHz Switching Frequency ($f_{SW}$)
- Cycle-By-Cycle Overcurrent Limit
- Auto-Skip Eco-Mode™ for High Efficiency at Light Load

## 2 Applications

- Wide Range of Applications for Low Voltage Systems
  - Digital TV Power Supplies
  - High Definition Blu-ray Disc™ Players
  - Networking Home Terminals
  - Digital Set Top Boxes (STB)

## 3 Description

The TPS54328 is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54328 enables system designers to complete the suite of various end-equipment power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54328 uses the D-CAP2 mode control that provides a fast transient response with no external compensation components.

The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Eco-mode operation at light loads. Eco-mode allows the TPS54328 to maintain high efficiency during lighter load conditions. The TPS54328 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V input ($V_{IN}$).

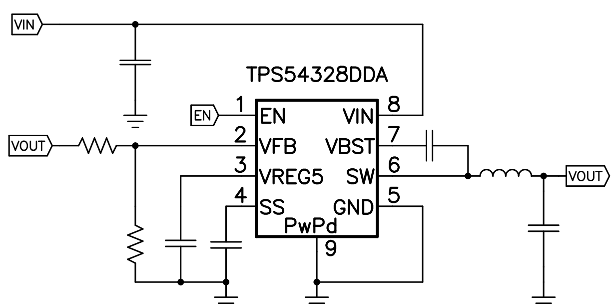
The output voltage can be programmed from 0.76 V to 7 V. The device also features an adjustable soft start time. The TPS54328 is available in 8-pin DDA and 10-pin DRC packages, and is designed to operate over the ambient temperature range of –40°C to 85°C.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS54328 | HSOP (8) | 4.89 mm × 3.90 mm |
| | VSON (10) | 3.00 mm × 3.00 mm |

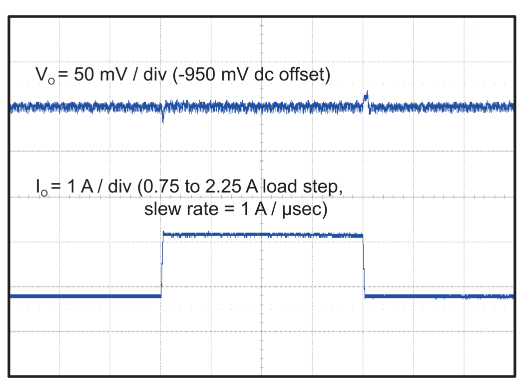
(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic**






**TPS54320 Transient Response**




Time = 50 µsec / div

## Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (November 2012) to Revision D | Page |
|---|---|
| • Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. | 1 |
| • Deleted *Ordering Information* table; see POA at the end of the data sheet | 1 |
| • Changed heartsick to heatsink in *Thermal Considerations* section | 17 |

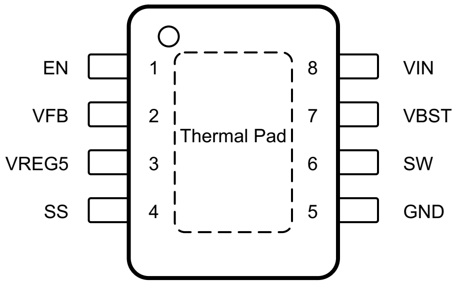
| Changes from Revision B (April 2012) to Revision C | Page |
|---|---|
| • Changed the Description text to include the DRC package | 1 |
| • Added the DRC-10 pin Package to the ORDERING INFORMATION table | 1 |
| • Added Figure 17 | 16 |

| Changes from Revision A (January 2012) to Revision B | Page |
|---|---|
| • Deleted Swift™ from the data sheet title | 1 |
| • Changed Figure 9 and Figure 10 | 13 |

| Changes from Original (November 2010) to Revision A | Page |
|---|---|
| • Added condition to the TYPICAL CHARACTERISTICS title line, all pages | 6 |
| • Changed the Functional Block Diagram | 8 |

# 5 Pin Configuration and Functions

**DDA Package**
**8-Pin HSOP**
**Top View**

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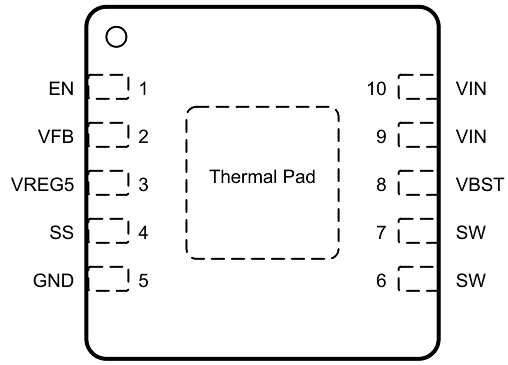
**DRC Package**
**10-Pin VSON**
**Top View**




Not to scale

**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | HSOP | VSON | | |
| EN | 1 | 1 | I | Enable input control. Active high. |
| GND | 5 | — | — | Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point. |
| | — | 5 | — | Ground pin. Connect sensitive SS and VFB returns to GND at a single point. |
| SS | 4 | 4 | I | Soft-start control. An external capacitor must be connected to GND. |
| SW | 6 | 6, 7 | O | Switch node connection between high-side NFET and low-side NFET. |
| VBST | 7 | 8 | I | Supply input for the high-side FET gate drive circuit. Connect 0.1-µF capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST. |
| VFB | 2 | 2 | I | Converter feedback input. Connect to output voltage with feedback resistor divider. |
| VIN | 8 | 9, 10 | I | Input voltage supply pin. |
| VREG5 | 3 | 3 | O | 5.5-V power-supply output. A capacitor (typically 1 µF) must be connected to GND. VREG5 is not active when EN is low. |
| Exposed Thermal Pad | Back side | — | — | Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND. |
| | — | Back side | — | Thermal pad of the package. PGND power ground return of internal low-side FET. Must be soldered to achieve appropriate dissipation. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | VIN, EN | –0.3 | 20 | V |
| | VBST | –0.3 | 26 | |
| | VBST (10 ns transient) | –0.3 | 28 | |
| | VBST (vs SW) | –0.3 | 6.5 | |
| | VFB, SS | –0.3 | 6.5 | |
| | SW | –2 | 20 | |
| | SW (10-ns transient) | –3 | 22 | |
| Output voltage | VREG5 | –0.3 | 6.5 | V |
| | GND | –0.3 | 0.3 | |
| Voltage from GND to thermal pad, $V_{diff}$ | | –0.2 | 0.2 | V |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Supply input voltage | | 4.5 | 18 | V |
| | Input voltage | VBST | –0.1 | 24 | V |
| | | VBST (10-ns transient) | –0.1 | 27 | |
| | | VBST(vs SW) | –0.1 | 5.7 | |
| | | SS | –0.1 | 5.7 | |
| | | EN | –0.1 | 18 | |
| | | VFB | –0.1 | 5.5 | |
| | | SW | –1.8 | 18 | |
| | | SW (10-ns transient) | –3 | 21 | |
| | | GND | –0.1 | 0.1 | |
| $V_{OUT}$ | Output voltage | VREG5 | –0.1 | 5.7 | V |
| $I_{OUT}$ | Output current | $I_{VREG5}$ | 0 | 10 | mA |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |
| $T_J$ | Operating junction temperature | | –40 | 150 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPS54328 DDA (HSOP) 8 PINS | TPS54328 DRC (VSON) 10 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 42.1 | 43.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 50.9 | 55.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 31.8 | 18.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 5 | 0.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 13.5 | 19.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 7.1 | 5.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range, $V_{IN}$ = 12 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $I_{VIN}$ | Operating non-switching supply current | VIN current, $T_A$ = 25°C, EN = 5 V, $V_{FB}$ = 0.8 V | | 800 | 1200 | µA |
| $I_{VINSDN}$ | Shutdown supply current | VIN current, $T_A$ = 25°C, EN = 0 V | | 1.8 | 10 | µA |
| **LOGIC THRESHOLD** | | | | | | |
| $V_{ENH}$ | EN high-level input voltage | EN | 1.6 | | | V |
| $V_{ENL}$ | EN low-level input voltage | EN | | | 0.45 | V |
| **$V_{FB}$ VOLTAGE AND DISCHARGE RESISTANCE** | | | | | | |
| $V_{FBTH}$ | VFB threshold voltage | $T_A$ = 25°C, $V_{OUT}$ = 1.05 V, $I_{OUT}$ = 10 mA, Eco-mode operation | | 772 | | mV |
| | | $T_A$ = 25°C, $V_{OUT}$ = 1.05 V, continuous mode operation | 749 | 765 | 781 | mV |
| $I_{VFB}$ | VFB input current | $V_{FB}$ = 0.8 V, $T_A$ = 25°C | | 0 | ±0.1 | µA |
| **VREG5 OUTPUT** | | | | | | |
| $V_{VREG5}$ | VREG5 output voltage | $T_A$ = 25°C, 6 V < $V_{IN}$ < 18 V, 0 < $I_{VREG5}$ < 5 mA | 5.2 | 5.5 | 5.7 | V |
| $V_{LN5}$ | Line regulation | 6 V < $V_{IN}$ < 18 V, $I_{VREG5}$ = 5 mA | | | 25 | mV |
| $V_{LD5}$ | Load regulation | 0 mA < $I_{VREG5}$ < 5 mA | | | 100 | mV |
| $I_{VREG5}$ | Output current | $V_{IN}$ = 6 V, $V_{VREG5}$ = 4 V, $T_A$ = 25°C | | 60 | | mA |
| **MOSFET** | | | | | | |
| $R_{DS(ON)H}$ | High-side switch resistance | $T_A$ = 25°C, $V_{BST}$ – SW = 5.5 V | | 100 | | mΩ |
| $R_{DS(ON)L}$ | Low-side switch resistance | $T_A$ = 25°C | | 70 | | mΩ |
| **CURRENT LIMIT** | | | | | | |
| $I_{OCL}$ | Current limit | $L_{OUT}$ = 1.5 µH[1], $T_A$ = –20ºC to 85ºC | 3.5 | 4.2 | 5.7 | A |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SDN}$ | Thermal shutdown threshold | Shutdown temperature [1] | | 165 | | °C |
| | | Hysteresis [1] | | 30 | | °C |
| **ON-TIME TIMER CONTROL** | | | | | | |
| $t_{ON}$ | ON time | $V_{IN}$ = 12 V, $V_{OUT}$ = 1.05 V | | 150 | | ns |
| $t_{OFF(MIN)}$ | Minimum off time | $T_A$ = 25°C, $V_{FB}$ = 0.7 V | | 260 | 310 | ns |
| **SOFT START** | | | | | | |
| $I_{SSC}$ | SS charge current | $V_{SS}$ = 0 V | 1.4 | 2 | 2.6 | µA |
| $I_{SSD}$ | SS discharge current | $V_{SS}$ = 0.5 V | 0.05 | 0.1 | | mA |

(1) Not production tested.

## Electrical Characteristics (continued)

over operating free-air temperature range, $V_{IN}$ = 12 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **UVLO** | | | | | | |
| UVLO | UVLO threshold | Wake up VREG5 voltage | 3.45 | 3.75 | 4.05 | V |
| | | Hysteresis VREG5 voltage | 0.17 | 0.32 | 0.45 | |

## 6.6 Typical Characteristics

$V_{IN}$ = 12 V, $T_A$ = 25°C (unless otherwise noted).

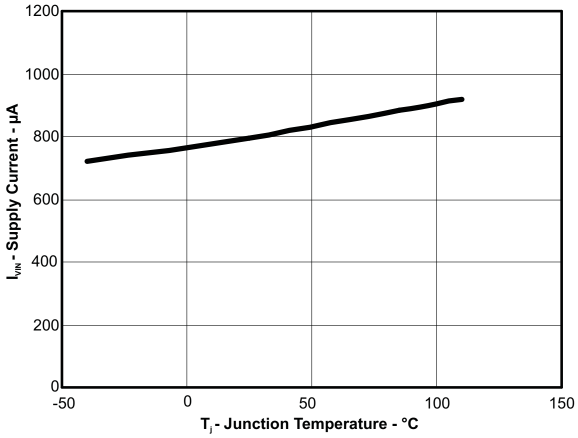



Figure 1. VIN Current vs Junction Temperature

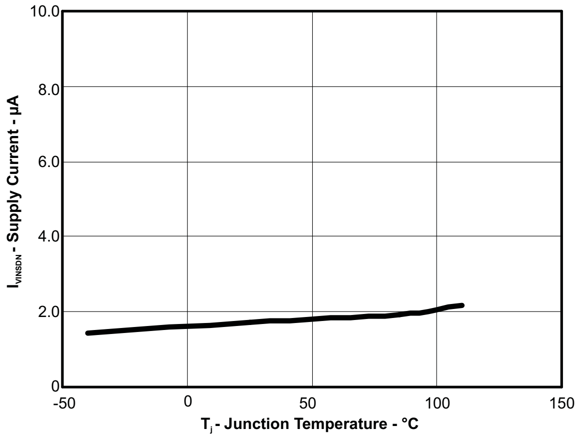



Figure 2. VIN Shutdown Current vs Junction Temperature

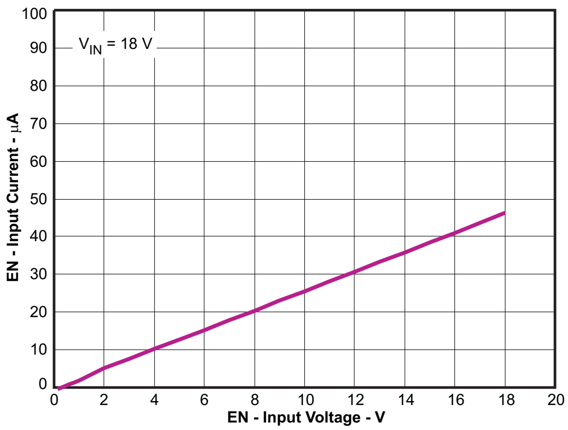



Figure 3. EN Current vs EN Voltage

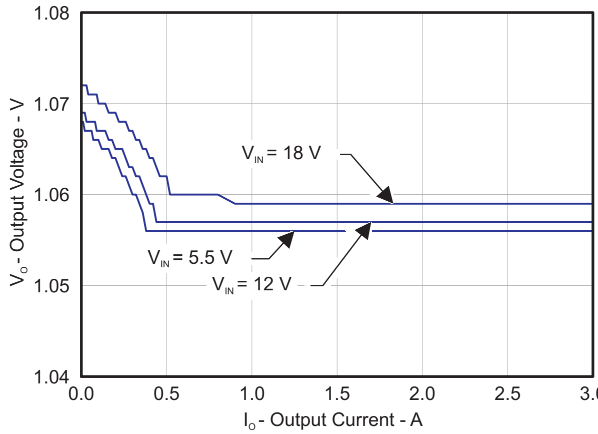



Figure 4. 1.05-V Output Voltage vs Output Current

## Typical Characteristics (continued)

$V_{IN}$ = 12 V, $T_A$ = 25°C (unless otherwise noted).

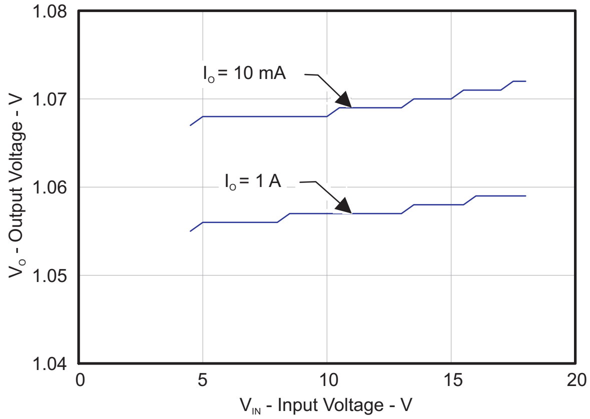


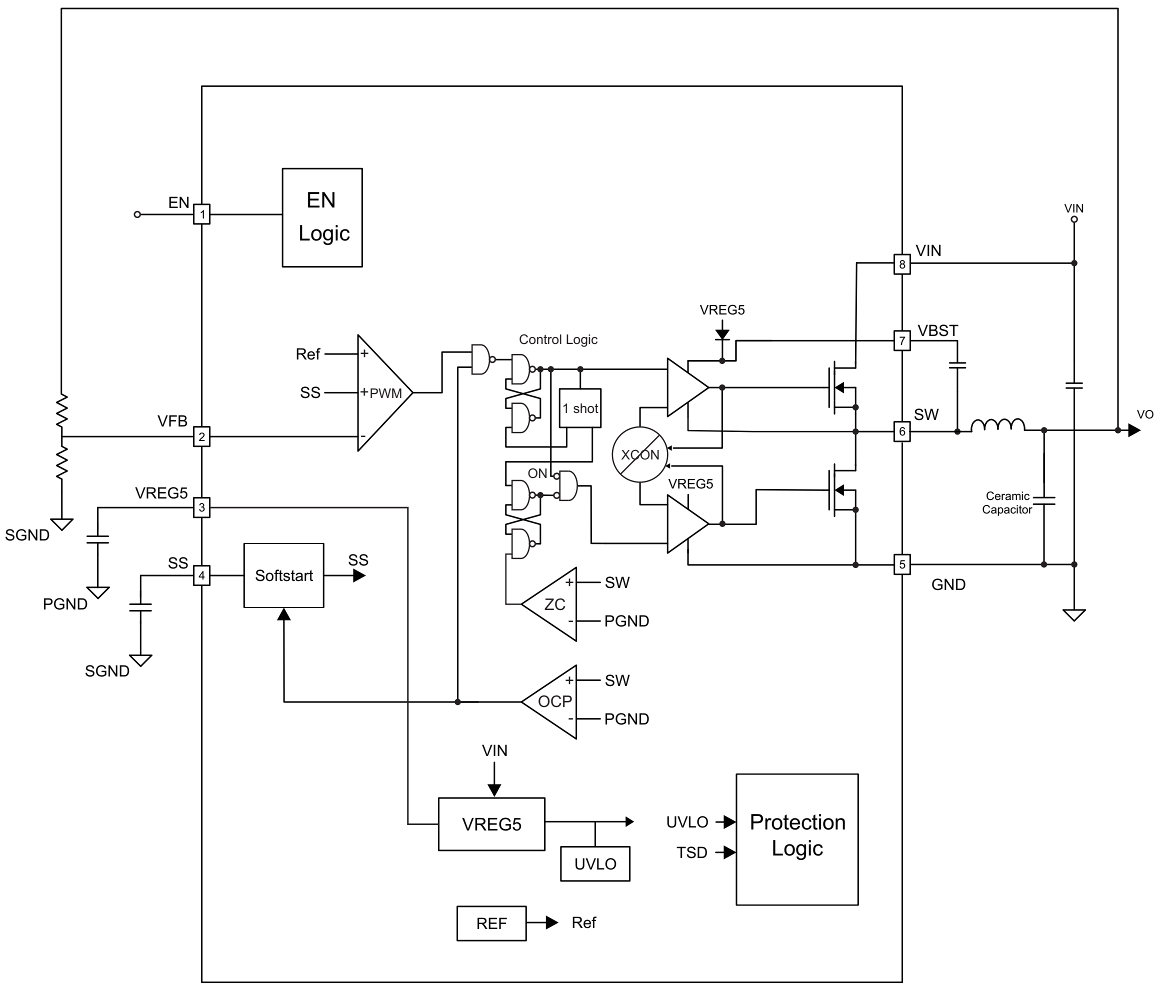

**Figure 5. 1.05-V Output Voltage vs Input Voltage**

# 7 Detailed Description

## 7.1 Overview

The TPS54328 is a 3-A, synchronous, step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2 mode control. The fast transient response of D-CAP2 control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low-ESR output capacitors including ceramic and special polymer types.

## 7.2 Functional Block Diagram






## 7.3 Feature Description

### 7.3.1 PWM Operation

The main control loop of the TPS54328 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 mode control. D-CAP2 mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

## Feature Description (continued)

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot is set by the converter input voltage ($V_{IN}$) and the output voltage ($V_{OUT}$) to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2 mode control.

### 7.3.2 PWM Frequency and Adaptive On-Time Control

TPS54328 uses an adaptive on-time control scheme and does not have a dedicated onboard oscillator. The TPS54328 runs with a pseudo-constant frequency of 700 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is $V_{OUT}$ / $V_{IN}$, the frequency is constant.

### 7.3.3 Auto-Skip Eco-Mode Control

The TPS54328 is designed with Auto-Skip Eco-Mode to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost the same as is was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \cdot L \cdot fsw} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN}} \tag{1}$$

### 7.3.4 Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 2-µA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in Equation 2. VFB voltage is 0.765 V and SS pin source current is 2 µA.

$$t_{SS}(ms) = \frac{C6(nF) \times V_{REF} \times 1.1}{I_{SS}(\mu A)} = \frac{C6(nF) \times 0.765 \times 1.1}{2} \tag{2}$$

The TPS54328 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage $V_{FB}$), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that $V_{OUT}$ starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

### 7.3.5 Current Protection

The output over-current protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by $V_{IN}$, $V_{OUT}$, the on-time, and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current $I_{OUT}$. The TPS54328 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching

## Feature Description (continued)

cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current one half of the peak-to-peak inductor current higher than the over-current threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the over current condition is removed, the output voltage returns to the regulated value. This protection is non-latching.

### 7.3.6 UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the VREG5 pin. When the VREG5 voltage is lower than UVLO threshold voltage, the TPS54328 is shut off. This protection is non-latching.

### 7.3.7 Thermal Shutdown

TPS54328 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latch protection.

## 7.4 Device Functional Modes

### 7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS54328 can operate in the normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS54328 operates at a quasi-fixed frequency of 700 kHz.

### 7.4.2 Standby Operation

When the device is operating in either normal CCM or forced CCM, it may be placed in standby operation mode by asserting the EN pin low.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPS54328 is typically used as step down converters, which convert a voltage from 4.5 V to 18 V to a lower voltage. WEBENCH® software is available to aid in the design and analysis of circuits.

## 8.2 Typical Application

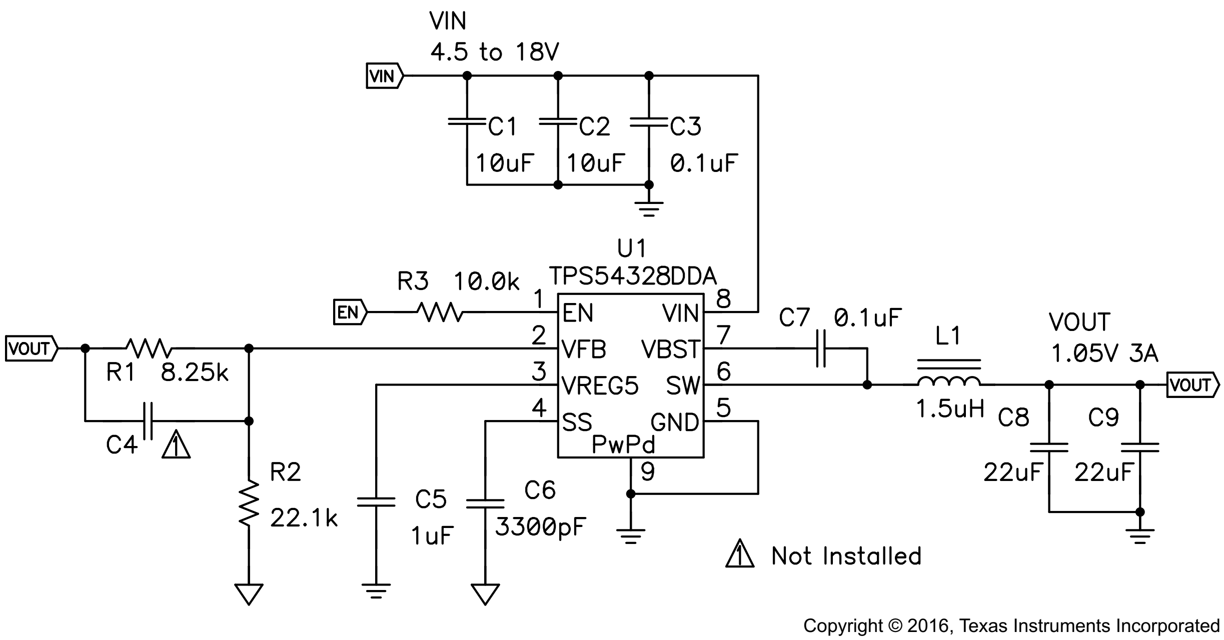



**Figure 6. Schematic Diagram**

### 8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

**Table 1. Design Parameters**

| PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage | 4.5 V to 18 V |
| Output voltage | 1.05 V |
| Output current | 3 A |
| Output voltage ripple | 50 $mV_{PP}$ |

### 8.2.2 Detailed Design Procedure

To begin the design process, you must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple

- Input voltage ripple

#### 8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends using 1% tolerance or better divider resistors. Start by using Equation 3 to calculate $V_{OUT}$.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance is more susceptible to noise and voltage errors from the VFB input current is more noticeable.

$$V_{OUT} = 0.765 \times \left(1 + \frac{R1}{R2}\right) \tag{3}$$

#### 8.2.2.2 Output Filter Selection

The output filter used with the TPS54328 is an LC circuit. This LC filter has a double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{4}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54328. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high-frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 4 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values in Table 2.

**Table 2. Recommended Component Values**

| OUTPUT VOLTAGE (V) | R1 (kΩ) | R2 (kΩ) | C4 (pF) | L1 (µH) | C8 + C9 (µF) |
|---|---|---|---|---|---|
| 1 | 6.81 | 22.1 | — | 1.5 | 22 – 68 |
| 1.05 | 8.25 | 22.1 | — | 1.5 | 22 – 68 |
| 1.2 | 12.7 | 22.1 | — | 1.5 | 22 – 68 |
| 1.8 | 30.1 | 22.1 | 5 - 22 | 2.2 | 22 – 68 |
| 2.5 | 49.9 | 22.1 | 5 - 22 | 2.2 | 22 – 68 |
| 3.3 | 73.2 | 22.1 | 5 - 22 | 2.2 | 22 – 68 |
| 5 | 124 | 22.1 | 5 - 22 | 3.3 | 22 – 68 |
| 6.5 | 165 | 22.1 | 5 - 22 | 3.3 | 22 – 68 |

Because the DC gain is dependent on the output voltage, the required inductor value increases as the output voltage increases. For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 5, Equation 6 and Equation 7. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 700 kHz for $f_{SW}$.

Use 700 kHz for $f_{SW}$. Make sure the chosen inductor is rated for the peak current of Equation 6 and the RMS current of Equation 7.

$$I_{IPP} = \frac{V_{OUT}}{V_{IN(max)}} \times \frac{V_{IN(max)} - V_{OUT}}{L_O \times f_{SW}} \tag{5}$$

$$I_{lpeak} = I_O + \frac{I_{lpp}}{2} \tag{6}$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{IPP}^2} \tag{7}$$

For this design example, the calculated peak current is 3.49 A and the calculated RMS current is 3.01 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54328 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22 µF to 68 µF. Use Equation 8 to determine the required RMS current rating for the output capacitor.

$$I_{Co(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (8)$$

For this design two TDK C3216X5R0J226M 22µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.271 A and each output capacitor is rated for 4 A.

#### 8.2.2.3 Input Capacitor Selection

The TPS54328 requires an input decoupling capacitor and a bulk capacitor is required depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. TI recommends an additional 0.1-µF capacitor from VIN to ground to improve the stability of the over-current limit function. The capacitor voltage rating requires to be greater than the maximum input voltage.

#### 8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST and SW pin for proper operation. TI recommends using a ceramic capacitor.

#### 8.2.2.5 VREG5 Capacitor Selection

A 1-µF ceramic capacitor must be connected between the VREG5 and GND pins for proper operation. TI recommends using a ceramic capacitor.

### 8.2.3 Application Curves

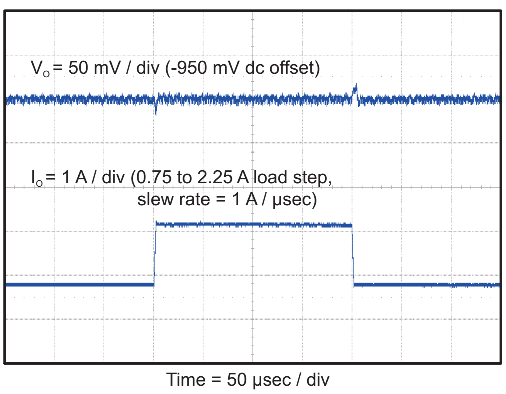



**Figure 7. 1.05 V, Load Transient Response**

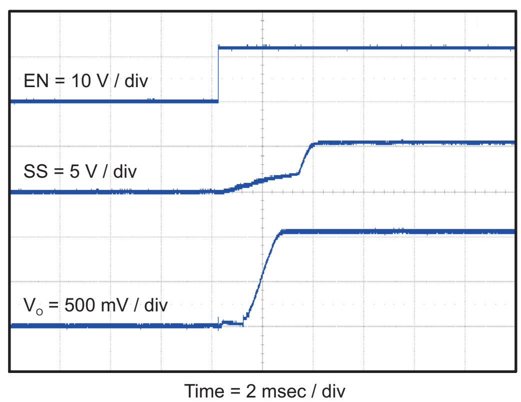



**Figure 8. Start-up Waveform**

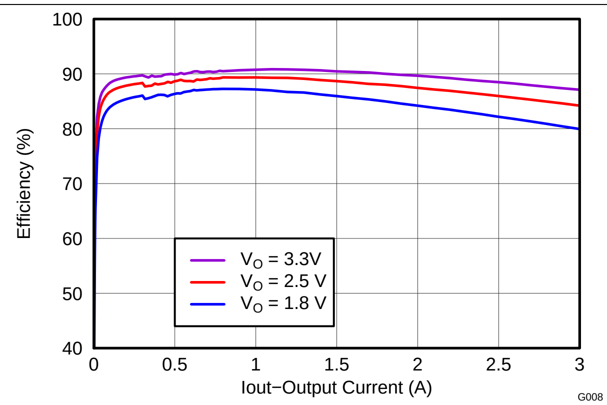



**Figure 9. Efficiency vs Output Current**

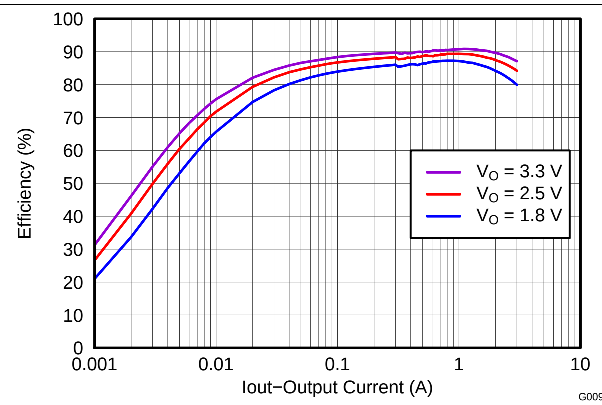



**Figure 10. Light Load Efficiency vs Output Current**

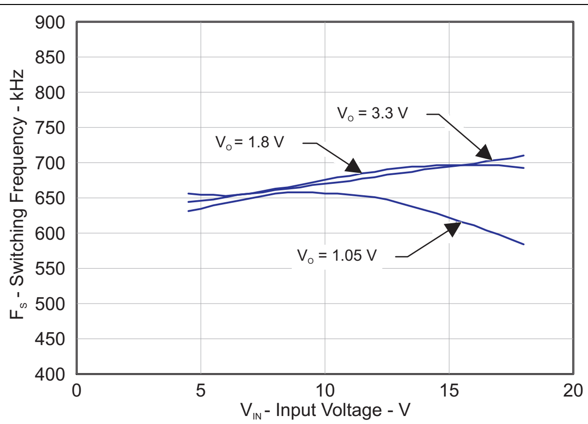



**Figure 11. Switching Frequency vs Input Voltage**

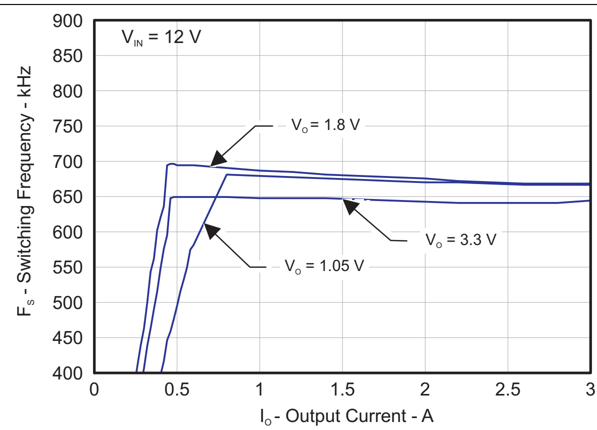
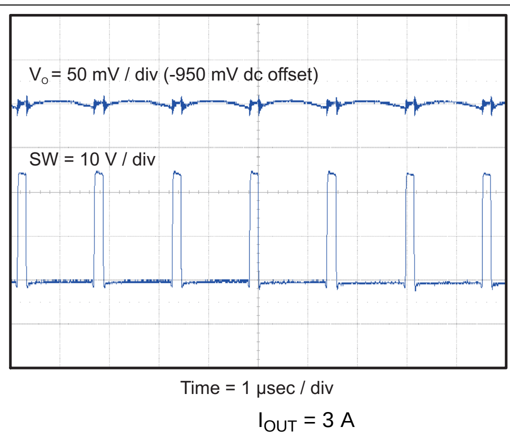


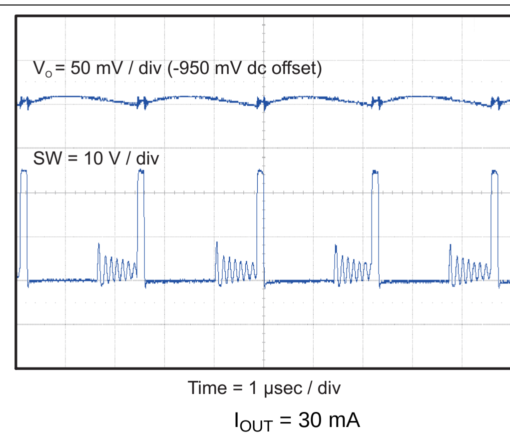

**Figure 12. Switching Frequency vs Output Current**




Time = 1 μsec / div

$I_{OUT}$ = 3 A

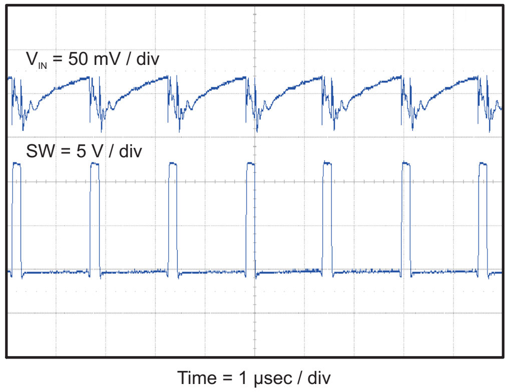
**Figure 13. Voltage Ripple at Output**




Time = 1 μsec / div

$I_{OUT}$ = 30 mA

**Figure 14. DCM Voltage Ripple at Output**




$I_{OUT}$ = 3 A

**Figure 15. Voltage Ripple at Input**

# 9 Power Supply Recommendations

The TPS54328 is designed to operate from input supply voltage of 4.5 V to 18 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 65%. Using that criteria, the minimum recommended input voltage is $V_{OUT}$ / 0.65.

# 10 Layout

## 10.1 Layout Guidelines

- Keep the input switching current loop as small as possible.
- Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections must be brought from the output to the feedback pin of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.
- Keep the pattern lines for VIN and PGND broad.
- Exposed pad of device must be connected to PGND with solder.
- VREG5 capacitor must be placed near the device, and connected PGND.
- Output capacitor must be connected to a broad pattern of the PGND.
- Voltage feedback loop must be as short as possible, and preferably with ground shield.
- Lower resistor of the voltage divider which is connected to the VFB pin must be tied to SGND.
- Providing sufficient vias is preferable for VIN, SW and PGND connection.
- PCB pattern for VIN, SW, and PGND must be as broad as possible.
- VIN capacitor must be placed as near as possible to the device.

## 10.2 Layout Example

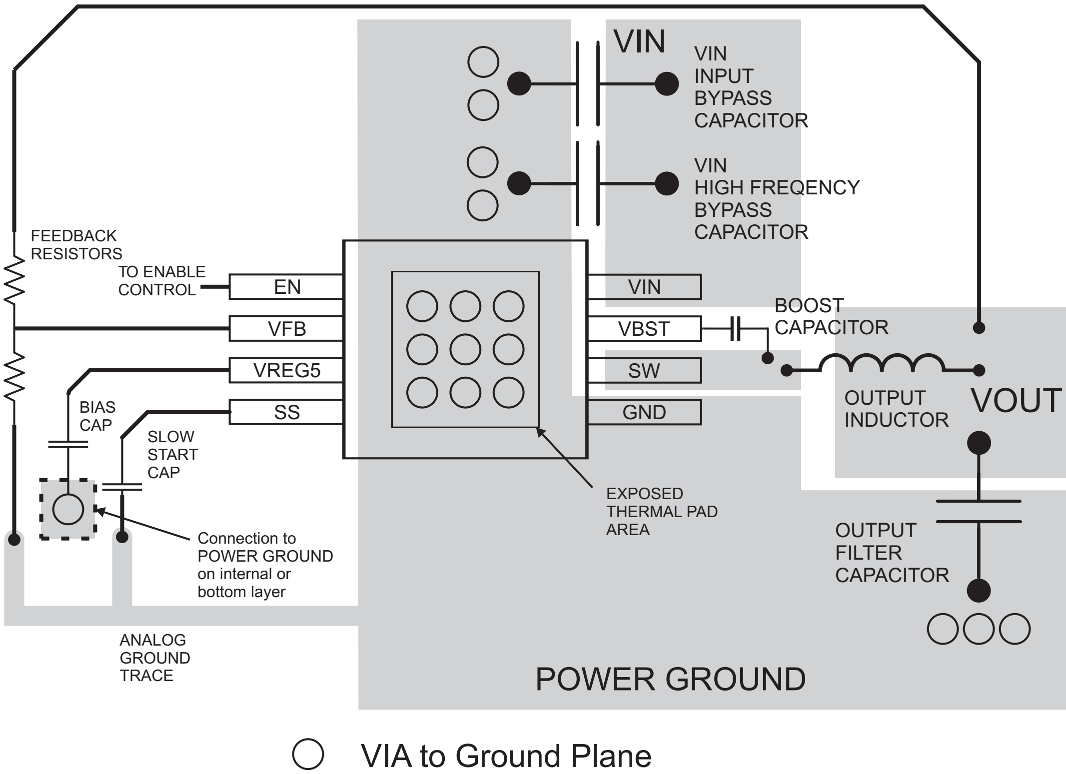



**Figure 16. PCB Layout**

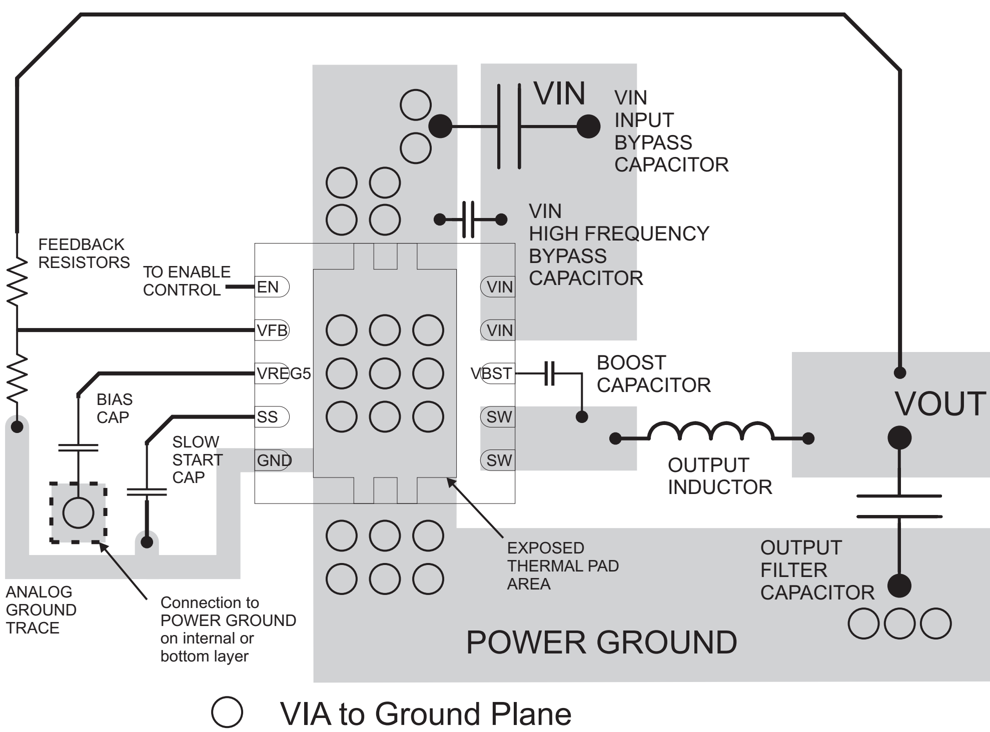



**Figure 17. PCB Layout for the DRC Package**

## 10.3 Thermal Considerations

This 8-pin DDA package incorporates an exposed thermal pad that is designed to be directly to an external heat sink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heat sink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heat sink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, see *PowerPAD™ Thermally Enhanced Package* and *PowerPAD™ Made Easy*.

The exposed thermal pad dimensions for this package are shown in Figure 18.

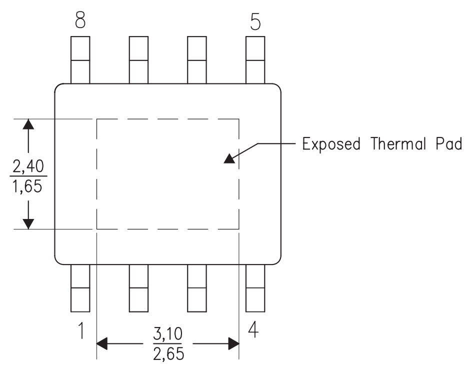



**Figure 18. Thermal Pad Dimensions**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Development Support

For the WEBENCH Tools, go to http://www.ti.com/lsds/ti/analog/webench/overview.page

## 11.2 Documentation Support

### 11.2.1 Related Documentation

For related documentation see the following:

- *PowerPAD™ Thermally Enhanced Package* (SLMA002)
- *PowerPAD™ Made Easy* (SLMA004)

## 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.5 Trademarks

D-CAP2, Eco-Mode, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
Blu-ray Disc is a trademark of Blu-ray Disc Association.
All other trademarks are the property of their respective owners.

## 11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS54328DDA | ACTIVE | SO PowerPAD | DDA | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-2-260C-1 YEAR | -40 to 85 | 54328 | Samples |
| TPS54328DDAR | ACTIVE | SO PowerPAD | DDA | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-2-260C-1 YEAR | -40 to 85 | 54328 | Samples |
| TPS54328DRCR | ACTIVE | VSON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 54328 | Samples |
| TPS54328DRCT | ACTIVE | VSON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 54328 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

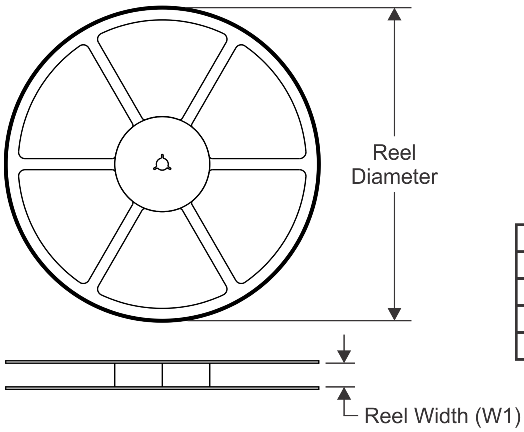
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

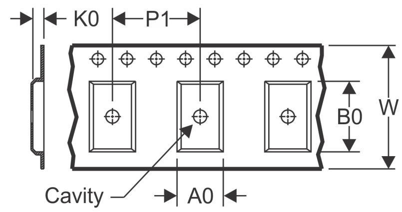
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

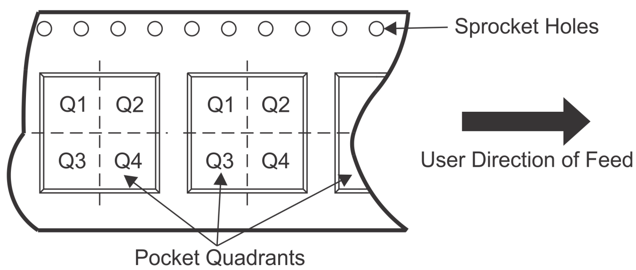



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

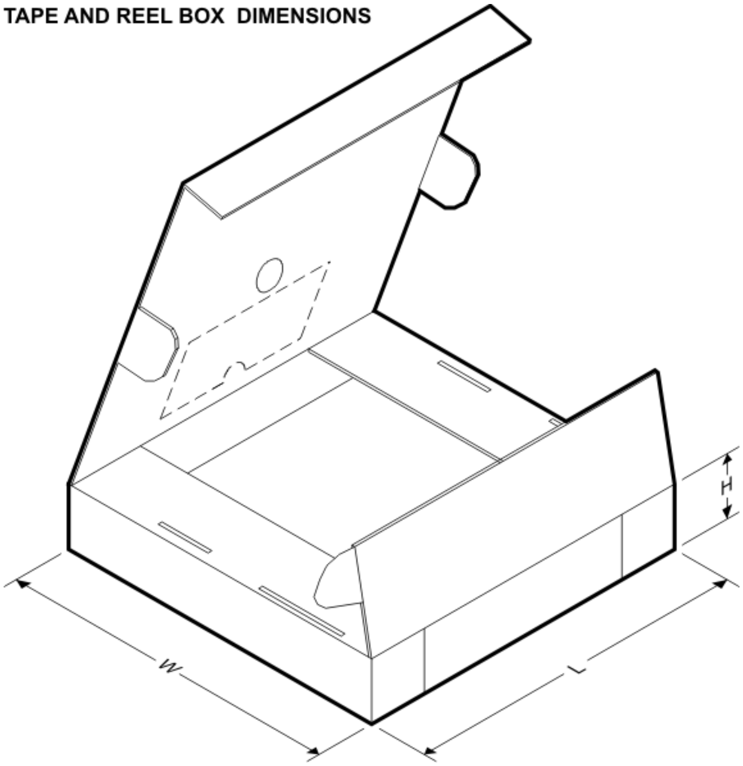
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS54328DDAR | SO Power PAD | DDA | 8 | 2500 | 330.0 | 12.8 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS54328DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS54328DRCT | VSON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

**TAPE AND REEL BOX DIMENSIONS**

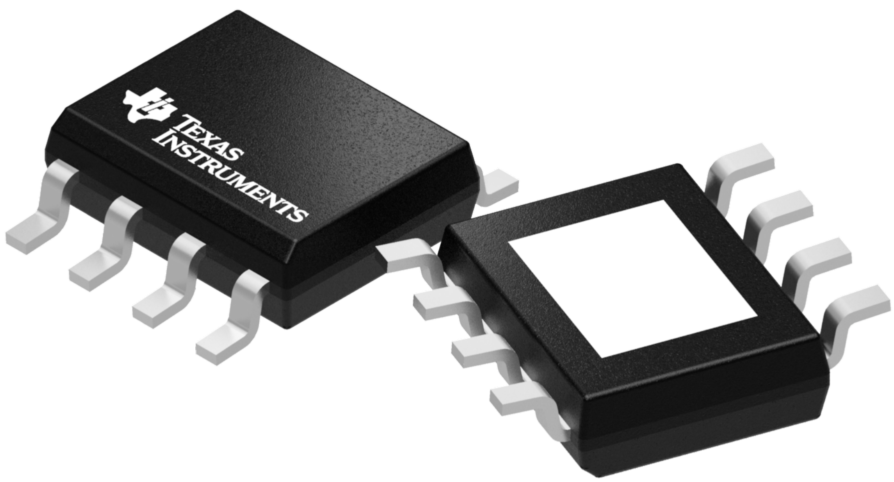



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS54328DDAR | SO PowerPAD | DDA | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TPS54328DRCR | VSON | DRC | 10 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS54328DRCT | VSON | DRC | 10 | 250 | 210.0 | 185.0 | 35.0 |

# DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

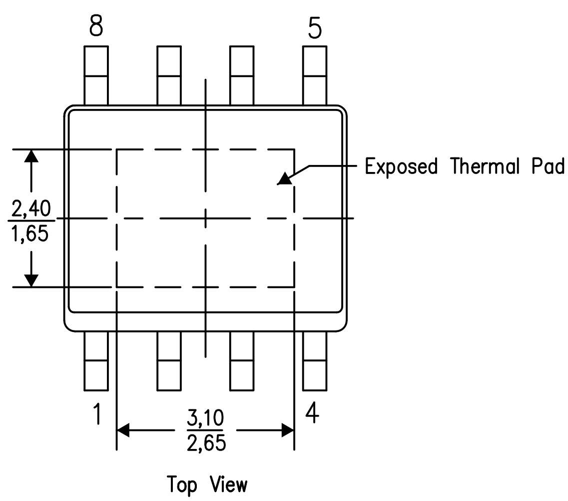
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

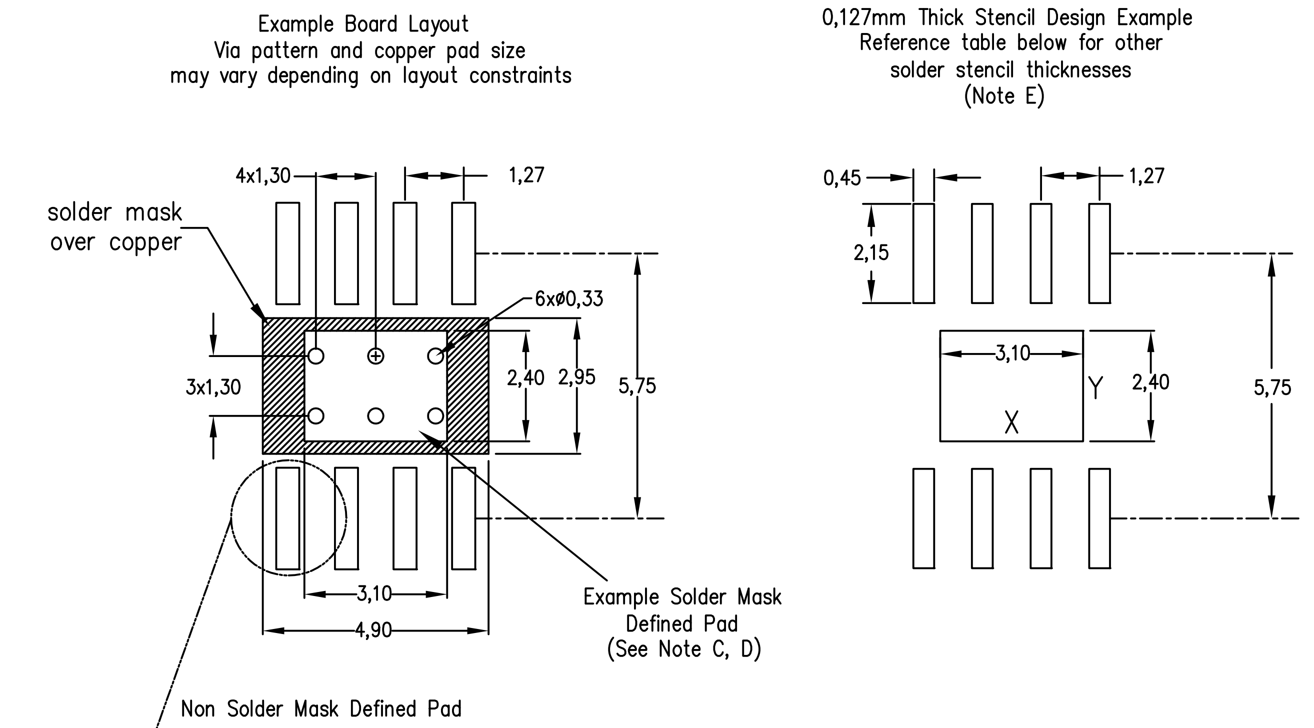


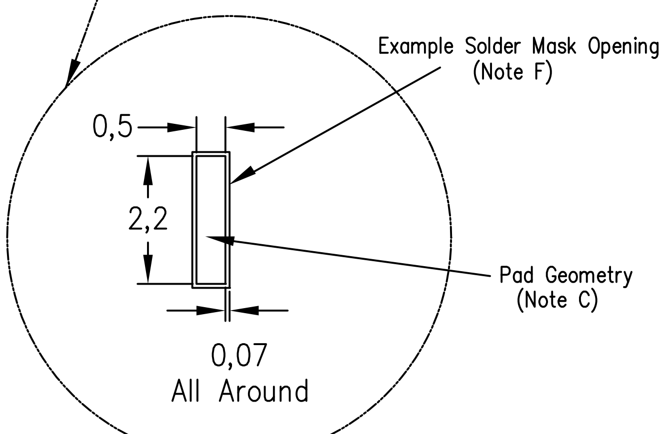

Exposed Thermal Pad Dimensions

4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

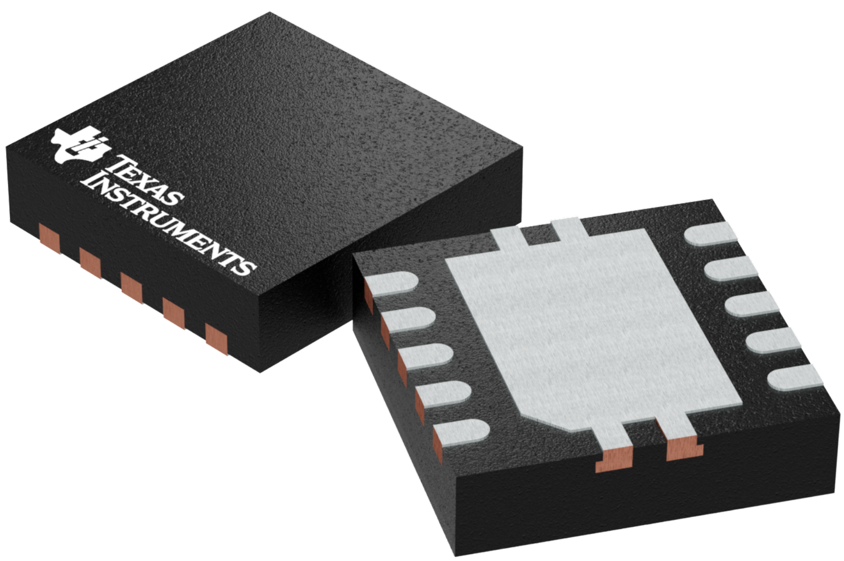


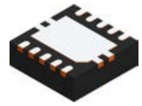

| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 3.3 | 2.6 |
| 0.127mm | 3.1 | 2.4 |
| 0.152mm | 2.9 | 2.2 |
| 0.178mm | 2.8 | 2.1 |

4208951–6/D 04/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



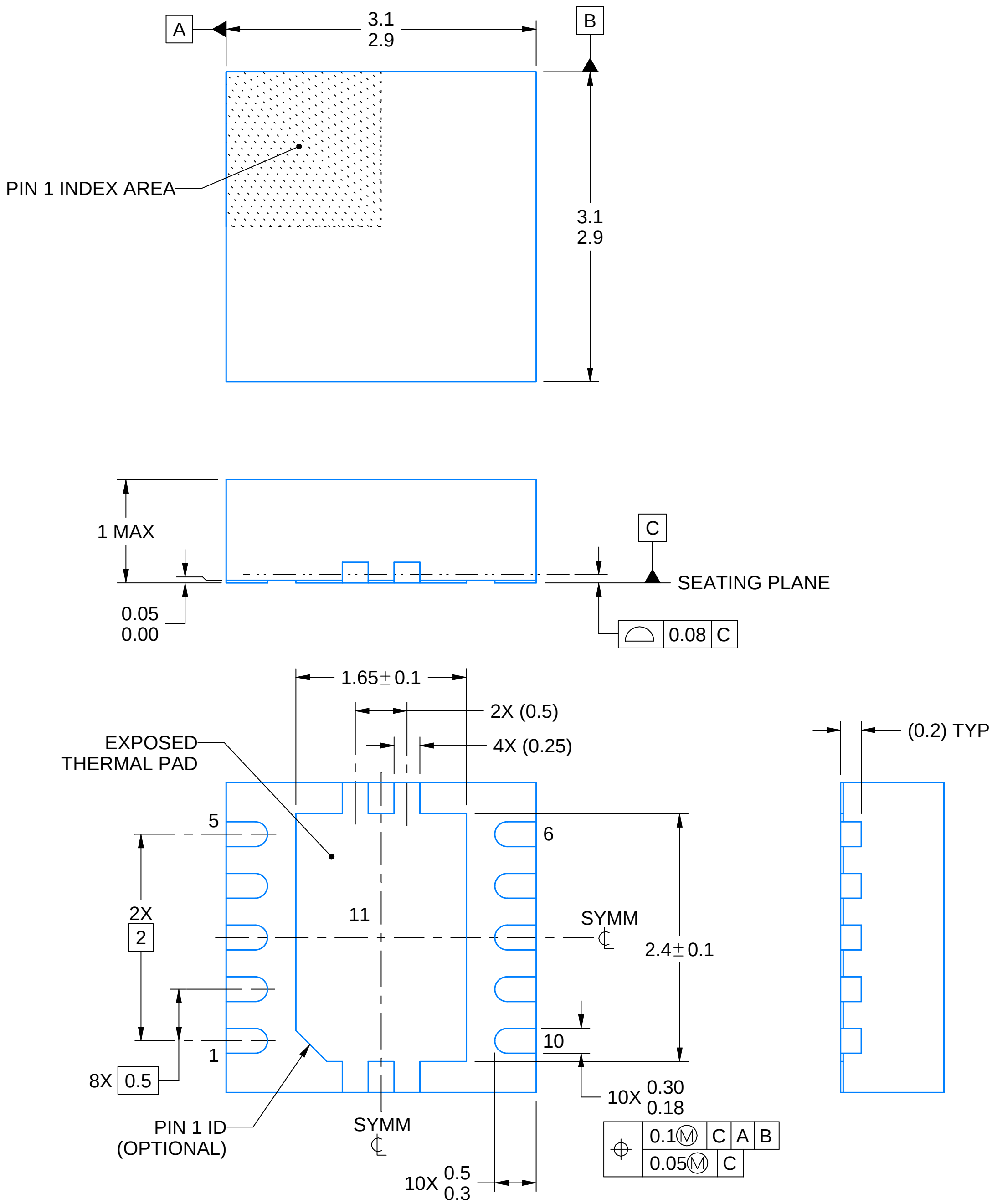
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



# PACKAGE OUTLINE

## VSON - 1 mm max height

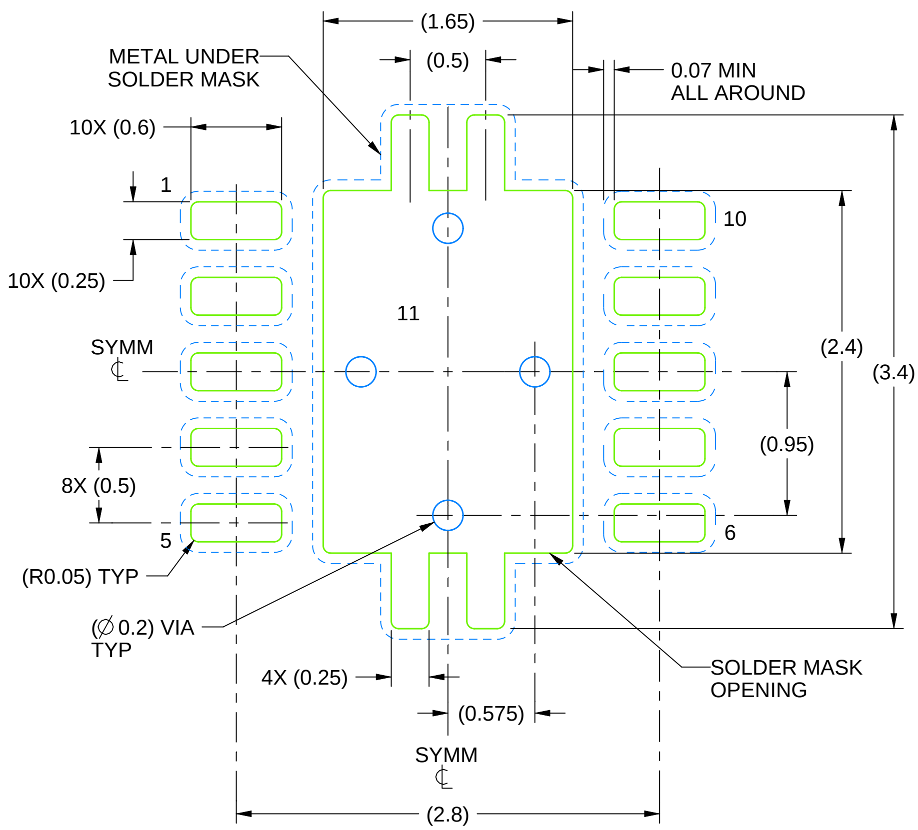
PLASTIC SMALL OUTLINE - NO LEAD




4218878/A 09/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

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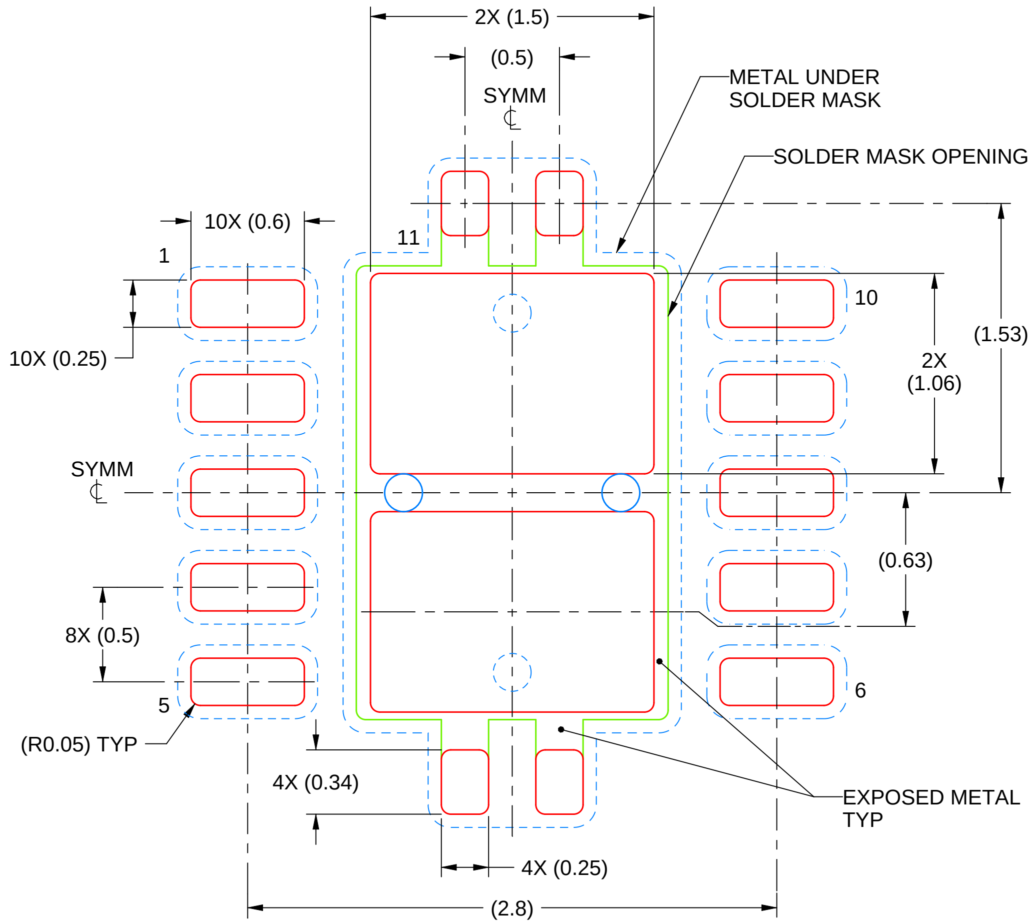
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/A 09/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# IMPORTANT NOTICE




Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265