AFBR-5972Z

Compact 650nm Transceiver with Compact Versatile-Link connector for Fast Ethernet over POF

Data Sheet

Description

The AFBR-5972Z Transceiver provides the system designer with the ability to implement Fast Ethernet (100 Mbps) over standard bandwidth 0.5±0.05 NA POF. It features a very compact design and has a form factor similar to the UTP connector. This transceiver features a new compact Versatile-Link duplex connector AFBR-4526Z and is compatible with existing simplex Versatile-Link connectors .

This product is lead free and compliant with RoHS.

Transmitter

The transmitter contains a 650nm LED with an integrated driver. The LED driver operates at 3.3 V. It receives a LVPECL/LVDS electrical input, and converts it into a modulated current driving the LED. The LED is packaged in an optical subassembly, part of the transmitter section. The optical subassembly couples the output optical power efficiently into POF fiber.

Receiver

The receiver utilizes a Si PIN photodiode. The PIN photodiode is packaged in an optical sub-assembly, part of the receiver section. This optical subassembly couples the optical power efficiently from POF fiber to the receiving PIN. The integrated IC operates at 3.3 V and converts the photocurrent into LVPECL electrical output.

Package

The transceiver package consists of three basic elements; two opto-electical subassemblies and the housing as illustrated in the block diagrams in Figure 1. The package outline drawing and pin-outs are shown in Figures 2 and 5.

Features

- Compatible to IEEE 802.3 100BASE-FX PMA using POF PMD
- Link lengths up to 50m POF (NA0.5) or 70m POF (NA0.3)
- Compact foot print
- 3.3V operation
- LVPECL input and output data connections
- LVPECL signal detect output
- Temperature range -40°C to 85°C

Applications

- Industrial Ethernet and Fast Ethernet over polymer optical fiber PMD
- Networking in harsh environments like factory automation or power generation and distribution
- Supporting various Ethernet Fieldbus protocols

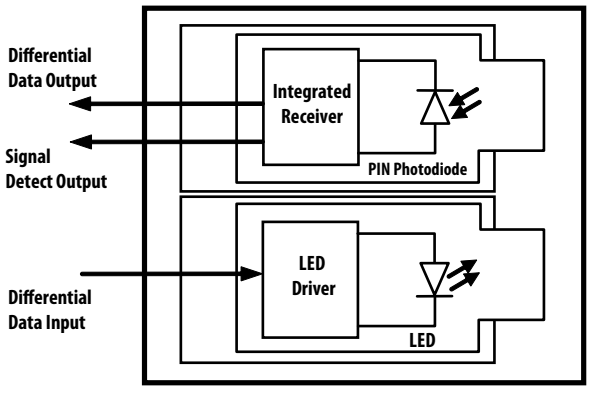
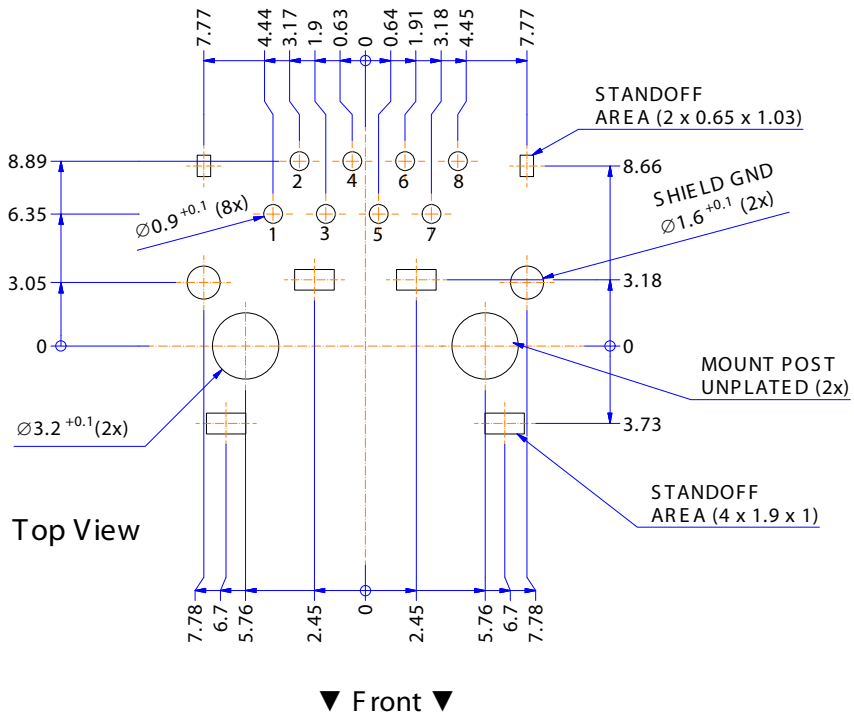


Figure 1. Block diagram.

Patent - www.avagotech.com/patents



NOTES:

1) Dimension: mm
2) General tolerance: ±0.05
3) Recommended PCB Thickness 1.57± 0.05
4) Pin description

PIN	FUNC
1	TD+
2	TD-
3	TxVcc
4	GND
5	RxVcc
6	SD
7	RD+
8	RD-

Figure 2. PCB footprint and Pin-out diagram.

The opto-electrical subassemblies utilize a high volume assembly process together with low cost lens elements which result in a cost effective building block. It consists of the active III-V devices, IC chips and various surface mounted passive components.

There are eight signal pins, four EMI shield solder posts and two mounting posts, which exit the bottom of the housing. The solder posts are isolated from the internal circuit of the transceiver and are to be connected to chassis ground. The mounting posts are to provide mechanical strength to hold the transceiver to the application board.

Pin Descriptions

Pin 1 TData+: transmitter data in. This input is a 3.3V LVPECL/LVDS compatible differential line.

Pin 2 TData-: transmitter data in negative. This input is a 3.3V LVPECL/LVDS compatible differential line.

Pin 3 TX Vcc: transmitter power supply pin. Provide +3.3 V DC via a transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the Tx Vcc pin.

Pin 4 GND: common ground pin. Directly connect this pin to the signal ground plane of the host board.

Pin 5 RX Vcc: receiver power supply pin. Provide +3.3 V DC via a receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the Rx Vcc pin

Pin 6. SD: signal detect pin. If an optical signal is present at the optical input, SD output is a logic "1". Absence of an optical input signal results in a logic "0" output. This pin can be used to drive a LVPECL input of an upstream circuit, such as Signal Detect input or Loss of Signal–bar.

Pin 7 RData+: receiver data out. This data line is a 3.3V LVPECL compatible differential line which should be properly terminated.

Pin 8 RData-: receiver data out negative. This data line is a 3.3V LVPECL compatible differential line which should be properly terminated. When SD is de-asserted, RData+ will be set to logic "0" and RData- will be set to logic "1".

Shield: This is to be connected to the equipment chassis ground.

Application circuit

The recommended application circuit is shown in figure 3.

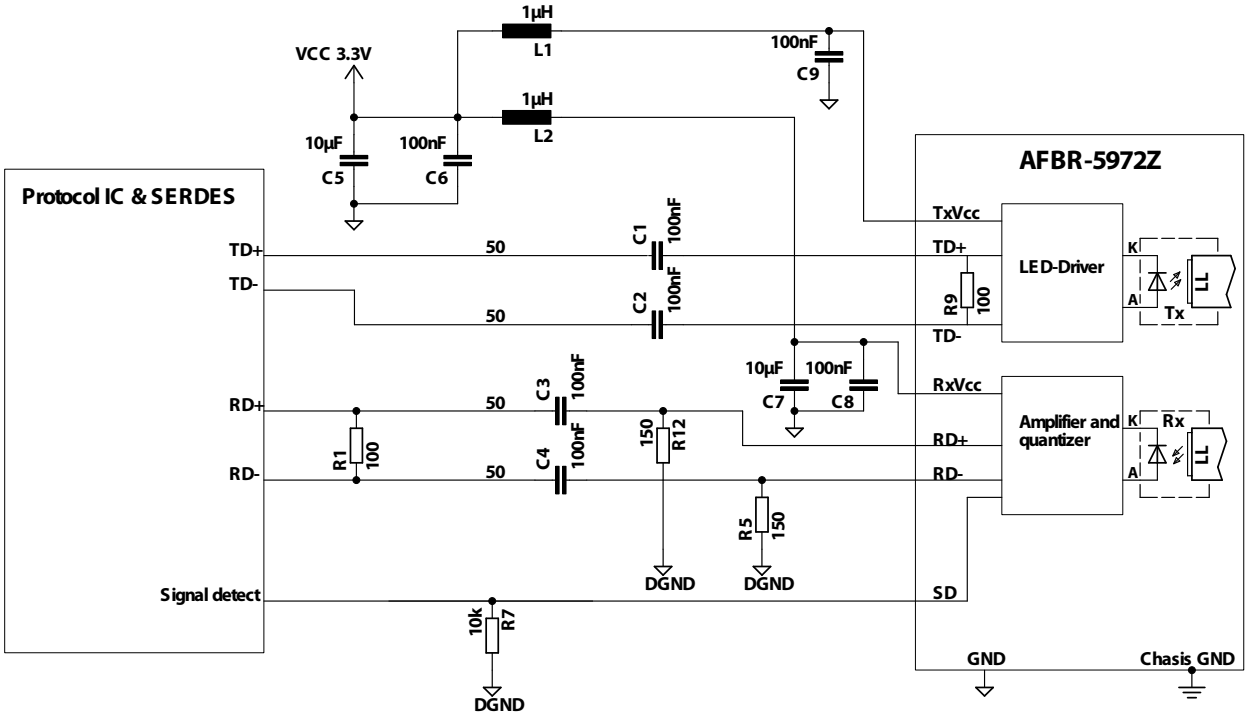


Figure 3. Recommended application circuit.

Board Layout – Decoupling Circuit and Ground Planes

It is important to take care of the layout of the application circuitry to achieve optimum performance of the transceiver. A power supply decoupling circuit is recommended to filter out noise, to assure optimal product performance. It is further recommended that a contiguous signal ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. It is also recommended that the shield posts be connected to the chassis ground to provide optimum EMI, ESD and EMS performance. This recommendation is in keeping with good high frequency board layout practices.

Regulatory compliance table

Feature	Test Method	Performance
Electrostatic discharge (ESD) to the electrical Pins	JESD22-A114	Withstands up to 2000V HBM applied between the electrical pins.
Immunity	Variation of IEC 61000-4-3	Typically shows no measurable effect from a 15V/m field swept from 8MHz to 1GHz applied to the transceiver when mounted on a circuit board without chassis enclosure.
Eye safety	EN 60825-1:52007	Laser class 1 product (LED radiation only). TÜV certificate: R 72102396. Caution – Use of controls or adjustments of performance or procedures other than those specified herein may result in hazardous radiation exposure.
Component recognition	Underwriter Laboratories	UL File #: E173874

Table 2. Transceiver diagnostics timing characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Time to initialize	t_init		5	ms	Note 1, figure 4
Hardware SD assert time	t_sd_on		100	µs	Note 2
Hardware SD de-assert time	t_sd_off		100	µs	Note 3

Notes:
1. Time from Power on to when the modulated optical output rises above 90% of nominal.
2. Time from valid optical signal to SD assertion.
3. Time from loss of optical signal to SD de-assertion.

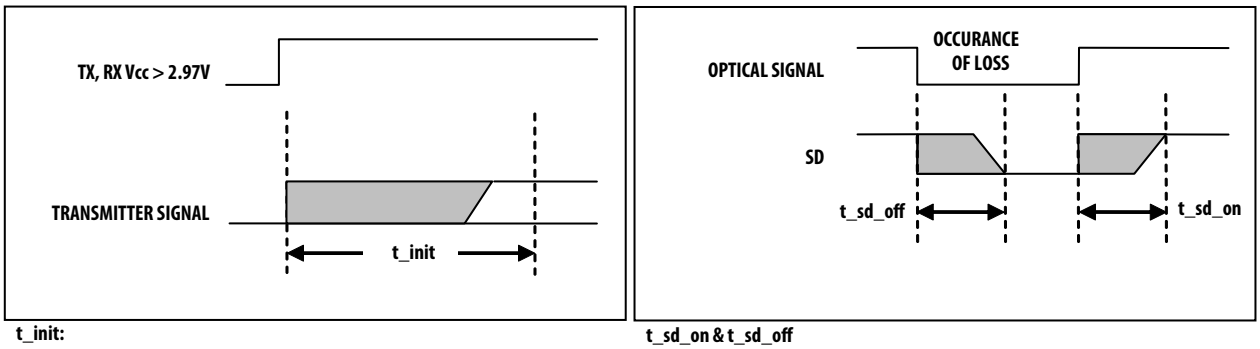


Figure 4. Transceiver timing diagrams

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation. all other parameters having values within the recommended operation conditions. It should not be assumed that limiting values of more than one parameter can be applied to the products at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T_S	-40	+100	°C	
Case Operating Temperature	T_C	-40	+85	°C	Note 4, 5
Lead Soldering Temperature	T_{sold}		260	°C	Note 6
Lead Soldering Time	t_{sold}		10	s	Note 6
Supply Voltage	V_{CC}	-0.5	4.0	V	
Data Input Voltage	V_I	-0.5	Vcc	V	
Differential Input Voltage	V_D		2.0	V	Peak to peak
Output Current LVPECL	I_{Dout}	-45	45	mA	

Notes:
4. Operating the product outside the maximum rated case operating temperature range will compromise its reliability and may damage the product.
5. The temperature is measured using a thermocouple connected to the hottest position of the housing.
6. The transceiver is Pb-free wave solderable.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Case Operating Temperature	T_C	-40		+85	°C	Note 1, 2
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Differential Input Voltage	V_D	0.22	0.8	1.6	V	Peak to peak
Input common mode voltage	V_{IN_CM}	GND+0.8		VCC-0.8	V	
Data and Signal Detect Output Load	R_L		50		Ω	
Signalling rate (Fast Ethernet)	B_{FE}		125		MBd	4B/5B. Note 3
Signalling rate (general)	B_G	10		125	MBd	Note 4

Notes:
1. The temperature is measured using a thermocouple connected to the housing.
2. Electrical and optical specifications of the product are guaranteed across recommended case operating temperature range only.
3. Ethernet auto-negotiation pulses are not supported.
4. Evaluation of 10MBd was performed using a biphase code.

Transceiver Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Current	I_{CC}		90	120	mA	Note 5
Power Dissipation	P_{DISS}	170	300	436	mW	Note 5
Power Supply Noise Reduction	P_{SNR}	50			mV	Peak to peak. Note 6

Notes
5. Characterized with LVPECL termination (82 Ohms to GND, 130 Ohms to V_{CC})
6. Fequencies from 0.1MHz to 100MHz.

Transmitter Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Average Launched Power (1mm POF. NA=0.5)	Po	-10	-6.5	-3.0	dBm	Note 7
Extinction ratio	EXT	10			dB	Note 7
Central Wavelength	λ_C	635	650	675	nm	Note 7
Spectral bandwidth RMS	λ_W			17	nm	
Optical Rise Time (10%-90%)	t_r		1.8	3.5	ns	Notes 7, 8
Optical Fall Time (90%-10%)	t_f		1.8	3.5	ns	Notes 7, 8
Duty Cycle Distortion Contributed by the Transmitter	DCD			1.0	ns	Note 7
Data dependent jitter	DDJ			0.6	ns	Note 7
Random Jitter Contributed by the Transmitter	RJ			0.76	ns	Peak to peak. Notes 7, 9
Overshoot	Ov		7	25	%	Note 7

Notes:
7. Measured at the end of 1 meter plastic optical fiber with a PRBS 2^7-1 sequence.
8. 10%...90% or 90%...10% respectively
9. Based on BER=$2.5x10^{-10}$

Receiver Electrical Characteristics

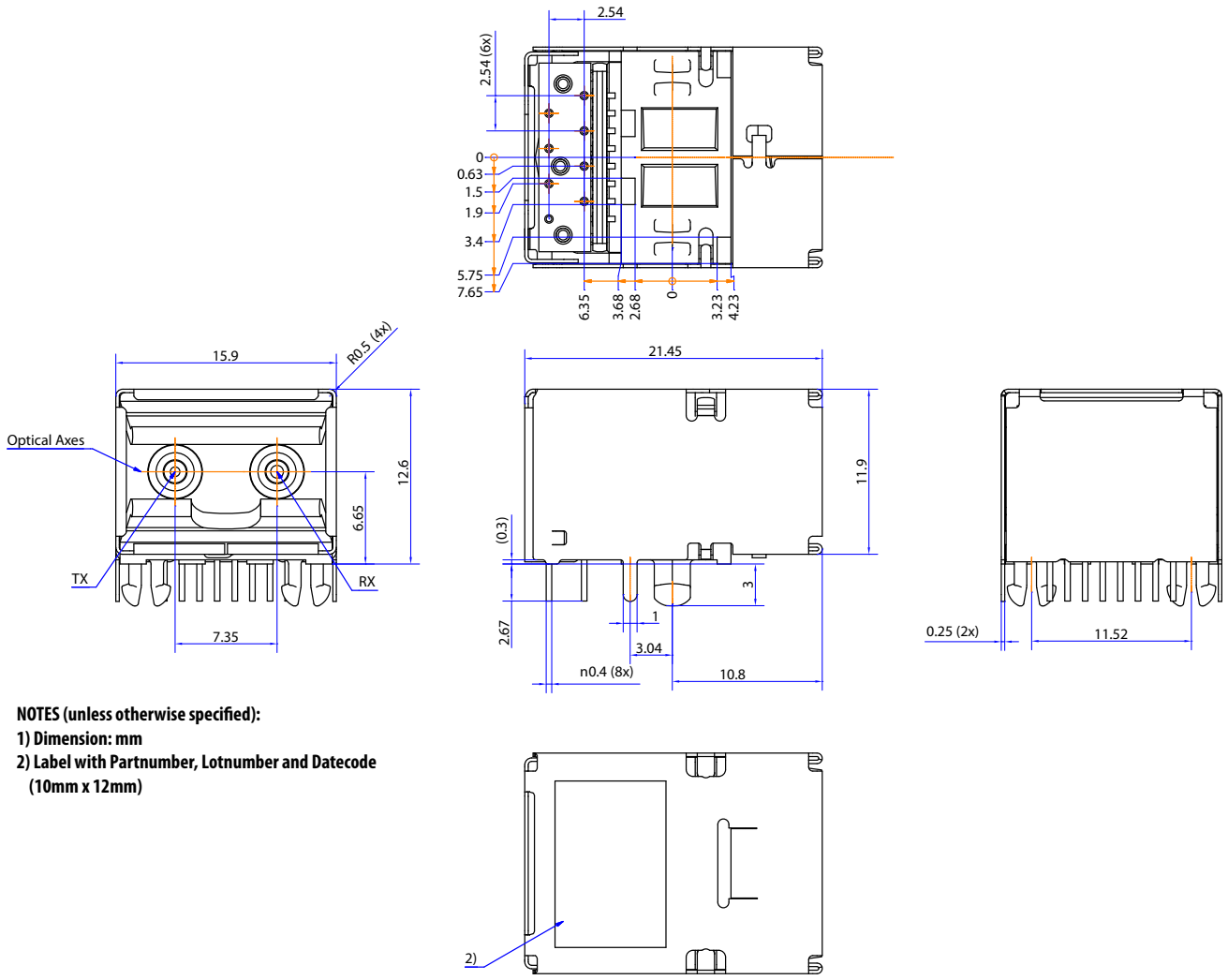
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Data Output Voltage - Low	V_{OL}-V_{CC}		-1.63		V	
Data Output Voltage - High	V_{OH}-V_{CC}		-0.99		V	
Data Output Voltage Swing	$\|V_{OH}-V_{OL}\|$	500		900	mV	Single ended
Data Output Rise Time (10%-90%)	t_r		2.8	3.0	ns	Note 1
Data Output Fall Time (90%-10%)	t_f		2.8	3.0	ns	Note 1
Duty Cycle Distortion	DCD			1.0	ns	
Data Dependent Jitter	DDJ			1.2	ns	Note 2
Random Jitter	RJ			2.14	ns	Peak to peak. Notes 2, 3
Signal Detect Output Voltage - Low	VOL-Vcc	-1.83	-1.75	-1.50	V	Terminations as shown in Fig. 3.
Signal Detect Output Voltage - High	VOH-Vcc	-1.16	-1.10	-0.88	V	Terminations as shown in Fig. 3.

Notes:
1. Characterized with LVPECL termination (82 Ohms to GND, 130 Ohms to V_{CC})
2. Contributed by Rx only.
3. Based on BER=$2.5x10^{-10}$

Receiver Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unstressed receiver sensitivity	CSEN	-26	-27		dBm	Note 4
Input Optical Power Maximum	PIN MAX			-3.0	dBm	Notes 4, 5
Central Wavelength	λ_C	635	650	675	nm	Notes 6
Spectral bandwidth RMS	λ_W			17	nm	Notes 6
Signal Detect Asserted	P_A		-29.5		dBm	
Signal Detect De-asserted	P_D		-31		dBm	
Signal Detect Hysteresis	P_A - P_D		1.0		dB	

Notes:
4. Average power. measured with a PRBS 2^7-1 sequence. BER < $2.5x10^{-10}$.
5. Input Optical Power Maximum is defined as the maximum optical average input power where the receiver duty cycle distortion reaches ±1 ns.
6. Measured at the end of 1 meter plastic optical fiber with a PRBS 2^7-1 sequence.



NOTES (unless otherwise specified):
1) Dimension: mm
2) Label with Partnumber, Lotnumber and Datecode (10mm x 12mm)

Figure 5. Package outline drawing

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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