REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Boilerplate update, part of 5 year review. ksr	06-08-30	Raymond Monnin

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

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REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A

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DRAWING APPROVAL DATE
88-09-23

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-88713**

SHEET 1 OF 11

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1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-88713	01	R	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	t_{PD}
01,05,09	C16L8	16-input 8-output AND-OR invert logic array	40,30,20 ns
02,06,10	C16R8	16-input 8-output registered AND-OR logic array	40,30,20 ns
03,07,11	C16R6	16-input 6-output registered AND-OR logic array	40,30,20 ns
04,08,12	C16R4	16-input 4-output registered AND-OR logic array	40,30,20 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20-lead	dual-in-line package
S	GDFP2-F20 or CDFP3-F20	20-lead	flat package
X	CQCC2-N20	20-terminal	square chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs in High Z	-0.5 V dc to +7.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
Output sink current	24 mA
Thermal resistance, junction-to-case (θ_{JC}):	See MIL-STD-1835
Maximum power dissipation (P_D) 1/	1.0 W
Maximum junction temperature (T_J)	+175°C
Lead temperature (soldering, 10 seconds maximum)	+260°C
Storage temperature range	-65°C to +150°C
Temperature under bias range	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
High-level input voltage (V_{IH})	2.0 V dc minimum
Low-level input voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.3), the devices shall be programmed by the manufacturer prior to test with a minimum of 50 percent of the total number of gates programmed or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.2.2 Programmed devices. The truth tables for programmed devices shall be as specified by an attached altered item drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{SS} = 0 V, I_{OH} = -2.0 mA, $V_{IN} = V_{IH}, V_{IL}$	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 12.0 mA, $V_{IN} = V_{IH}$ or V_{IL}	1, 2, 3	All		0.4	V
Input high voltage 2/	V_{IH}		1, 2, 3	All	2.0		V
Input low voltage 2/	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	V_{IN} = 5.5 V to GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V and GND	1, 2, 3	All	-100	100	µA
Output short circuit current 3/ 4/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V	1, 2, 3	All		-300	mA
Power supply current 5/	I_{CC}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = GND	1, 2, 3	All		70	mA
Input capacitance 4/	C_{IN}	V_{IN} = 0 V, V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz (see 4.3.1c)	4	All		7	pF
Output capacitance 4/	C_{OUT}		4	All		7	pF
Input or feedback to non-registered output	t_{PD}	V_{CC} = 5.5 V See figures 3 and 4	9, 10, 11	01, 03, 04		40	ns
				05, 07, 08		30	
				09, 11, 12		20	
Input to output enable	t_{EA}		9, 10, 11	01, 03, 04		40	ns
				05, 07, 08		30	
				09, 11, 12		20	
Input to output disable 4/ 6/	t_{ER}		9, 10, 11	01, 03, 04		40	ns
				05, 07, 08		30	
				09, 11, 12		20	
$\overline{OE}$ to output enable	t_{PZX}		9, 10, 11	02, 03, 04		25	ns
				06, 07, 08		25	
				10, 11, 12		20	
$\overline{OE}$ to output disable 4/ 6/	t_{PXZ}		9, 10, 11	02, 03, 04		25	ns
				06, 07, 08		25	
				10, 11, 12		20	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock to output 7/	t_{CO}	V_{CC} = 5.5 V See figures 3 and 4	9, 10, 11	02, 03, 04		25	ns
				06, 07, 08		20	
				10, 11, 12		15	
Input or feedback setup time 7/	t_{SU}		9, 10, 11	02, 03, 04	35		ns
				06, 07, 08	25		
				10, 11, 12	20		
Hold time 7/	t_H		9, 10, 11	02, 03, 04	0		ns
				06, 07, 08	0		
				10, 11, 12	0		
Clock period 4/ 7/	t_P		9, 10, 11	02, 03, 04	60		ns
				06, 07, 08	45		
				10, 11, 12	35		
Clock width 4/ 7/	t_W		9, 10, 11	02, 03, 04	25		ns
				06, 07, 08	20		
				10, 11, 12	12		
Maximum frequency 4/ 7/	f_{MAX}		9, 10, 11	02, 03, 04	16.5		MHz
				06, 07, 08	22		
				10, 11, 12	28.5		

1/ AC test are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 3, configuration A.

2/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

3/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed one second.

4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

5/ To calculate I_{CC} at any given operating frequency, use 70 mA + I_{CC}(AC), where I_{CC}(AC) = (0.6 mA/MHz) x (operating frequency in MHz).

6/ Transition is measured at steady state high level -500 mV or steady state low level +500 mV on the output from the 1.5 V level on the input and the output load on figure 3, configuration B.

7/ Test applies only to registered outputs.

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3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.10.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures and all input and output terminals tested.

d. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of Group A, subgroups 9, 10, and 11.

(1) A sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturers option, the sample may be increased to 24 total devices with no more than four total device failures allowable.

(2) Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) TA = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. For quality conformance inspection, the programmability sample (see 4.3.1d) shall be included in subgroup 1 test.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

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Device types	01,05,09	02,06,10	03,07,11	04,08,12
Case outlines	R, S, X	R, S, X	R, S, X	R, S, X
Terminal number	Terminal symbol			
1	I_0	CP	CP	CP
2	I_1	I_0	I_0	I_0
3	I_2	I_1	I_1	I_1
4	I_3	I_2	I_2	I_2
5	I_4	I_3	I_3	I_3
6	I_5	I_4	I_4	I_4
7	I_6	I_5	I_5	I_5
8	I_7	I_6	I_6	I_6
9	I_8	I_7	I_7	I_7
10	V_{SS}	V_{SS}	V_{SS}	V_{SS}
11	I_9	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
12	O_0	O_0	I/O_0	I/O_0
13	I/O_1	O_1	O_1	I/O_1
14	I/O_2	O_2	O_2	O_2
15	I/O_3	O_3	O_3	O_3
16	I/O_4	O_4	O_4	O_4
17	I/O_5	O_5	O_5	O_5
18	I/O_6	O_6	O_6	I/O_6
19	O_7	O_7	I/O_7	I/O_7
20	V_{CC}	V_{CC}	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

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Device types 01, 05, and 09

Inputs										Outputs							
I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	O_0
X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z

Device types 02, 06, and 10

Inputs										Outputs							
CP	$\overline{OE}$	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
X	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
X	L	X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H

Device types 03, 07, and 11

Inputs										Outputs							
CP	$\overline{OE}$	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	I/O_7	O_6	O_5	O_4	O_3	O_2	O_1	I/O_0
X	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
X	L	X	X	X	X	X	X	X	X	Z	H	H	H	H	H	H	Z

Device types 04, 08, and 12

Inputs										Outputs							
CP	$\overline{OE}$	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	I/O_7	I/O_6	O_5	O_4	O_3	O_2	I/O_1	I/O_0
X	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
X	L	X	X	X	X	X	X	X	X	Z	Z	H	H	H	H	Z	Z

NOTES:
1. Z = Three state
2. X = Don't care

FIGURE 2. Truth tables (unprogrammed).

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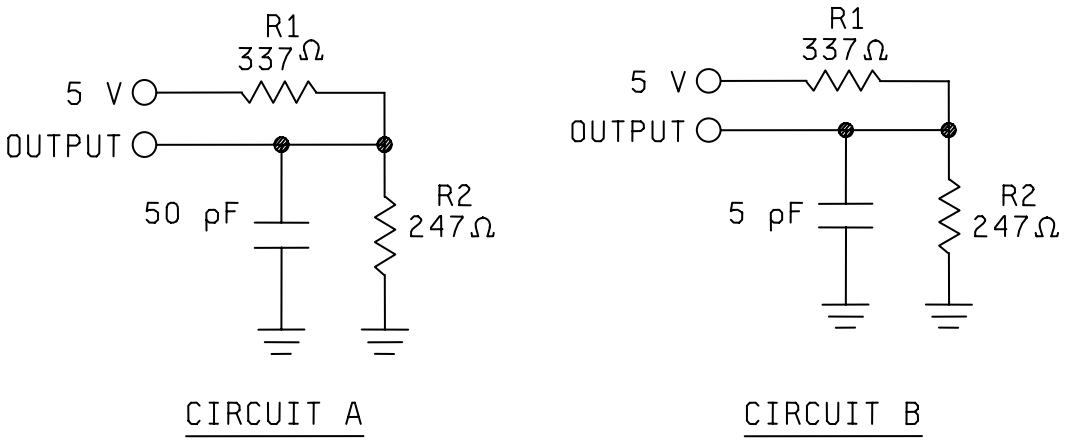

FIGURE 3. Output load circuit.

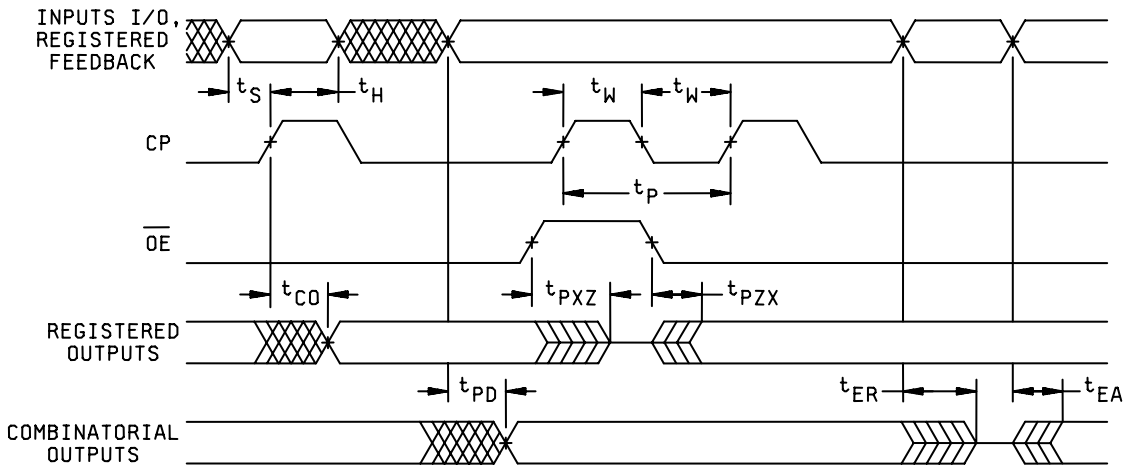

FIGURE 4. Switching waveforms.

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TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8A, 8B
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8A, 8B, 9
Group A test requirements (method 5005)	1,2,3,4**,7,8A,8B, 9, 10,11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8

1/ * indicates PDA applies to subgroups 1 and 7.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ ** see 4.3.1c.

4/ Subgroups 7 and 8 shall consist of verifying the data pattern.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-08-30

Approved sources of supply for SMD 5962-88713 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8871301RA	0C7V7	PALC16L8-40DMB
5962-8871301SA	0C7V7	PALC16L8-40KMB
5962-8871301XA	0C7V7	PALC16L8-40LMB
5962-8871302RA	0C7V7	PALC16R8-40DMB
5962-8871302SA	0C7V7	PALC16R8-40KMB
5962-8871302XA	0C7V7	PALC16R8-40LMB
5962-8871303RA	0C7V7	PALC16R6-40DMB
5962-8871303SA	0C7V7	PALC16R6-40KMB
5962-8871303XA	0C7V7	PALC16R6-40LMB
5962-8871304RA	3/	PALC16R4-40DMB
5962-8871304SA	3/	PALC16R4-40KMB
5962-8871304XA	3/	PALC16R4-40LMB
5962-8871305RA	0C7V7	PALC16L8-30DMB
5962-8871305SA	0C7V7	PALC16L8-30KMB
5962-8871305XA	0C7V7	PALC16L8-30LMB
5962-8871306RA	0C7V7	PALC16R8-30DMB
5962-8871306SA	0C7V7	PALC16R8-30KMB
5962-8871306XA	0C7V7	PALC16R8-30LMB
5962-8871307RA	0C7V7	PALC16R6-30DMB
5962-8871307SA	0C7V7	PALC16R6-30KMB
5962-8871307XA	0C7V7	PALC16R6-30LMB
5962-8871308RA	3/	PALC16R4-30DMB
5962-8871308SA	3/	PALC16R4-30KMB
5962-8871308XA	3/	PALC16R4-30LMB

See footnotes at end of table.

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Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8871309RA	0C7V7	PALC16L8-20DMB
5962-8871309SA	0C7V7	PALC16L8-20KMB
5962-8871309XA	0C7V7	PALC16L8-20LMB
5962-8871310RA	0C7V7	PALC16R8-20DMB
5962-8871310SA	0C7V7	PALC16R8-20KMB
5962-8871310XA	0C7V7	PALC16R8-20LMB
5962-8871311RA	0C7V7	PALC16R6-20DMB
5962-8871311SA	0C7V7	PALC16R6-20KMB
5962-8871311XA	0C7V7	PALC16R6-20LMB
5962-8871312RA	3/	PALC16R4-20DMB
5962-8871312SA	3/	PALC16R4-20KMB
5962-8871312XA	3/	PALC16R4-20LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

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