Operational Amplifier, Railto-Rail Output, 3 MHz BW

The NCx2007x series operational amplifiers provide rail–to–rail output operation, 3 MHz bandwidth, and are available in single, dual, and quad configurations. Rail–to–rail operation enables the user to make optimal use of the entire supply voltage range while taking advantage of 3 MHz bandwidth. The NCx2007x can operate on supply voltages as low as 2.7 V over the temperature range of –40°C to 125° C. At a 2.7 V supply, the high bandwidth provides a slew rate of 2.8 V/µs while only consuming 405 µA of quiescent current per channel. The wide supply range allows the NCx2007x to run on supply voltages as high as 36 V, making it ideal for a broad range of applications. Since this is a CMOS device, high input impedance and low bias currents make it ideal for interfacing to a wide variety of signal sensors. The NCx2007x devices are available in a variety of compact packages. Automotive qualified options are available under the NCV prefix.

Features

- Rail-To-Rail Output
- Wide Supply Range: 2.7 V to 36 V
- Wide Bandwidth: 3 MHz typical at $V_S = 2.7 \text{ V}$
- High Slew Rate: 2.8 V/ μ s typical at V_S = 2.7 V
- Low Supply Current: 405 μA per channel at $V_S = 2.7 \ V$
- Low Input Bias Current: 5 pA typical
- Wide Temperature Range: -40°C to 125°C
- Available in a variety of packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Current Sensing
- Signal Conditioning
- Automotive

End Products

- Notebook Computers
- Portable Instruments
- Power Supplies



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SOT-553 CASE 463B TSOP-5 CASE 483





Micro8[™] CASE 846A SOIC-8 CASE 751





TSSOP-8 CASE 948S

TSSOP-14 CASE 948G



SOIC-14 NB CASE 751A

DEVICE MARKING INFORMATION

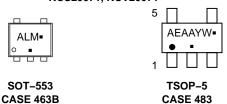
See general marking information in the device marking section on page 2 of this data sheet.

ORDERING INFORMATION

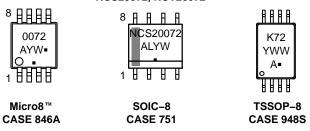
See detailed ordering and shipping information on page 4 of this data sheet.

MARKING DIAGRAMS

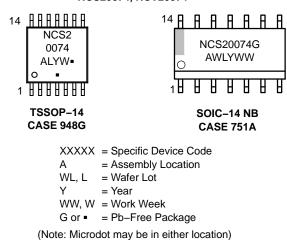
Single Channel Configuration NCS20071, NCV20071



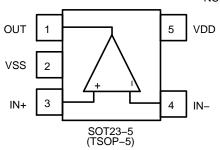
Dual Channel Configuration NCS20072, NCV20072

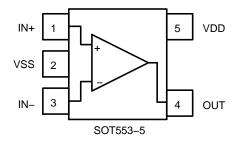


Quad Channel Configuration NCS20074, NCV20074

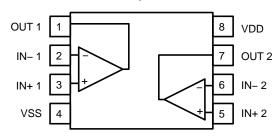


Single Channel Configuration NCS20071, NCV20071





Dual Channel Configuration NCS20072, NCV20072



Quadruple Channel Configuration NCS20074, NCV20074

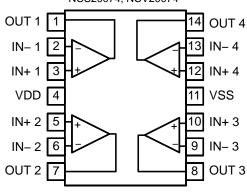


Figure 1. Pin Connections

ORDERING INFORMATION

Device	Configuration	Automotive	Marking	Package	Shipping [†]
NCS20071SN2T1G		No	AEA	TSOP-5 (Pb-Free)	3000 / Tape and Reel
NCS20071XV53T2G	Single	INO	AL	SOT553-5 (Pb-Free)	4000 / Tape and Reel
NCV20071SN2T1G*	Single	Va a	AEA	TSOP-5 (Pb-Free)	3000 / Tape and Reel
NCV20071XV53T2G*		Yes	AL	SOT553-5 (Pb-Free)	4000 / Tape and Reel
NCS20072DMR2G			0072	Micro8 (MSOP8) (Pb-Free)	4000 / Tape and Reel
NCS20072DR2G		No	NCS20072	SOIC-8 (Pb-Free)	2500 / Tape and Reel
NCS20072DTBR2G	Post		K72	TSSOP-8 (Pb-Free)	2500 / Tape and Reel
NCV20072DMR2G*	Dual			0072	Micro8 (MSOP8) (Pb-Free)
NCV20072DR2G*]	Yes	NCS20072	SOIC-8 (Pb-Free)	2500 / Tape and Reel
NCV20072DTBR2G*			K72	TSSOP-8 (Pb-Free)	2500 / Tape and Reel
NCS20074DR2G		N	NCS20074	SOIC-14 (Pb-Free)	2500 / Tape and Reel
NCS20074DTBR2G	Outed	No	NCS2 0074	TSSOP-14 (Pb-Free)	2500 / Tape and Reel
NCV20074DR2G*	Quad	Vo.	NCS20074	SOIC-14 (Pb-Free)	2500 / Tape and Reel
NCV20074DTBR2G*		Yes	NCS2 0074	TSSOP-14 (Pb-Free)	2500 / Tape and Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP

Capable.

ABSOLUTE MAXIMUM RATINGS (Note 1)

	Rating	Symbol	Limit	Unit	
Supply Voltage (V _{DD} – V _{SS}) (Note 4)	V _S	40	V	
Input Voltage		V _{CM}	$V_{SS} - 0.2$ to $V_{DD} + 0.2$	V	
Differential Input Voltage (N	lote 2)	V_{ID}	±V _s	V	
Maximum Input Current		I _{IN}	±10	mA	
Maximum Output Current (Note 3)	I _O	±100		
Continuous Total Power Dis	s Total Power Dissipation (Note 4) P _D 200				
Maximum Junction Temper	ature	T_J	150		
Storage Temperature Rang	e	T _{STG}	-65 to 150	°C	
Mounting Temperature (Infr	rared or Convection – 20 sec)	T _{mount}	260	°C	
ESD Capability (Note 5)	Human Body Model Machine Model – NCx20071 Machine Model – NCx20072, NCx20074 Charged Device Model – NCx20071, NCx20072 Charged Device Model – NCx20074	HBM MM MM CDM CDM	2000 200 150 2000 (C6) 1000 (C6)	V	
Latch-Up Current (Note 6)		I _{LU}	100	mA	
Moisture Sensitivity Level (Note 7)	MSL	Level 1		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
- 2. Maximum input current must be limited to ±10 mA. Series connected resistors of at least 500 Ω on both inputs may be used to limit the maximum input current to ±10 mA.
- 3. Total power dissipation must be limited to prevent the junction temperature from exceeding the 150°C limit.
- 4. Continuous short circuit operation to ground at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of the maximum output current rating over the long term may adversely affect reliability. Shorting output to either VDD or VSS will adversely affect reliability.
- 5. This device series incorporates ESD protection and is tested by the following methods:
 - ESD Human Body Model tested per JEDEC standard JS-001 (AEC-Q100-002)
 - ESD Machine Model tested per JEDEC standard JESD22-A115 (AEC-Q100-003)
 - ESD Charged Device Model tested per JEDEC standard JESD22-C101 (AEC-Q100-011)
- 6. Latch-up Current tested per JEDEC standard JESD78 (AEC-Q100-004)
- 7. Moisture Sensitivity Level tested per IPC/JEDEC standard J-STD-020A

THERMAL INFORMATION

Parameter	Symbol	Package	Single Layer Board (Note 8)	Multi–Layer Board (Note 9)	Unit	
		SOT23-5 / TSOP5	265	195		
		SOT553-5	325	244		
	$\theta_{\sf JA}$	Micro8 / MSOP8	236	167		
Junction-to-Ambient		SOIC-8	190	131	°C/W	
		TSSOP-8	253	194	1	
		SOIC-14	142	101		
		TSSOP-14	179	128	1	

- 8. Values based on a 1S standard PCB according to JEDEC51-3 with 1.0 oz copper and a 300 mm² copper area
- 9. Values based on a 1S2P standard PCB according to JEDEC51-7 with 1.0 oz copper and a 100 mm² copper area

OPERATING RANGES

Parameter	Symbol	Min	Max	Unit
Operating Supply Voltage (Single Supply)	Vs	2.7	36	V
Operating Supply Voltage (Split Supply)	Vs	±1.35	±18	V
Differential Input Voltage (Note 10)	V_{ID}		V _S	V
Input Common Mode Voltage Range	V _{CM}	V _{SS}	V _{DD} – 1.35	V
Ambient Temperature	T _A	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

10. Maximum input current must be limited to ± 10 mA. See Absolute Maximum Ratings for more information.

ELECTRICAL CHARACTERISTICS AT V_S = 2.7 V

 $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid}$ -supply unless otherwise noted. All limits are guaranteed by testing or statistical analysis. **Boldface** limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 11, 12)

Parameter	Symbol	Cond	itions	Min	Тур	Max	Unit
INPUT CHARACTERISTICS							
		NO	20074		1.3	±3.5	
	.,	NCX2	20071			±4.5	1 .,
Input Offset Voltage	V _{OS}	NC-20070	NC-20074		1.3	±3	mV
		NCX20072	, NCx20074			±4	
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$T_A = 25^{\circ}C$ to $125^{\circ}C$			2		μV/°C
Input Bias Current (Note 12)	1				5	200	рA
input bias current (Note 12)	I _{IB}					1500	PΑ
		NCv20071	, NCx20072		2	75	_
Input Offset Current (Note 12)	laa	NCX20071	, NCX20072			500	- Δ
input Onset Current (Note 12)	los	NCv	20074		2	75	pА
		NCx20074				200	
Channel Separation	XTLK	DC	NCx20072		100		dB
Спаппет Зераганоп	AILK	NCx20074			115		uВ
Differential Input Resistance	R _{ID}				5		GΩ
Common Mode Input Resistance	R _{IN}				5		GΩ
Differential Input Capacitance	C _{ID}				1.5		pF
Common Mode Input Capacitance	C _{CM}				3.5		pF
Common Mode Rejection Ratio	CMRR	Va. = Vaa + 0.2	V to V _{DD} – 1.35 V	90	110		dB
Common wode rejection ratio	CIVILLIA	VCM - VSS + 0.2	V 10 VDD - 1.33 V	69			UD
OUTPUT CHARACTERISTICS							
Open Loop Voltage Gain	Δ			96	118		dB
Open Loop voltage Gain	A _{VOL}			86			uВ
Output Current Capability (Note 13)	la la	Op amp sin	king current		70		mA
Output Current Capability (Note 13)	I _O	Op amp sou	rcing current		50		IIIA
Output Voltage High	V _{OH}	Voltage output swii	ng from positive rail		0.006	0.15	V
Output voltage riigii	VOH	voltage output swit	ng nom positive rail			0.22	V
Output Voltage Low	V _{OL}	Voltage output swir	ng from negative rail		0.005	0.15	V
Output voltage Low	VOL	voltage output swii	ig iroin negative raii			0.22	V
AC CHARACTERISTICS							
Unity Gain Bandwidth	UGBW	C _L =	25 pF		3		MHz
Slew Rate at Unity Gain	SR	$C_L = 20 pF$	$R_L = 2 k\Omega$		2.8		V/μs
Phase Margin	ϕ_{m}	C _L =	25 pF		50		٥
Gain Margin	A _m	C _L =	25 pF		14		dB
Settling Time	to	V _O = 1 Vpp,	Settling time to 0.1%		0.6		li e
County Time	t _S Ga	Gain = 1, C _L = 20 pF Settling time to 0.0			1.2		μS

- 11. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
- 12. Performance guaranteed over the indicated operating temperature range by design and/or characterization.
- 13. Power dissipation must be limited to prevent junction temperature from exceeding 150°C. See Absolute Maximum Ratings for more information.

ELECTRICAL CHARACTERISTICS AT V_S = 2.7 V

 $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid}$ –supply unless otherwise noted. All limits are guaranteed by testing or statistical analysis. **Boldface** limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 11, 12)

Parameter	Symbol	Cond	itions	Min	Тур	Max	Unit
NOISE CHARACTERISTICS							
Total Harmonic Distortion plus Noise	THD+N	V _{IN} = 0.5 Vpp, f		0.05		%	
Inner Deferred Valters Naise	_	f = 1	kHz		30		5\//s\ U=
Input Referred Voltage Noise	e _n	f = 10 kHz			20		- nV/√ Hz
Input Referred Current Noise	i _n	f = 1 kHz			90		fA/√ Hz
SUPPLY CHARACTERISTICS							
Davisa Comple Daiostica Datia	DCDD	No Load		114	135		-ID
Power Supply Rejection Ratio	PSRR	NO L	-oad	100			dB
		NC20074	Noteed		420	625	
D		NCx20071	No load			765	
Power Supply Quiescent Current	I _{DD}		Dan dia sanda a dan d		405	525	μΑ
		NCx20072, NCx20074 Per channel, no load				625	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- 11. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
- 12. Performance guaranteed over the indicated operating temperature range by design and/or characterization.
- 13. Power dissipation must be limited to prevent junction temperature from exceeding 150°C. See Absolute Maximum Ratings for more information.

ELECTRICAL CHARACTERISTICS AT V_S = 5 V

 $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid-supply}$ unless otherwise noted. All limits are guaranteed by testing or statistical analysis. **Boldface** limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 14, 15)

Parameter	Symbol	C	Conditions	Min	Тур	Max	Unit
INPUT CHARACTERISTICS							-
			10.00074		1.3	±3.5	
Inner to Office to Voltage		ı	NCx20071			±4.5	m)/
Input Offset Voltage	Vos	NO00	0070 NO.00074		1.3	±3	mV
		NCx20072, NCx20074				±4	
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$T_A = 1$	25°C to 125 °C		2		μV/°C
Innut Diag Compat (Nata 45)					5	200	^
Input Bias Current (Note 15)	I _{IB}					1500	pА
		NCx20071, NCx20072			2	75	- n^
land Offeet Comment (Nate 45)	1 . 1					500	
Input Offset Current (Note 15)	los		10.00074		2	75	- pA
		'	NCx20074			200	
0, 10,	VTIL		NCx20072		100		
Channel Separation	XTLK	DC	NCx20074		115		dB
Differential Input Resistance	R _{ID}		•		5		GΩ
Common Mode Input Resistance	R _{IN}				5		GΩ
Differential Input Capacitance	C _{ID}				1.5		pF
Common Mode Input Capacitance	C _{CM}				3.5		pF

- 14. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
- 15. Performance guaranteed over the indicated operating temperature range by design and/or characterization.
- 16. Power dissipation must be limited to prevent junction temperature from exceeding 150°C. See Absolute Maximum Ratings for more information.

ELECTRICAL CHARACTERISTICS AT $V_S = 5 \text{ V}$

 $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid}$ -supply unless otherwise noted. All limits are guaranteed by testing or statistical analysis. **Boldface** limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 14, 15)

Parameter	Symbol	Cond	itions	Min	Тур	Max	Unit
INPUT CHARACTERISTICS	•,	1			-71		
				102	125		
Common Mode Rejection Ratio	CMRR	$V_{CM} = V_{SS} + 0.2$	V to V _{DD} – 1.35 V	80	0		dB
OUTPUT CHARACTERISTICS		l					
				96	120		
Open Loop Voltage Gain	A_{VOL}			86			dB
		Op amp sin	king current		50		
Output Current Capability (Note 16)	I _O	Op amp sou	rcing current		60		mA
0	.,,				0.013	0.20	.,
Output Voltage High	V _{OH}	Voltage output swing from positive rail				0.25	_ V
Output Valta as I am	V	Valta and acceptant accept	a fue as a section well		0.01	0.10	
Output Voltage Low	V_{OL}	voltage output swir	ng from negative rail			0.15	V
AC CHARACTERISTICS							
Unity Gain Bandwidth	UGBW	C _L = 25 pF			3		MHz
Slew Rate at Unity Gain	SR	$C_{L} = 20 \text{ pF}$	$R_L = 2 k\Omega$		2.7		V/μs
Phase Margin	ϕ_{m}	C _L =	25 pF		50		0
Gain Margin	A_{m}	C _L =	25 pF		14		dB
Settling Time	4	$V_O = 3 \text{ Vpp},$ Gain = 1, $C_L = 20 \text{ pF}$	Settling time to 0.1%		1.2		0
Settling Time	t _S	Gain = 1, $C_L = 20 \text{ pF}$	Settling time to 0.01%		5.6		μS
NOISE CHARACTERISTICS							
Total Harmonic Distortion plus Noise	THD+N	V _{IN} = 2.5 Vpp, f	= 1 kHz, Av = 1		0.009		%
Input Referred Voltage Noice	0	f = 1	kHz		30		nV/√ Hz
Input Referred Voltage Noise	e _n	f = 10) kHz		20		TIV/ V⊓Z
Input Referred Current Noise	i _n	f = 1	kHz		90		fA/√Hz
SUPPLY CHARACTERISTICS							
Dower Cumply Dejection Datio	PSRR	No.1	and	114	135		dB
Power Supply Rejection Ratio	PSKK	No Load		100			uБ
	_	NCv20071	No load		430	635	
Power Supply Ouiocoopt Current		NCx20071	เพษายลน			775	μΑ
Power Supply Quiescent Current		NCv20072 NCv20074	Per channel, no load		410	530	μΑ
		NCx20072, NCx20074 Per channel, no load				630	1

^{14.} Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

^{15.} Performance guaranteed over the indicated operating temperature range by design and/or characterization.

^{16.} Power dissipation must be limited to prevent junction temperature from exceeding 150°C. See Absolute Maximum Ratings for more information.

ELECTRICAL CHARACTERISTICS AT $V_S = 10 \text{ V}$

 $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid-supply}$ unless otherwise noted. All limits are guaranteed by testing or statistical analysis. Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 17, 18)

Parameter	Symbol	Cond	litions	Min	Тур	Max	Unit
INPUT CHARACTERISTICS							
lanut Offact Valtage	\ <i>\</i>	NOve	20074		1.3	±3.5	mV
Input Offset Voltage	V _{OS}	NCX2	20071			±4.5	mV
Input Offset Voltage	V	NCv20072	NCv20074		1.3	±3	mV
Input Offset Voltage	V _{OS}	NCX20072	, NCx20074			±4	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	T _A = 25°C	C to 125°C		2		μV/°C
Input Bias Current (Note 18)	I _{IB}				5	200	pА
input Blue Current (Note 10)	'IВ					1500	ρ/\
		NCv20071	, NCx20072		2	75	_
Input Offset Current (Note 18)	loo	NCX20071	, 110,20072			500	nΔ
input Offset Current (Note 18)	los	NCv	NCx20074		2	75	p A
		NOX	20074			200	
Channel Separation	XTLK	DC	NCx20072		100		dB
Charmer Separation	XILK	NCx20074			115		uВ
Differential Input Resistance	R _{ID}				5		GΩ
Common Mode Input Resistance	R _{IN}				5		GΩ
Differential Input Capacitance	C_{ID}				1.5		pF
Common Mode Input Capacitance	C _{CM}				3.5		pF
Common Mode Rejection Ratio	CMRR	VV102	V to V _{DD} – 1.35 V	110	130		dB
Common wode Rejection Ratio	CIVIKK	V _{CM} = V _{SS} + 0.2	v to v _{DD} = 1.33 v	87			
OUTPUT CHARACTERISTICS							
Open Loop Voltage Gain	۸			98	120		dB
Open Loop voltage Gain	A _{VOL}			88			αБ
Output Current Capability (Note 10)	I-	Op amp sin	king current		50		mΛ
Output Current Capability (Note 19)	lo	Op amp sou	rcing current		65		mA
Output Voltage High	V	Voltage output awii	ng from positivo roil		0.023	0.08	V
Output Voltage High	V _{OH}	voltage output swii	ng from positive rail			0.10	V
Output Voltage Low	V	Voltage output owir	og from pogotivo roil		0.022	0.3	V
Output voltage Low	V _{OL}	voltage output swii	ng from negative rail			0.35	V
AC CHARACTERISTICS							
Unity Gain Bandwidth	UGBW	C _L =	25 pF		3		MHz
Slew Rate at Unity Gain	SR	C _L = 20 pF	$R_L = 2 k\Omega$		2.6		V/μs
Phase Margin	ϕ_{m}	C _L =	25 pF		50		0
Gain Margin	A _m	C _L =	25 pF		14		dB
Settling Time	+	$V_{O} = 8.5 \text{ Vpp},$	Settling time to 0.1%		3.4		
Jeming Time	t _S (Gain = 1, $C_L = 20 \text{ pF}$	Settling time to 0.01%		6.8		μS

^{17.} Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

^{18.} Performance guaranteed over the indicated operating temperature range by design and/or characterization.

^{19.} Power dissipation must be limited to prevent junction temperature from exceeding 150°C. See Absolute Maximum Ratings for more information.

ELECTRICAL CHARACTERISTICS AT V_S = 10 V

 $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid-supply}$ unless otherwise noted. All limits are guaranteed by testing or statistical analysis. Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 17, 18)

Parameter	Symbol	Cond	itions	Min	Тур	Max	Unit
NOISE CHARACTERISTICS							
Total Harmonic Distortion plus Noise	THD+N	V _{IN} = 7.5 Vpp, f		0.004		%	
Inner Defermed Voltage Naise	_	f = 1	kHz		30		->///
Input Referred Voltage Noise	e _n	f = 10	f = 10 kHz		20		- nV/√ Hz
Input Referred Current Noise	i _n	f = 1 kHz			90		fA/√ Hz
SUPPLY CHARACTERISTICS							
Davisa Comple Daiostica Datia	DCDD	No Load		114	135		-10
Power Supply Rejection Ratio	PSRR	NO L	-oad	100			dB
		NC20074	Noteed		430	645	
D		NCx20071	No load			785	1 ,
Power Supply Quiescent Current	I _{DD}		Day shawasi wa laad		416	540	μΑ
		NCx20072, NCx20074 Per channel, no load				640	1

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- 17. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
- 18. Performance guaranteed over the indicated operating temperature range by design and/or characterization.
- 19. Power dissipation must be limited to prevent junction temperature from exceeding 150°C. See Absolute Maximum Ratings for more information.

ELECTRICAL CHARACTERISTICS AT V_S = 36 V

 $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid-supply}$ unless otherwise noted. All limits are guaranteed by testing or statistical analysis. Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 20, 21)

Parameter	Symbol	Cond	ditions	Min	Тур	Max	Unit	
INPUT CHARACTERISTICS								
	Vos	NCx20071			1.3	±3.5	mV	
Innut Officet Voltage		NCX	20071			±4.5	mV	
Input Offset Voltage		NCv20073	2, NCx20074		1.3	±3	mV	
		NCX20072	z, NCX20074			±4	mV	
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$T_A = 25^{\circ}$	C to 125°C		2		μV/°C	
Input Bias Current (Note 21)					5	200		
	I _{IB}	NCx20071	NCx20071, NCx20072			2000	pА	
		NCx			1500			
		NCv20074	NCx20071, NCx20072		2	75		
January Offices Community (Nation 24)		NCX20071				1000		
Input Offset Current (Note 21)	los	NO	20074		2	75	pA	
		NCX	20074			200		
Oh a saad Oan and Car	VTLIC	DO	NCx20072		100		-ID	
Channel Separation	XTLK	DC	NCx20074		115		dB	
Differential Input Resistance	R _{ID}		•		5		GΩ	
Common Mode Input Resistance	R _{IN}				5		GΩ	

- 20. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
- 21. Performance guaranteed over the indicated operating temperature range by design and/or characterization.
- 22. Power dissipation must be limited to prevent junction temperature from exceeding 150°C. See Absolute Maximum Ratings for more information.

ELECTRICAL CHARACTERISTICS AT V_S = 36 V $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid}$ –supply unless otherwise noted. All limits are guaranteed by testing or statistical analysis. Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 20, 21)

Parameter	Symbol	Cond	litions	Min	Тур	Max	Unit
INPUT CHARACTERISTICS						•	
Differential Input Capacitance	C _{ID}				1.5		pF
Common Mode Input Capacitance	C _{CM}				3.5		pF
			$V_{CM} = V_{SS} + 0.2 \text{ V to}$	118	135		
		NCx20071	$V_{CM} = V_{SS} + 0.2 \text{ V to}$ $V_{DD} - 1.35 \text{ V}$	95			
			Vov. = Voo + 0.2 V to	120	145		4D
Common Mode Rejection Ratio	CMRR	NCx20072	$V_{CM} = V_{SS} + 0.2 \text{ V to}$ $V_{DD} - 1.35 \text{ V}$	95			dB
		NCx20074	$V_{CM} = V_{SS} + 0.2 \text{ V to}$	120	145		
			$V_{CM} = V_{SS} + 0.2 \text{ V to}$ $V_{DD} - 1.35 \text{ V}$	85			
OUTPUT CHARACTERISTICS		•			•		
0 1 1/1 0 1				98	120		
Open Loop Voltage Gain	A_{VOL}		-	88			dB
0 0		Op amp sinking current			50		
Output Current Capability (Note 22)	I _O	Op amp sou	rcing current		65		mA
					0.074	0.15	
			NCx20071			0.22	- V
Output Voltage High		Voltage output swing			0.074	0.10	
	V_{OH}	from positive rail	NCx20072			0.15	
					0.074	0.10	
			NCx20074			0.12	
0	.,				0.065	0.3	.,
Output Voltage Low	V_{OL}	Voltage output swir	ng from negative rail			0.35	V
AC CHARACTERISTICS						-	
Unity Gain Bandwidth	UGBW	C _L =	25 pF		3		MHz
Slew Rate at Unity Gain	SR	C _L = 20 pF	$R_L = 2 k\Omega$		2.4		V/μs
Phase Margin	ϕ_{m}	C _L =	25 pF		50		0
Gain Margin	A _m	C _L =	25 pF		14		dB
0.411		V _O = 10 Vpp,	Settling time to 0.1%		3.2		
Settling Time	t _S	Gain = 1, $C_L = 20 \text{ pF}$	Settling time to 0.01%		7		μS
NOISE CHARACTERISTICS							
Total Harmonic Distortion plus Noise	THD+N	V _{IN} = 28.5 Vpp,	f = 1 kHz, Av = 1		0.001		%
Innut Defended Velicing Nation	_	f = 1	l kHz		30		->//
Input Referred Voltage Noise	e _n	f = 1	0 kHz		20		nV/√Hz
Input Referred Current Noise	i _n	f = 1	l kHz		90		fA/√Hz

^{20.} Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

^{21.} Performance guaranteed over the indicated operating temperature range by design and/or characterization.

^{22.} Power dissipation must be limited to prevent junction temperature from exceeding 150°C. See Absolute Maximum Ratings for more information.

ELECTRICAL CHARACTERISTICS AT V_S = 36 V $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid}$ –supply unless otherwise noted. All limits are guaranteed by testing or statistical analysis. Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 20, 21)

Parameter	Symbol	Conditions		Min	Тур	Max	Unit
SUPPLY CHARACTERISTICS							
Davies County Daisation Datie	DODD	Na	Land	114	135		40
Power Supply Rejection Ratio	PSRR	INO I	Load	100			aB
		NCv20074	No load		480	700	
	NCx20071	No load			840		
Power Supply Quiescent Current I _{DD} NCx20072 Per channel		NCv20072	Der channel no load		465	570	dB μA
	Per channer, no load			700	μΑ		
		NCv20074	Der channel no load		465	600	
	NCx20074 Per channel, no load			700			

^{20.} Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

^{21.} Performance guaranteed over the indicated operating temperature range by design and/or characterization.

^{22.} Power dissipation must be limited to prevent junction temperature from exceeding 150°C. See Absolute Maximum Ratings for more information.

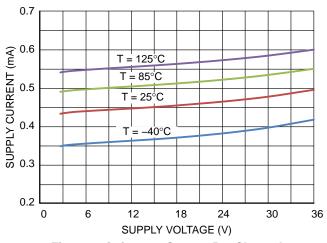


Figure 2. Quiescent Current Per Channel vs. Supply Voltage

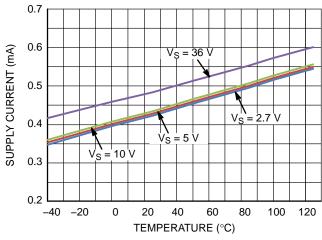


Figure 3. Quiescent Current vs. Temperature

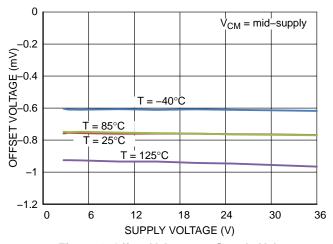


Figure 4. Offset Voltage vs. Supply Voltage

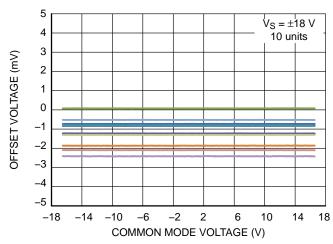


Figure 5. Input Offset Voltage vs. Common Mode Voltage

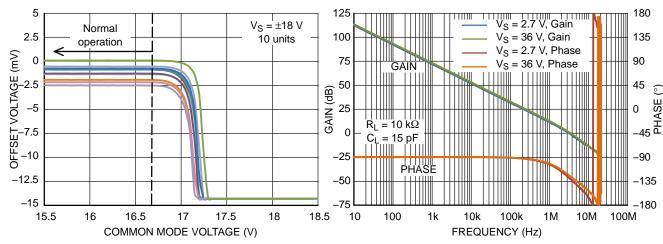


Figure 6. Input Offset Voltage vs. Common Mode Voltage

Figure 7. Gain and Phase vs. Frequency

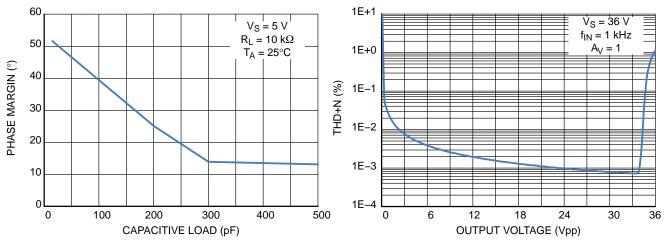


Figure 8. Phase Margin vs. Capacitive Load

Figure 9. THD+N vs. Output Voltage

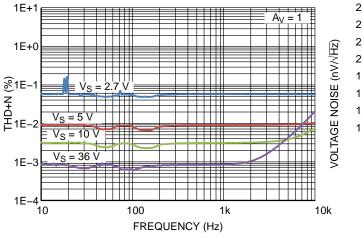


Figure 10. THD+N vs. Frequency

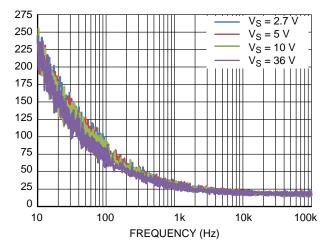


Figure 11. Input Voltage Noise vs. Frequency

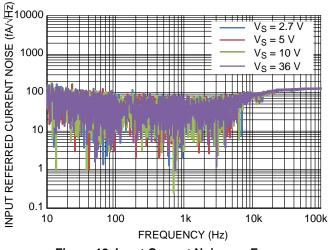


Figure 12. Input Current Noise vs. Frequency

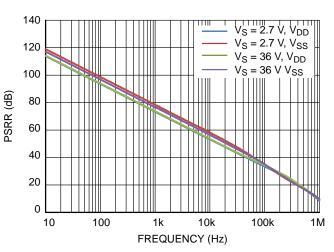
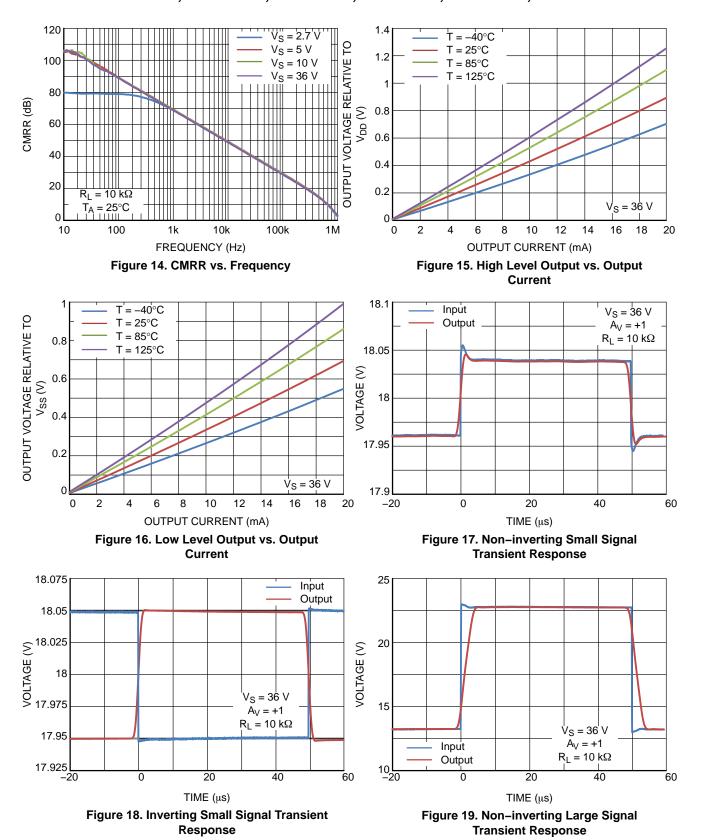


Figure 13. PSRR vs. Frequency



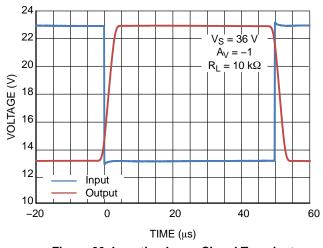


Figure 20. Inverting Large Signal Transient Response

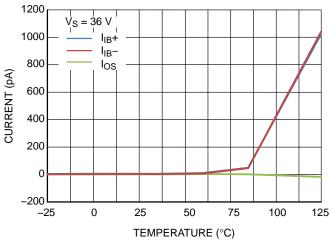


Figure 21. Input Bias and Offset Current vs.
Temperature

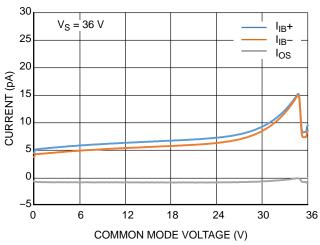


Figure 22. Input Bias Current vs. Common Mode Voltage

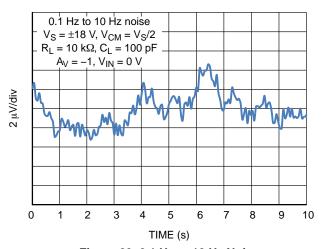


Figure 23. 0.1 Hz to 10 Hz Noise

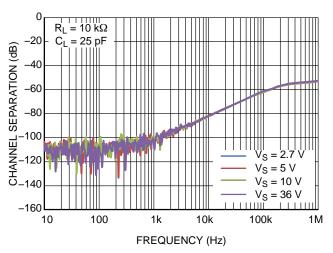


Figure 24. Channel Separation vs. Frequency

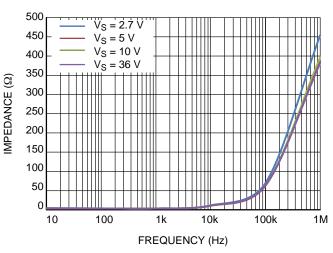
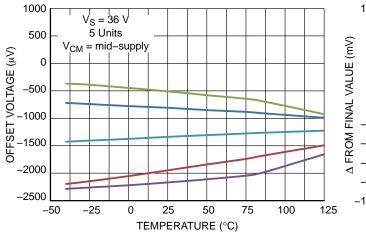


Figure 25. Open Loop Output Impedance



V_S = 36 V 10 V step 8 6 4 2 0 $\pm 1/2$ LSB = $\pm 0.024\%$ -2 -4 -6 -8 -10 5 25 10 15 20 30 35 40 45 50 TIME (µs)

Figure 26. Offset Voltage vs. Temperature

Figure 27. Large Signal Settling Time

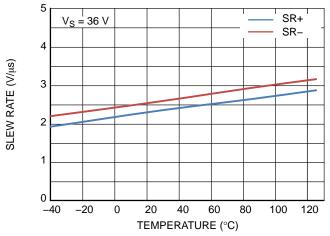


Figure 28. Slew Rate vs. Temperature

APPLICATIONS INFORMATION

Input Circuit

The NCS2007x input stage has a PMOS input pair and ESD protection diodes. The input pair is internally connected by back–to–back Zener diodes with a reverse voltage of 5.5 V. To protect the internal circuitry, the input current must be limited to 10 mA. When operating the

NCS2007x at differential voltages greater than $V_{ID}=26~V$, series resistors can be added externally to limit the input current flowing between the input pins. Adding 500 Ω resistors in series with the input prevents the current from exceeding 10 mA over the entire operating range up to 36 V.

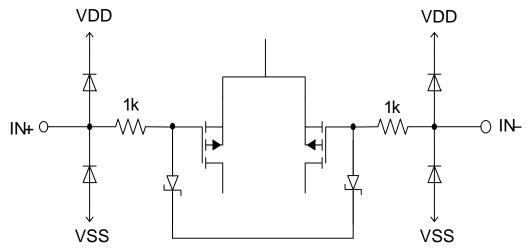


Figure 29. Differential Input Pair

Output

The NCS2007x has a class AB output stage with rail-to-rail output swing.

High output currents can cause the junction temperature to exceed the 150°C absolute maximum rating. In the case of a short circuit where the output is connected to either supply rail, the amount of current the op amp can source and sink is described by the output current capability parameter

listed in the Electrical Characteristics. The junction temperature at a given power dissipation, P, can be calculated using the following formula:

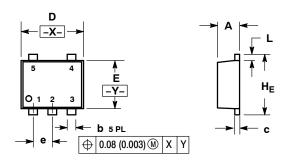
$$T_J = T_A + P \times \theta_{JA}$$

The thermal resistance between junction and ambient, θ_{JA} , is provided in the Thermal Information section of this datasheet.

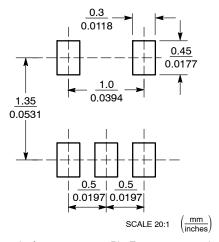


SOT-553, 5 LEAD CASE 463B **ISSUE C**

DATE 20 MAR 2013



RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETERS
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH
 THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM
 THICKNESS OF BASE MATERIAL.

	MILLIMETERS IN			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
С	0.08	0.13	0.18	0.003	0.005	0.007
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.15	1.20	1.25	0.045	0.047	0.049
е		0.50 BSC		0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	1.55	1.60	1.65	0.061	0.063	0.065

GENERIC MARKING DIAGRAM*



XX = Specific Device Code

M = Date Code

= Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

STYLE 1: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR	STYLE 2: PIN 1. CATHODE 2. COMMON ANODE 3. CATHODE 2 4. CATHODE 3 5. CATHODE 4	STYLE 3: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. CATHODE 1	STYLE 4: PIN 1. SOURCE 1 2. DRAIN 1/2 3. SOURCE 1 4. GATE 1 5. GATE 2	STYLE 5: PIN 1. ANODE 2. EMITTER 3. BASE 4. COLLECTOR 5. CATHODE
STYLE 6: PIN 1. EMITTER 2 2. BASE 2 3. EMITTER 1 4. COLLECTOR 1 5. COLLECTOR 2/BASE 1	STYLE 7: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR	STYLE 8: PIN 1. CATHODE 2. COLLECTOR 3. N/C 4. BASE 5. EMITTER	STYLE 9: PIN 1. ANODE 2. CATHODE 3. ANODE 4. ANODE 5. ANODE	

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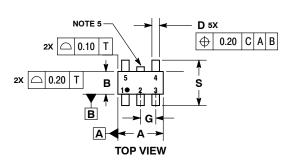
ISSUE	REVISION	DATE
Α	ADDED STYLES 3-9. REQ. BY D. BARLOW	11 NOV 2003
В	ADDED NOMINAL VALUES AND UPDATED GENERIC MARKING DIAGRAM. REQ. BY HONG XIAO	27 MAY 2005
С	UPDATED DIMENSIONS D, E, AND HE. REQ. BY J. LETTERMAN.	20 MAR 2013

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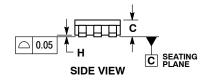


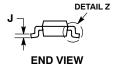
TSOP-5 **CASE 483 ISSUE N**

DATE 12 AUG 2020









NOTES:

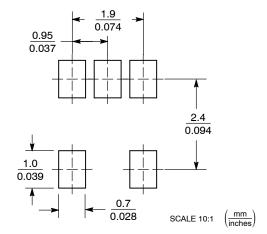
- DIMENSIONING AND TOLERANCING PER ASME
- CONTROLLING DIMENSION: MILLIMETERS.
 MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH
 THICKNESS. MINIMUM LEAD THICKNESS IS THE
 MINIMUM THICKNESS OF BASE MATERIAL.
- MINIMUM I HICKNESS OF BASE MAI EHIAL.

 DIMENSIONS A AND B DO NOT INCLUDE MOLD
 FLASH, PROTRUSIONS, OR GATE BURRS. MOLD
 FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT
 EXCEED 0.15 PER SIDE. DIMENSION A.

 OPTIONAL CONSTRUCTION: AN ADDITIONAL
- TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS			
DIM	MIN	MAX		
Α	2.85	3.15		
В	1.35	1.65		
С	0.90	1.10		
D	0.25	0.50		
G	0.95	BSC		
Н	0.01	0.10		
J	0.10	0.26		
K	0.20	0.60		
М	0° 10°			
S	2.50	3.00		

SOLDERING FOOTPRINT*



^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*





XXX = Specific Device Code XXX = Specific Device Code

= Assembly Location = Date Code

= Year = Pb-Free Package

= Work Week W

= Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

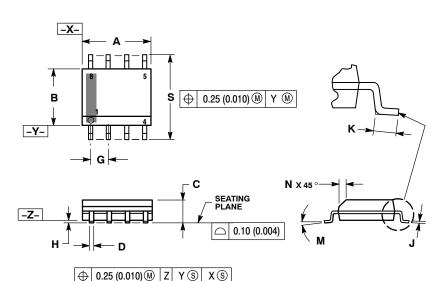
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SOIC-8 NB CASE 751-07 **ISSUE AK**

DATE 16 FEB 2011



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.80	5.00	0.189	0.197
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27	1.27 BSC		0 BSC
Н	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
М	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

XXXXXX

AYWW

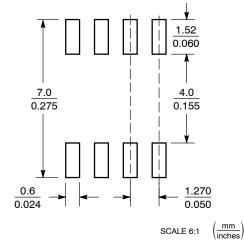
Discrete

 \mathbb{H} H

AYWW

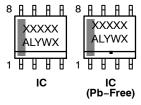
Discrete (Pb-Free)

SOLDERING FOOTPRINT*



^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code = Assembly Location = Wafer Lot = Year

XXXXXX = Specific Device Code = Assembly Location Α ww = Work Week = Work Week = Pb-Free Package = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-8 NB CASE 751-07 ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	7. BASE, #1 8. EMITTER, #1 STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
5. RXE 6. VEE 7. GND 8. ACC STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

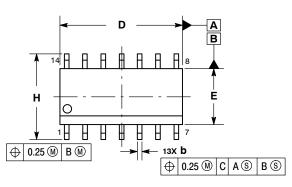
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DESCRIPTION:	SOIC-8 NB		PAGE 2 OF 2

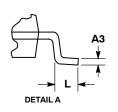
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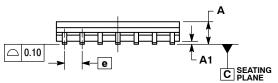
SOIC-14 NB CASE 751A-03 ISSUE L

DATE 03 FEB 2016









MILLIMETERS DIM MIN MAX MIN MAX A 1.35 1.75 0.054 0.068

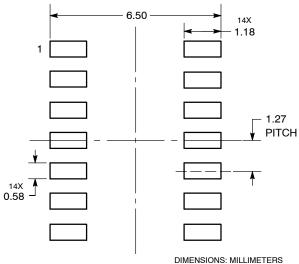
A1	0.10	0.25	0.004	0.010
АЗ	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
Е	3.80	4.00	0.150	0.157
е	1.27	BSC	0.050 BSC	
Н	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
М	0 °	7°	0 °	7°

5. MAXIMUM MOLD PROTRUSION 0.15 PER

NOTES:
1. DIMENSIONING AND TOLERANCING PER

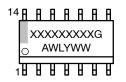
ASME Y14.5M, 1994.
CONTROLLING DIMENSION: MILLIMETERS. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code Α = Assembly Location

WL = Wafer Lot Υ = Year = Work Week WW G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator. "G" or microdot " ■". may or may not be present.

STYLES ON PAGE 2

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SOIC-14 CASE 751A-03 ISSUE L

DATE 03 FEB 2016

STYLE 1: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. NO CONNECTION 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. NO CONNECTION 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 2: CANCELLED	STYLE 3: PIN 1. NO CONNECTION 2. ANODE 3. ANODE 4. NO CONNECTION 5. ANODE 6. NO CONNECTION 7. ANODE 8. ANODE 9. ANODE 10. NO CONNECTION 11. ANODE 12. ANODE 13. NO CONNECTION 14. COMMON CATHODE	STYLE 4: PIN 1. NO CONNECTION 2. CATHODE 3. CATHODE 4. NO CONNECTION 5. CATHODE 6. NO CONNECTION 7. CATHODE 8. CATHODE 9. CATHODE 10. NO CONNECTION 11. CATHODE 12. CATHODE 13. NO CONNECTION 14. COMMON ANODE
STYLE 5: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. NO CONNECTION 7. COMMON ANODE 8. COMMON CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. ANODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE	STYLE 7: PIN 1. ANODE/CATHODE 2. COMMON ANODE 3. COMMON CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. ANODE/CATHODE 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. COMMON CATHODE 12. COMMON ANODE 13. ANODE/CATHODE 14. ANODE/CATHODE	STYLE 8: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. ANODE/CATHODE 7. COMMON ANODE 8. COMMON ANODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. NO CONNECTION 12. ANODE/CATHODE 13. ANODE/CATHODE 14. COMMON CATHODE

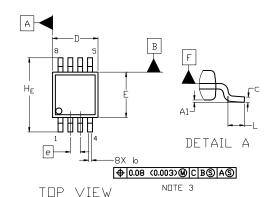
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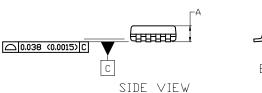
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Micro8 CASE 846A-02 ISSUE K

DATE 16 JUL 2020



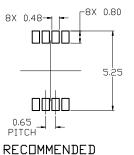




END VIEW

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: MILLIMETERS
- DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
- DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
- A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



MOUNTING FOOTPRINT

DIM	MILLIMETE		RS
ויונע	MIN.	N□M.	MAX.
Α	-	-	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
Ε	2.90	3.00	3.10
е		0.65 BSC	;
HE	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code Α = Assembly Location

Υ = Year W = Work Week = Pb-Free Package

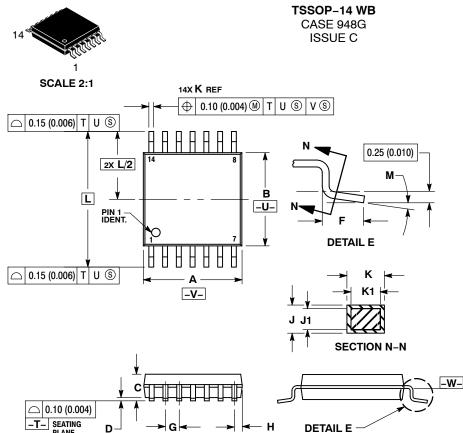
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:	STYLE 2:	STYLE 3:
PIN 1. SOURCE	PIN 1. SOURCE 1	PIN 1. N-SOURCE
SOURCE	2. GATE 1	2. N-GATE
SOURCE	3. SOURCE 2	3. P-SOURCE
GATE	4. GATE 2	4. P-GATE
DRAIN	5. DRAIN 2	5. P-DRAIN
DRAIN	6. DRAIN 2	6. P-DRAIN
7. DRAIN	7. DRAIN 1	7. N-DRAIN
8. DRAIN	8. DRAIN 1	8. N-DRAIN

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DESCRIPTION:	MICRO8		PAGE 1 OF 1

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DATE 17 FEB 2016

- NOTES.

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

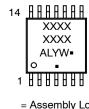
 3. DIMENSION A DOES NOT INCLUDE MOLD
- FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 DIMENSION B DOES NOT INCLUDE
- INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION SHALL
- INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.

 6. TERMINAL NUMBERS ARE SHOWN FOR DEFERENCE ONLY
- REFERENCE ONLY.
 DIMENSION A AND B ARE TO BE
- DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026 BSC	
Н	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40	BSC	0.252	BSC
М	o°	8 °	0 °	8 °

GENERIC MARKING DIAGRAM*



= Assembly Location

= Wafer Lot ٧ = Year

W = Work Week

= Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

1	
14X 0.36	DIMENSIONS: MILLIMETERS

SOLDERING FOOTPRINT

7.06

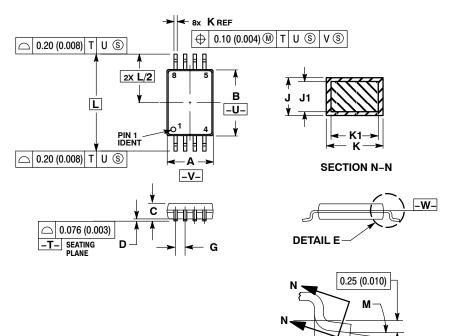
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TSSOP-8 CASE 948S-01 ISSUE C

DATE 20 JUN 2008



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
- 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	2.90	3.10	0.114	0.122
В	4.30	4.50	0.169	0.177
С		1.10		0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65	BSC	0.026 BSC	
J	0.09	0.20	0.004	800.0
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252	
М	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code = Assembly Location

= Year WW = Work Week = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

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DETAIL E

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PAGE 2 OF 2

ISSUE	REVISION	DATE
0	RELEASED FOR PRODUCTION.	18 APR 2000
Α	ADDED MARKING DIAGRAM INFORMATION. REQ. BY V. BASS.	13 JAN 2006
В	CORRECTED MARKING DIAGRAM PIN 1 LOCATION AND MARKING. REQ. BY C. REBELLO.	13 MAR 2006
С	REMOVED EXPOSED PAD VIEW AND DIMENSIONS P AND P1. CORRECTED MARKING INFORMATION. REQ. BY C. REBELLO.	20 JUN 2008

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