LMV431x Low-Voltage (1.24-V) Adjustable Precision Shunt Regulators

1 Features

- Low-Voltage Operation/Wide Adjust Range (1.24 V/30 V)
- 0.5% Initial Tolerance (LMV431B)
- Temperature Compensated for Industrial Temperature Range (39 PPM/°C for the LMV431AI)
- Low Operation Current (55 µA)
- Low Output Impedance (0.25 Ω)
- Fast Turn-On Response
- Low Cost

2 Applications

- Shunt Regulator
- Series Regulator
- Current Source or Sink
- Voltage Monitor
- Error Amplifier
- 3-V Off-Line Switching Regulator
- Low Dropout N-Channel Series Regulator

3 Description

The LMV431, LMV431A and LMV431B are precision 1.24 V shunt regulators capable of adjustment to 30 V. Negative feedback from the cathode to the adjust pin controls the cathode voltage, much like a non-inverting op amp configuration (Refer to *Symbol and Functional Diagrams*). A two-resistor voltage divider terminated at the adjust pin controls the gain of a 1.24 V band-gap reference. Shorting the cathode to the adjust pin (voltage follower) provides a cathode voltage of a 1.24 V.

The LMV431, LMV431A and LMV431B have respective initial tolerances of 1.5%, 1%, and 0.5%, and functionally lend themselves to several applications that require zener diode type performance at low voltages. Applications include a 3 V to 2.7 V low drop-out regulator, an error amplifier in a 3 V off-line switching regulator and even as a voltage detector. These parts are typically stable with capacitive loads greater than 10 nF and less than 50 pF.

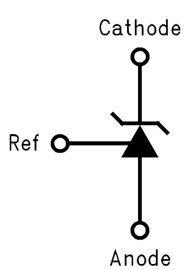
The LMV431, LMV431A and LMV431B provide performance at a competitive price.

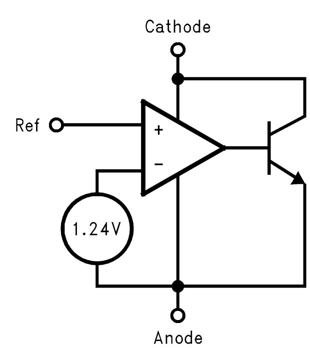
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV431	SOT-23 (5)	2.90 mm x 1.60 mm
LMV431	TO-92 (3)	4.30 mm x 4.30 mm
LMV431	SOT-23 (3)	2.92 mm x 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Symbol and Functional Diagrams





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5 Revision History

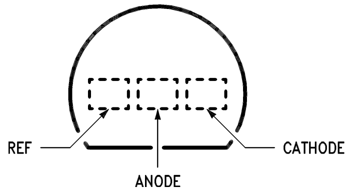
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (May 2005) to Revision G **Page**

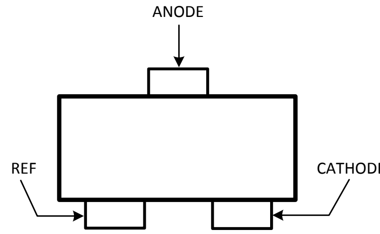
- Changed formatting to match new TI datasheet guidelines; added Device Information and Handling Ratings tables, Layout, and Device and Documentation Support sections; reformatted Detailed Description and Application and Implementation sections. 1
- Added spec 4

6 Pin Configurations and Functions

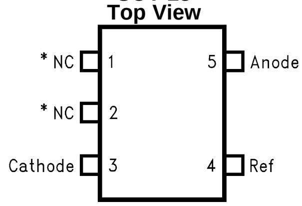
TO-92: Plastic Package
Top View



SOT-23
Top View



SOT-23
Top View



*Pin 1 is not internally connected.

*Pin 2 is internally connected to Anode pin. Pin 2 should be either floating or connected to Anode pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
Operating temperature	Industrial (LMV431AI, LMV431I)	−40	85	°C
	Commercial (LMV431AC, LMV431C, LMV431BC)	0	70	
Lead temperature	TO-92 Package/SOT-23 -5,-3 Package (Soldering, 10 sec.)		265	
Internal power dissipation [2]	TO-92		0.78	W
	SOT-23-5, -3 Package		0.28	W
Cathode voltage			35	V
Continuous cathode current		−30	30	mA
Reference input current		−.05	3	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Ratings apply to ambient temperature at 25°C. Above this temperature, derate the TO-92 at 6.2 mW/°C, and the SOT-23-5 at 2.2 mW/°C. See derating curve in Operating Condition section.

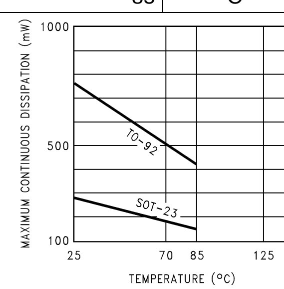
7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]		2000	V

(1) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Cathode voltage		V_{REF}		30	V
Cathode current		0.1		15	mA
Temperature	LMV431AI	−40		85	°C
Derating Curve (Slope = $-1/R_{\theta JA}$)					

7.4 Thermal Information

THERMAL METRIC [1]		LMV431	LMV431	LMV431	UNIT
		SOT-23	SOT-23	TO-92	
		3 PINS	5 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance [2]	455	455	161	°C/W

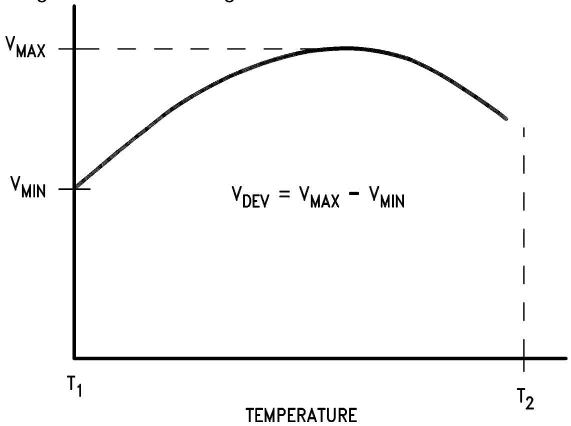
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) $T_{J\ Max}$ = 150°C, $T_J = T_A + (R_{\theta JA}\ P_D)$, where P_D is the operating power of the device.

7.5 LMV431C Electrical Characteristics

T_A = 25°C unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference Voltage	$V_Z = V_{REF}$, I_Z = 10 mA *(See Figure 32)*	T_A = 25°C	1.222	1.24	1.258	V
			T_A = Full Range	1.21		1.27	
V_{DEV}	Deviation of Reference Input Voltage Over Temperature (1)	$V_Z = V_{REF}$, I_Z = 10 mA, T_A = Full Range *(See Figure 32)*			4	12	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	I_Z = 10 mA *(see Figure 33)* V_Z from V_{REF} to 6 V R_1 = 10 kΩ, R_2 = ∞ and 2.6 kΩ			−1.5	−2.7	mV/V
I_{REF}	Reference Input Current	R_1 = 10 kΩ, R_2 = ∞ I_I = 10 mA *(see Figure 33)*			0.15	0.5	µA
$\propto I_{REF}$	Deviation of Reference Input Current over Temperature	R_1 = 10 kΩ, R_2 = ∞, I_I = 10 mA, T_A = Full Range *(see Figure 33)*			0.05	0.3	µA
$I_{Z(MIN)}$	Minimum Cathode Current for Regulation	$V_Z = V_{REF}$*(see Figure 32)*			55	80	µA
$I_{Z(OFF)}$	Off-State Current	V_Z= 6 V, V_{REF} = 0 V *(see Figure 34)*			0.001	0.1	µA
r_Z	Dynamic Output Impedance (2)	$V_Z = V_{REF}$, I_Z = 0.1 mA to 15 mA Frequency = 0 Hz *(see Figure 32)*			0.25	0.4	Ω

(1) Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range. See the following:



The average temperature coefficient of the reference input voltage, $\propto V_{REF}$, is defined as:

$$\propto V_{REF}\ \frac{ppm}{°C} = \frac{\pm\left(\frac{V_{Max} - V_{Min}}{V_{REF}(\text{at } 25°C)}\right)10^6}{T_2 - T_1} = \frac{\pm\left(\frac{V_{DEV}}{V_{REF}(\text{at } 25°C)}\right)10^6}{T_2 - T_1}$$

Where: $T_2 - T_1$ = full temperature change. $\propto V_{REF}$ can be positive or negative depending on whether the slope is positive or negative.
Example: V_{DEV} = 6 mV, V_{REF} = 1240 mV, $T_2 - T_1$ = 125°C.

$$\propto V_{REF} = \frac{\left(\frac{6.0\ mV}{1240\ mV}\right)10^6}{125°C} = +39\ ppm/°C$$

(2) The dynamic output impedance, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R1 and R2, (see *Figure 33*), the dynamic output impedance of the overall circuit, r_Z, is defined as:

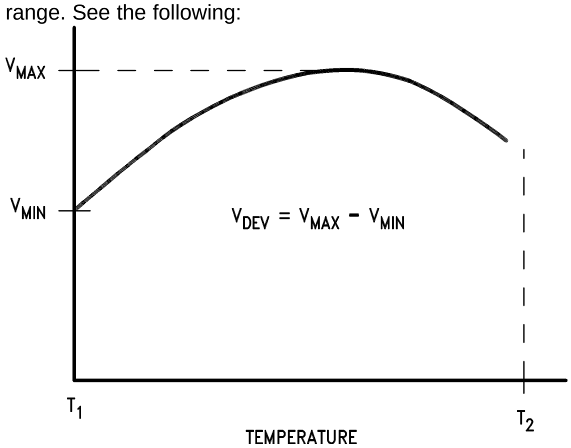
$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z\left(1 + \frac{R1}{R2}\right)\right]$$

7.6 LMV431I Electrical Characteristics

T_A = 25°C unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference Voltage	$V_Z = V_{REF}$, I_Z = 10 mA (*See Figure 32*)	T_A = 25°C	1.222	1.24	1.258	V
			T_A = Full Range	1.202		1.278	V
V_{DEV}	Deviation of Reference Input Voltage Over Temperature[1]	$V_Z = V_{REF}$, I_Z = 10 mA, T_A = Full Range (*See Figure 32*)			6	20	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	I_Z = 10mA (*see Figure 33*) V_Z from V_{REF} to 6V R_1 = 10 kΩ, R_2 = ∞ and 2.6kΩ			−1.5	−2.7	mV/V
I_{REF}	Reference Input Current	R_1 = 10 kΩ, R_2 = ∞ I_I = 10 mA (*see Figure 33*)			0.15	0.5	µA
$\propto I_{REF}$	Deviation of Reference Input Current over Temperature	R_1 = 10 kΩ, R_2 = ∞, I_I = 10 mA, T_A = Full Range (*see Figure 33*)			0.1	0.4	µA
$I_{Z(MIN)}$	Minimum Cathode Current for Regulation	$V_Z = V_{REF}$(*see Figure 32*)			55	80	µA
$I_{Z(OFF)}$	Off-State Current	V_Z = 6 V, V_{REF} = 0V (*see Figure 34*)			0.001	0.1	µA
r_Z	Dynamic Output Impedance[2]	$V_Z = V_{REF}$, I_Z = 0.1 mA to 15 mA Frequency = 0 Hz (*see Figure 32*)			0.25	0.4	Ω

(1) Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range. See the following:



The average temperature coefficient of the reference input voltage, $\propto V_{REF}$, is defined as:

$$\propto V_{REF}\ \frac{ppm}{°C} = \frac{\pm\left(\frac{V_{Max} - V_{Min}}{V_{REF}(\text{at } 25°C)}\right)10^6}{T_2 - T_1} = \frac{\pm\left(\frac{V_{DEV}}{V_{REF}(\text{at } 25°C)}\right)10^6}{T_2 - T_1}$$

Where: $T_2 - T_1$ = full temperature change. $\propto V_{REF}$ can be positive or negative depending on whether the slope is positive or negative.
Example: V_{DEV} = 6 mV, V_{REF} = 1240 mV, $T_2 - T_1$ = 125°C.

$$\propto V_{REF} = \frac{\left(\frac{6.0\text{ mV}}{1240\text{ mV}}\right)10^6}{125°C} = +39\text{ ppm}/°C$$

(2) The dynamic output impedance, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R1 and R2, (see *Figure 33*), the dynamic output impedance of the overall circuit, r_Z, is defined as:

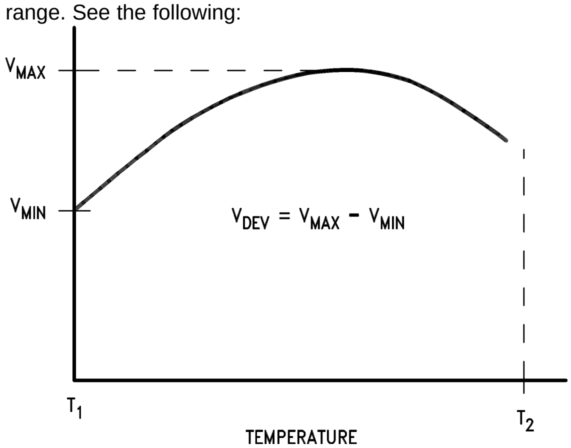
$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z\left(1 + \frac{R1}{R2}\right)\right]$$

7.7 LMV431AC Electrical Characteristics

T_A = 25°C unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference Voltage	$V_Z = V_{REF}$, I_Z = 10 mA (See Figure 32)	T_A = 25°C	1.228	1.24	1.252	V
			T_A = Full Range	1.221		1.259	
V_{DEV}	Deviation of Reference Input Voltage Over Temperature (1)	$V_Z = V_{REF}$, I_Z = 10 mA, T_A = Full Range (See Figure 32)			4	12	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	I_Z = 10 mA (see Figure 33) V_Z from V_{REF} to 6 V R_1 = 10 kΩ, R_2 = ∞ and 2.6 kΩ			−1.5	−2.7	mV/V
I_{REF}	Reference Input Current	R_1 = 1 kΩ, R_2 = ∞ I_I = 10 mA (see Figure 33)			0.15	0.50	µA
$\propto I_{REF}$	Deviation of Reference Input Current over Temperature	R_1 = 10 kΩ, R_2 = ∞, I_I = 10 mA, T_A = Full Range (see Figure 33)			0.05	0.3	µA
$I_{Z(MIN)}$	Minimum Cathode Current for Regulation	$V_Z = V_{REF}$(see Figure 32)			55	80	µA
$I_{Z(OFF)}$	Off-State Current	V_Z = 6 V, V_{REF} = 0V (see Figure 34)			0.001	0.1	µA
r_Z	Dynamic Output Impedance (2)	$V_Z = V_{REF}$, I_Z = 0.1mA to 15mA Frequency = 0 Hz (see Figure 32)			0.25	0.4	Ω

(1) Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range. See the following:



The average temperature coefficient of the reference input voltage, $\propto V_{REF}$, is defined as:

$$\propto V_{REF}\ \frac{ppm}{°C} = \frac{\pm\left(\frac{V_{Max} - V_{Min}}{V_{REF}(\text{at } 25°C)}\right)10^6}{T_2 - T_1} = \frac{\pm\left(\frac{V_{DEV}}{V_{REF}(\text{at } 25°C)}\right)10^6}{T_2 - T_1}$$

Where: $T_2 - T_1$ = full temperature change. $\propto V_{REF}$ can be positive or negative depending on whether the slope is positive or negative.
Example: V_{DEV} = 6 mV, V_{REF} = 1240 mV, $T_2 - T_1$ = 125°C.

$$\propto V_{REF} = \frac{\left(\frac{6.0\text{ mV}}{1240\text{ mV}}\right)10^6}{125°C} = +39\text{ ppm}/°C$$

(2) The dynamic output impedance, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R1 and R2, (see Figure 33), the dynamic output impedance of the overall circuit, r_Z, is defined as:

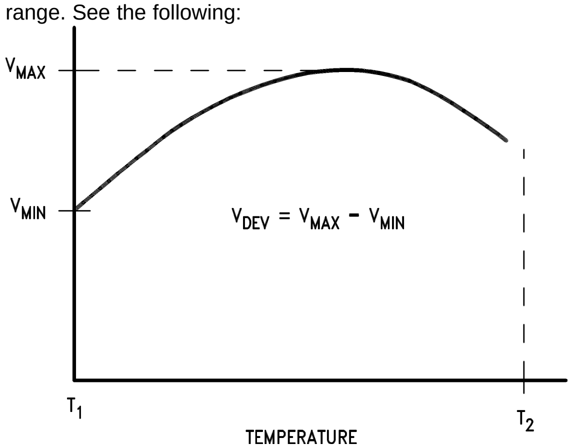
$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z\left(1 + \frac{R1}{R2}\right)\right]$$

7.8 LMV431AI Electrical Characteristics

T_A = 25°C unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference Voltage	$V_Z = V_{REF}$, I_Z = 10mA *(See Figure 32)*	T_A = 25°C	1.228	1.24	1.252	V
			T_A = Full Range	1.215		1.265	V
V_{DEV}	Deviation of Reference Input Voltage Over Temperature (1)	$V_Z = V_{REF}$, I_Z = 10mA, T_A = Full Range *(See Figure 32)*			6	20	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	I_Z = 10mA *(see Figure 33)* V_Z from V_{REF} to 6 V R_1 = 10 kΩ, R_2 = ∞ and 2.6 kΩ			−1.5	−2.7	mV/V
I_{REF}	Reference Input Current	R_1 = 10 kΩ, R_2 = ∞ I_I = 10 mA *(see Figure 33)*			0.15	0.5	µA
$\propto I_{REF}$	Deviation of Reference Input Current over Temperature	R_1 = 10 kΩ, R_2 = ∞, I_I = 10 mA, T_A = Full Range *(see Figure 33)*			0.1	0.4	µA
$I_{Z(MIN)}$	Minimum Cathode Current for Regulation	$V_Z = V_{REF}$*(see Figure 32)*			55	80	µA
$I_{Z(OFF)}$	Off-State Current	V_Z = 6 V, V_{REF} = 0 V *(see Figure 34)*			0.001	0.1	µA
r_Z	Dynamic Output Impedance (2)	$V_Z = V_{REF}$, I_Z = 0.1 mA to 15 mA Frequency = 0 Hz *(see Figure 32)*			0.25	0.4	Ω

(1) Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range. See the following:



The average temperature coefficient of the reference input voltage, $\propto V_{REF}$, is defined as:

$$\propto V_{REF}\,\frac{ppm}{°C} = \frac{\pm\left(\frac{V_{Max} - V_{Min}}{V_{REF}(\text{at } 25°C)}\right)10^6}{T_2 - T_1} = \frac{\pm\left(\frac{V_{DEV}}{V_{REF}(\text{at } 25°C)}\right)10^6}{T_2 - T_1}$$

Where: $T_2 - T_1$ = full temperature change. $\propto V_{REF}$ can be positive or negative depending on whether the slope is positive or negative.
Example: V_{DEV} = 6 mV, V_{REF} = 1240 mV, $T_2 - T_1$ = 125°C.

$$\propto V_{REF} = \frac{\left(\frac{6.0\text{ mV}}{1240\text{ mV}}\right)10^6}{125°C} = +39\text{ ppm}/°C$$

(2) The dynamic output impedance, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R1 and R2, (see *Figure 33*), the dynamic output impedance of the overall circuit, r_Z, is defined as:

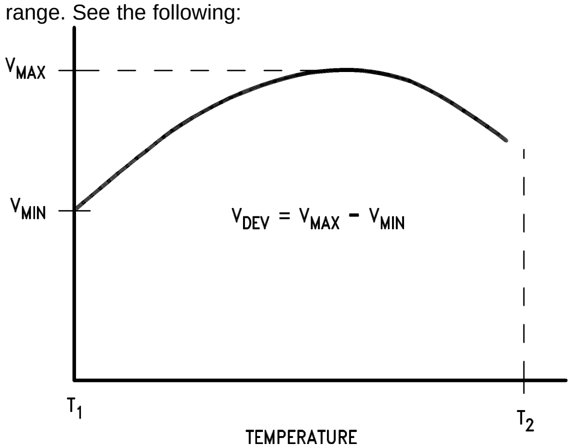
$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z\left(1 + \frac{R1}{R2}\right)\right]$$

7.9 LMV431BC Electrical Characteristics

T_A = 25°C unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference Voltage	$V_Z = V_{REF}$, I_Z = 10 mA *(See Figure 32)*	T_A = 25°C	1.234	1.24	1.246	V
			T_A = Full Range	1.227		1.253	V
V_{DEV}	Deviation of Reference Input Voltage Over Temperature (1)	$V_Z = V_{REF}$, I_Z = 10 mA, T_A = Full Range *(See Figure 32)*			4	12	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	I_Z = 10 mA *(see Figure 33)* V_Z from V_{REF} to 6 V R_1 = 10 kΩ, R_2 = ∞ and 2.6 kΩ			−1.5	−2.7	mV/V
I_{REF}	Reference Input Current	R_1 = 10 kΩ, R_2 = ∞ I_I = 10 mA *(see Figure 33)*			0.15	0.50	µA
$\propto I_{REF}$	Deviation of Reference Input Current over Temperature	R_1 = 10 kΩ, R_2 = ∞, I_I = 10 mA, T_A = Full Range *(see Figure 33)*			0.05	0.3	µA
$I_{Z(MIN)}$	Minimum Cathode Current for Regulation	$V_Z = V_{REF}$ *(see Figure 32)*			55	80	µA
$I_{Z(OFF)}$	Off-State Current	V_Z = 6 V, V_{REF} = 0V *(see Figure 34)*			0.001	0.1	µA
r_Z	Dynamic Output Impedance (2)	$V_Z = V_{REF}$, I_Z = 0.1mA to 15mA Frequency = 0 Hz *(see Figure 32)*			0.25	0.4	Ω

(1) Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range. See the following:



The average temperature coefficient of the reference input voltage, $\propto V_{REF}$, is defined as:

$$\propto V_{REF}\ \frac{ppm}{°C} = \frac{\pm\left(\frac{V_{Max} - V_{Min}}{V_{REF}(\text{at } 25°C)}\right)10^6}{T_2 - T_1} = \frac{\pm\left(\frac{V_{DEV}}{V_{REF}(\text{at } 25°C)}\right)10^6}{T_2 - T_1}$$

Where: $T_2 - T_1$ = full temperature change. $\propto V_{REF}$ can be positive or negative depending on whether the slope is positive or negative.
Example: V_{DEV} = 6 mV, V_{REF} = 1240 mV, $T_2 - T_1$ = 125°C.

$$\propto V_{REF} = \frac{\left(\frac{6.0\ mV}{1240\ mV}\right)10^6}{125°C} = +39\ ppm / °C$$

(2) The dynamic output impedance, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R1 and R2, (see Figure 33), the dynamic output impedance of the overall circuit, r_Z, is defined as:

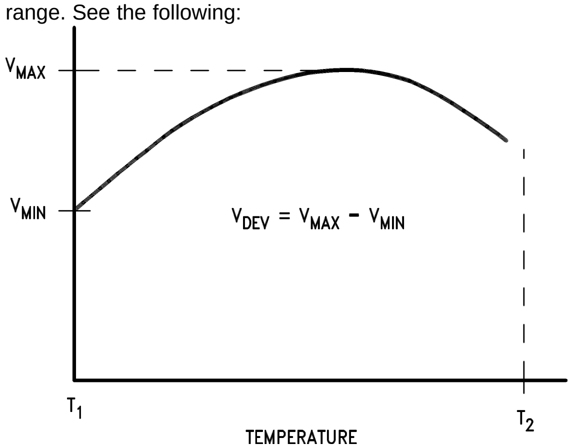
$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z\left(1 + \frac{R1}{R2}\right)\right]$$

7.10 LMV431BI Electrical Characteristics

T_A = 25°C unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference Voltage	$V_Z = V_{REF}$, I_Z = 10 mA *(See Figure 32)*	T_A = 25°C	1.234	1.24	1.246	V
			T_A = Full Range	1.224		1.259	V
V_{DEV}	Deviation of Reference Input Voltage Over Temperature[(1)]	$V_Z = V_{REF}$, I_Z = 10 mA, T_A = Full Range *(See Figure 32)*			6	20	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	I_Z = 10 mA *(see Figure 33)* V_Z from V_{REF} to 6V R_1 = 10 kΩ, R_2 = ∞ and 2.6 kΩ			−1.5	−2.7	mV/V
I_{REF}	Reference Input Current	R_1 = 10 kΩ, R_2 = ∞ I_I = 10 mA *(see Figure 33)*			0.15	0.50	µA
$\propto I_{REF}$	Deviation of Reference Input Current over Temperature	R_1 = 10 kΩ, R_2 = ∞, I_I = 10 mA, T_A = Full Range *(see Figure 33)*			0.1	0.4	µA
$I_{Z(MIN)}$	Minimum Cathode Current for Regulation	$V_Z = V_{REF}$*(see Figure 32)*			55	80	µA
$I_{Z(OFF)}$	Off-State Current	V_Z = 6 V, V_{REF} = 0 V *(see Figure 34)*			0.001	0.1	µA
r_Z	Dynamic Output Impedance[(2)]	$V_Z = V_{REF}$, I_Z = 0.1 mA to 15 mA Frequency = 0 Hz *(see Figure 32)*			0.25	0.4	Ω

(1) Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range. See the following:



The average temperature coefficient of the reference input voltage, $\propto V_{REF}$, is defined as:

$$\propto V_{REF}\ \frac{ppm}{°C} = \frac{\pm\left(\frac{V_{Max} - V_{Min}}{V_{REF}(at\ 25°C)}\right)10^6}{T_2 - T_1} = \frac{\pm\left(\frac{V_{DEV}}{V_{REF}(at\ 25°C)}\right)10^6}{T_2 - T_1}$$

Where: $T_2 - T_1$ = full temperature change. $\propto V_{REF}$ can be positive or negative depending on whether the slope is positive or negative.
Example: V_{DEV} = 6 mV, V_{REF} = 1240 mV, $T_2 - T_1$ = 125°C.

$$\propto V_{REF} = \frac{\left(\frac{6.0\ mV}{1240\ mV}\right)10^6}{125°C} = +39\ ppm/°C$$

(2) The dynamic output impedance, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R1 and R2, (see Figure 33), the dynamic output impedance of the overall circuit, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z\left(1 + \frac{R1}{R2}\right)\right]$$

7.11 Typical Performance Characteristics

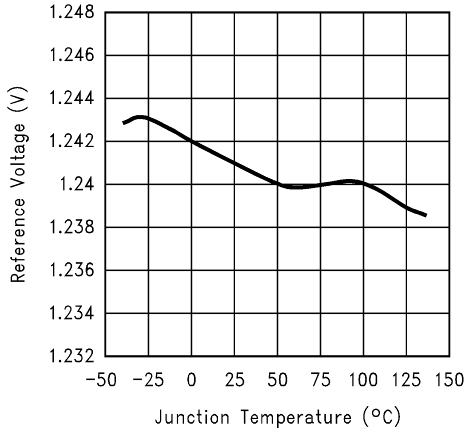


Figure 1. Reference Voltage vs. Junction Temperature

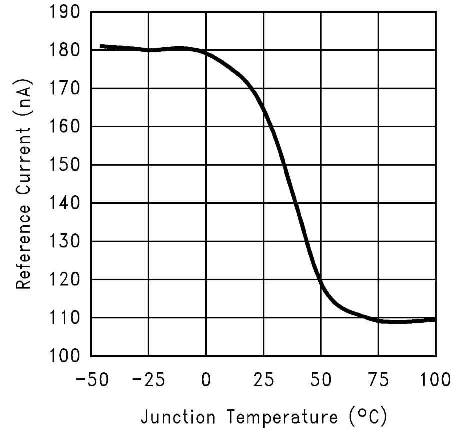


Figure 2. Reference Input Current vs. Junction Temperature

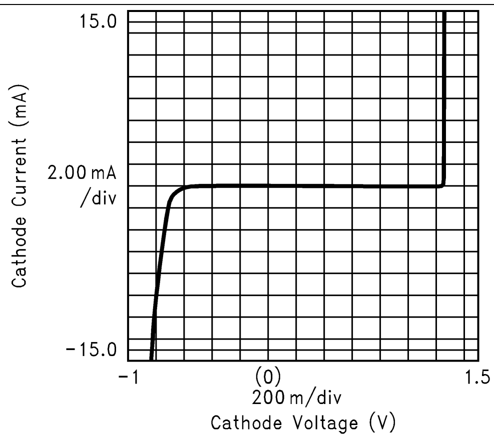


Figure 3. Cathode Current vs. Cathode Voltage 1

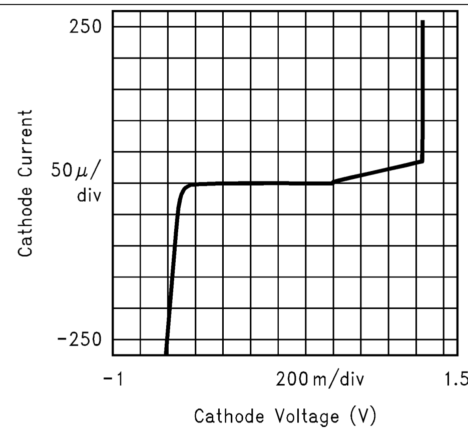


Figure 4. Cathode Current vs. Cathode Voltage 2

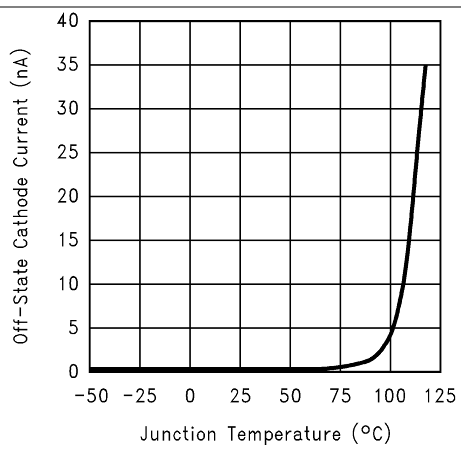


Figure 5. Off-State Cathode Current vs. Junction Temperature

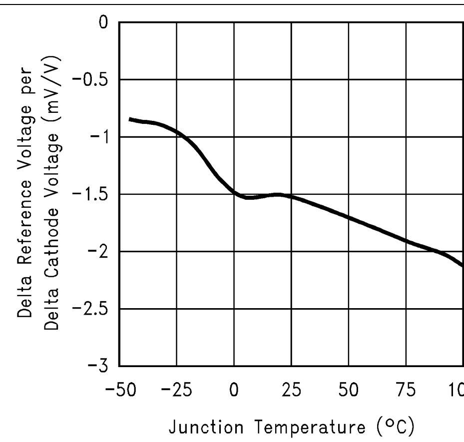


Figure 6. Delta Reference Voltage Per Delta Cathode Voltage vs. Junction Temperature

Typical Performance Characteristics (continued)

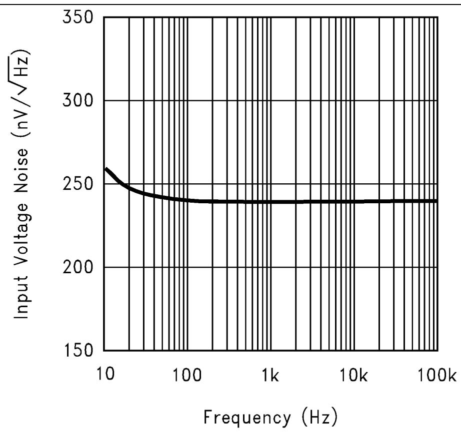


Figure 7. Input Voltage Noise vs. Frequency

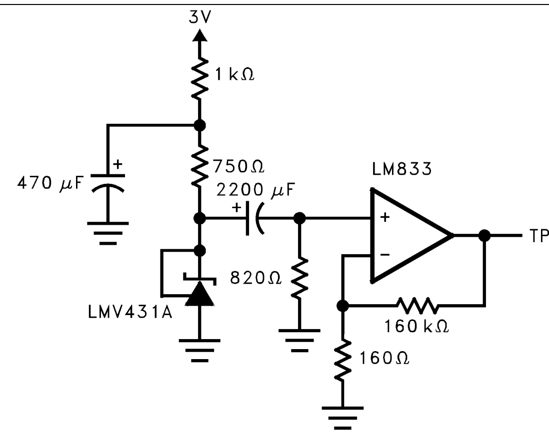


Figure 8. Test Circuit For Input Voltage Noise vs. Frequency

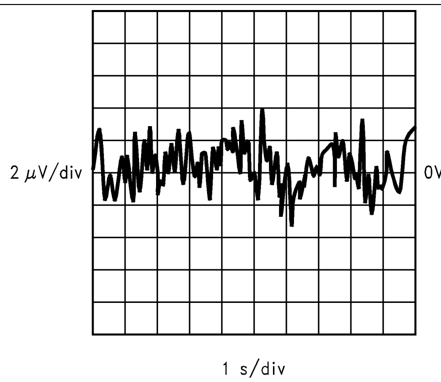
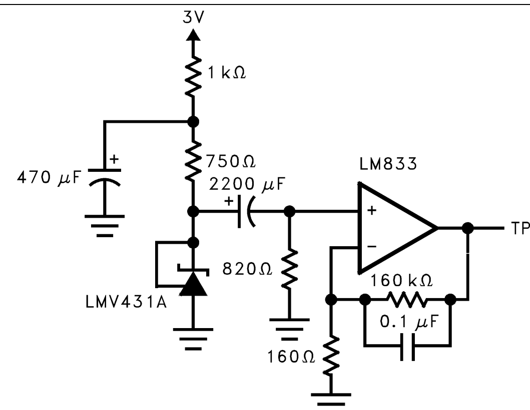


Figure 9. Low Frequency Peak To Peak Noise



BW = 0.1 Hz To 10 Hz

Figure 10. Test Circuit For Peak To Peak Noise

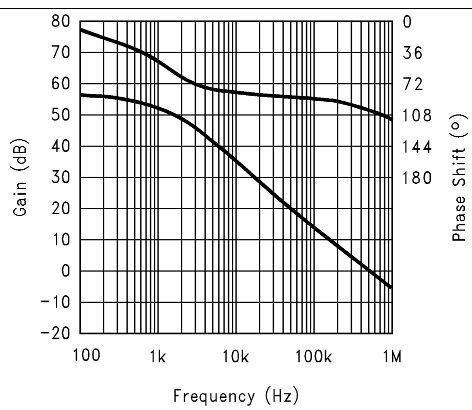


Figure 11. Small Signal Voltage Gain And Phase Shift vs. Frequency

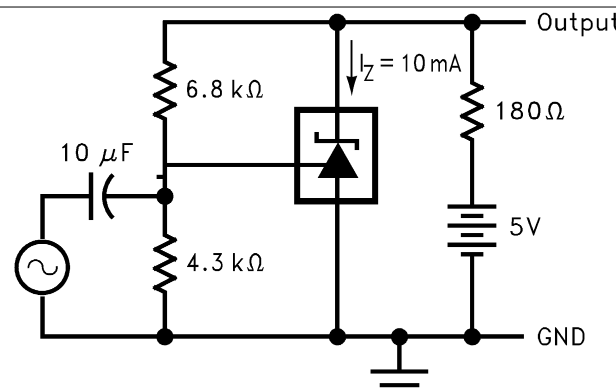


Figure 12. Test Circuit For Voltage Gain And Phase Shift vs. Frequency

Typical Performance Characteristics (continued)

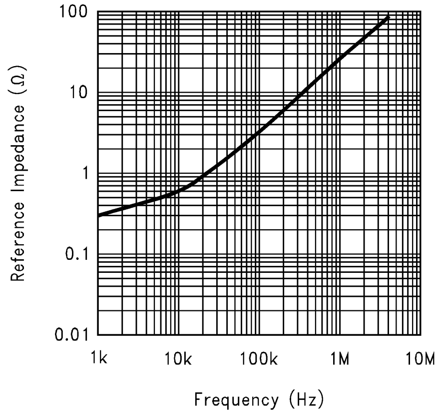


Figure 13. Reference Impedance vs. Frequency

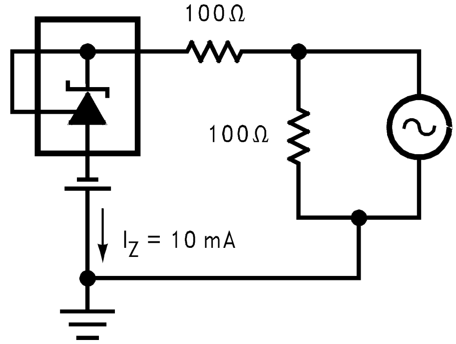


Figure 14. Test Circuit For Reference Impedance vs. Frequency

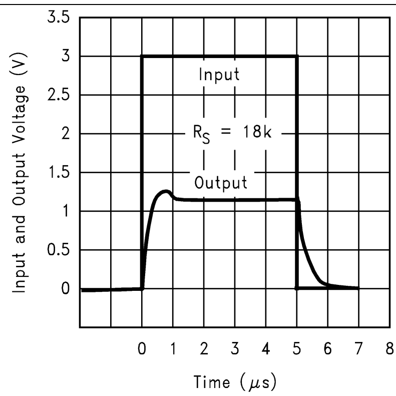


Figure 15. Pulse Response 1

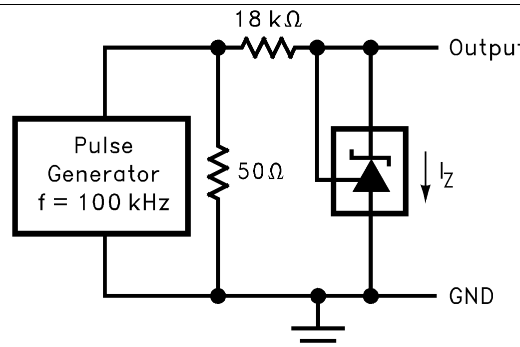


Figure 16. Test Circuit For Pulse Response 1

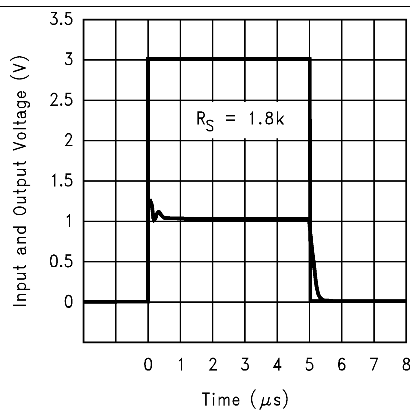


Figure 17. Pulse Response 2

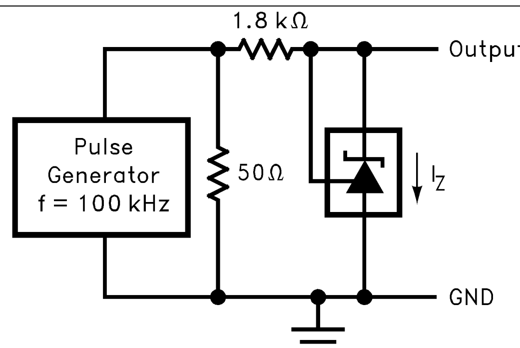


Figure 18. Test Circuit For Pulse Response 2

Typical Performance Characteristics (continued)

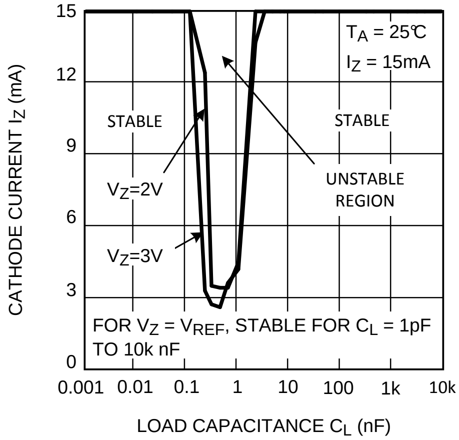


Figure 19. LMV431 Stability Boundary Condition

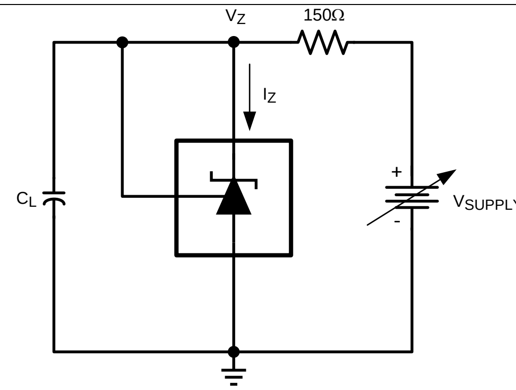


Figure 20. Test Circuit For V_Z = V_{REF}

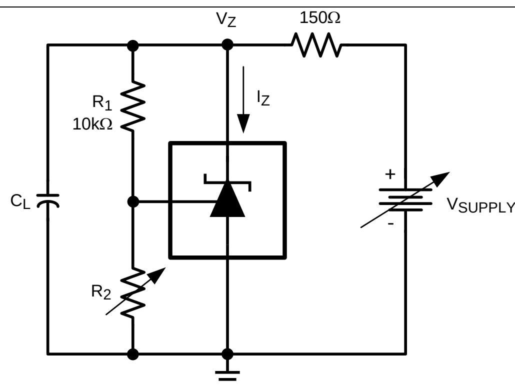
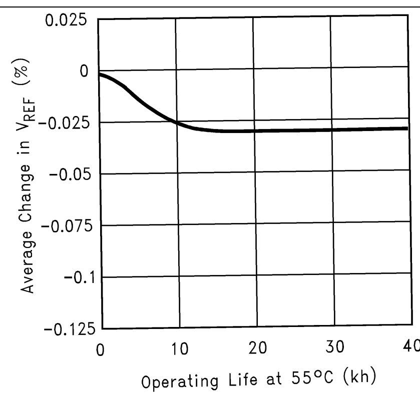


Figure 21. Test Circuit For V_Z = 2V, 3V

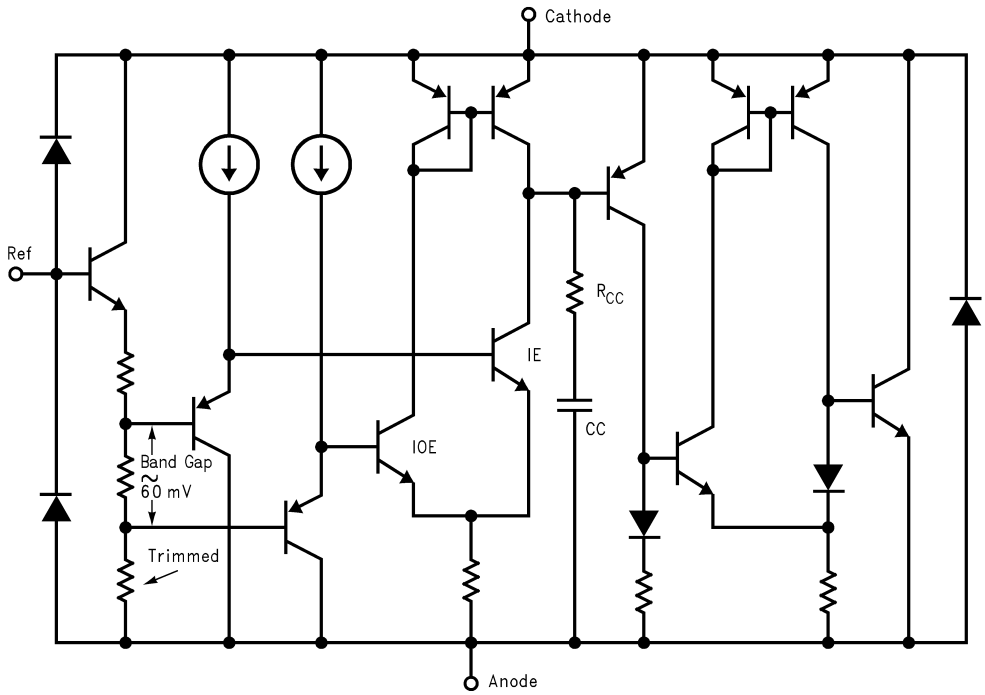


Extrapolated from life-test data taken at 125°C; the activation energy assumed is 0.7eV.

Figure 22. Percentage Change In V_{REF} vs. Operating Life At 55°C

8 Detailed Description

8.1 Functional Block Diagram

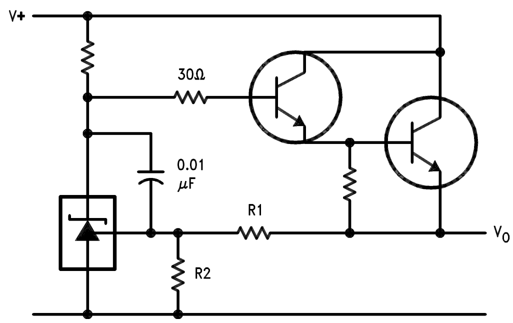


9 Application and Implementation

NOTE

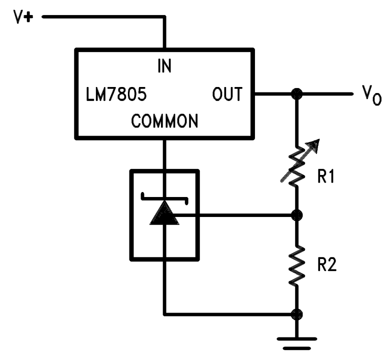
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application



$$V_O \approx \left(1+\frac{R1}{R2}\right)V_{REF}$$

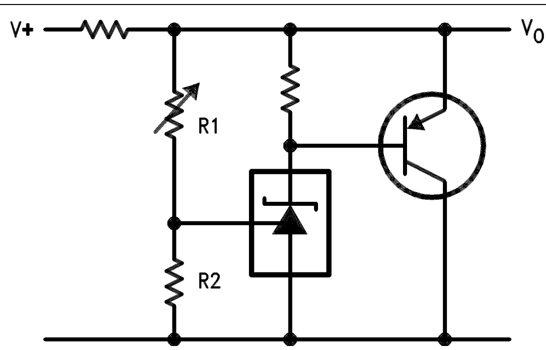
Figure 23. Series Regulator



$$V_O = \left(1+\frac{R1}{R2}\right)V_{REF}$$

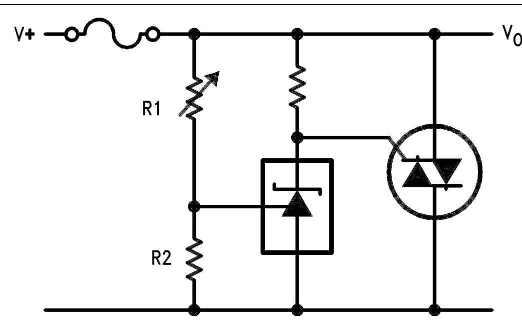
$$V_{O\,MIN} = V_{REF} + 5\ V$$

Figure 24. Output Control of a Three-Terminal Fixed Regulator



$$V_O \approx \left(1+\frac{R1}{R2}\right)V_{REF}$$

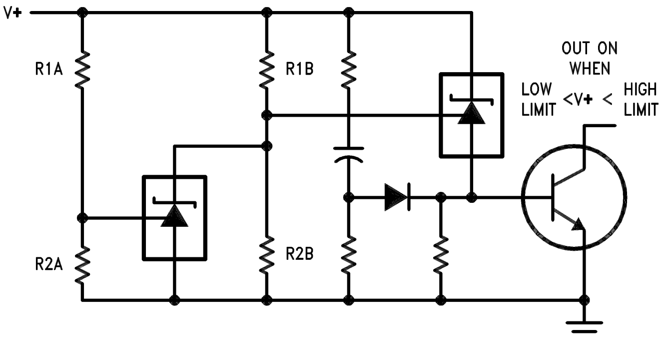
Figure 25. Higher Current Shunt Regulator



$$V_{LIMIT} \approx \left(1+\frac{R1}{R2}\right)V_{REF}$$

Figure 26. Crow Bar

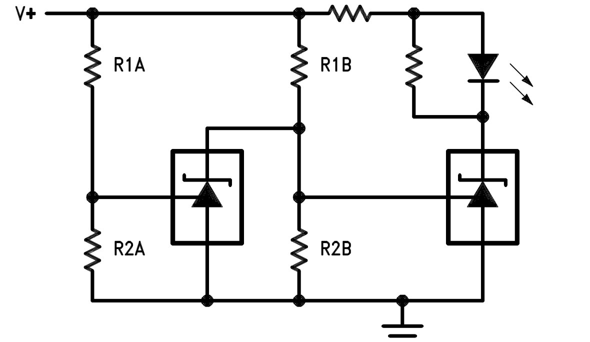
Typical Application (continued)



$$\text{LOW LIMIT} \approx V_{REF}\left(1+\frac{R1B}{R2B}\right)+V_{BE}$$

$$\text{HIGH LIMIT} \approx V_{REF}\left(1+\frac{R1A}{R2A}\right)$$

Figure 27. Overvoltage/Undervoltage Protection Circuit



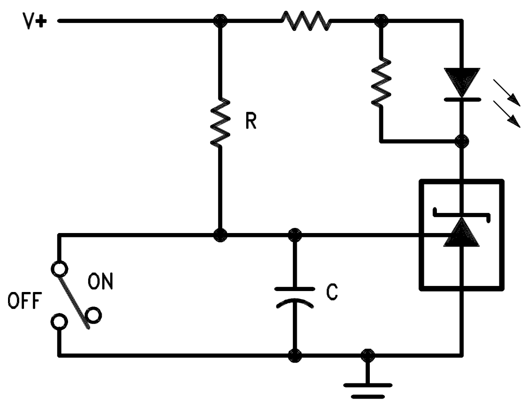
$$\text{LOW LIMIT} \approx V_{REF}\left(1+\frac{R1B}{R2B}\right)$$

$$\text{HIGH LIMIT} \approx V_{REF}\left(1+\frac{R1A}{R2A}\right)$$

LED ON WHEN

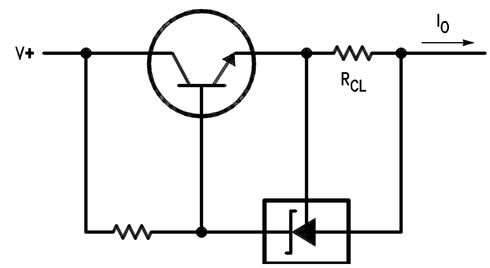
LOW LIMIT $<$ V^+ $<$ HIGH LIMIT

Figure 28. Voltage Monitor



$$\text{DELAY} = R \cdot C \cdot \ell n \frac{V+}{(V^+) - V_{REF}}$$

Figure 29. Delay Timer



$$I_O = \frac{V_{REF}}{R_{CL}}$$

Figure 30. Current Limiter or Current Source

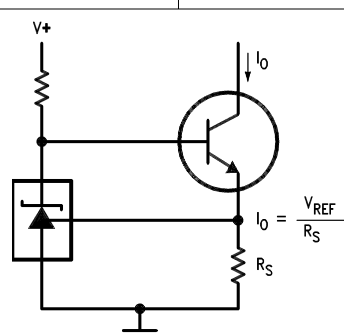


Figure 31. Constant Current Sink

9.2 DC/AC Test Circuit

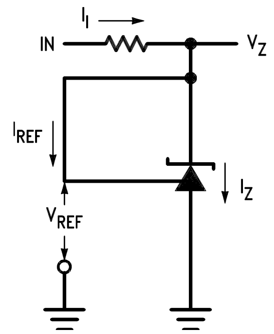


Figure 32. Test Circuit For $V_Z = V_{REF}$

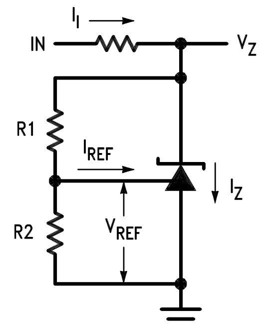


Figure 33. Test Circuit For $V_Z > V_{REF}$

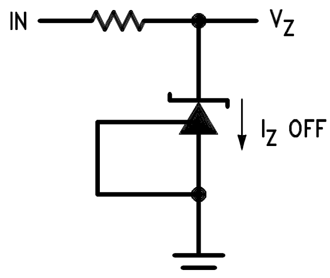


Figure 34. Test Circuit For Off-State Current

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV431	Click here	Click here	Click here	Click here	Click here
LMV431A	Click here	Click here	Click here	Click here	Click here
LMV431B	Click here	Click here	Click here	Click here	Click here

10.2 Trademarks

All trademarks are the property of their respective owners.

10.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV431ACM5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	0 to 70	N09A	
LMV431ACM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	N09A	Samples
LMV431ACM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	N09A	Samples
LMV431AIM5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	N08A	
LMV431AIM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	N08A	Samples
LMV431AIM5X	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	N08A	
LMV431AIM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	N08A	Samples
LMV431AIMF	NRND	SOT-23	DBZ	3	1000	TBD	Call TI	Call TI	-40 to 85	RLA	
LMV431AIMF/NOPB	ACTIVE	SOT-23	DBZ	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	RLA	Samples
LMV431AIMFX	NRND	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 85	RLA	
LMV431AIMFX/NOPB	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	RLA	Samples
LMV431AIZ/LFT3	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type		LMV431 AIZ	Samples
LMV431AIZ/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 85	LMV431 AIZ	Samples
LMV431BCM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		N09C	Samples
LMV431BCM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		N09C	Samples
LMV431BIMF	NRND	SOT-23	DBZ	3	1000	TBD	Call TI	Call TI	-40 to 85	RLB	
LMV431BIMF/NOPB	ACTIVE	SOT-23	DBZ	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	RLB	Samples
LMV431BIMFX/NOPB	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	RLB	Samples
LMV431CM5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	0 to 70	N09B	
LMV431CM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	N09B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV431CM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	N09B	Samples
LMV431CZ/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	0 to 70	LMV431 CZ	Samples
LMV431IM5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	N08B	
LMV431IM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	N08B	Samples
LMV431IM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	N08B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

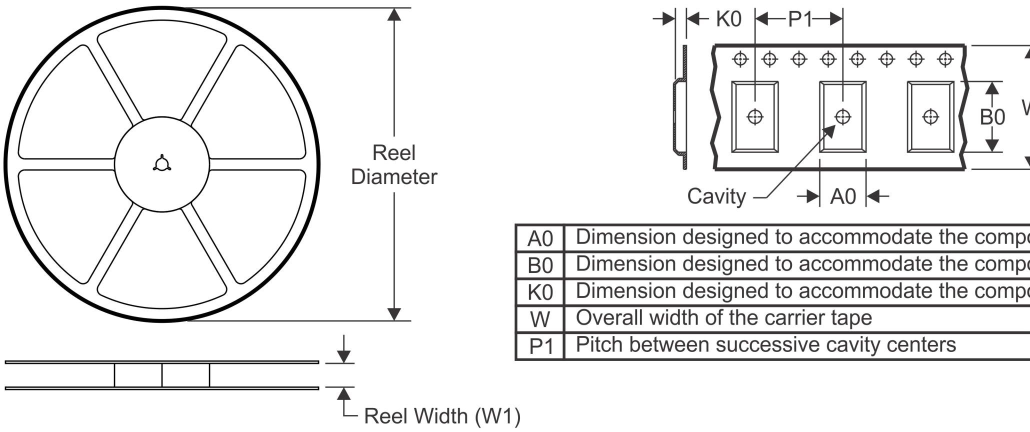
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

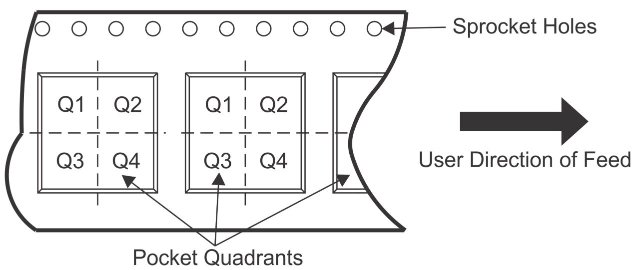
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

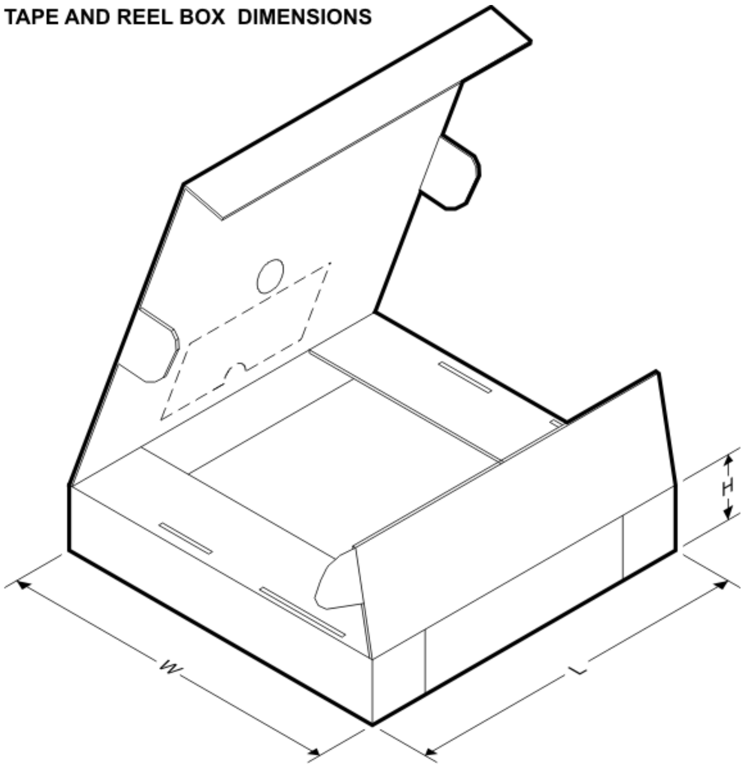


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV431ACM5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431ACM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431ACM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431AIM5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431AIM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431AIM5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431AIM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431AIMF	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LMV431AIMF/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LMV431AIMFX	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LMV431AIMFX/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LMV431BCM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431BCM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431BIMF	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LMV431BIMF/NOPB	SOT-23	DBZ	3	1000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LMV431BIMFX/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LMV431CM5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431CM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV431CM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431IM5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431IM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV431IM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

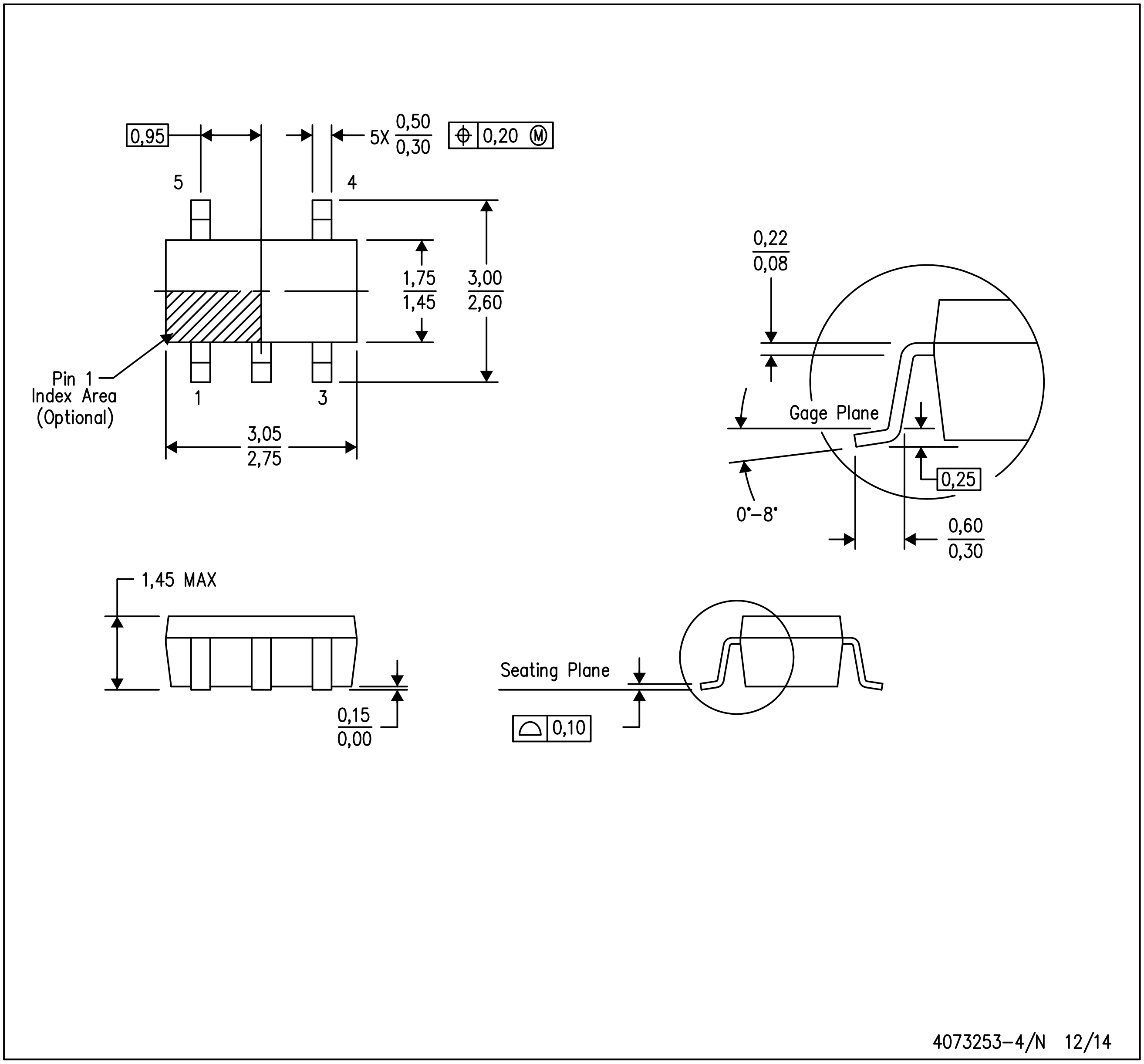


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV431ACM5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV431ACM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV431ACM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV431AIM5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV431AIM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV431AIM5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV431AIM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV431AIMF	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LMV431AIMF/NOPB	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LMV431AIMFX	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LMV431AIMFX/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LMV431BCM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV431BCM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

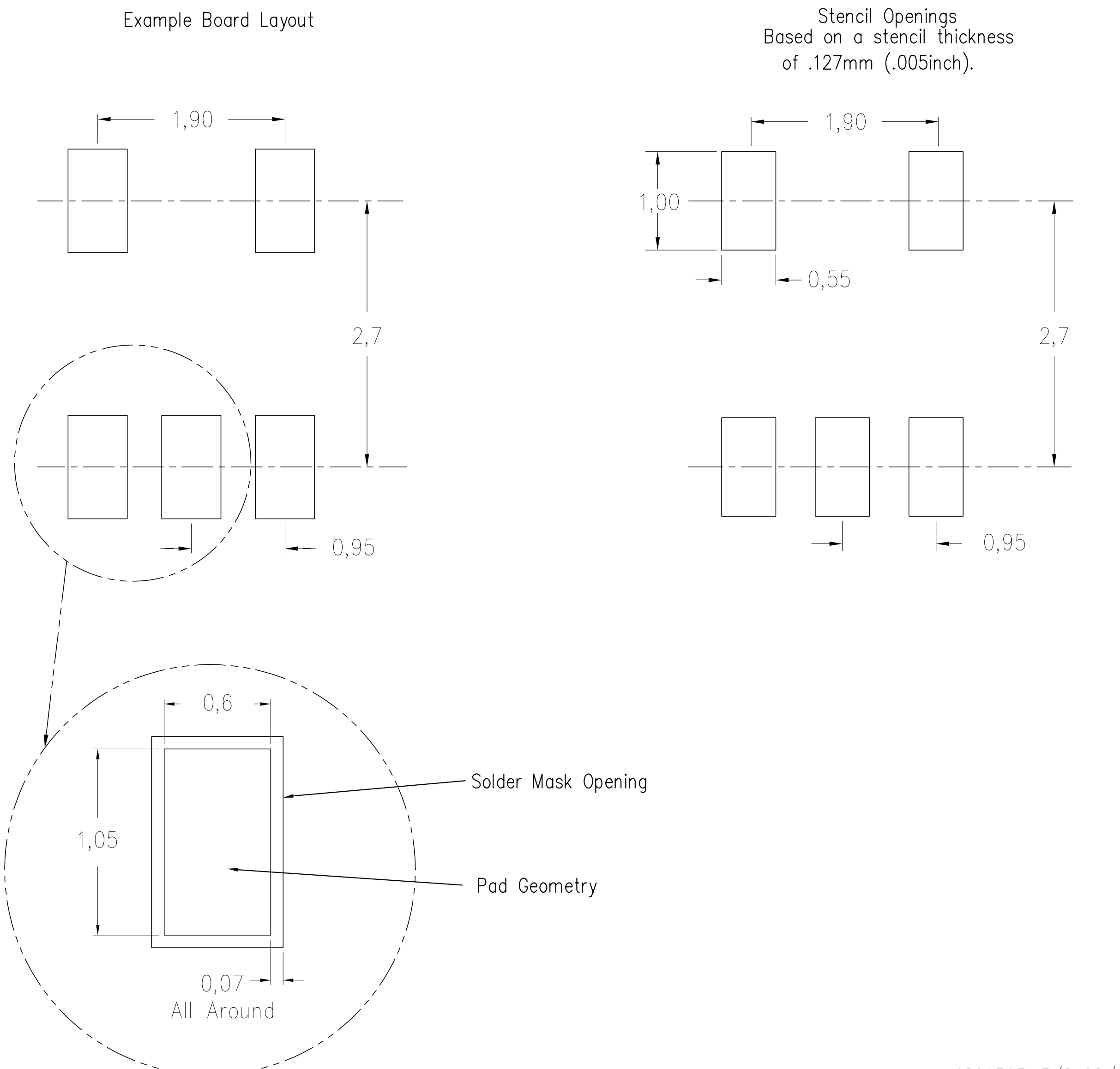
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV431BIMF	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LMV431BIMF/NOPB	SOT-23	DBZ	3	1000	210.0	185.0	35.0
LMV431BIMFX/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LMV431CM5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV431CM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV431CM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV431IM5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV431IM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV431IM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



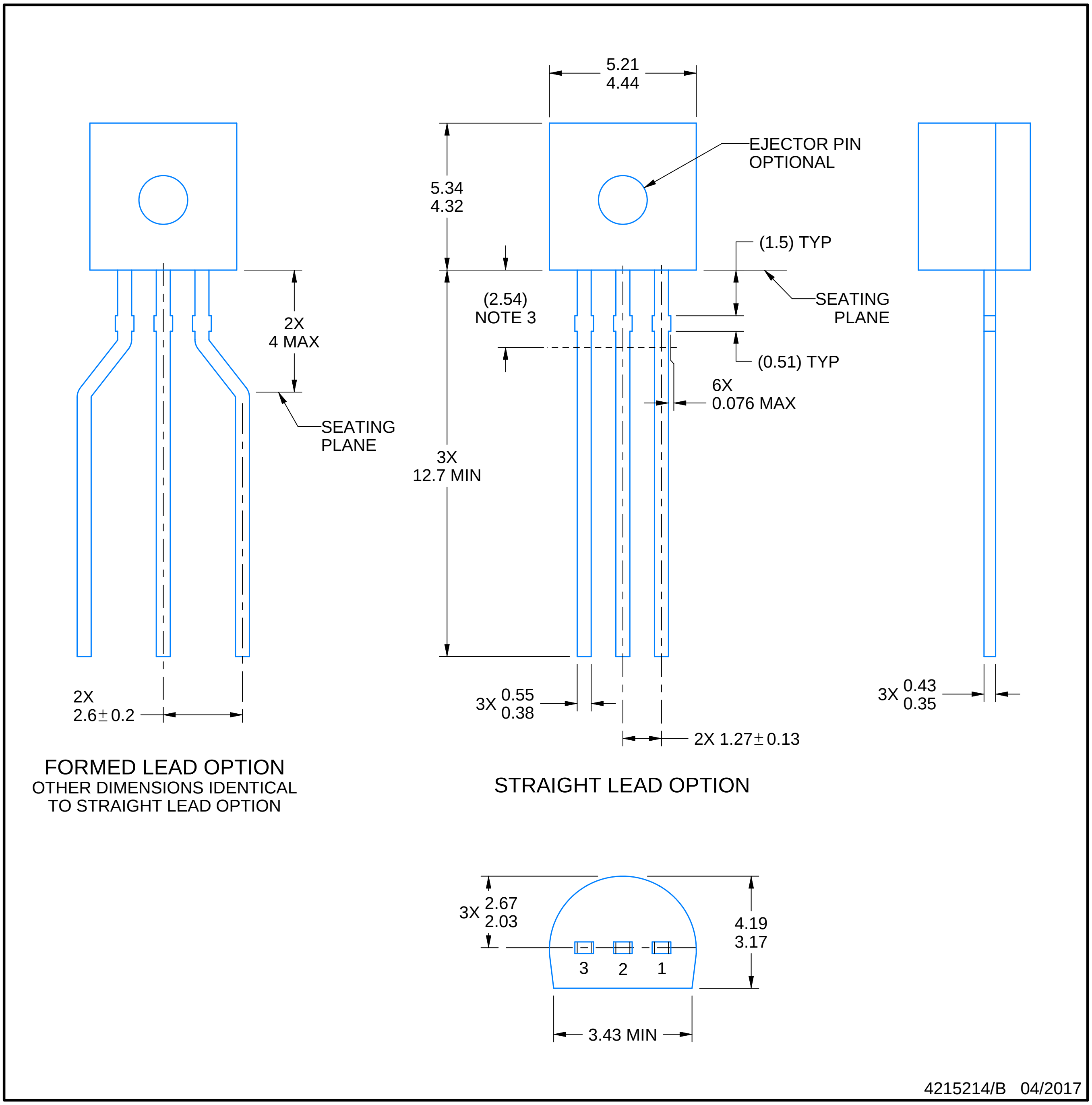
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



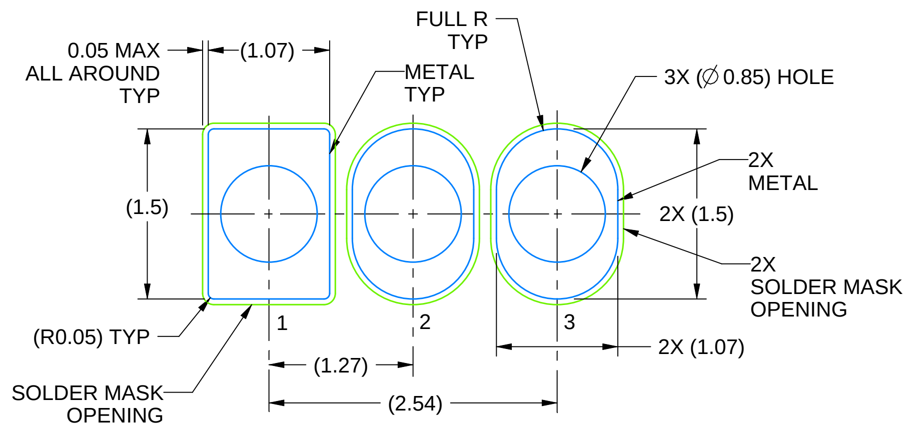
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

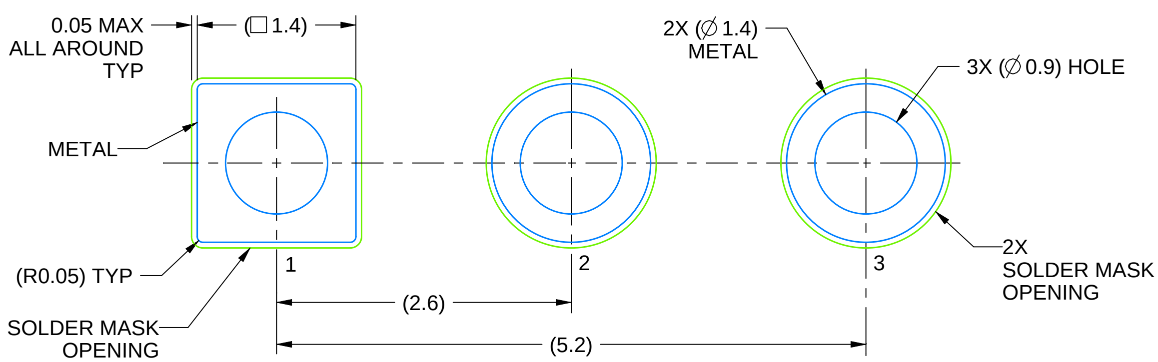


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.

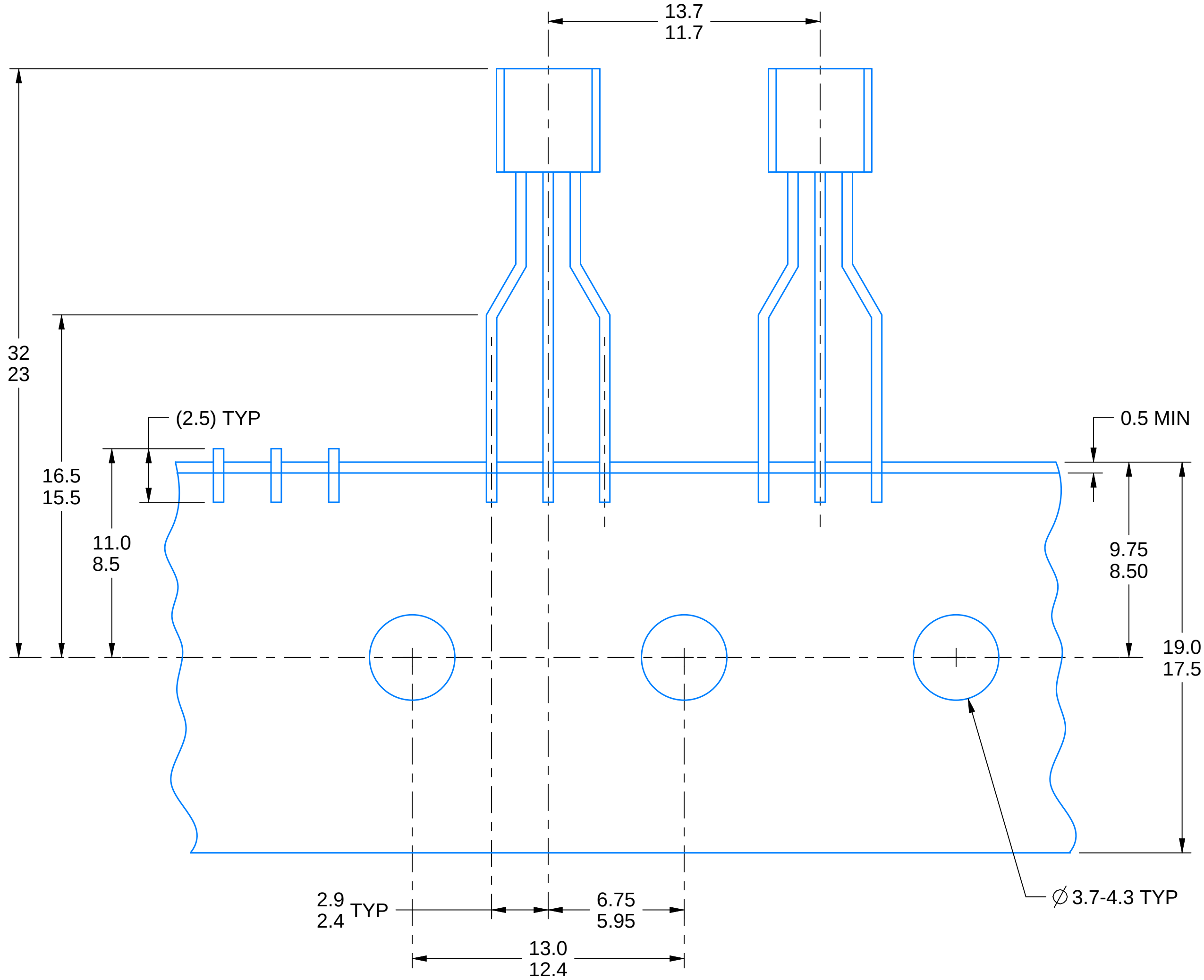


LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



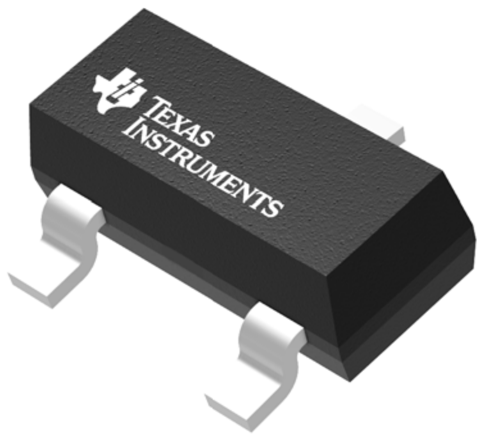
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

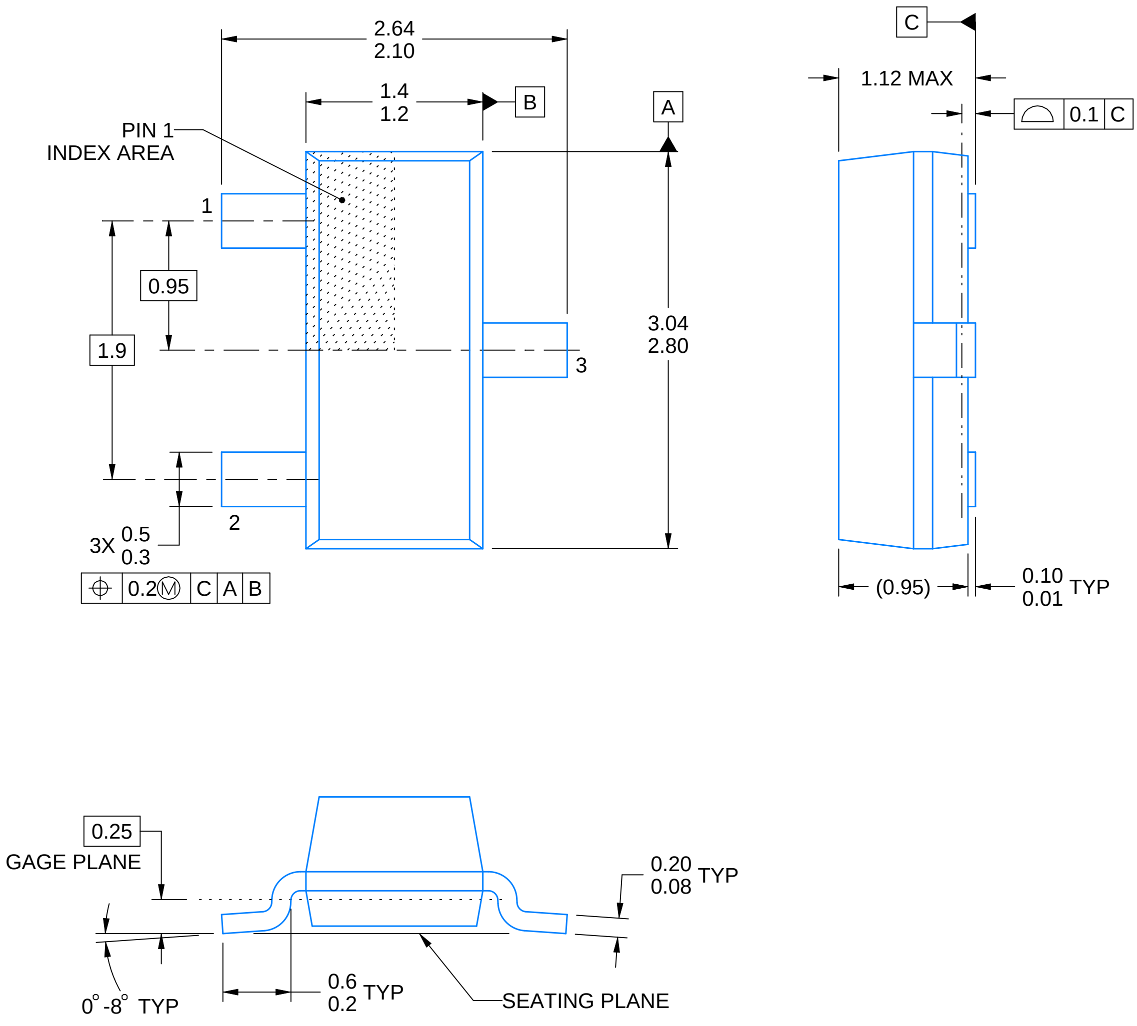


FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017



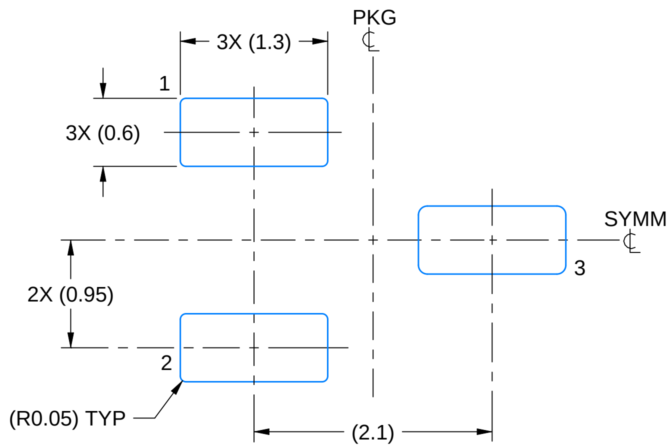
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



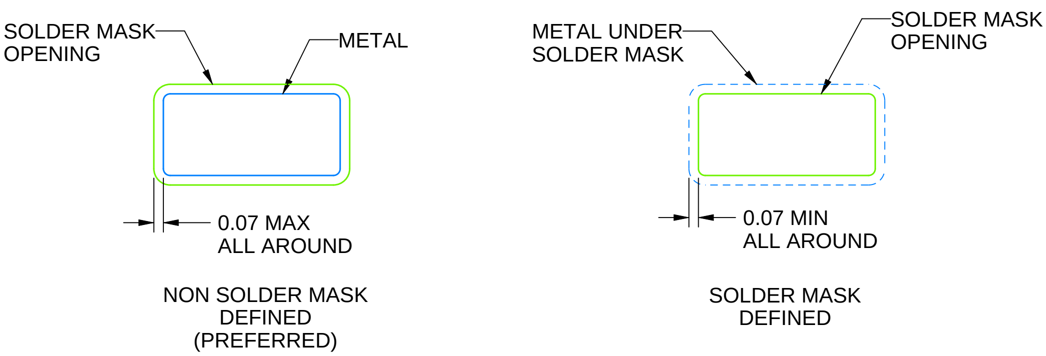
4214838/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.



LAND PATTERN EXAMPLE
SCALE:15X

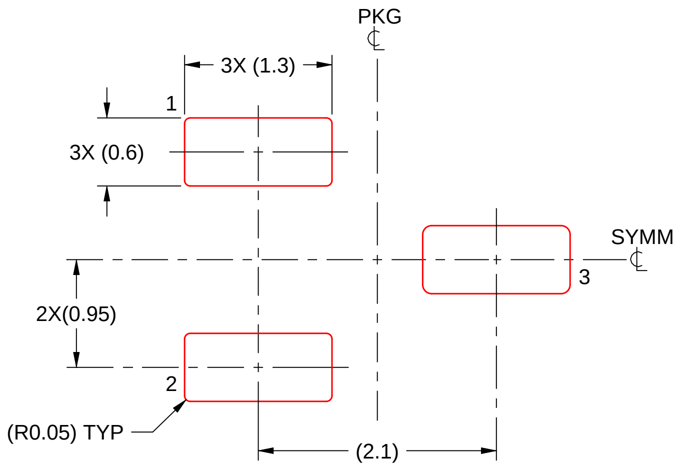


SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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