EVALUATION KIT AVAILABLE

TC7660S

SUPER CHARGE PUMP DC-TO-DC VOLTAGE CONVERTER

FEATURES

- **Oscillator boost from 10kHz to 45kHz**
- **Converts +5V Logic Supply to ±5V System**
- **Wide Input Voltage Range ..... 1.5V to 12V**
- **Efficient Voltage Conversion 99.9%**
- **Excellent Power Efficiency 98%**
- **Low Power Supply ..... 80μA @ 5 V_{IN}**
- **Low Cost and Easy to Use**
  — Only Two External Capacitors Required
- **Available in Small Outline (SOIC) Package**
- **Improved ESD Protection ..... Up to 10kV**
- **No External Diode Required for High Voltage Operation**

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC7660SCOA	8-Pin SOIC	0°C to +70°C
TC7660SCPA	8-Pin Plastic DIP	0°C to +70°C
TC7660SEJA	8-Pin CerDIP	– 40°C to +85°C
TC7660SEOA	8-Pin SOIC	– 40°C to +85°C
TC7660SEPA	8-Pin Plastic DIP	– 40°C to +85°C
TC7660SMJA	8-Pin CerDIP	– 55°C to +125°C
TC7660EV	***Evaluation Kit for Charge Pump Family***	

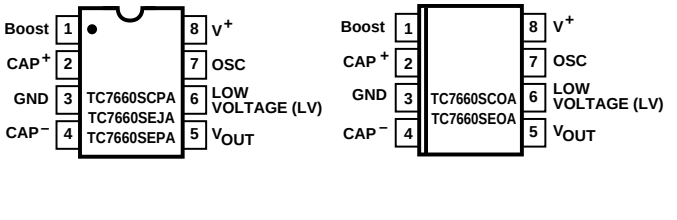
GENERAL DESCRIPTION

The TC7660S is a pin-compatible upgrade to the Industry standard TC7660 charge pump voltage converter. It converts a +1.5V to +12V input to a corresponding -1.5V to -12V output using only two low-cost capacitors, eliminating inductors and their associated cost, size and EMI. Added features include an extended supply range to 12V, and a frequency boost pin for higher operating frequency, allowing the use of smaller external capacitors.

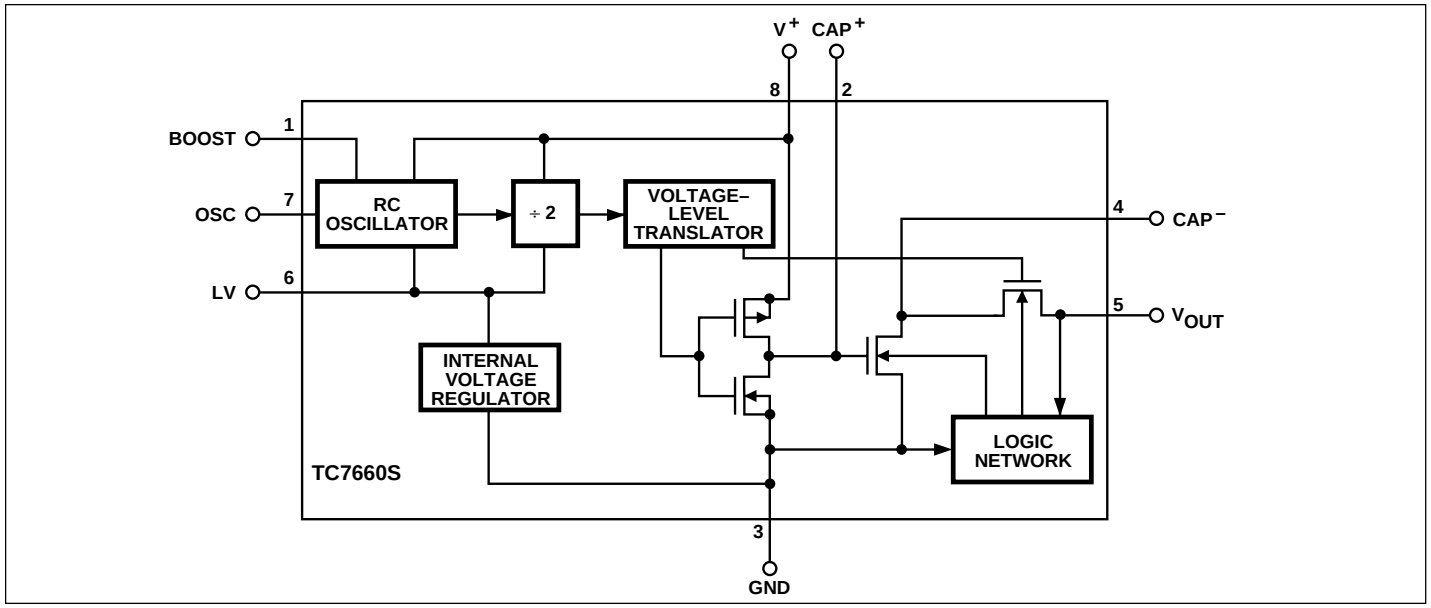
The on-board oscillator operates at a nominal frequency of 10kHz. Frequency is increased to 45kHz when pin 1 is connected to V+. Operation below 10kHz (for lower supply current applications) is possible by connecting an external capacitor from OSC to ground (with pin 1 open).

The TC7660S is available in both 8-pin DIP and 8-pin small outline (SOIC) packages in commercial and extended temperature ranges.

PIN CONFIGURATION (DIP AND SOIC)



FUNCTIONAL BLOCK DIAGRAM



TC7660S

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ..... +13V
LV, Boost, OSC Inputs
Voltage (Note 1) ..... – 0.3V to (V^+ +0.3V) for V^+ < 5.5V
(V^+ – 5.5V) to (V^+ +0.3V) for V^+ > 5.5V
Current Into LV (Note 1) ..... 20µA for V^+ > 3.5V
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) ..... Continuous
Power Dissipation ($T_A \leq 70°C$) (Note 2)
CerDIP 800mW
Plastic DIP 730mW
SOIC 470mW

Operating Temperature Range
C Suffix ..... 0°C to +70°C
E Suffix ..... – 40°C to +85°C
M Suffix ..... – 55°C to +125°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

T_A = +25°C, V^+ = 5V, C_{OSC} = 0, Test Circuit (Figure 1), unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I^+	Supply Current (Boost pin OPEN or GND)	$R_L = \infty$	—	80	160	µA
		0°C ≤ T_A ≤ +70°C	—	—	180	
		– 40°C ≤ T_A ≤ +85°C	—	—	180	
		– 55°C ≤ T_A ≤ +125°C	—	—	200	
I^+	Supply Current (Boost pin = V^+)	0°C ≤ T_A ≤ +70°C	—	—	300	µA
		– 40°C ≤ T_A ≤ +85°C	—	—	350	
		– 55°C ≤ T_A ≤ +125°C	—	—	400	
V^+_H	Supply Voltage Range, High	Min ≤ T_A ≤ Max, R_L = 10kΩ, LV Open	3	—	12	V
V^+_L	Supply Voltage Range, Low	Min ≤ T_A ≤ Max, R_L = 10kΩ, LV to GND	1.5	—	3.5	V
R_{OUT}	Output Source Resistance	I_{OUT} = 20mA	—	60	100	Ω
		I_{OUT} = 20mA, 0°C ≤ T_A ≤ +70°C	—	70	120	
		I_{OUT} = 20mA, – 40°C ≤ T_A ≤ +85°C	—	70	120	
		I_{OUT} = 20mA, – 55°C ≤ T_A ≤ +125°C	—	105	150	
		V^+ = 2V, I_{OUT} = 3mA, LV to GND				
		0°C ≤ T_A ≤ +70°C	—	—	250	Ω
		– 55°C ≤ T_A ≤ +125°C	—	—	400	
F_{OSC}	Oscillator Frequency	Pin 7 open; Pin 1 open or GND	—	10	—	kHz
		Boost Pin = V^+	—	45	—	
P_{EFF}	Power Efficiency	R_L = 5 kΩ; Boost Pin Open	96	98	—	%
		$T_{MIN} \leq T_A \leq T_{MAX}$; Boost Pin Open	95	98	—	
		Boost Pin = V^+	—	88	—	
V_{OUT} E_{FF}	Voltage Conversion Efficiency	$R_L = \infty$	99	99.9	—	%
Z_{OSC}	Oscillator Impedance	V^+ = 2V	—	1	—	MΩ
		V^+ = 5V	—	100	—	kΩ

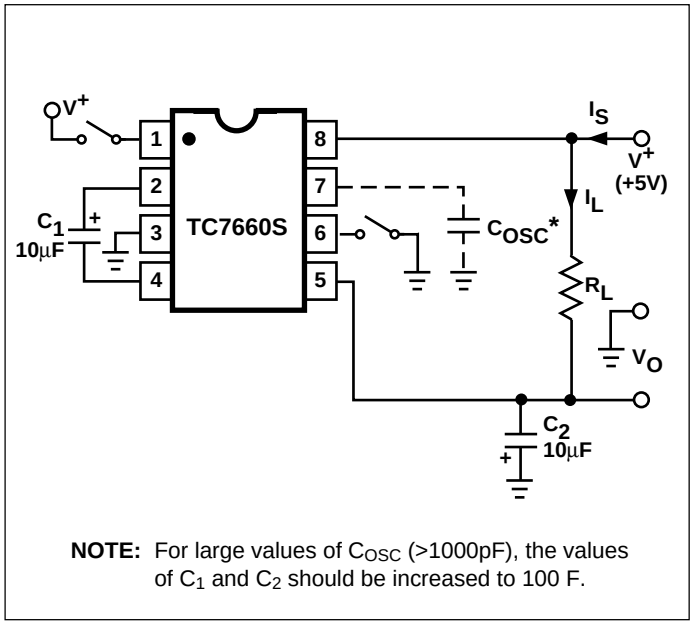
NOTES: 1. Connecting any input terminal to voltages greater than V^+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the TC7660S.
2. Derate linearly above 50°C by 5.5mW/°C.

Detailed Description

The TC7660S contains all the necessary circuitry to implement a voltage inverter, with the exception of two external capacitors, which may be inexpensive 10 µF polarized electrolytic capacitors. Operation is best understood by considering Figure 2, which shows an idealized voltage inverter. Capacitor C_1 is charged to a voltage V^+ for the half cycle when switches S_1 and S_3 are closed. (**Note:** Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 negatively by V+ volts. Charge is then transferred from C_1 to C_2, such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2.

The four switches in Figure 2 are MOS power switches; S_1 is a P-channel device, and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse-biased with respect to their sources, but not so much as to degrade their ON resistances. In addition, at circuit start-up, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this will result in high power losses and probable device latch-up.

This problem is eliminated in the TC7660S by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.



NOTE: For large values of C_{OSC} (>1000pF), the values of C_1 and C_2 should be increased to 100 F.

Figure 1. TC7660S Test Circuit

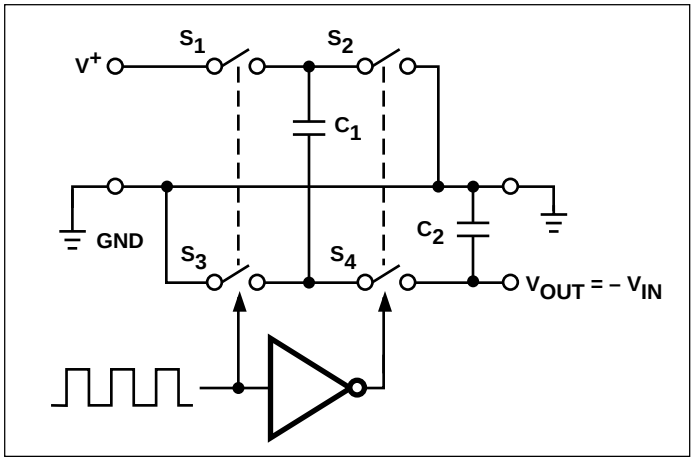


Figure 2. Idealized Charge Pump Inverter

The voltage regulator portion of the TC7660S is an integral part of the anti-latch-up circuitry. Its inherent voltage drop can, however, degrade operation at low voltages. To improve low-voltage operation, the “LV” pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure latch-up-proof operation and prevent device damage.

Theoretical Power Efficiency Considerations

In theory, a capacitive charge pump can approach 100% efficiency if certain conditions are met:

(1) The drive circuitry consumes minimal power.

(2) The output switches have extremely low ON resistance and virtually no offset.

(3) The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TC7660S approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 2) compared to the value of R_L, there will be a substantial difference in voltages V_1 and V_2. Therefore, it is desirable not only to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

TC7660S

Dos and Don'ts

- Do not exceed maximum supply voltages.
- Do not connect the LV terminal to GND for supply voltages greater than 3.5V.
- Do not short circuit the output to V^+ supply for voltages above 5.5V for extended periods; however, transient conditions including start-up are okay.
- When using polarized capacitors in the inverting mode, the + terminal of C_1 must be connected to pin 2 of the TC7660S and the + terminal of C_2 must be connected to GND.

Simple Negative Voltage Converter

Figure 3 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5V to +12V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5V.

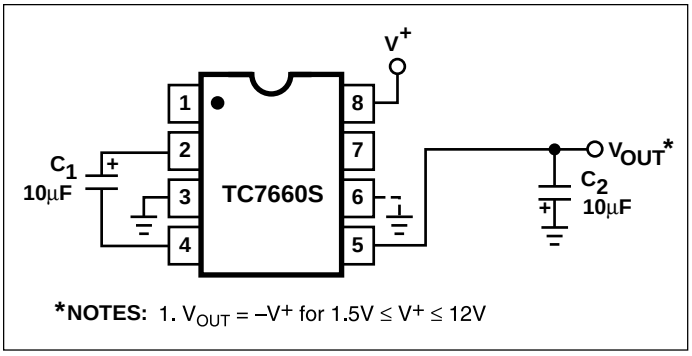


Figure 3. Simple Negative Converter

The output characteristics of the circuit in Figure 3 are those of a nearly ideal voltage source in series with 70Ω. Thus, for a load current of –10mA and a supply voltage of +5V, the output voltage would be – 4.3V.

The dynamic output impedance of the TC7660S is due, primarily, to capacitive reactance of the charge transfer capacitor (C_1). Since this capacitor is connected to the output for only 1/2 of the cycle, the equation is:

$$X_C = \frac{2}{2\pi f\, C_1} = 3.18\Omega,$$

where f = 10kHz and C_1 = 10µF.

Paralleling Devices

Any number of TC7660S voltage converters may be paralleled to reduce output resistance (Figure 4). The reservoir capacitor, C_2, serves all devices, while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\ (\text{of TC7660S})}{n\ (\text{number of devices})}$$

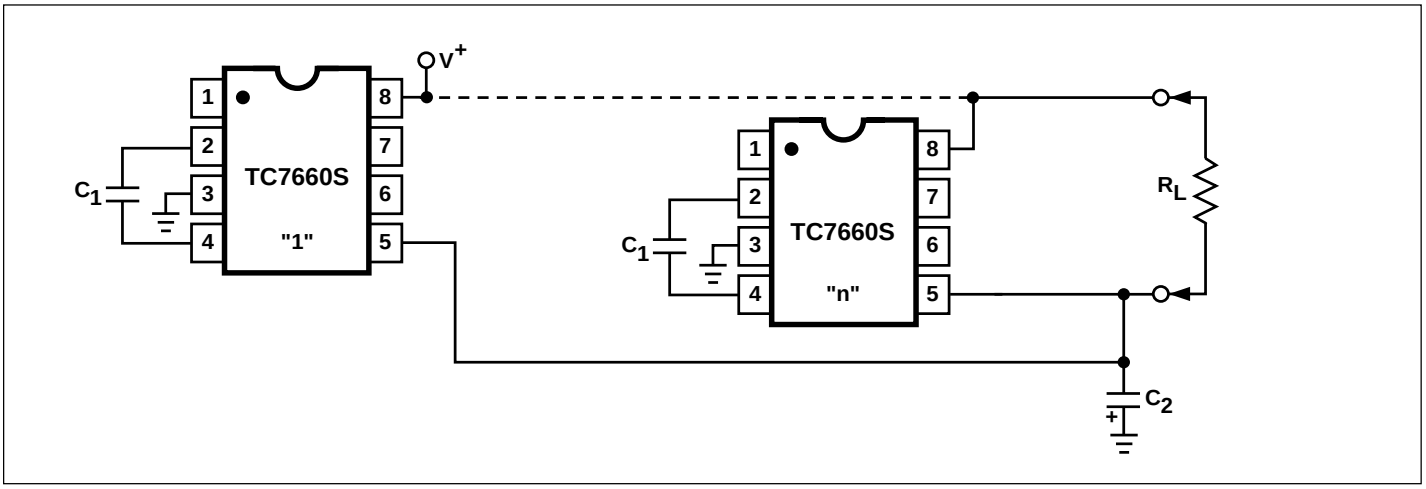


Figure 4. Paralleling Devices Lowers Output Impedance

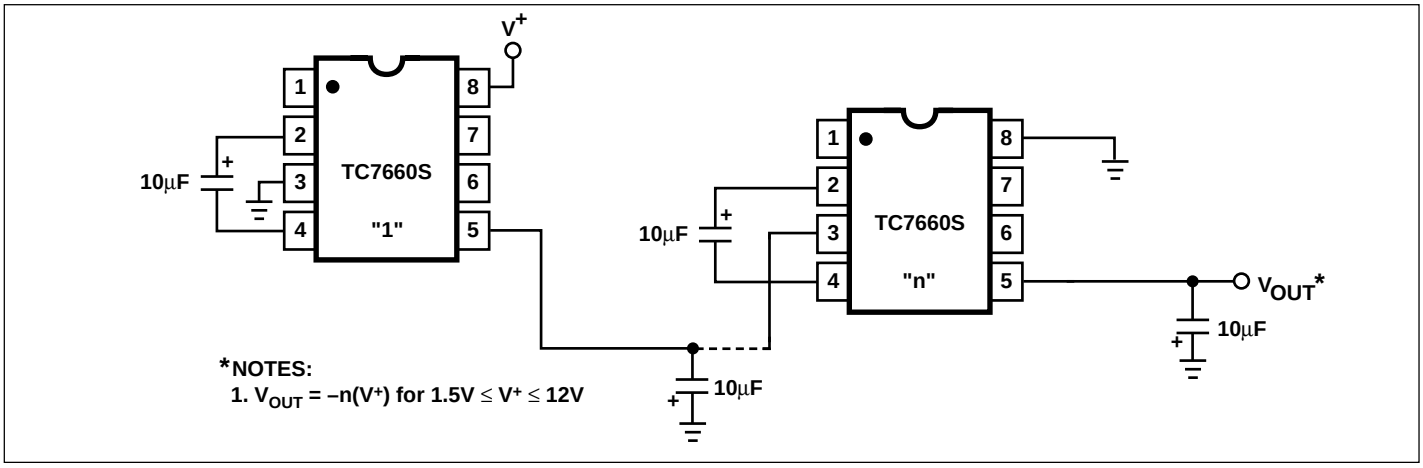


Figure 5. Increased Output Voltage by Cascading Devices

Cascading Devices

The TC7660S may be cascaded as shown (Figure 5) to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\,(V_{IN})$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TC7660S R_{OUT} values.

Changing the TC7660S Oscillator Frequency

It may be desirable in some applications (due to noise or other considerations) to increase the oscillator frequency. Pin 1, frequency boost pin may be connected to V^+ to increase oscillator frequency to 45kHz from a nominal of 10kHz for an input supply voltage of 5.0 volts. The oscillator may also be synchronized to an external clock as shown in Figure 6. In order to prevent possible device latch-up, a 1kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pull-up resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be ½ of the clock frequency. Output transitions occur on the positive-going edge of the clock.

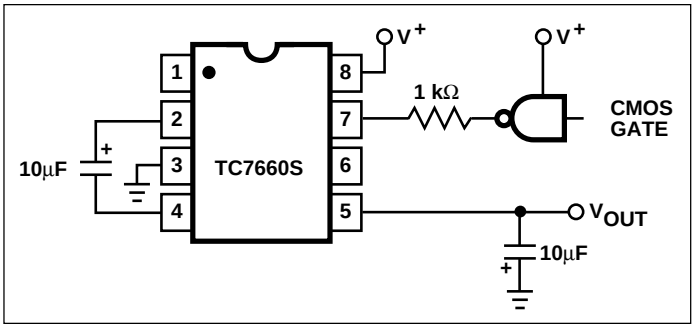


Figure 6. External Clocking

It is also possible to increase the conversion efficiency of the TC7660S at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 7. Lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and the reservoir (C_2) capacitors. To overcome this, increase the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (OSC) and pin 8 (V^+) will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and necessitate a corresponding increase in the values of C_1 and C_2 (from 10µF to 100µF).

Positive Voltage Multiplication

The TC7660S may be employed to achieve positive voltage multiplication using the circuit shown in Figure 8. In this application, the pump inverter switches of the TC7660S are used to charge C_1 to a voltage level of $V^+ – V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2V^+) – (2V_F)$, or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for V^+ = 5V and an output current of 10mA, it will be approximately 60Ω.

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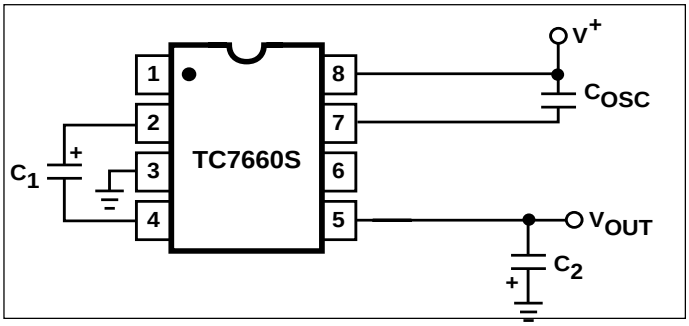


Figure 7. Lowering Oscillator Frequency

Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 9 combines the functions shown in Figures 3 and 8 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9V and – 5V from an existing +5V supply. In this instance, capacitors C_1 and C_3 perform the pump and reservoir functions, respectively, for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir, respectively, for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

Efficient Positive Voltage Multiplication/Conversion

Since the switches that allow the charge pumping operation are bidirectional, the charge transfer can be performed backwards as easily as forwards. Figure 10 shows a TC7660S transforming – 5V to +5V (or +5V to +10V, etc.). The only problem here is that the internal clock and switch-drive section will not operate until some positive voltage has been generated. An initial inefficient pump, as shown in Figure 9, could be used to start this circuit up, after which it will bypass the other (D_1 and D_2 in Figure 9 would never turn on), or else the diode and resistor shown dotted in Figure 10 can be used to "force" the internal regulator on.

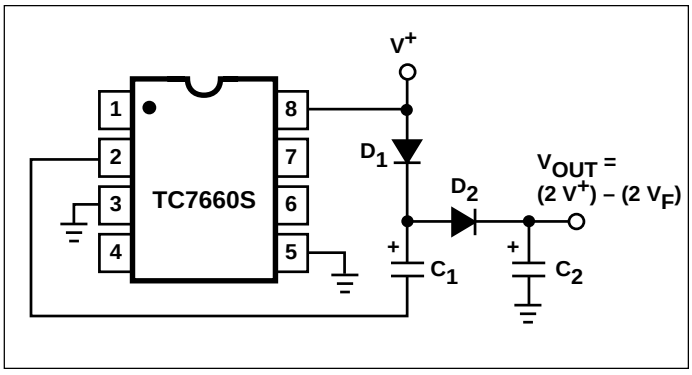


Figure 8. Positive Voltage Multiplier

Voltage Splitting

The same bidirectional characteristics used in Figure 10 can also be used to split a higher supply in half, as shown in Figure 11. The combined load will be evenly shared between the two sides. Once again, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 5, +15V can be converted (via +7.5V and – 7.5V) to a nominal –15V, though with rather high series resistance (~250Ω).

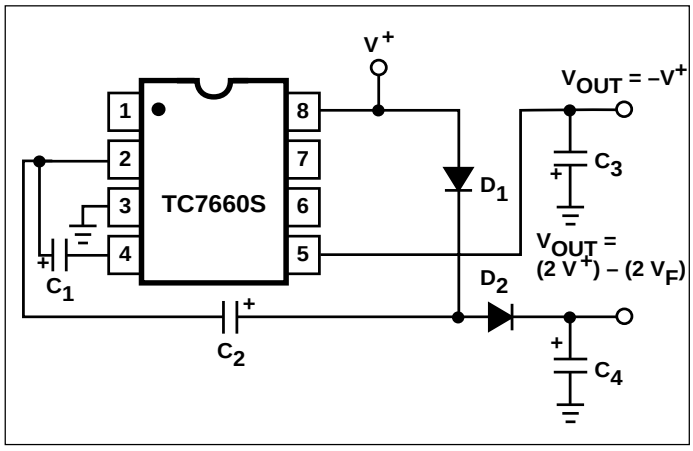


Figure 9. Combined Negative Converter and Positive Multiplier

Negative Voltage Generation for Display ADCs

The TC7106 is designed to work from a 9V battery. With a fixed power supply system, the TC7106 will perform conversions with input signal referenced to power supply ground.

Negative Supply Generation for 4½ Digit Data Acquisition System

The TC7135 is a 4½ digit ADC operating from ±5V supplies. The TC7660S provides an inexpensive –5V source. (See AN16 and AN17 for TC7135 interface details and software routines.)

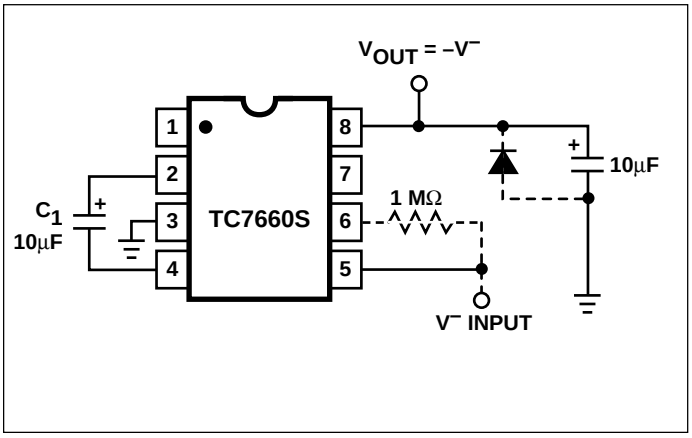


Figure 10. Positive Voltage Multiplier

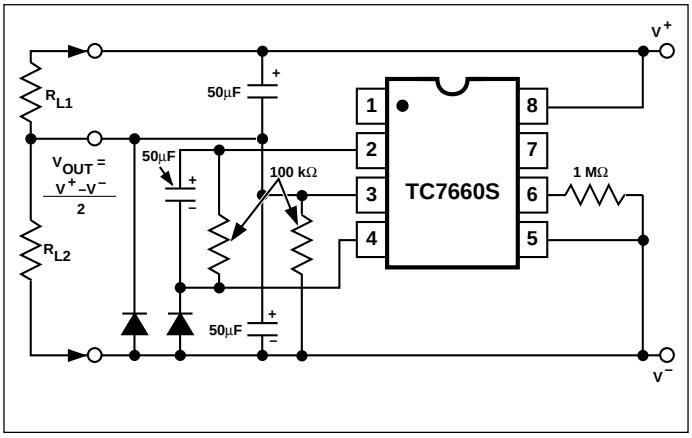
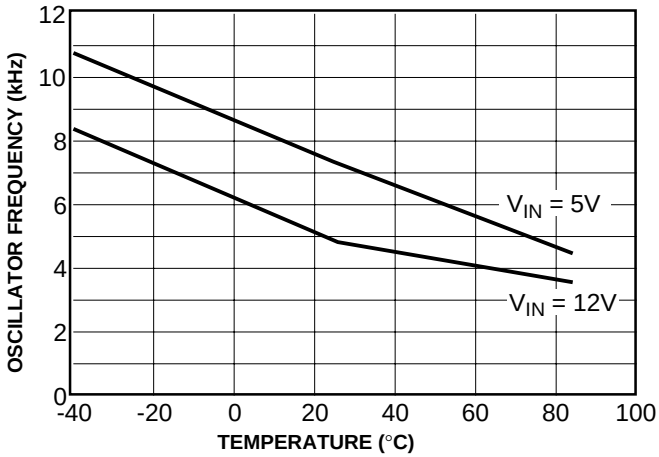


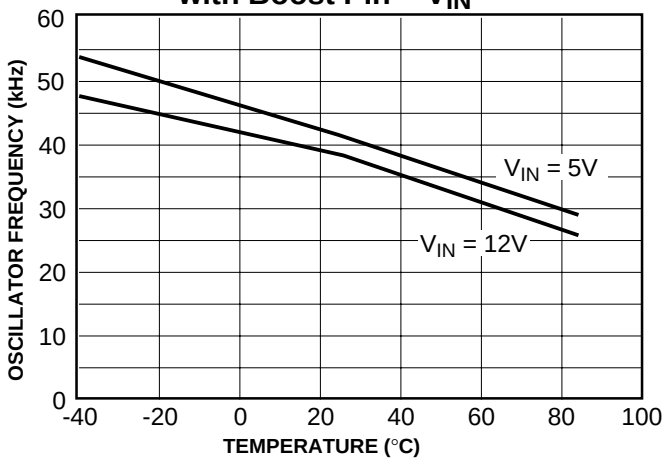
Figure 11. Splitting a Supply in Half

TYPICAL CHARACTERISTICS

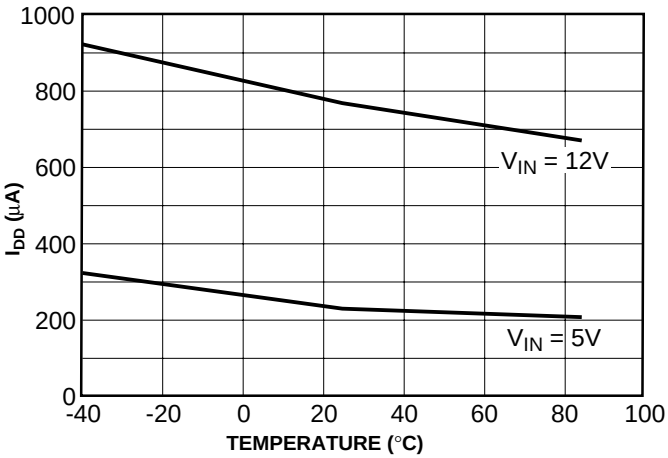
Unloaded Osc Freq vs. Temperature



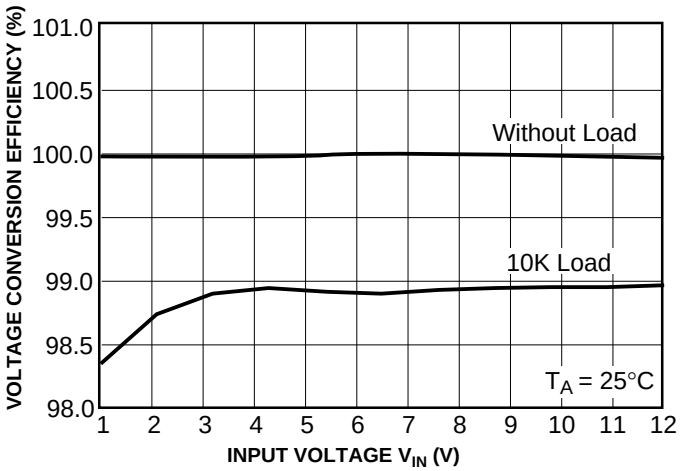
Unloaded Osc Freq vs. Temperature with Boost Pin = V_{IN}



Supply Current vs. Temperature (with Boost Pin = V_{IN})



Voltage Conversion



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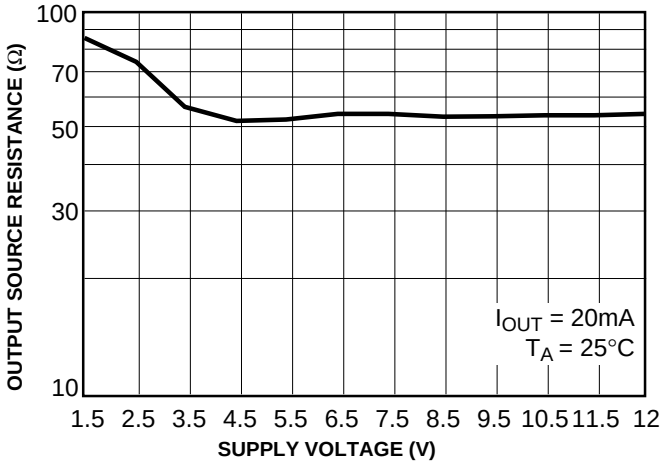
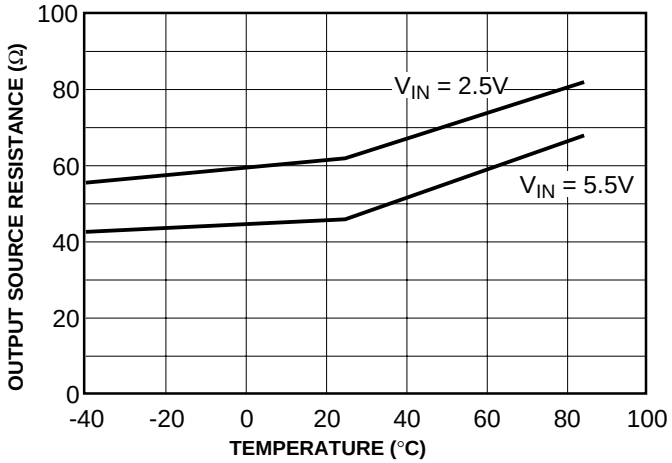
TYPICAL CHARACTERISTICS (Cont.)

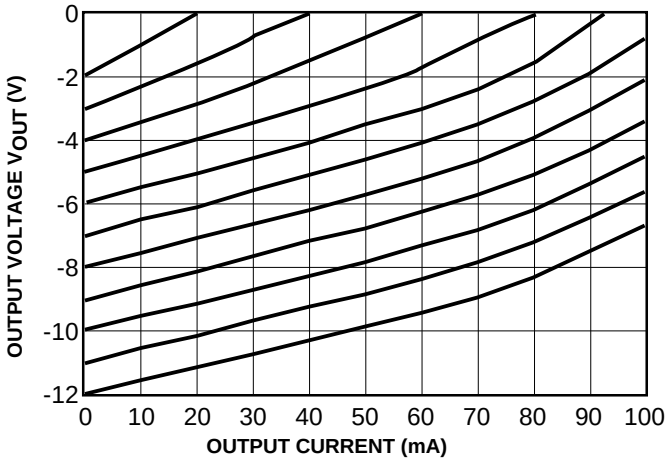
Output Source Resistance vs. Supply Voltage



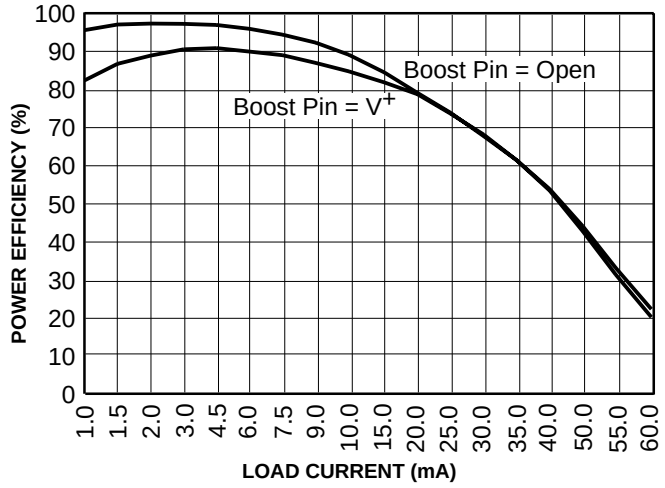
Output Source Resistance vs. Temperature



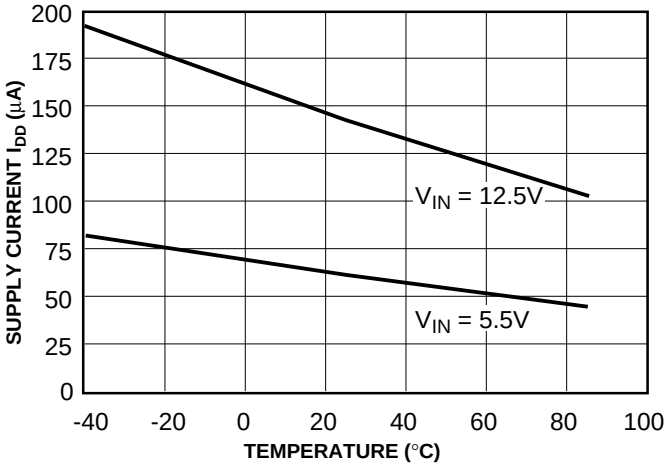
Output Voltage vs. Output Current



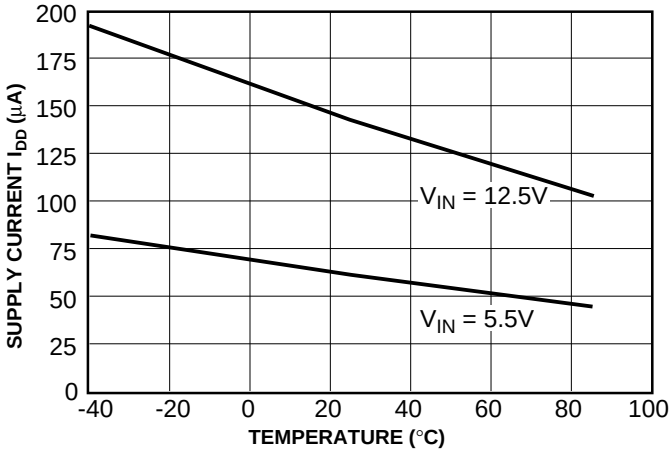
Power Conversion Efficiency vs. Load



Supply Current vs. Temperature

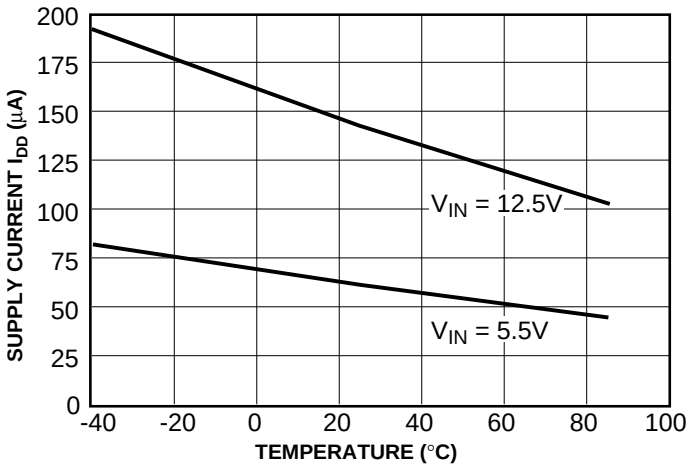


Supply Current vs. Temperature



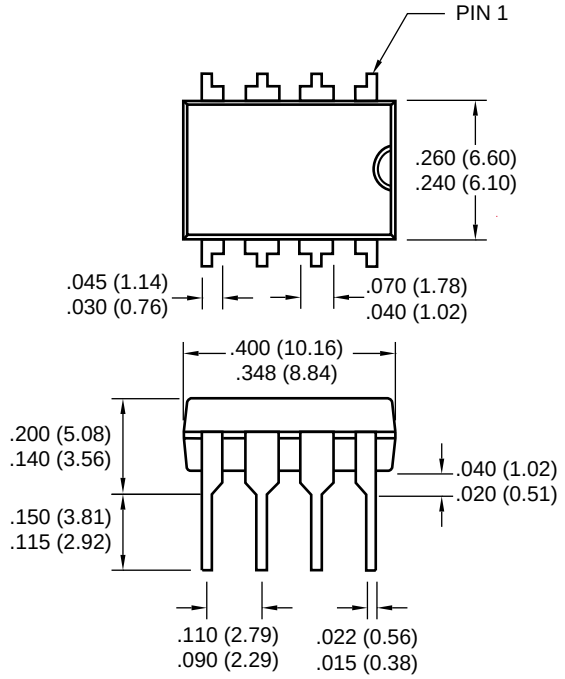
TYPICAL CHARACTERISTICS (Cont.)

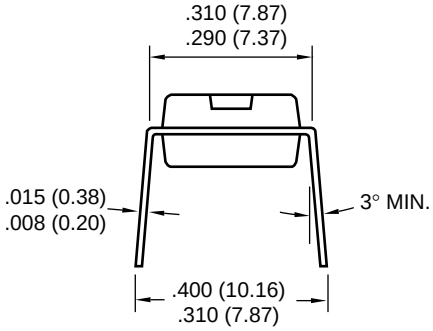
Supply Current vs. Temperature



PACKAGE DIMENSIONS

8-Pin Plastic DIP





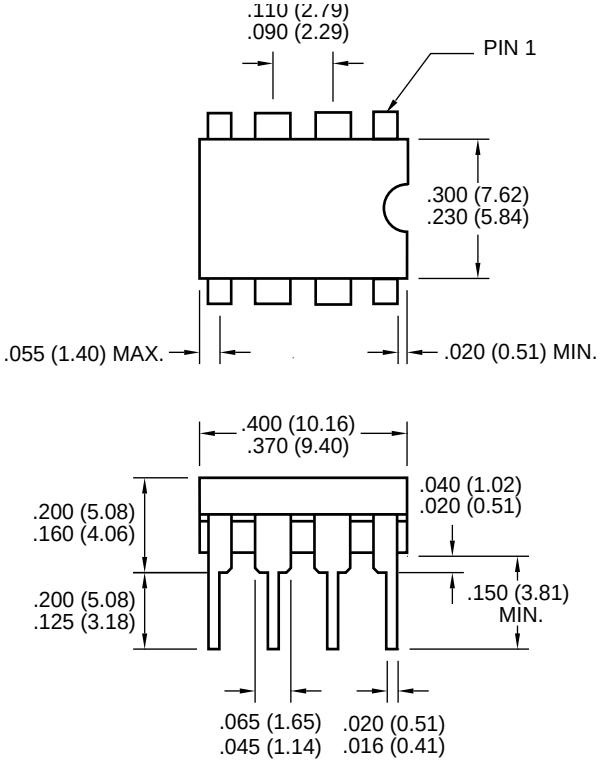
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Dimensions: inches (mm)

TC7660S

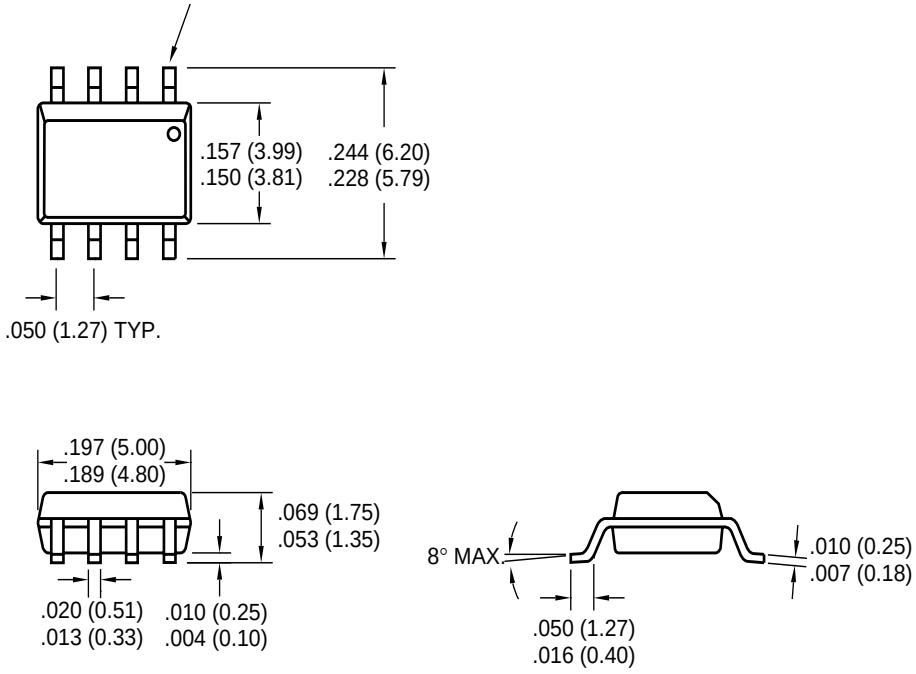
PACKAGE DIMENSIONS (CONT.)

8-Pin CerDIP



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

8-Pin Plastic SOIC



Dimensions: inches (mm)

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