TPS56C215 4.5-V to 17-V Input , 12-A Synchronous Step-Down SWIFT™ Converter

1 Features

- Integrated 13.5-mΩ and 4.5-mΩ MOSFETs
- Support 14-A Continuous I_{OUT}
- Reference Voltage: 600 mV with ±1% Tolerance from –40°C to 150°C Junction Temperature
- Output Voltage Range: 0.6 V to 5.5 V
- Supports All Ceramic Output Capacitors
- D-CAP3™ Control Mode for Fast Transient Response
- Selectable Forced Continuous Conduction Mode (FCCM) or Auto-Skipping Eco-mode™ for High Light-Load Efficiency
- Selectable F_{SW} of 400 kHz, 800 kHz and 1.2 MHz
- Monotonic Start Up into Pre-biased Outputs
- Three Adjustable Current Limit Settings with Cycle-by-Cycle Over-Current Limiting Control
- External 5V bias for enhanced efficiency
- Adjustable Soft Start with a Default 1-ms Soft Start Time
- –40°C to 150°C Operating junction temperature
- Small 3.5-mm x 3.5-mm HotRod™ QFN Package
- Supported at the WEBENCH™ Design Center

2 Applications

- Server, Cloud-Computing, Storage
- Telecom & Networking, Point-of-Load (POL)
- IPCs, Factory Automation, PLC, Test Measurement
- High end DTV

3 Description

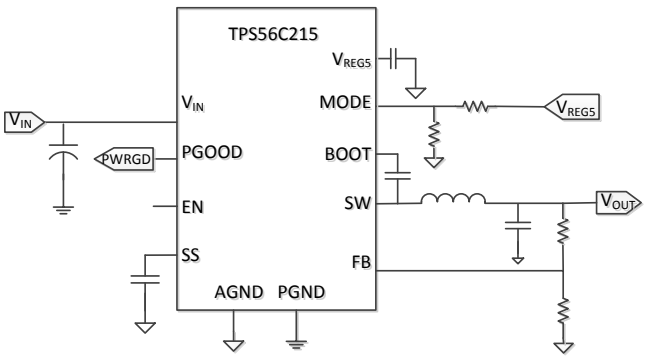
The TPS56C215 is a small-sized, synchronous buck converter with an adaptive on-time D-CAP3™ control mode. The device offers ease-of-use and low bill-of material count for space-conscious power systems. This device features high-performance low RDSon integrated MOSFETs, accurate 0.6-V reference, and an integrated boost switch. Competitive features include very-low external-component count, fast load transient response, auto-skip mode operation, internal soft-start control, and no requirement for external compensation. A forced continuous conduction mode helps meet tight voltage regulation accuracy requirements for performance DSPs and FPGAs. The TPS56C215 is available in a thermally enhanced 18-pin HotRod™ QFN package and is specified from –40°C to 150°C junction temperature.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS56C215	VQFN (18)	3.5 mm x 3.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



Efficiency vs Output Current

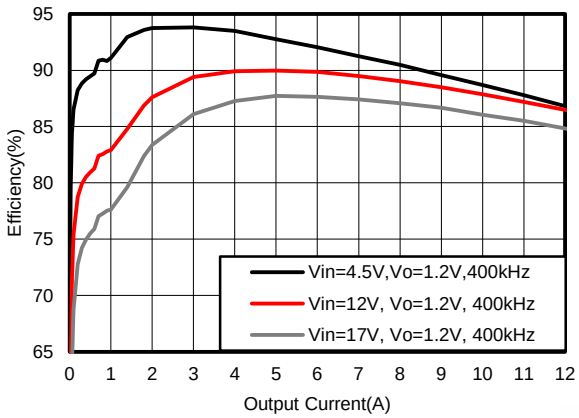


Table of Contents

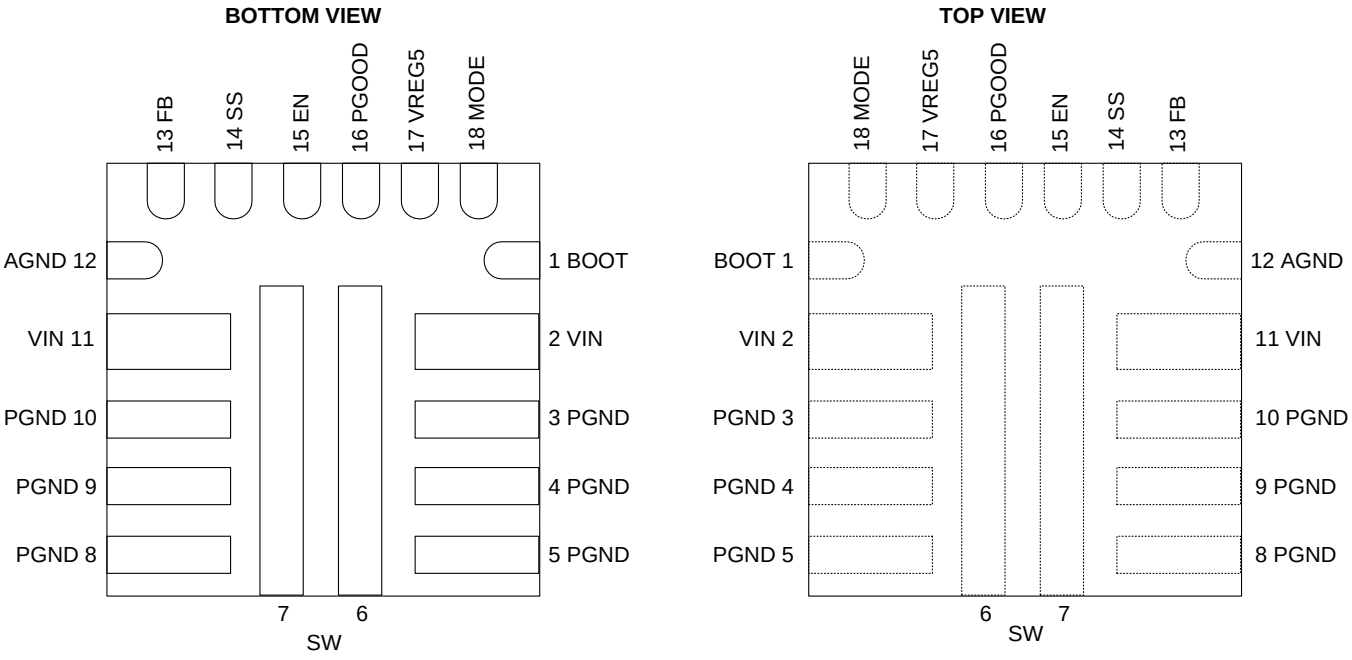
4 Revision History

Changes from Original (March 2016) to Revision A **Page**

- Added content for full Production data sheet ... 1

5 Pin Configuration and Functions

RNN Package
18-Pin VQFN



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect a 0.1uF ceramic capacitor between BOOT and SW.
VIN	2,11	P	Input voltage supply pin
PGND	3, 4, 5, 8, 9, 10	G	GND terminal for the controller circuit and the internal circuitry
SW	6, 7	O	Switch node
AGND	12	G	Ground of internal analog circuitry. Connect GND to PGND plane with a short trace.
FB	13	I	Converter feedback input. Connect to output voltage with resistor divider
SS	14	O	Connecting an external capacitor sets the SS time. If no external capacitor is connected the startup is with a default of 1 ms
EN	15	I	Enable input control, floats high.
PGOOD	16	O	Open Drain Power Good Indicator, becomes low if output voltage is low due to thermal shutdown, OV, EN shutdown or during SS.
VREG5	17	I/O	4.7-V LDO output that supplies internal circuitry and gate driver. Bypass it with a 4.7-µF capacitor. Can also be driven externally with a 5V input
MODE	18	I	Connect this pin to a resistor divider between VREG5 and GND for different options

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input Voltage	VIN	–0.3	20	V
	SW	–2	19	V
	SW(10 ns transient)	–3	20	V
	EN	–0.3	6.5	V
	BOOT –SW	–0.3	6.5	V
	BOOT	–0.3	25.5	V
	SS, MODE, FB	–0.3	6.5	V
	VREG5	–0.3	6	V
Output Voltage	PGOOD	–0.3	6.5	V
Output Current (2)	I_{OUT}		14	A
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) In order to be consistent with the TI reliability requirement of 100k Power-On-Hours at 105°C junction temperature, the output current should not exceed 14A continuously under 100% duty operation as to prevent electromigration failure in the solder. Higher junction temperature or longer power-on hours are achievable at lower than 14A continuos output current.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input Voltage	VIN	4.5		17	V
	SW	–1.8		17	V
	BOOT	–0.1		23.5	V
	VREG5	–0.1		5.2	V

6.4 Thermal Information

THERMAL METRIC (1)		RNN PACKAGE 18 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN=12V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	VIN supply current	T_J = 25°C, V_{EN}=5 V, non switching		600	700	µA
I_{VINSDN}	VIN shutdown current	T_J = 25°C, V_{EN}=0 V		7		µA
LOGIC THRESHOLD						
V_{ENH}	EN H-level threshold voltage		1.175	1.225	1.3	V
V_{ENL}	EN L-level threshold voltage		1.025	1.104	1.15	V
V_{ENHYS}				0.121		V
I_{ENp1}	EN pull-up current	V_{EN} = 1.0 V	0.35	1.91	2.95	µA
I_{ENp2}		V_{EN} = 1.3 V	3	4.197	5.5	µA
FEEDBACK VOLTAGE						
V_{FB}	FB voltage	T_J = 25°C	598	600	602	mV
		T_J = 0°C to 85°C	597.5	600	602.5	mV
		T_J = –40°C to 85°C	594	600	602.5	mV
		T_J = –40°C to 150°C	594	600	606	mV
LDO VOLTAGE						
VREG5	LDO Output voltage	T_J = –40°C to 150°C	4.58	4.7	4.83	V
ILIM5	LDO Output Current limit	T_J = –40°C to 150°C	100	150	200	mA
MOSFET						
$R_{DS(on)H}$	High side switch resistance	T_J = 25°C, V_{VREG5} = 4.7 V		13.5		mΩ
$R_{DS(on)L}$	Low side switch resistance	T_J = 25°C, V_{VREG5} = 4.7 V		4.5		mΩ
SOFT START						
I_{ss}	Soft start charge current	T_J = -40°C to 150°C	4.9	6	7.1	µA
CURRENT LIMIT						
I_{OCL}	Current Limit (Low side sourcing)	ILIM-1 option, Valley Current	9.775	11.5	13.225	A
		ILIM option, Valley Current	11.73	13.8	15.87	A
		ILIM+1 option, Valley Current	13.6	16	18.4	A
	Current Limit (Low side negative)	Valley Current		4		A
POWER GOOD						
$V_{PGOODTH}$	PGOOD threshold	V_{FB} falling (fault)		84%		
		V_{FB} rising (good)		93%		
		V_{FB} rising (fault)		116%		
		V_{FB} falling (good)		107%		
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP threshold	OVP detect		121% x V_{FB}		
V_{UVP}	Output UVP threshold	Hiccup detect		68% x V_{FB}		
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature		160		°C
		Hysteresis		15		°C
$T_{SDN\ VREG5}$	VREG5 thermal shutdown threshold	Shutdown temperature		171		°C
		Hysteresis		18		°C
UVLO						
UVLO	UVLO threshold	VREG5 rising voltage		4.3		V
		VREG5 falling voltage		3.57		V
		VREG5 hysteresis		730		mV

6.6 Timing Requirements

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ON-TIME TIMER CONTROL						
t_{ON}	SW On Time	VIN = 2 V, V_{OUT}=3.3 V, F_{SW} = 800 kHz	310	340	380	ns
$t_{ON\ min}$	SW Minimum on time	VIN = 17 V, V_{OUT}=0.6 V, F_{SW}= 1200 kHz		54		ns
t_{OFF}	SW Minimum off time	25°C, V_{FB}=0.5 V			310	ns
SOFT START						
t_{SS}	Soft start time	Internal soft start time		1.045		ms
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
t_{UVPDEL}	Output Hiccup delay relative to SS time	UVP detect		1		cycle
t_{UVPEN}	Output Hiccup enable delay relative to SS time	UVP detect		7		cycle

6.7 Typical Characteristics

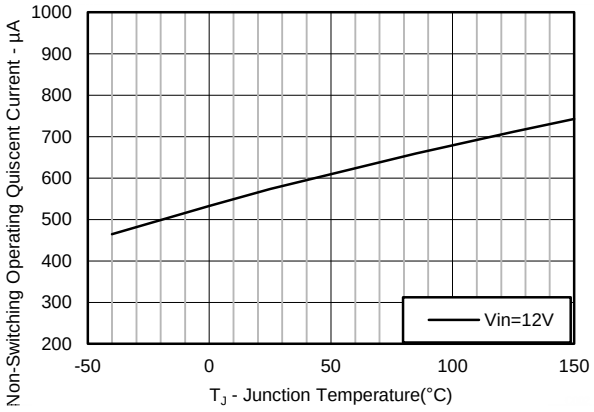


Figure 1. Quiescent Current vs Temperature

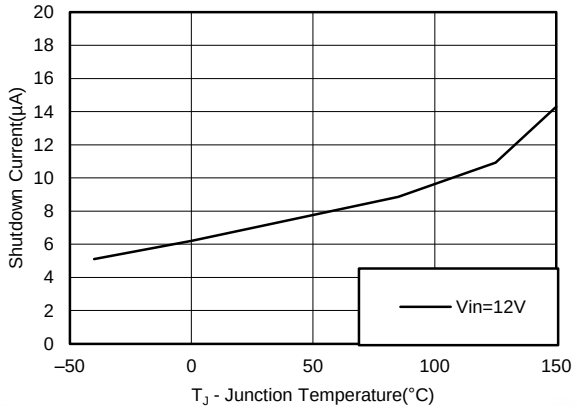


Figure 2. Shutdown Current vs Temperature

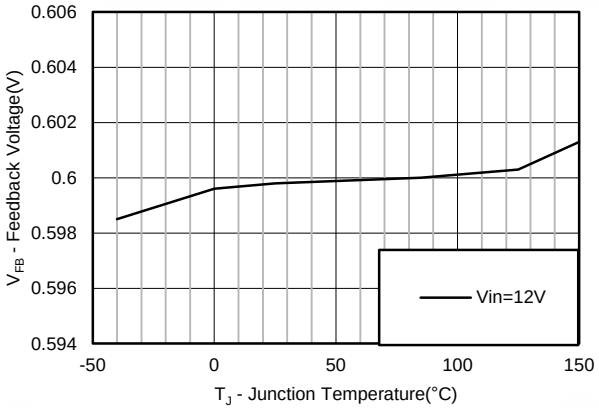


Figure 3. Feedback Voltage vs Temperature

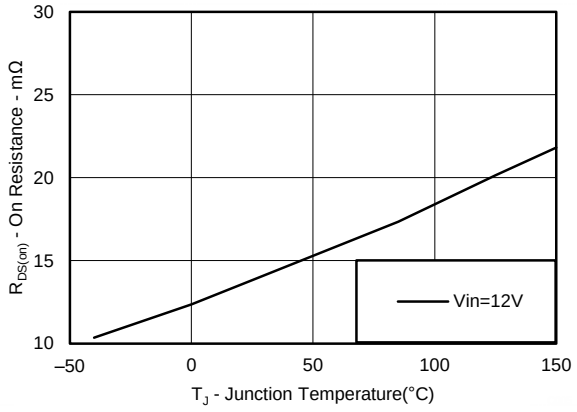


Figure 4. High-side R_{dson} vs Temperature

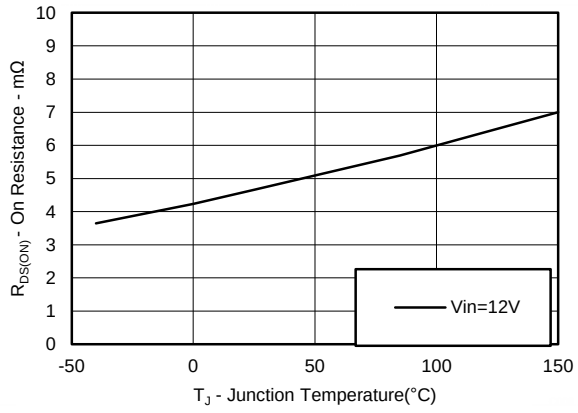


Figure 5. Low-side R_{dson} vs Temperature

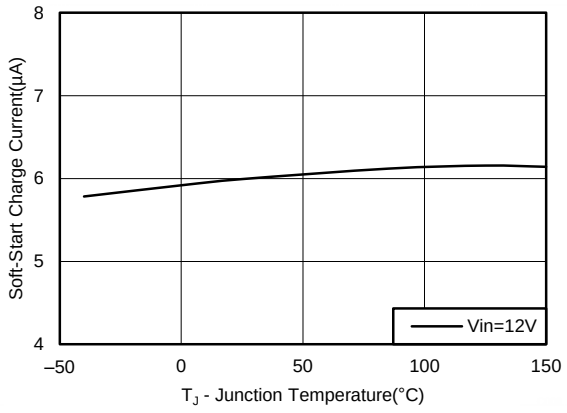


Figure 6. Soft-Start Charge Current vs Temperature

Typical Characteristics (continued)

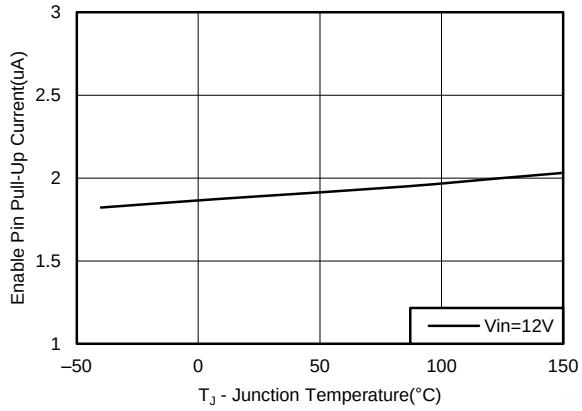


Figure 7. Enable Pull-Up Current, V_{EN} =1.0V

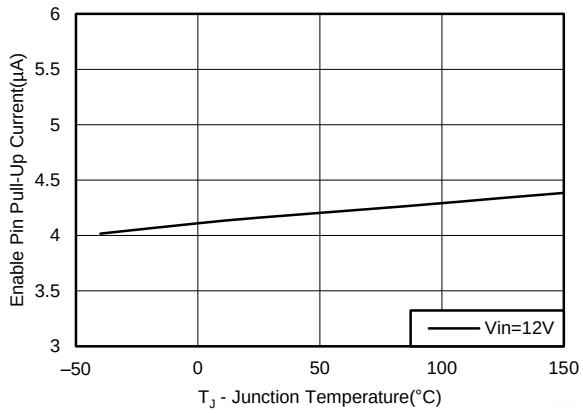


Figure 8. Enable Pull-Up Current, V_{EN} =1.3V

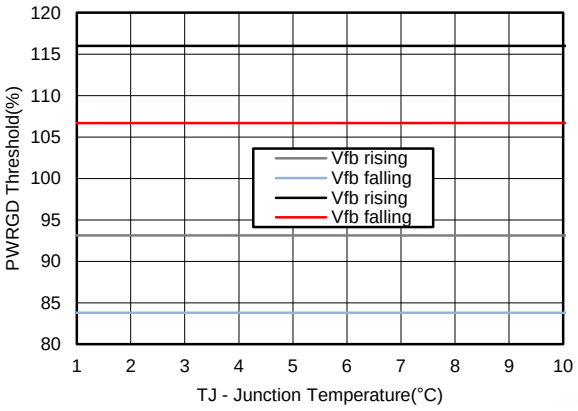


Figure 9. PGOOD Threshold vs Temperature

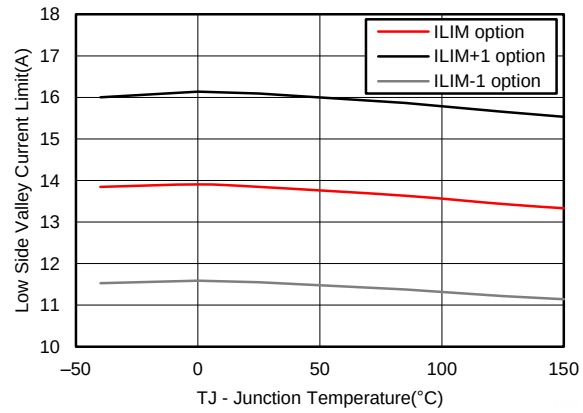


Figure 10. Current Limit vs Temperature

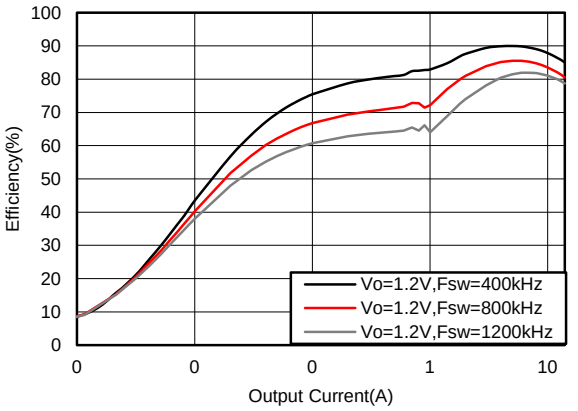


Figure 11. Efficiency with Internal VREG5 = 4.7V, V_{IN} = 12V

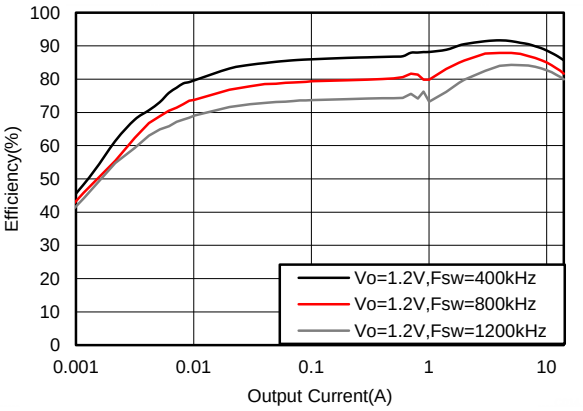


Figure 12. Efficiency with External VREG5 = 5V, V_{IN}=12V

Typical Characteristics (continued)

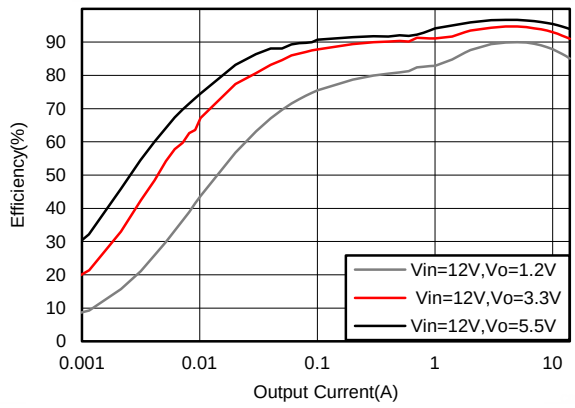


Figure 13. Efficiency, Mode = DCM, F_{SW} = 400kHz

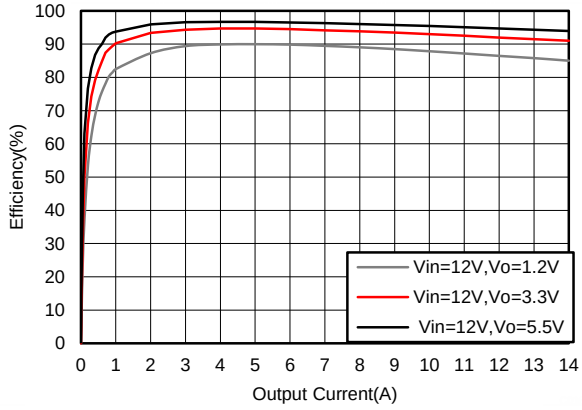


Figure 14. Efficiency, Mode = FCCM, F_{SW} = 400kHz

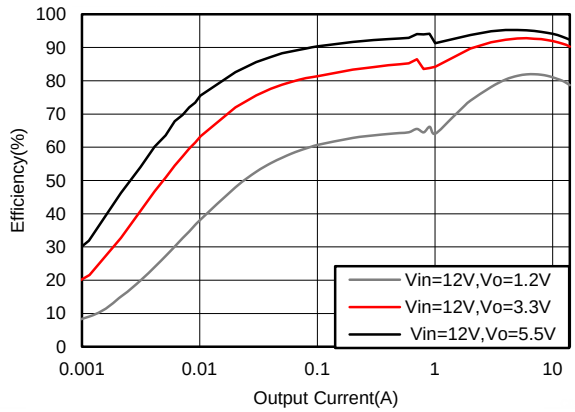


Figure 15. Efficiency, Mode = DCM, F_{SW} = 1200kHz

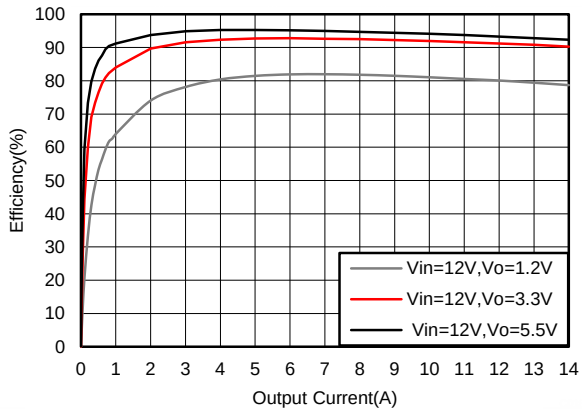


Figure 16. Efficiency, Mode = FCCM, F_{SW} = 1200kHz

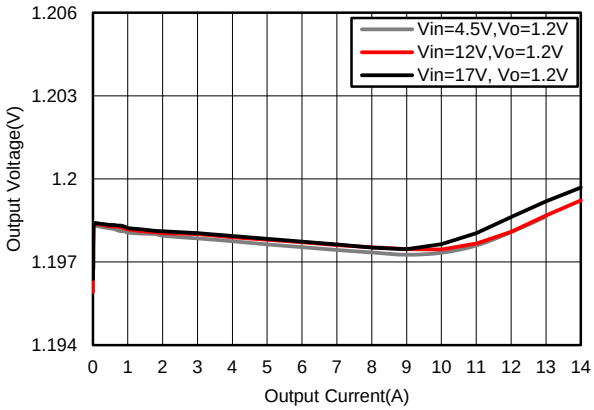


Figure 17. Load Regulation, F_{SW} = 800kHz

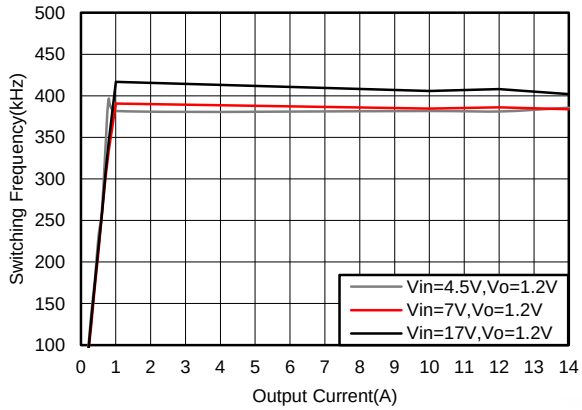


Figure 18. F_{SW} Load Regulation, Mode = DCM, F_{SW} = 400kHz

Typical Characteristics (continued)

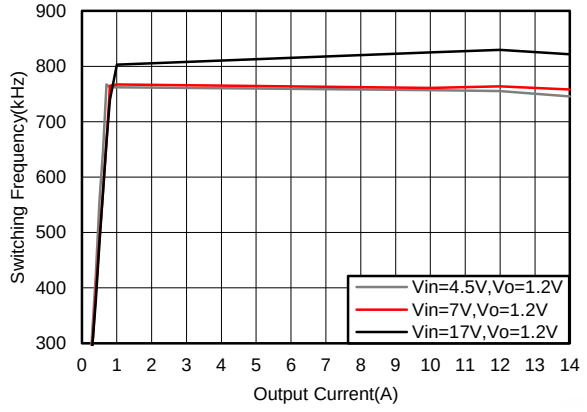


Figure 19. F_{SW} Load Regulation, Mode = DCM, F_{SW} = 800kHz

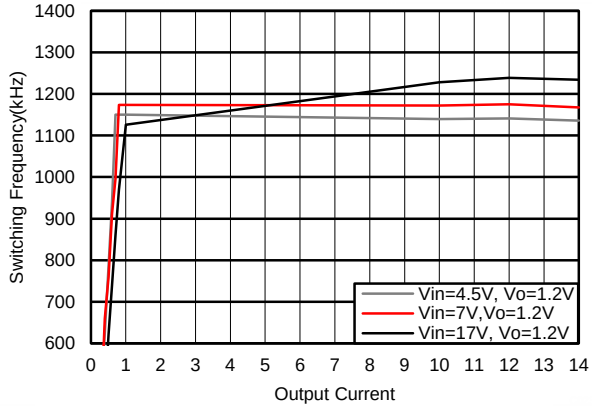


Figure 20. F_{SW} Load Regulation, Mode = DCM, F_{SW} = 1200kHz

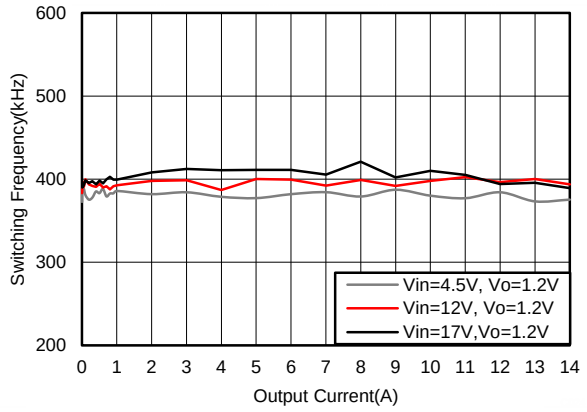


Figure 21. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 400kHz

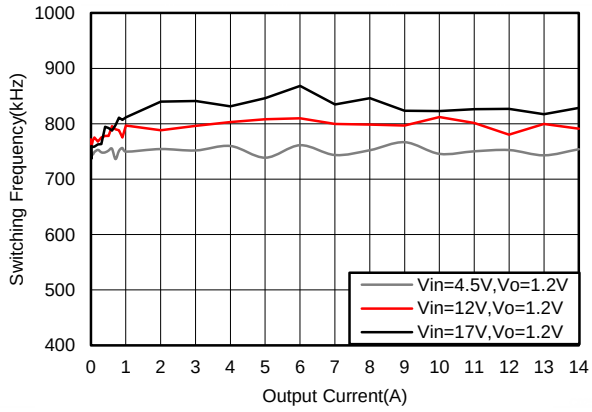


Figure 22. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 800kHz

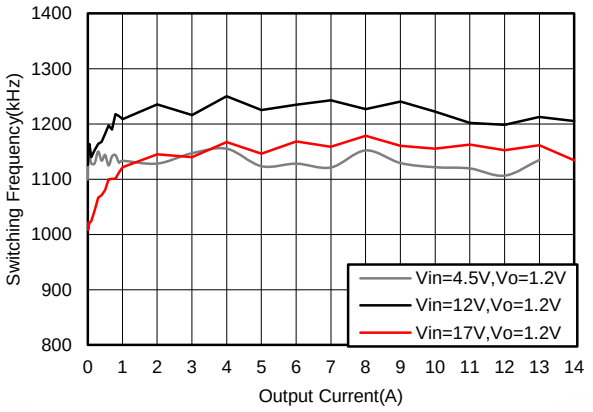


Figure 23. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 1200kHz

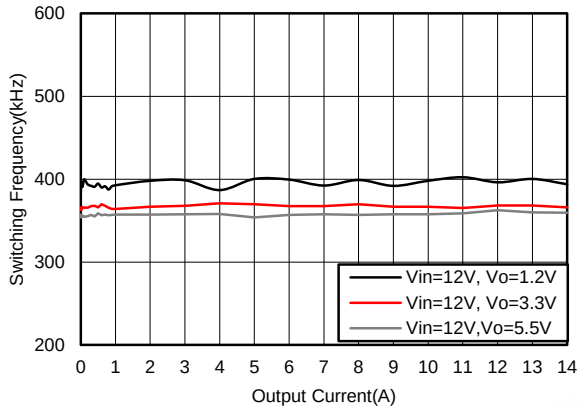


Figure 24. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 400kHz

Typical Characteristics (continued)

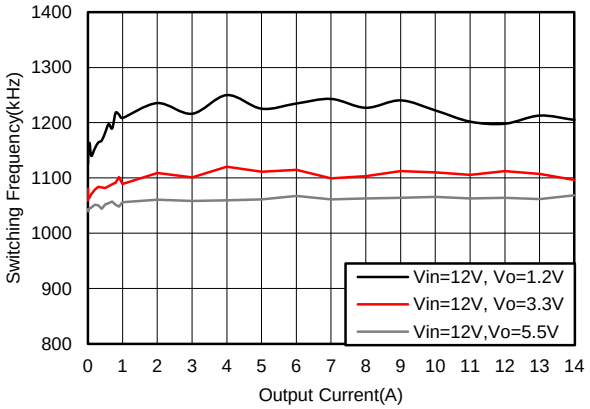


Figure 25. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 1200kHz

7 Detailed Description

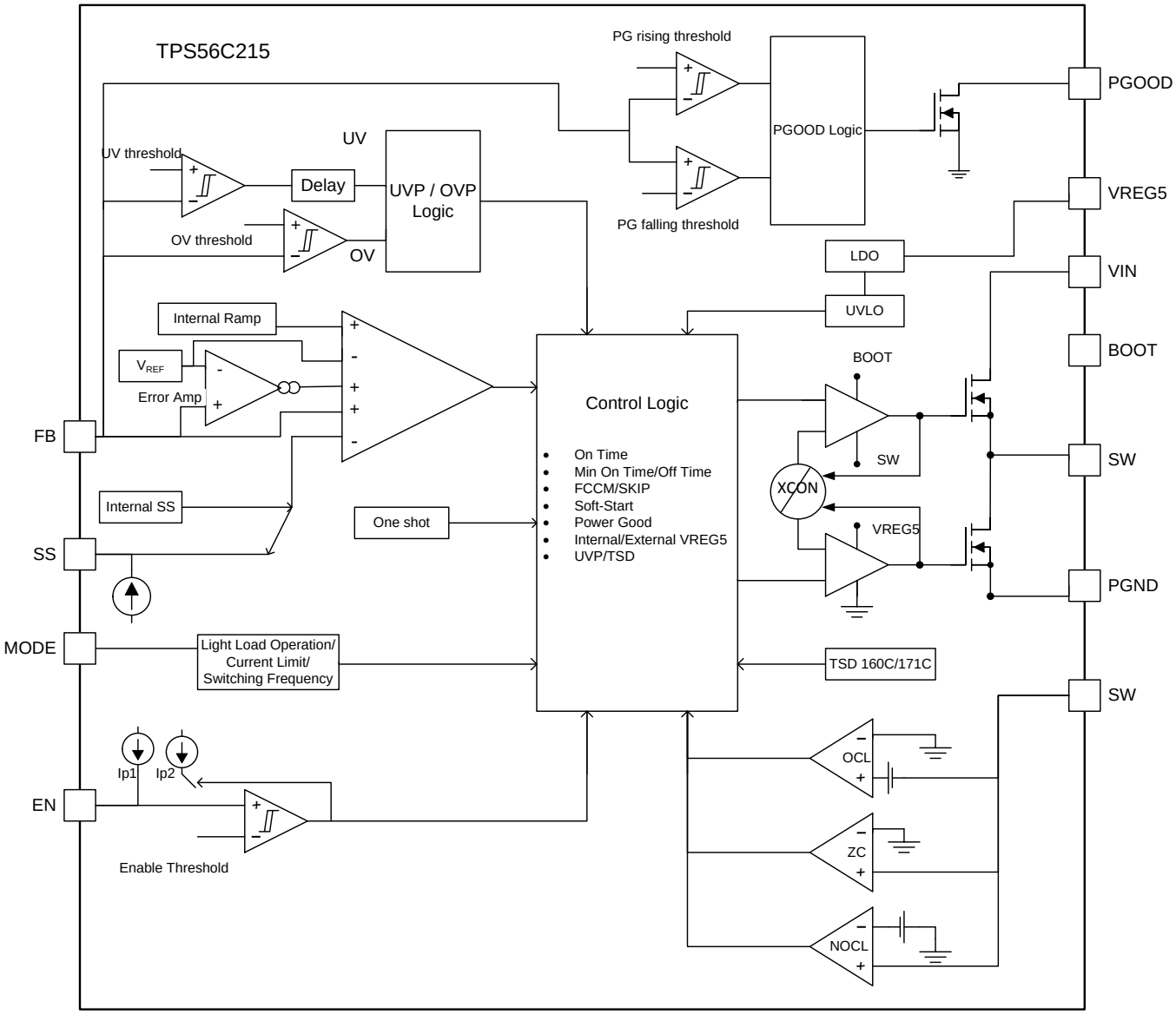
7.1 Overview

The TPS56C215 is a synchronous step down buck converter which can operate from 4.5-V to 17-V input voltage. It has 13.5-mΩ and 4.5-mΩ integrated MOSFETs for high efficiency upto 14A. The device employs D-CAP3™ mode control providing fast transient response with no external compensation components and accurate feedback voltage. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Eco-mode™ operation at light loads. Eco-mode™ allows the TPS56C215 to maintain high efficiency during lighter load conditions. The TPS56C215 is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

The device has a 4.7 V internal LDO that is the bias for all internal circuitry. It has an option to overdrive the internal LDO with an external 5V on the VREG5 pin which improves the converter's efficiency. The under voltage lockout (UVLO) circuit monitors the VREG5 voltage to protect the internal circuitry from low input voltages. The device has a mode pin, the voltage on this pin allows to choose between different modes of frequency, current limit and the two operating modes (Eco-mode™ or FCCM).

The default start-up is at an input voltage of 4.2 V typically. The device has an internal pull-up current source on the EN pin which can enable the device even with the pin floating. The VIN UVLO voltage to can be adjusted with two external resistors connected between VIN and EN. It has a soft start pin that can be used to reduce inrush currents during start-up and the customer can use an external capacitor to adjust the start-up rate. The device is protected from output short and undervoltage conditions and also under thermal fault conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation and D-CAP3™ Control

The TPS56C215 combines the adaptive on-time PWM control with a proprietary D-CAP3™ control which enables low external component count with a fast load transient response while maintaining a good output voltage accuracy. At the beginning of each switching cycle the high side MOSFET is turned on for an on-time set by an internal one shot timer. This on time is set based on the converter's input voltage, output voltage and the pseudo-fixed frequency that is set by the mode pin. Hence it is called an adaptive on-time control. The one shot timer resets and turns on again once the feedback voltage falls below the internal reference voltage. An internal RAMP is generated and fed to the FB pin to simulate the output ripple. This enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for DCAP3 control topology.

Feature Description (continued)

The TPS56C215 includes an error amplifier that makes the output voltage very accurate. For any control topologies supporting no external compensation design, there is a range of the output filter it can support. The output filter used with the TPS56C215 is a low pass L-C circuit. This L-C filter has double pole that is described in

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS56C215. The low frequency L-C double pole has a 180 degree in phase. At the output filter frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40dB to –20dB per decade and increases the phase to 90 degree one decade above the zero frequency. The internal ripple injection high frequency zero is changed according to the switching frequency selected as shown in table below. The inductor and capacitor selected for the output filter must be such that the double pole is located close enough to the high-frequency zero so that the phase boost provided by the high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequence of the overall system should usually be targeted to be less than one-fifth of the switching frequency.

Table 1. Ripple Injection Zero

Switching Frequency (kHz)	Zero Location (kHz)
400	7.1
800	14.3
1200	21.4

Table 2 lists the inductor values and part numbers that are used to plot the efficiency curves in the Typical Characteristics section.

Table 2. Inductor Values

V_{OUT}(V)	F_{SW}(kHz)	L(uH)	Würth Part Number(1)
1.2	400	1.2	744325120
	800	0.68	744311068
	1200	0.47	744314047
3.3	400	2.4	744325240
	800	1.5	7443552150
	1200	1.2	744325120
5.5	400	3.3	744325330
	800	2.4	744325240
	1200	1.5	7443552150

(1) See Third-Party Products disclaimer

7.3.2 Eco-mode™ Control

The TPS56C215 is designed with Eco-mode™ to increase efficiency at light loads. This option can be chosen by the mode pin as described below. As the output current decreases from heavy load condition, the inductor current is also reduced. If the output current is reduced enough, the inductor current ripple valley reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side MOSFET is turned off when a zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept approximately the same as it is in continuous conduction mode. The off-time increases as it takes more time to discharge the output capacitor to the level of the reference voltage with smaller load current. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated from Equation 2.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

After identifying the application requirements, design the output inductance so that the inductor peak-to-peak ripple current is approximately between 20% and 30% of the $I_{CC(max)}$ (peak current in the application). it is also important to size the inductor properly so that the valley current doesn't hit the negative low side current limit.

7.3.3 4.7 V LDO

TPS56C215 has an internal 4.7-V linear regulator that is the bias for all the internal circuitry and mosfet gate drivers. This pin needs to be bypassed with a 4.7-µF capacitor. An external 5 V can be applied to this pin which turns off the internal LDO and the LDO switches to the external 5-V rail. This enhances the efficiency of the converter because the quiescent current now runs off this 5-V rail instead of the VIN supply. The UVLO circuit monitors the VREG5 voltage and disables the output when VIN falls below the UVLO threshold.

7.3.4 Mode Selection

TPS56C215 has a mode pin and the voltage on this pin is measured during startup to select between 16 different states which are a combination of current limit, switching frequency and light load operation. The device can operate at three different current limits which support an output continuos current of 10 A, 12 A and 14 A. It can operate at three different pseudo fixed frequencies of 400 kHz, 800 kHz and 1200 kHz. However while operating with 1200 kHz switching frequency the highest current limit setting is not supported. Mode setting is shown in Table 3 and uses a resistor divider from VREG5. The mode pin setting can be reset only by VIN power cycling. The resister divider settings are based on the internal VREG5 voltage which is 4.7 V typically.

Table 3. Mode Pin Resistor Settings

R_{M_L} (kΩ)	R_{M_H} (kΩ)	MODE	I_{OUT} (A)	FREQUENCY (kHz)
5	309	FCCM	10	400
10	200	FCCM	12	400
20	232	FCCM	14	400
20	158	FCCM	10	800
20	120	FCCM	12	800
50	237	FCCM	14	800
50	191	FCCM	10	1200
50	158	FCCM	12	1200
50	137	DCM	10	400
50	118	DCM	12	400
50	100	DCM	14	400
50	86.6	DCM	10	800
50	78.7	DCM	12	800
50	68	DCM	14	800
50	60.4	DCM	10	1200
50	52.3	DCM	12	1200

Figure 26 below shows the typical start-up sequence of the device once the enable signal crosses the EN turn-on threshold. After the voltage on VREG5 crosses the rising UVLO threshold it takes 100us to read the first mode setting and approximately 100us from there to finish the last mode setting. The output voltage starts ramping after the mode reading is done.

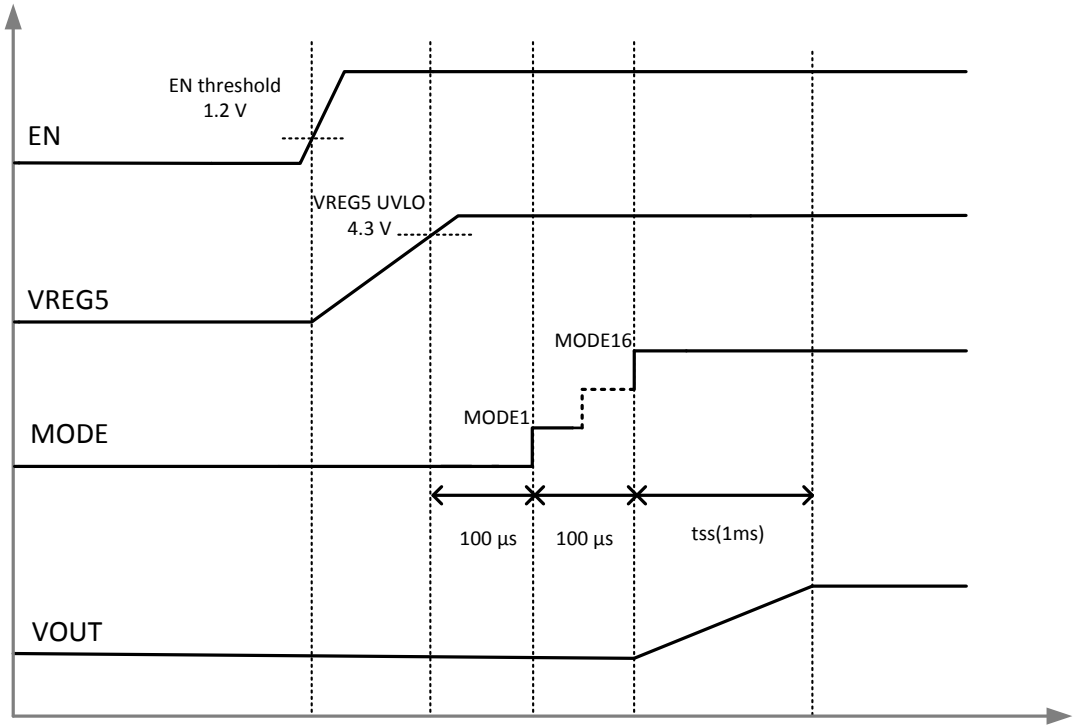


Figure 26. Power-Up Sequence

7.3.5 Soft Start and Pre-biased Soft Start

The TPS56C215 has adjustable soft-start. When the EN pin becomes high, the SS charge current (Iss) begins charging the capacitor connected from the SS pin to GND (Css). The devices tracks the lower of the internal soft start voltage or the external soft start voltage as the reference. The equation for the soft start time, T_{SS} is shown in Equation 3:

$$T_{SS(ms)} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (3)$$

where

- V_{REF} is 0.6 V and I_{SS} is 6 µA

If the output capacitor is pre-biased at startup, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.6 Enable and Adjustable UVLO

The Enable pin controls the turn-on and turn-off of the device. When Enable voltage is above the turn-on threshold of 1.2 V, the device starts switching and when it falls below the turn-off threshold it stops switching. The device has an internal pull-up current source on this pin that allows the user to float this pin to enable the device. If the customer application requires a different turn-on and turn-off thresholds the Enable pin can be configured as shown in Figure 27 below by connecting a resistor divider between Vin and enable. The enable pin has a pull-up current Ip1 that sets the default state of the pin when it is floating. This current increases to Ip2 when the enable voltage crosses the turn-on threshold. The UVLO thresholds can be set by using Equation 4 and Equation 5.

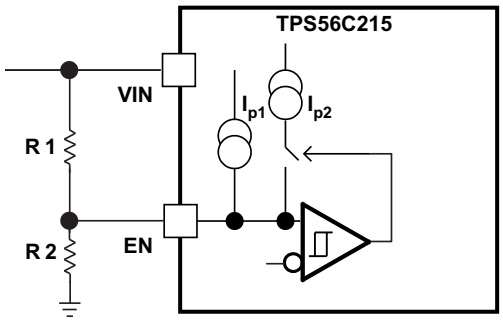


Figure 27. Adjustable VIN Under Voltage Lock Out

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_{p1}\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + \left(I_{p1} - I_{p2}\right)} \quad (4)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1\ I_{p2}}$$

where

- I_{p2} = 4.197 µA
- I_{p1} = 1.91 µA
- $V_{ENRISING}$ = 1.225 V
- $V_{ENFALLING}$ = 1.104 V (5)

7.3.7 Power Good

The power good output, PGOOD is an open drain output. Once the V_{FB} is between 93% and 107% of the internal reference voltage the PGOOD is de-asserted and floats after a 200 µs de-glitch time. A pull-up resistor of 10 kΩ is recommended to pull it up to a voltage source of 5 V or lower. The PGOOD pin is pulled low when V_{FB} is lower than UVLO or greater than OV; or, in an event of thermal shutdown or during the soft start period

7.3.8 Over Current Protection and Under Voltage Protection

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. During the on time of the high-side FET switch, the switch current increases at a linear rate determined by input voltage , output voltage, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. The low-side switch voltage is monitored during the low side on time which is proportional to the switch current. If the measured voltage is above the voltage proportional to current limit, the low side FET stays on until the current level becomes lower than the OCL level which reduces the output current available. When the current is limited the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 68% of the target voltage, the UV comparator detects it and shuts down the device after a wait time of 1ms, the device re-starts after a hiccup time of 7ms. In this type of valley detect control the load current is higher than the OCL threshold by one half of the peak to peak inductor ripple current. When the over-current condition is removed, the output voltage returns to the regulated value. If an OCL condition happens during start-up then the device enters hiccup-mode immediately without a wait time of 1ms.

7.3.9 Out-of-Bounds Operation

The device has an out-of-bounds (OOB) overvoltage protection that protects the output load at a much lower overvoltage threshold of 8% above the target voltage. OOB protection does not trigger an overvoltage fault, OOB protection operates as an early no-fault overvoltage protection mechanism. During the OOB operation, the controller operates in forced PWM mode only by turning on the low-side FET. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor thus causing the output voltage to fall quickly toward the setpoint. During the operation, the cycle-by cycle negative current limit is also activated to ensure the safe operation of the internal FETs.

7.3.10 UVLO Protection

Under voltage lock out protection (UVLO) monitors the internal VREG5 regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.11 Thermal Shutdown

The device monitors the temperature of itself. If the device temperature exceeds the threshold value (T_{SDN} typically 160°C) the device shuts off. This is a non-latch protection. During start up, if the device temperature is higher than 160°C the device does not start switching and does not load the mode settings. If the device temp goes higher than T_{SDN} threshold after startup, it stops switching with soft start reset to ground and the discharge switch turns on. The device re-starts switching when the temperature goes below threshold but OTP/mode settings are not re-loaded again.

There is a second higher thermal protection on the device $T_{SDN\ VREG5}$ which protects it from over temperature condition not caused by the switching of the device itself. This threshold is at typically 170°C. When the device stops switching after reaching the first thermal shutdown threshold but still continues to heat up, the VREG5 output shuts off when it reaches 170°C, thereby shutting off completely.

7.3.12 Output Voltage Discharge

The device has a 500ohm discharge switch that discharges the output through SW node during any event of fault like OV, UV, TSD and Vin UVLO and also when the enable voltage is below the turn-on threshold.

7.4 Device Functional Modes

7.4.1 Light Load Operation

When the MODE pin is selected to operate in continue conduction mode, the converter operates in continuous conduction mode (CCM) during light-load conditions. During CCM, the switching frequency is maintained to an almost constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light loading. If the mode pin is selected to operate in DCM mode the device enters pulse skip mode after the inductor valley ripple current crosses zero that maintains higher efficiency with longer switching frequency.

7.4.2 Standby Operation

The device can be place in standby from any mode by pulling the Enable pin low. The device operates with a low shut-down current when in standby condition.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The schematic of Figure 28 shows a typical application for TPS56C215. This design converts an input voltage range of 4.5 V to 17 V down to 1.2 V with a maximum output current of 12 A.

8.2 Typical Application

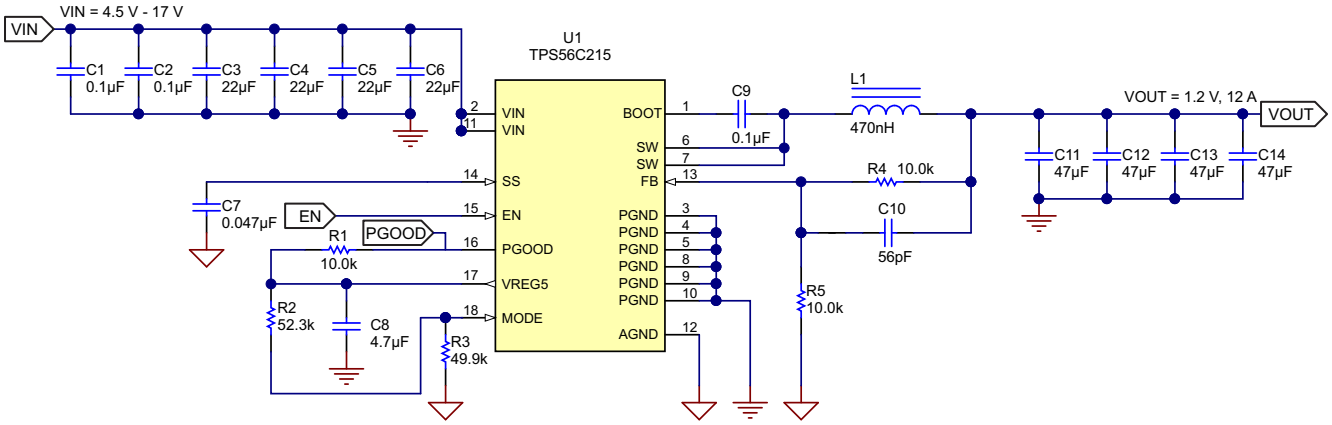


Figure 28. Application Schematic

8.2.1 Design Requirements

Table 4. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage			1.2		V
I_{OUT}	Output current			12		A
ΔV_{OUT}	Transient response	9-A load step		40		mV
V_{IN}	Input voltage		4.5	12	17	V
$V_{OUT(ripple)}$	Output voltage ripple			20		$mV_{(P-P)}$
	Start input voltage	Input voltage rising		Internal UVLO		V
	Stop input voltage	Input voltage falling		Internal UVLO		V
f_{SW}	Switching frequency			1.2		MHz
Operating Mode				DCM		
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 External Component Selection

8.2.2.1.1 Output Voltage Set Point

To change the output voltage of the application, it is necessary to change the value of the upper feedback resistor. By changing this resistor the user can change the output voltage above 0.6 V. See Equation 6

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{UPPER}}{R_{LOWER}} \right) \quad (6)$$

8.2.2.1.2 Switching Frequency and Mode Selection

Switching Frequency, current limit and switching mode (DCM or FCCM) are set by a voltage divider from VREG5 to GND connected to the MODE pin. See Table 3 for possible MODE pin configurations. Switching frequency selection is a tradeoff between higher efficiency and smaller system solution size. Lower switching frequency yields higher overall efficiency but relatively bigger external components. Higher switching frequencies cause additional switching losses which impact efficiency and thermal performance. For this design 1.2 MHz is chosen as the switching frequency, the switching mode is DCM and the output current is 12 A.

8.2.2.1.3 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor should have a ripple current rating higher than the inductor ripple current. See Table 5 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using Equation 7 and Equation 8. It is important that the inductor is rated to handle these currents.

$$IL_{rms} = \sqrt{\left(I_{O^2} + \frac{1}{12} \times \left(\frac{V_O \times (V_{inmax} - V_O)}{Vinmax \times L1 \times f_{SW}} \right)^2 \right)} \quad (7)$$

$$IL_{PEAK} = I_{OUT} + \frac{I_{ripple}}{2} \quad (8)$$

During transient/short circuit conditions the inductor current can increase up to the current limit of the device so it is safe to choose an inductor with a saturation current higher than the peak current under current limit condition.

8.2.2.1.4 Output Capacitor Selection

After selecting the inductor the output capacitor needs to be optimized. In DCAP3, the regulator reacts within one cycle to the change in the duty cycle so the good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in Table 5

Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor should be less than Voripple/Iripple

Table 5. Recommended Component Values

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	f_{SW} (kHz)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)	C_{FF} (pF)
0.6	10	0	400	0.68	300	500	–
			800	0.47	100	500	–
			1200	0.33	88	500	–
1.2		10	400	1.2	100	500	–
			800	0.68	88	500	–
			1200	0.47	88	500	–
3.3		45.3	400	2.4	88	500	100–220
			800	1.5	88	500	100–220
			1200	1.2	88	500	100–220
5.5		82.5	400	3.3	88	500	100–220
			800	2.4	88	500	100–220
			1200	1.5	88	700	100–220

8.2.2.1.5 Input Capacitor Selection

The minimum input capacitance required is given in Equation 9.

$$C_{IN(min)} = \frac{I_{LOAD} \times V_{OUT}}{V_{ripple} \times V_{IN} \times f_{SW}} \quad (9)$$

TI recommends using a high quality X5R or X7R input decoupling capacitors of 40 µF on the input voltage pin. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by Equation 10 below:

$$I_{cirms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{inmin}} \times \frac{(V_{inmin} - V_{out})}{V_{inmin}}} \quad (10)$$

8.2.3 Application Curves

Figure 29 through Figure 45 apply to the circuit of Figure 28. V_{IN} = 12 V. T_a = 25 °C unless otherwise specified.

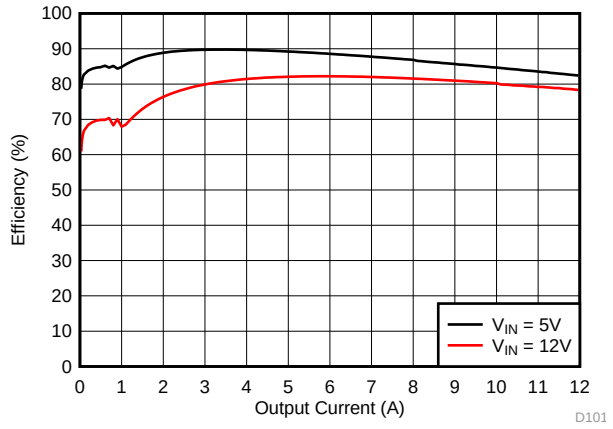


Figure 29. Efficiency

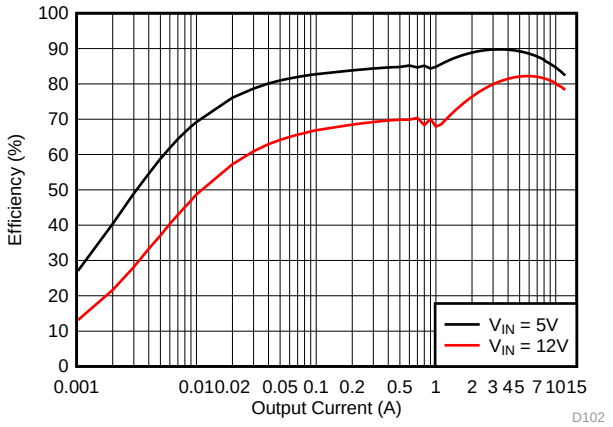


Figure 30. Light Load Efficiency

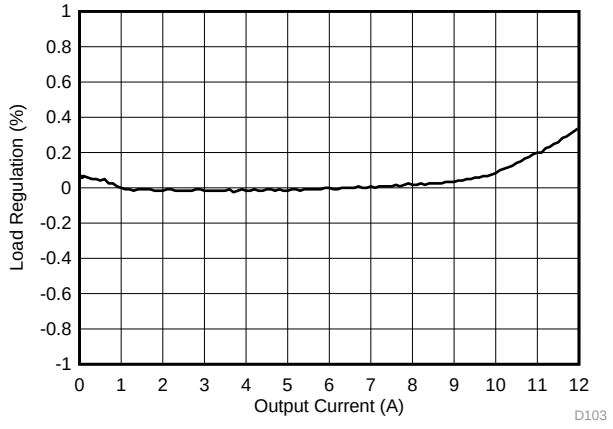


Figure 31. Load Regulation, V_{IN} = 5 V

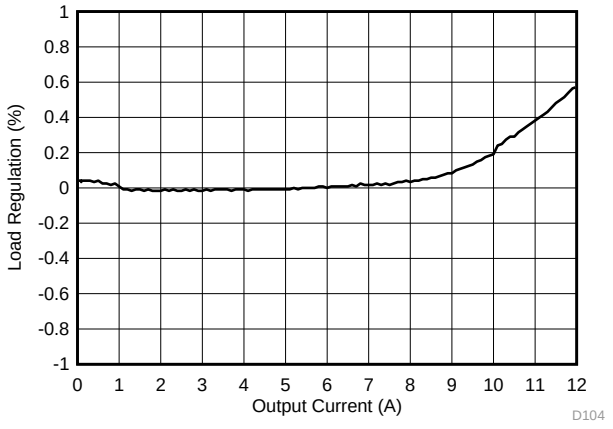


Figure 32. Load Regulation, V_{IN} = 12 V

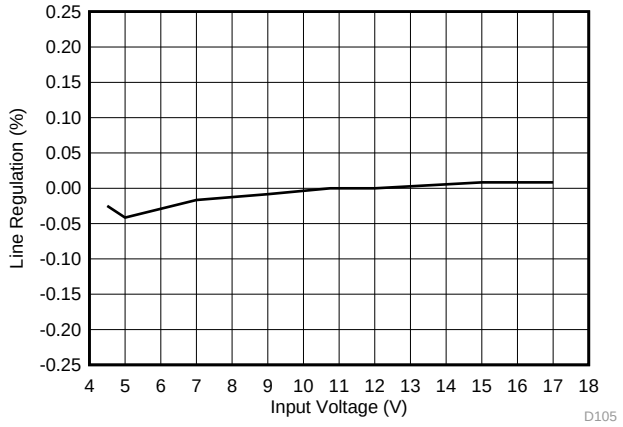


Figure 33. Line Regulation, I_{OUT} = 6 A

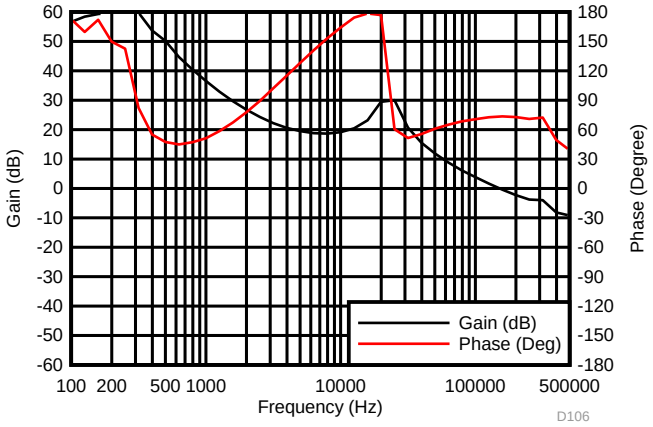


Figure 34. Loop Response, I_{OUT} = 6 A

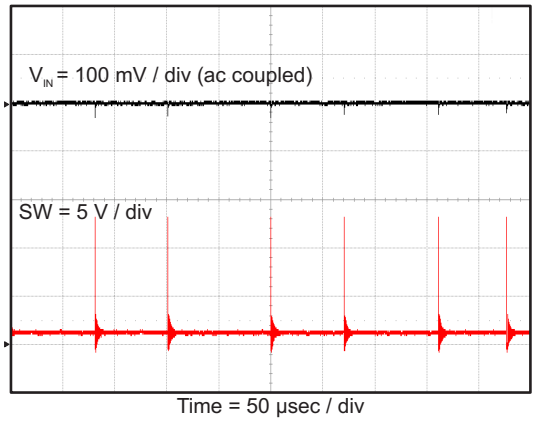


Figure 35. Input Voltage Ripple, I_{OUT} = 10 mA

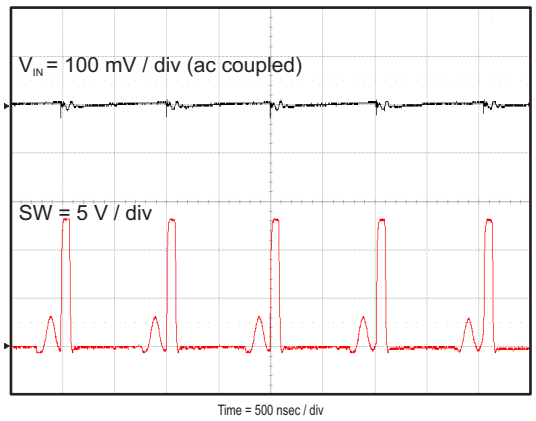


Figure 36. Input Voltage Ripple, I_{OUT} = 800 mA

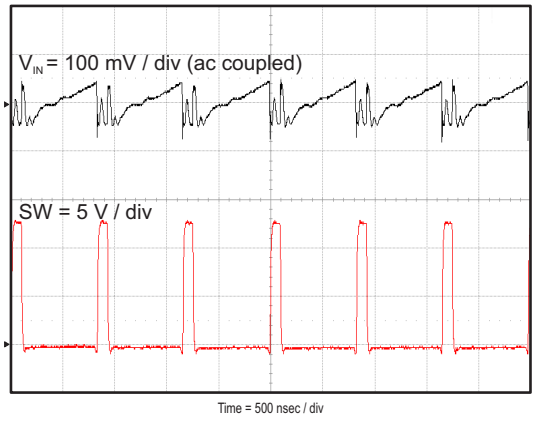


Figure 37. Input Voltage Ripple, I_{OUT} = 12 A

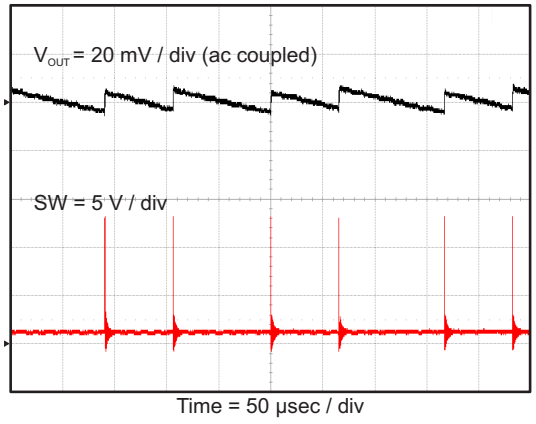


Figure 38. Output Voltage Ripple, I_{OUT} = 10 mA

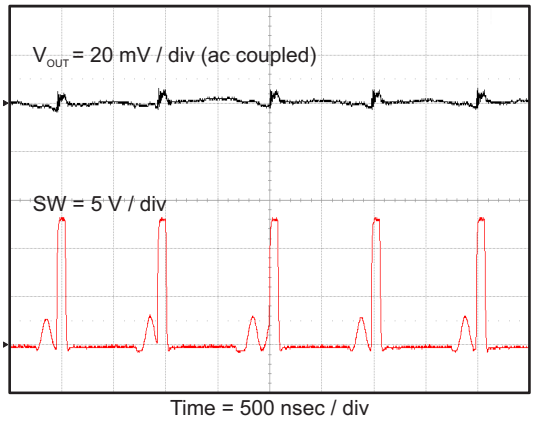


Figure 39. Output Voltage Ripple, I_{OUT} = 800 mA

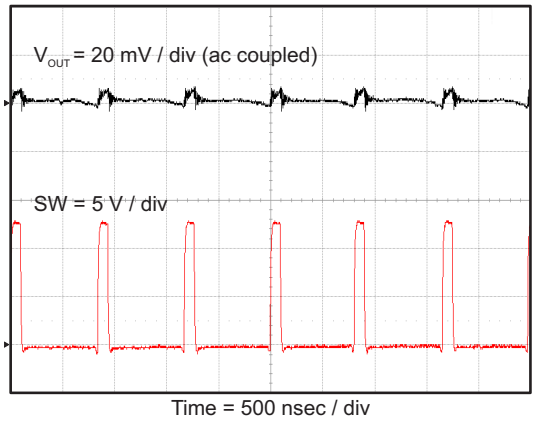


Figure 40. Output Voltage Ripple, I_{OUT} = 12 A

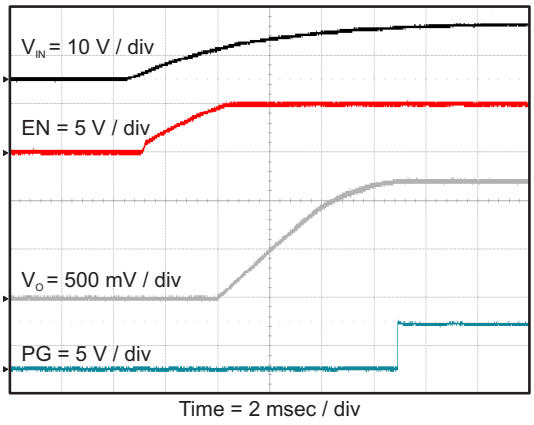


Figure 41. Start Up Relative to V_{IN} Rising

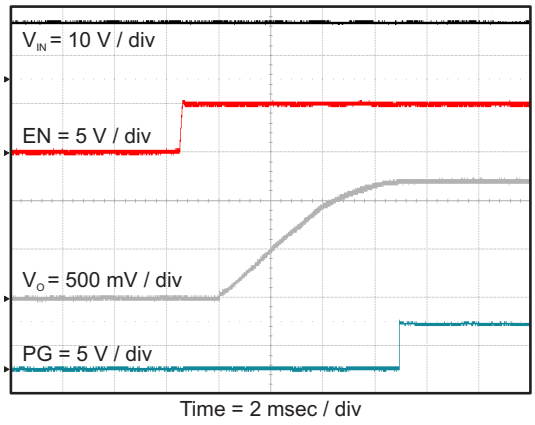


Figure 42. Start Up Relative to EN Rising

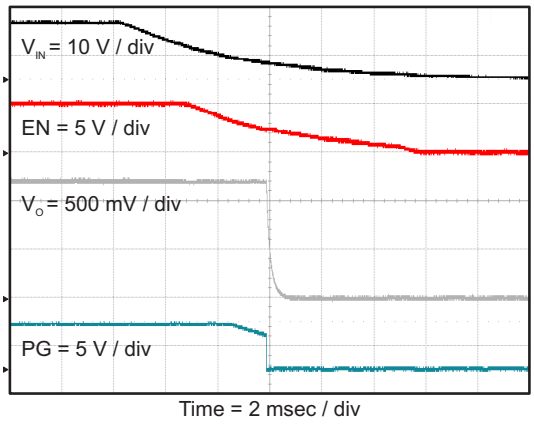


Figure 43. Shut Down Relative to V_{IN} Falling

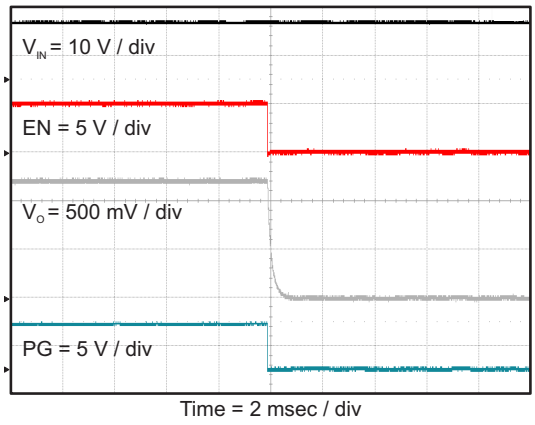


Figure 44. Shut Down Relative to EN Falling

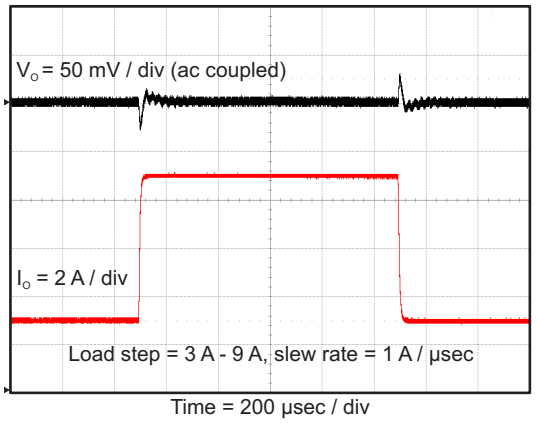


Figure 45. Transient Response

9 Power Supply Recommendations

The TPS56C215 is intended to be powered by a well regulated dc voltage. The input voltage range is 4.5 to 17 V. TPS56C215 is a buck converter. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS56215 circuit, some additional input bulk capacitance is recommended. Typical values are 100 µF to 470 µF.

10 Layout

10.1 Layout Guidelines

- Recommend a four-layer or six-layer PCB for good thermal performance and with maximum ground plane. 3" x 3", four-layer PCB with 2-oz. copper used as example.
- Recommend having equal caps on each side of the IC. Place them right across Vin as close as possible.
- Inner layer 1 will be ground with the PGND to AGND net tie
- Inner layer2 has Vin copper pour that has vias to the top layer Vin. **Place multiple vias under the device near VIN and GND and near input capacitors** to reduce parasitic inductance and improve thermal performance
- Bottom later is GND with the BOOT trace routing.
- Feedback should be referenced to the quite AGND and routed away from the switch node.
- VIN trace must be wide to reduce the trace impedance.

10.2 Layout Example

Figure 46 shows the recommended top side layout. Component reference designators are the same as the circuit shown in Figure 28. Resistor divider for EN is not used in the circuit of Figure 28, but are shown in the layout for reference.

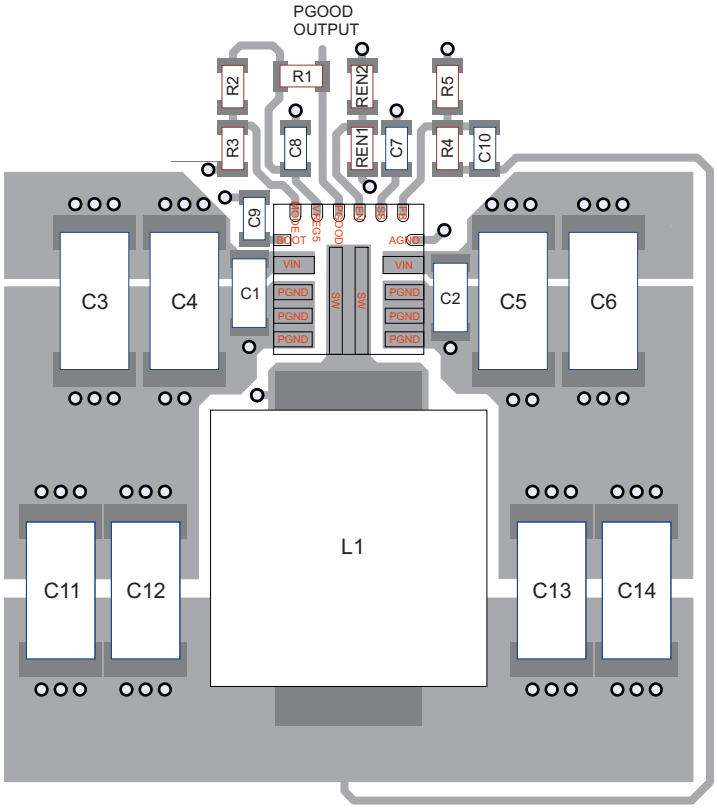


Figure 46. Top Side Layout

Layout Example (continued)

Figure 47 shows the recommended layout for the first internal layer. It is comprised of a large PGND plane and a smaller ANGD island. AGND and PGND are connected at a single point to reduce circulating currents.

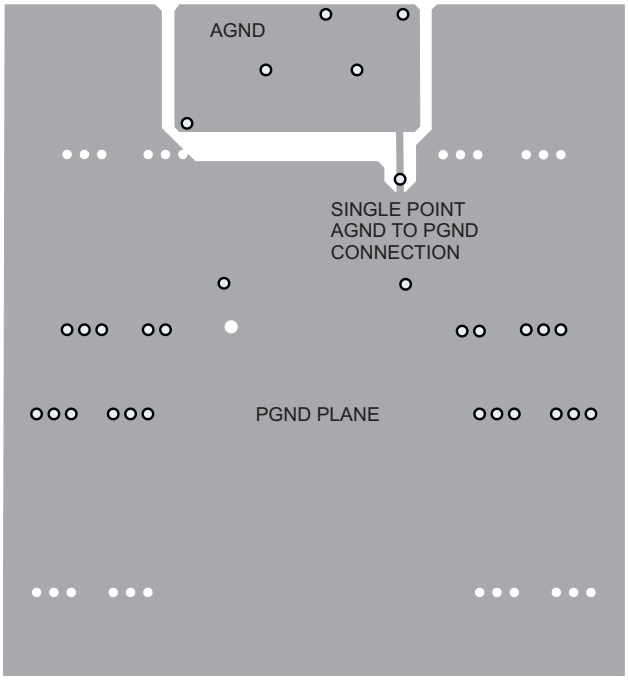


Figure 47. Mid Layer 1 Layout

Figure 48 shows the recommended layout for the second internal layer. It is comprised of a large PGND plane, a smaller copper fill area to connect the two top side V_{IN} copper areas and a second V_{OUT} copper fill area.

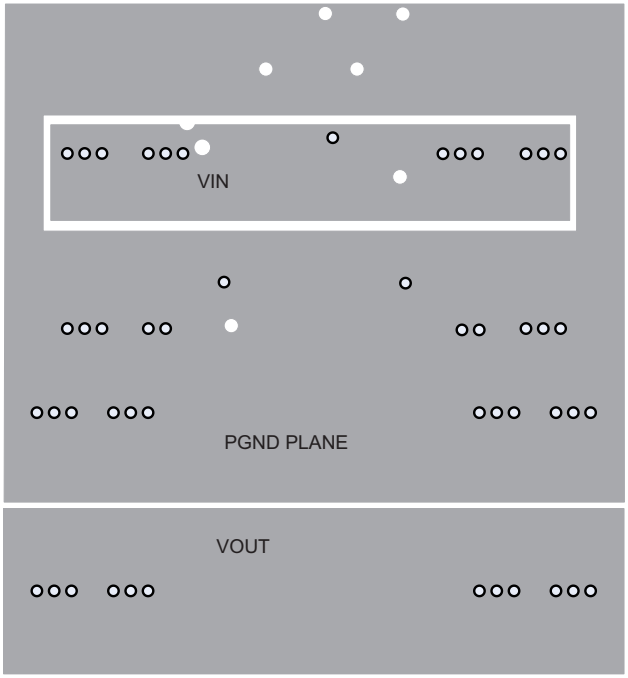


Figure 48. Mid Layer 2 Layout

Layout Example (continued)

Figure 49 shows the recommended layout for the bottom layer. It is comprised of a large PGND plane and a trace to connect the BOOT capacitor to the SW node.

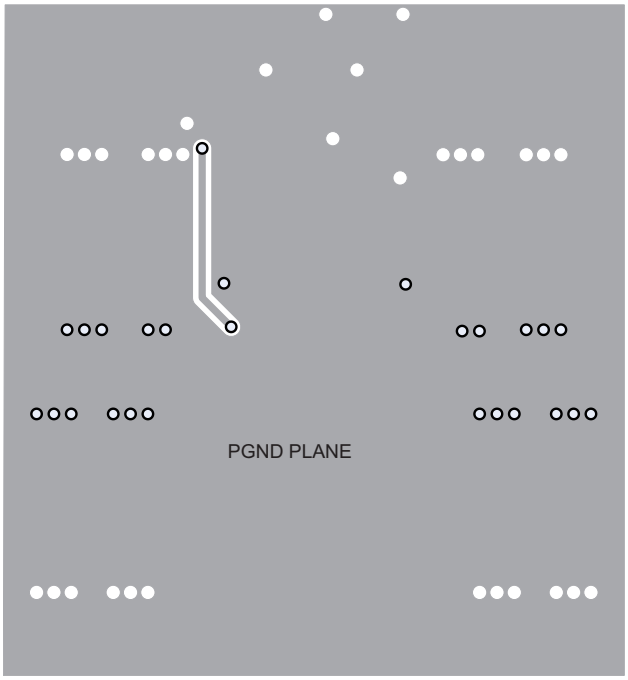


Figure 49. Bottom Layer Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Development Support

The evaluation module for system validation in shown in Figure 50.

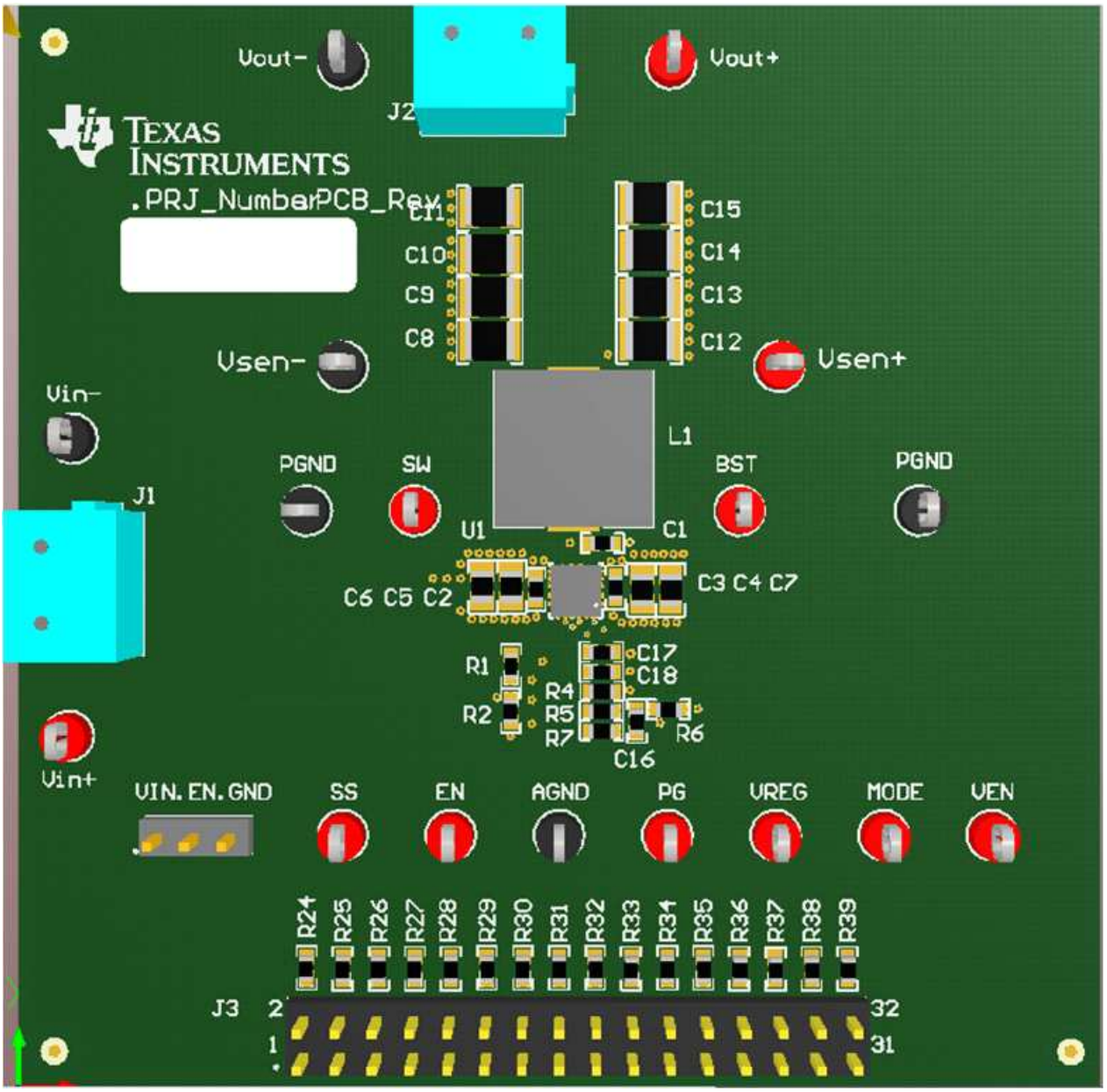


Figure 50. System Validation EVM Board

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

D-CAP3, Eco-mode, HotRod, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS56C215RNNR	ACTIVE	VQFN-HR	RNN	18	3000	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	56C215	Samples
TPS56C215RNNT	ACTIVE	VQFN-HR	RNN	18	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	56C215	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

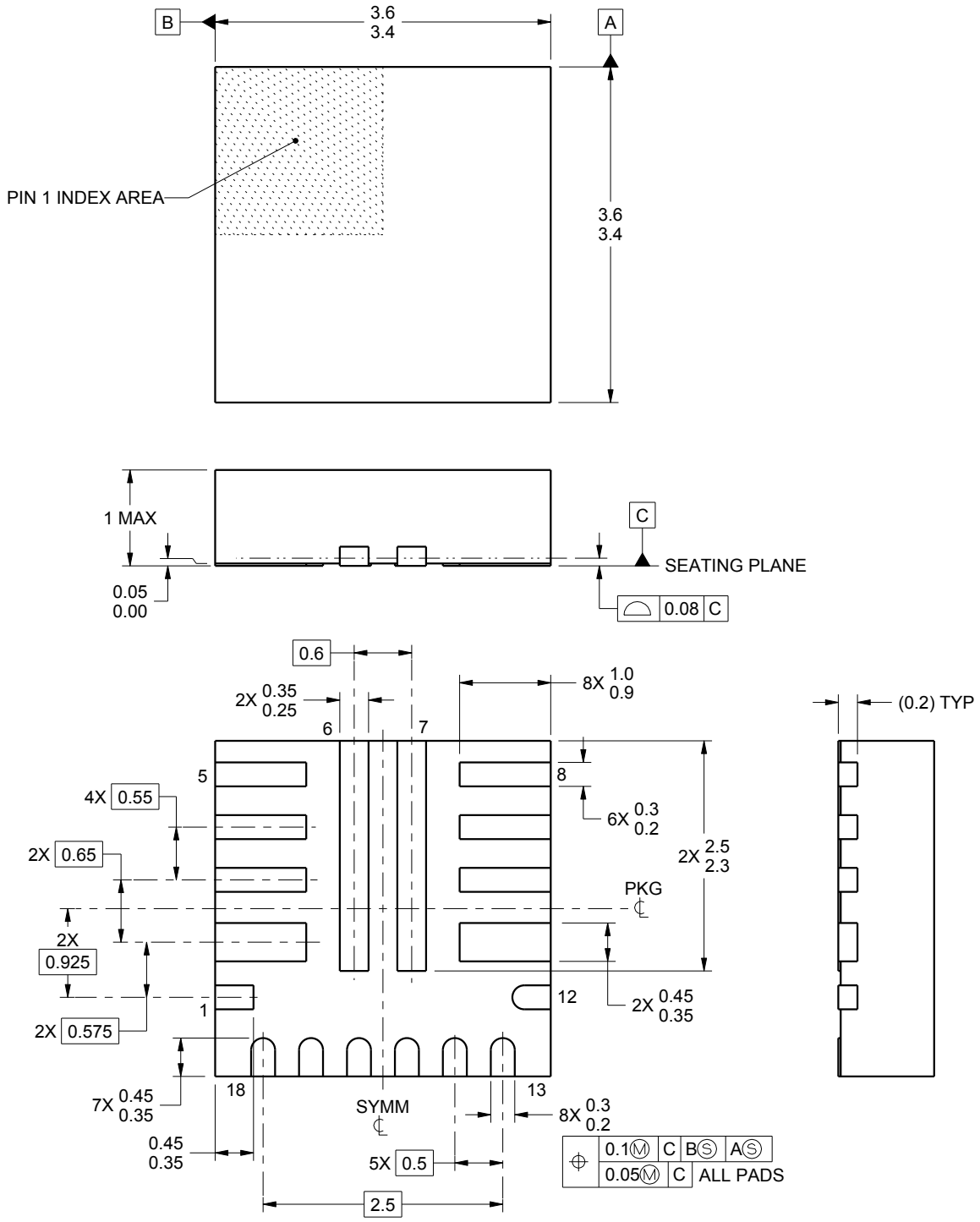
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

RNN0018A

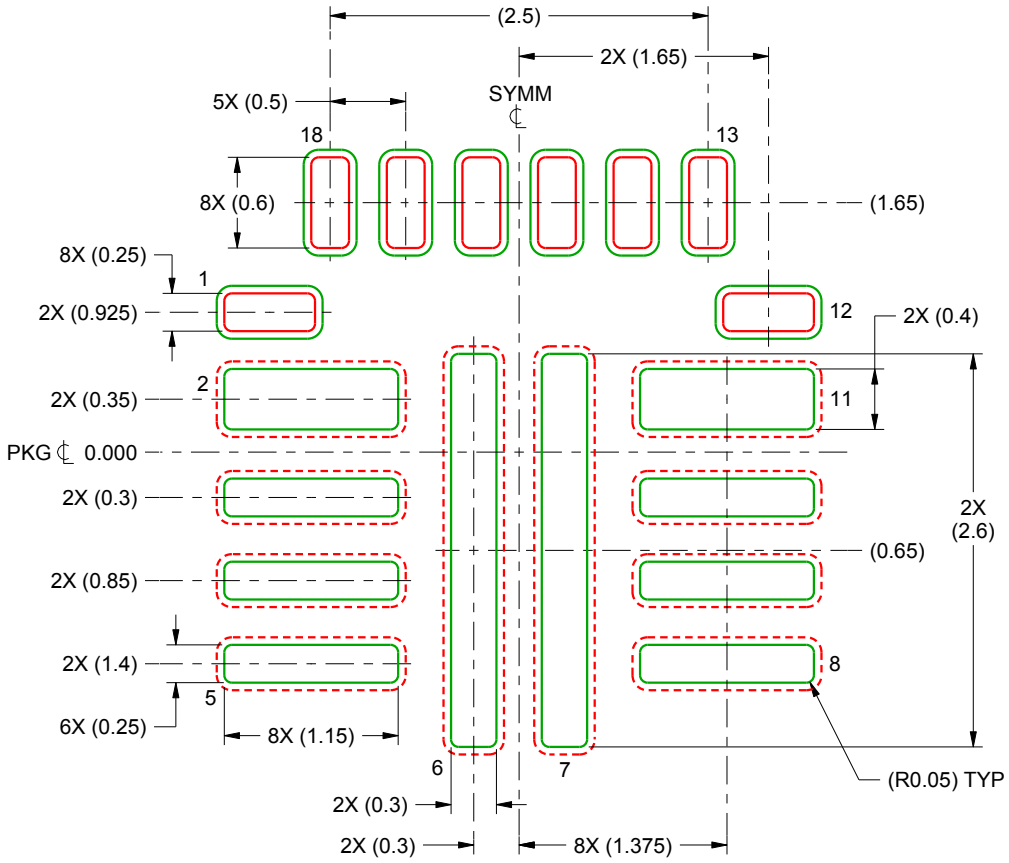
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

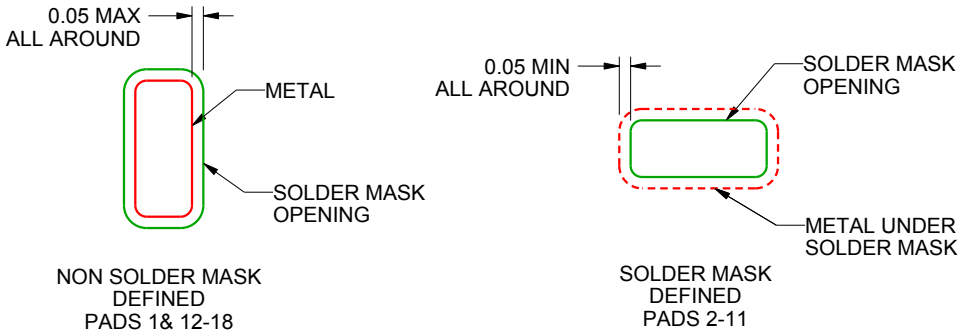


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:20X

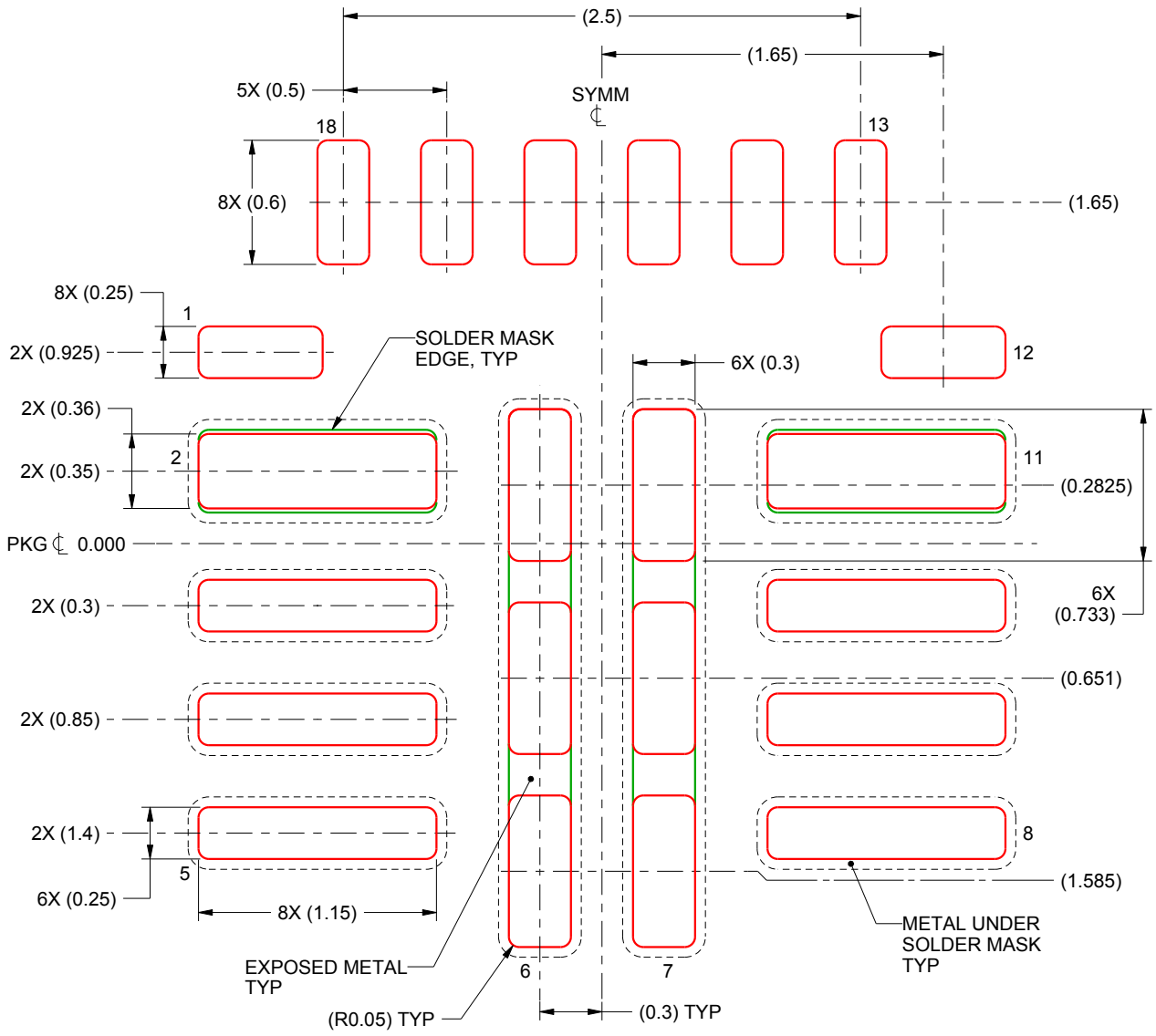


SOLDER MASK DETAILS

4222688/A 01/2016

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 6 & 7: 83% - PADS 2 & 11: 90%
SCALE:30X

4222688/A 01/2016

NOTES: (continued)

5. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265