FEATURES:

- **Phase-Lock Loop Clock Distribution**
- **10MHz to 133MHz operating frequency**
- **Distributes one clock input to one bank of five and one bankd of four outputs**
- **Separate output enable for each output bank**
- **Output Skew < 250ps**
- **Low jitter <200 ps cycle-to-cycle**
- **IDT2309-1 for Standard Drive**
- **IDT2309-1H for High Drive**
- **No external RC network required**
- **Operates at 3.3V V_{DD}**
- **Available in SOIC and TSSOP packages**

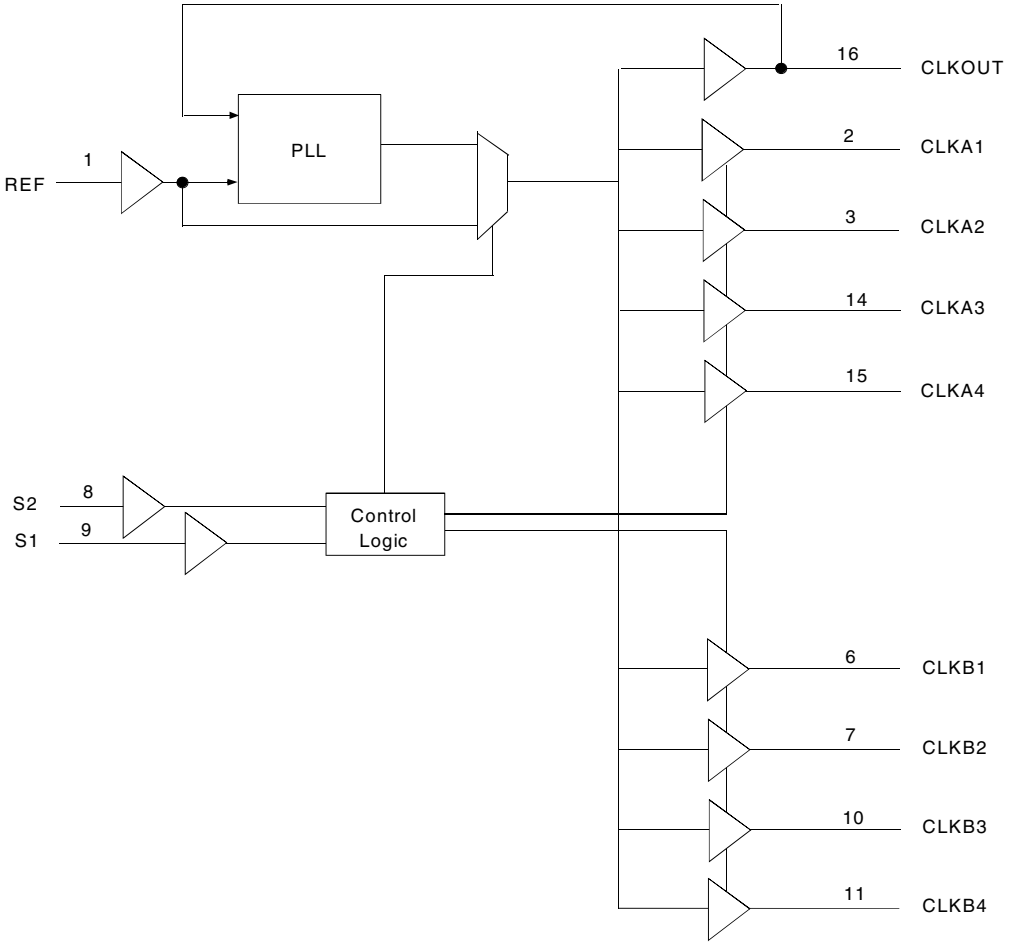
DESCRIPTION:

The IDT2309 is a high-speed phase-lock loop (PLL) clock buffer, designed to address high-speed clock distribution applications. The zero delay is achieved by aligning the phase between the incoming clock and the output clock, operable within the range of 10 to 133MHz.

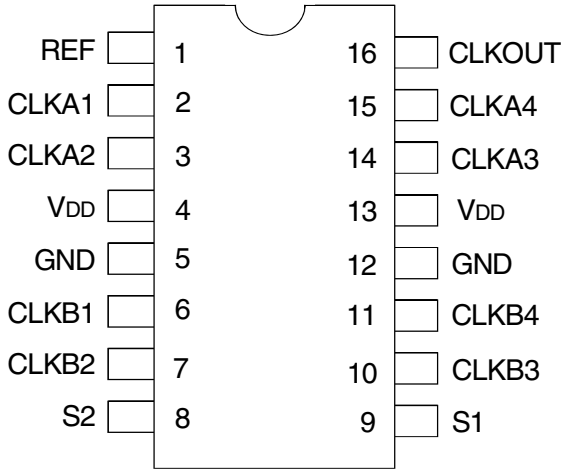
The IDT2309 is a 16-pin version of the IDT2305. The IDT2309 accepts one reference input, and drives two banks of four low skew clocks. The -1H version of this device operates at up to 133MHz frequency and has higher drive than the -1 device. All parts have on-chip PLLs which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad. In the absence of an input clock, the IDT2309 enters power down, and the outputs are tri-stated. In this mode, the device will draw less than 25µA.

The IDT2309 is characterized for both Industrial and Commercial operation.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ TSSOP
TOP VIEW

APPLICATIONS:

- **SDRAM**
- **Telecom**
- **Datacom**
- **PC Motherboards/Workstations**
- **Critical Path Delay Designs**

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
V_{DD}	Supply Voltage Range	–0.5 to +4.6	V
V_I (2)	Input Voltage Range (REF)	–0.5 to +5.5	V
V_I	Input Voltage Range (except REF)	–0.5 to V_{DD}+0.5	V
I_{IK} (V_I < 0)	Input Clamp Current	–50	mA
I_O (V_O = 0 to V_{DD})	Continuous Output Current	±50	mA
V_{DD} or GND	Continuous Current	±100	mA
T_A = 55°C (in still air)(3)	Maximum Power Dissipation	0.7	W
T_{STG}	Storage Temperature Range	–65 to +150	°C
Operating Temperature	Commercial Temperature Range	0 to +70	°C
Operating Temperature	Industrial Temperature Range	-40 to +85	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

PIN DESCRIPTION

Pin Name	Pin Number	Type	Functional Description
REF	1	IN	Input reference clock, 5 Volt tolerant input
CLKA1(1)	2	Out	Output clock for bank A
CLKA2(1)	3	Out	Output clock for bank A
V_{DD}	4, 13	PWR	3.3V Supply
GND	5, 12	GND	Ground
CLKB1(1)	6	Out	Output clock for bank B
CLKB2(1)	7	Out	Output clock for bank B
S2(2)	8	IN	Select input Bit 2
S1(2)	9	IN	Select input Bit 1
CLKB3(1)	10	Out	Output clock for bank B
CLKB4(1)	11	Out	Output clock for bank B
CLKA3(1)	14	Out	Output clock for bank A
CLKA4(1)	15	Out	Output clock for bank A
CLKOUT(1)	16	Out	Output clock, internal feedback on this pin

NOTES:
1. Weak pull down on all outputs.
2. Weak pull ups on these inputs.

FUNCTION TABLE(1)

S2	S1	CLKA	CLKB	CLKOUT(2)	Output Source	PLL Shut Down
L	L	Tri-State	Tri-State	Driven	PLL	N
L	H	Driven	Tri-State	Driven	PLL	N
H	L	Driven	Driven	Driven	REF	Y
H	H	Driven	Driven	Driven	PLL	N

NOTES:
1. H = HIGH Voltage Level.
   L = LOW Voltage Level
2. This output is driven and has an internal feedback for the PLL. The load on this ouput can be adjusted to change the skew between the REF and the output.

DC ELECTRICAL CHARACTERISTICS - COMMERCIAL

Symbol	Parameter	Conditions		Min.	Max.	Unit
V_{IL}	Input LOW Voltage Level			—	0.8	V
V_{IH}	Input HIGH Voltage Level			2	—	V
I_{IL}	Input LOW Current	V_{IN} = 0V		—	50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		—	100	µA
V_{OL}	Output LOW Voltage	Standard Drive	I_{OL} = 8mA	—	0.4	V
		High Drive	I_{OL} = 12mA (-1H)			
V_{OH}	Output HIGH Voltage	Standard Drive	I_{OH} = -8mA	2.4	—	V
		High Drive	I_{OH} = -12mA (-1H)			
I_{DD_PD}	Power Down Current	REF = 0MHz (S2 = S1 = H)		—	12	µA
I_{DD}	Supply Current	Unloaded Outputs at 66.66MHz, SEL inputs at V_{DD} or GND		—	32	mA

OPERATING CONDITIONS - COMMERCIAL

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage	3	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance < 100MHz	—	30	pF
	Load Capacitance 100MHz - 133MHz	—	10	
C_{IN}	Input Capacitance	—	7	pF

SWITCHING CHARACTERISTICS (2309-1) - COMMERCIAL (1,2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_1	Output Frequency	10pF Load	10	—	133	MHz
		30pF Load	10	—	100	
	Duty Cycle = $t_2 \div t_1$	Measured at 1.4V, F_{OUT} = 66.66MHz	40	50	60	%
t_3	Rise Time	Measured between 0.8V and 2V	—	—	2.5	ns
t_4	Fall Time	Measured between 0.8V and 2V	—	—	2.5	ns
t_5	Output to Output Skew	All outputs equally loaded	—	—	250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge(2)	Measured at $V_{DD}/2$	—	0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge(2)	Measured at $V_{DD}/2$ in PLL bypass mode (IDT2309 only)	1	5	8.7	ns
t_7	Device-to-Device Skew	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	—	0	700	ps
t_J	Cycle-to-Cycle Jitter	Measured at 66.66MHz, loaded outputs	—	—	200	ps
t_{LOCK}	PLL Lock Time	Stable power supply, valid clock presented on REF pin	—	—	1	ms

NOTES:
1. REF Input has a threshold voltage of $V_{DD}/2$.
2. All parameters specified with loaded outputs.

SWITCHING CHARACTERISTICS (2309-1H) - COMMERCIAL (1,2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_1	Output Frequency	10pF Load	10	—	133	MHz
		30pF Load	10	—	100	
	Duty Cycle = $t_2 \div t_1$	Measured at 1.4V, F_{OUT} = 66.66MHz	40	50	60	%
	Duty Cycle = $t_2 \div t_1$	Measured at 1.4V, F_{OUT} <50MHz	45	50	55	%
t_3	Rise Time	Measured between 0.8V and 2V	—	—	1.5	ns
t_4	Fall Time	Measured between 0.8V and 2V	—	—	1.5	ns
t_5	Output to Output Skew	All outputs equally loaded	—	—	250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at $V_{DD}/2$	—	0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at $V_{DD}/2$ in PLL bypass mode (IDT2309 only)	1	5	8.7	ns
t_7	Device-to-Device Skew	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	—	0	700	ps
t_8	Output Slew Rate	Measured between 0.8V and 2V using Test Circuit 2	1	—	—	V/ns
t_J	Cycle-to-Cycle Jitter	Measured at 66.66MHz, loaded outputs	—	—	200	ps
t_{LOCK}	PLL Lock Time	Stable power supply, valid clock presented on REF pin	—	—	1	ms

NOTES:
1. REF Input has a threshold voltage of $V_{DD}/2$.
2. All parameters specified with loaded outputs.

DC ELECTRICAL CHARACTERISTICS - INDUSTRIAL

Symbol	Parameter	Conditions		Min.	Max.	Unit
V_{IL}	Input LOW Voltage Level			—	0.8	V
V_{IH}	Input HIGH Voltage Level			2	—	V
I_{IL}	Input LOW Current	V_{IN} = 0V		—	50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		—	100	µA
V_{OL}	Output LOW Voltage	Standard Drive	I_{OL} = 8mA	—	0.4	V
		High Drive	I_{OL} = 12mA (-1H)			
V_{OH}	Output HIGH Voltage	Standard Drive	I_{OH} = -8mA	2.4	—	V
		High Drive	I_{OH} = -12mA (-1H)			
I_{DD_PD}	Power Down Current	REF = 0MHz (S2 = S1 = H)		—	25	µA
I_{DD}	Supply Current	Unloaded Outputs at 66.66MHz, SEL inputs at V_{DD} or GND		—	35	mA

OPERATING CONDITIONS - INDUSTRIAL

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage	3	3.6	V
T_A	Operating Temperature (Ambient Temperature)	-40	+85	°C
C_L	Load Capacitance < 100MHz	—	30	pF
	Load Capacitance 100MHz - 133MHz	—	10	
C_{IN}	Input Capacitance	—	7	pF

SWITCHING CHARACTERISTICS (2309-1) - INDUSTRIAL (1,2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_1	Output Frequency	10pF Load	10	—	133	MHz
		30pF Load	10	—	100	
	Duty Cycle = $t_2 \div t_1$	Measured at 1.4V, F_{OUT} = 66.66MHz	40	50	60	%
t_3	Rise Time	Measured between 0.8V and 2V	—	—	2.5	ns
t_4	Fall Time	Measured between 0.8V and 2V	—	—	2.5	ns
t_5	Output to Output Skew	All outputs equally loaded	—	—	250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at $V_{DD}/2$	—	0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at $V_{DD}/2$ in PLL bypass mode (IDT2309 only)	1	5	8.7	ns
t_7	Device-to-Device Skew	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	—	0	700	ps
t_J	Cycle-to-Cycle Jitter	Measured at 66.66MHz, loaded outputs	—	—	200	ps
t_{LOCK}	PLL Lock Time	Stable power supply, valid clock presented on REF pin	—	—	1	ms

NOTES:
1. REF Input has a threshold voltage of $V_{DD}/2$.
2. All parameters specified with loaded outputs.

SWITCHING CHARACTERISTICS (2309-1H) - INDUSTRIAL (1,2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_1	Output Frequency	10pF Load	10	—	133	MHz
		30pF Load	10	—	100	
	Duty Cycle = $t_2 \div t_1$	Measured at 1.4V, F_{OUT} = 66.66MHz	40	50	60	%
	Duty Cycle = $t_2 \div t_1$	Measured at 1.4V, F_{OUT} <50MHz	45	50	55	%
t_3	Rise Time	Measured between 0.8V and 2V	—	—	1.5	ns
t_4	Fall Time	Measured between 0.8V and 2V	—	—	1.5	ns
t_5	Output to Output Skew	All outputs equally loaded	—	—	250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at $V_{DD}/2$	—	0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge	Measured at $V_{DD}/2$ in PLL bypass mode (IDT2309 only)	1	5	8.7	ns
t_7	Device-to-Device Skew	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	—	0	700	ps
t_8	Output Slew Rate	Measured between 0.8V and 2V using Test Circuit 2	1	—	—	V/ns
t_J	Cycle-to-Cycle Jitter	Measured at 66.66MHz, loaded outputs	—	—	200	ps
t_{LOCK}	PLL Lock Time	Stable power supply, valid clock presented on REF pin	—	—	1	ms

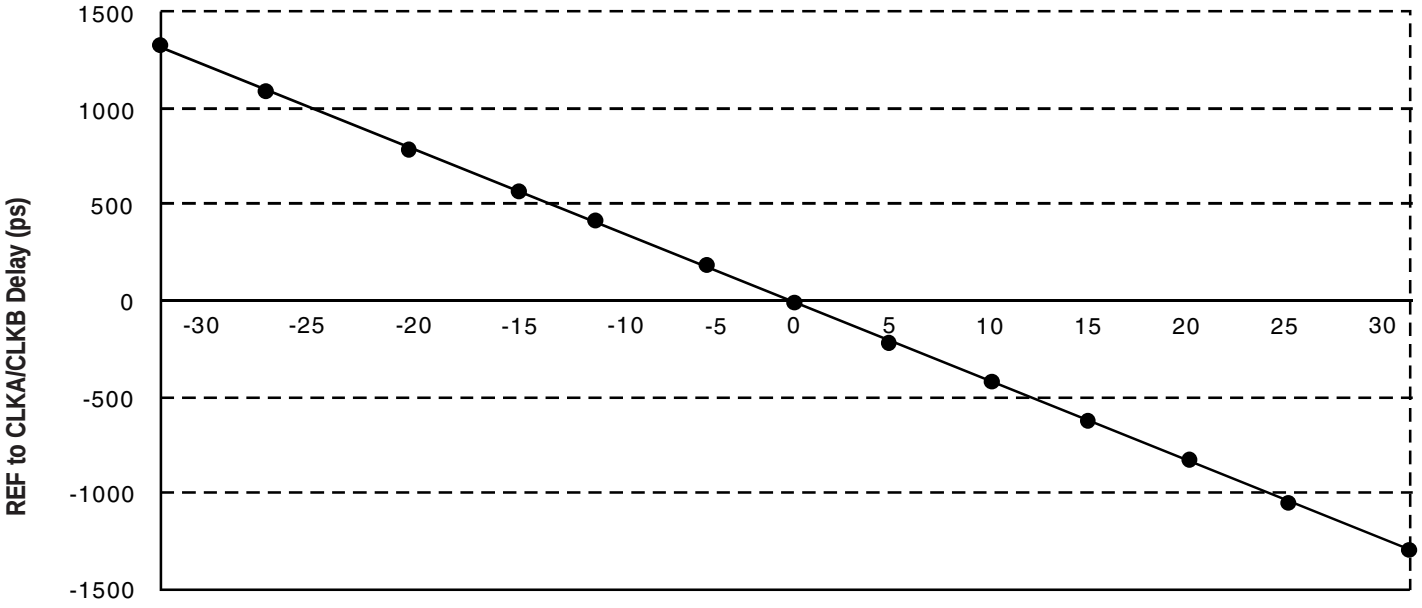
NOTES:
1. REF Input has a threshold voltage of $V_{DD}/2$.
2. All parameters specified with loaded outputs.

ZERO DELAY AND SKEW CONTROL

All outputs should be uniformly loaded in order to achieve Zero I/O Delay. Since the CLKOUT pin is the internal feedback for the PLL, its relative loading can affect and adjust the input/output delay. The Output Load Difference diagram illustrates the PLL's relative loading with respect to the other outputs that can adjust the Input-Output (I/O) Delay.

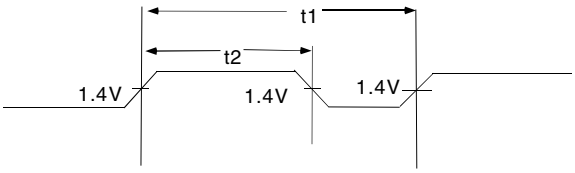
For designs utilizing zero I/O Delay, all outputs including CLKOUT must be equally loaded. Even if the output is not used, it must have a capacitive load equal to that on the other outputs in order to obtain true zero I/O Delay. If I/O Delay adjustments are needed, use the Output Load Difference diagram to calculate loading differences between the CLKOUT pin and other outputs. For zero output-to-output skew, all outputs must be loaded equally.

REF TO CLKA/CLKB RELAY vs. OUTPUT LOAD DIFFERENCE BETWEEN CLKOUT PIN AND CLKA/CLKB PINS

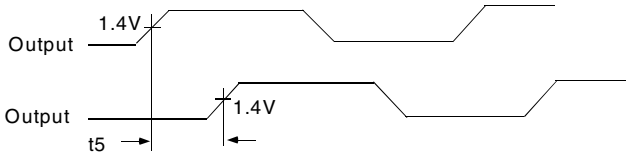


OUTPUT LOAD DIFFERENCE BETWEEN CLKOUT PIN AND CLKA/CLKB PINS (pF)

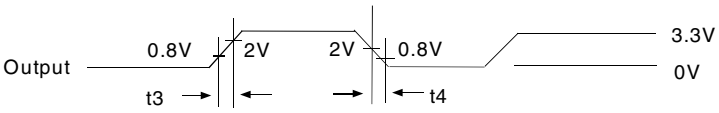
SWITCHING WAVEFORMS



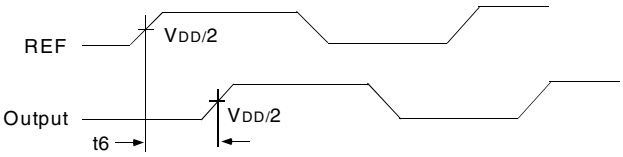
Duty Cycle Timing



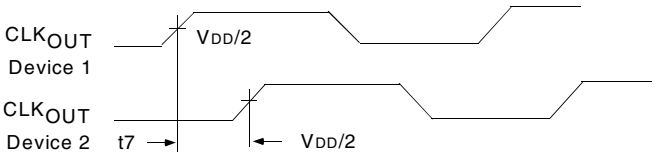
Output to Output Skew



All Outputs Rise/Fall Time

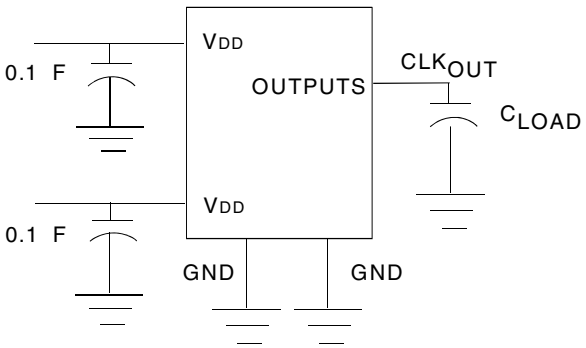


Input to Output Propagation Delay

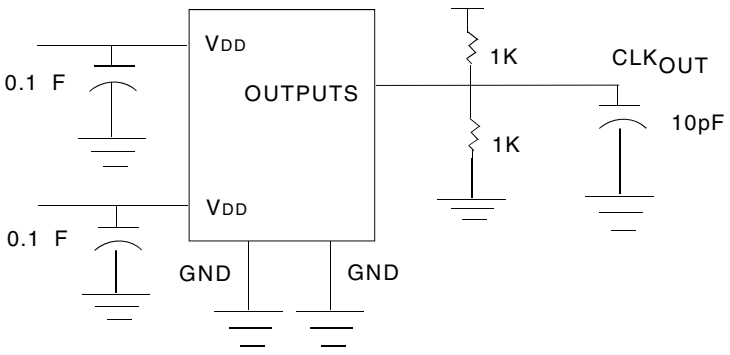


Device to Device Skew

TEST CIRCUITS

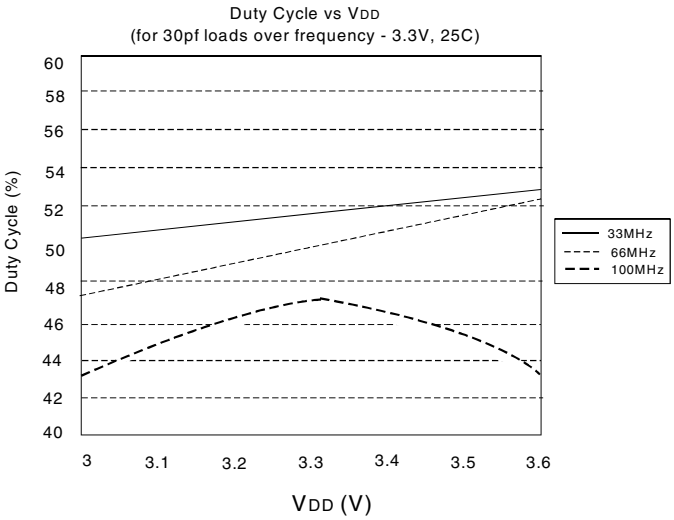


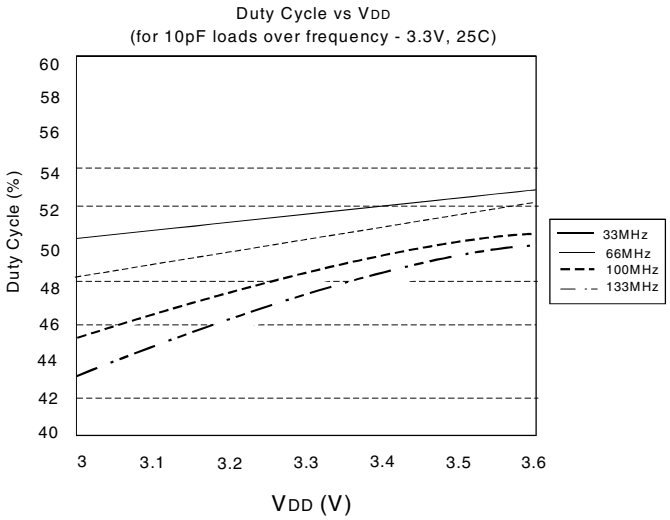
Test Circuit 1 (all Parameters Except t8)

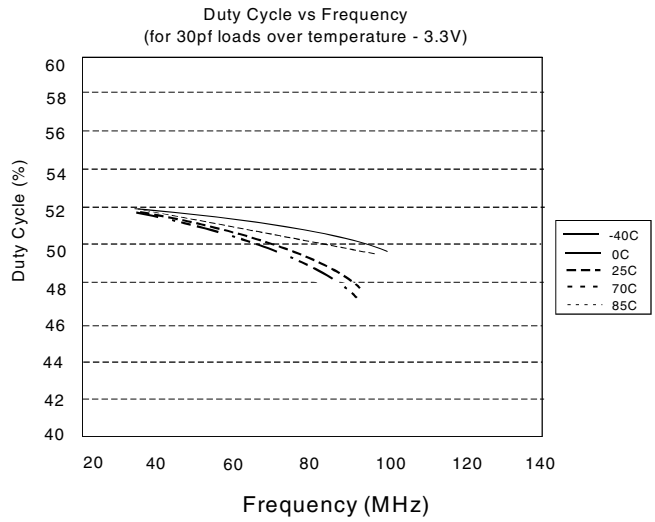


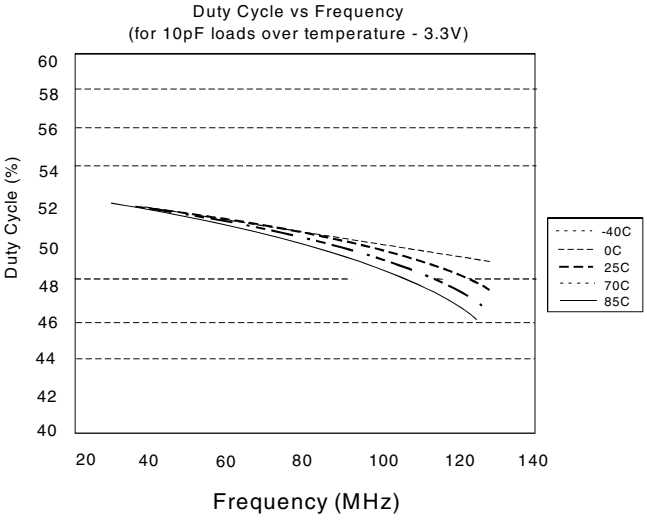
Test Circuit 2 (t8, Output Slew Rate On -1H Devices)

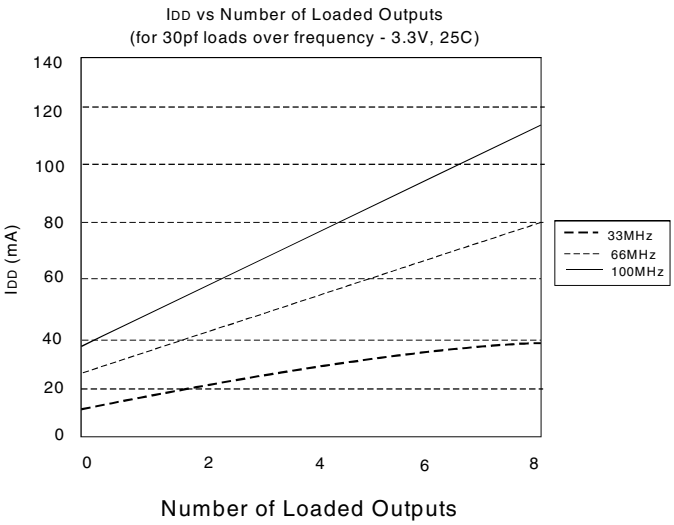
TYPICAL DUTY CYCLE(1) AND IDD TRENDS(2) FOR IDT2309-1

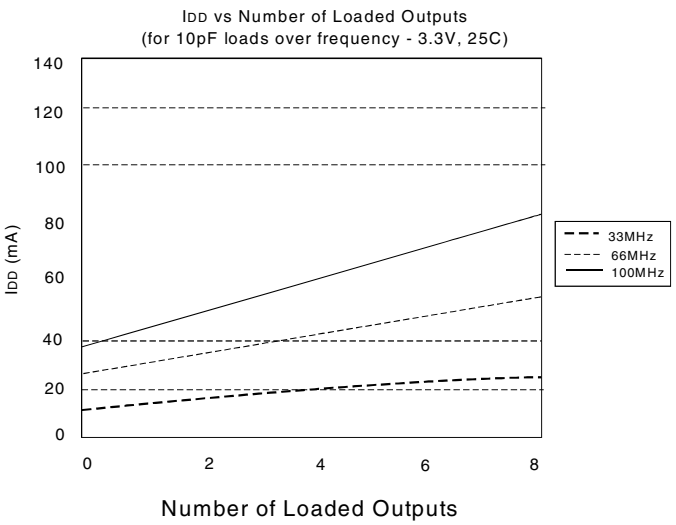








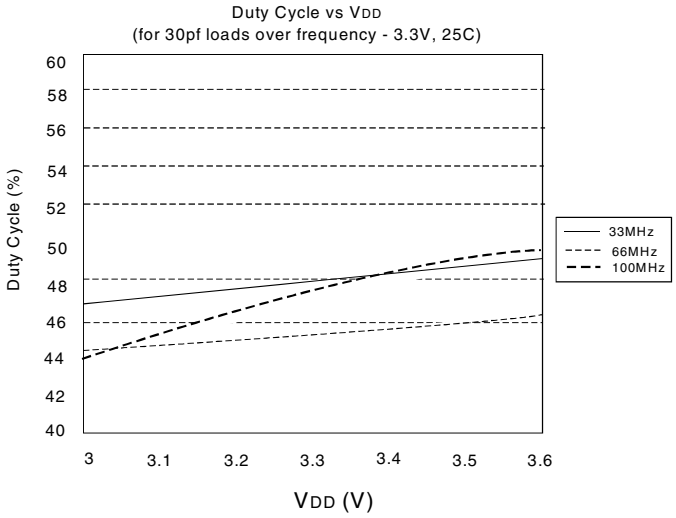


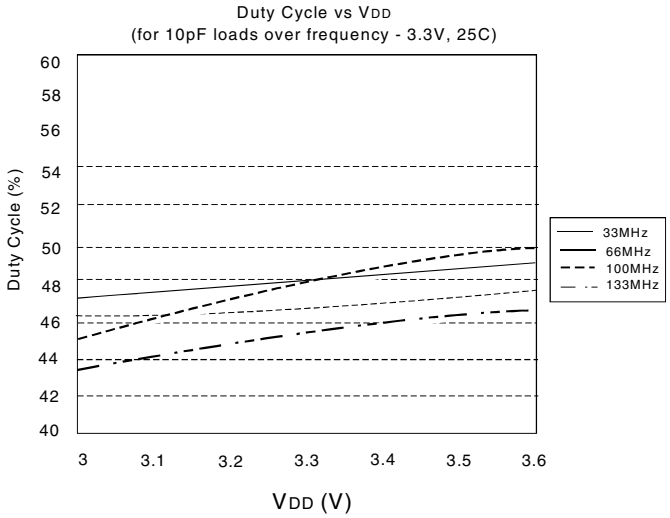


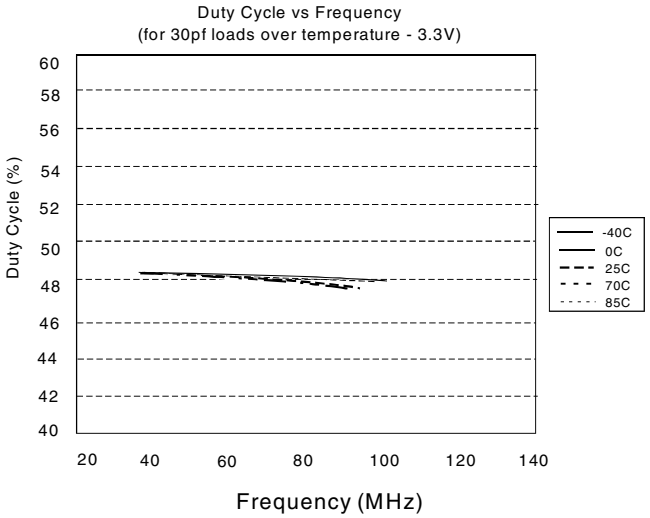
NOTES:

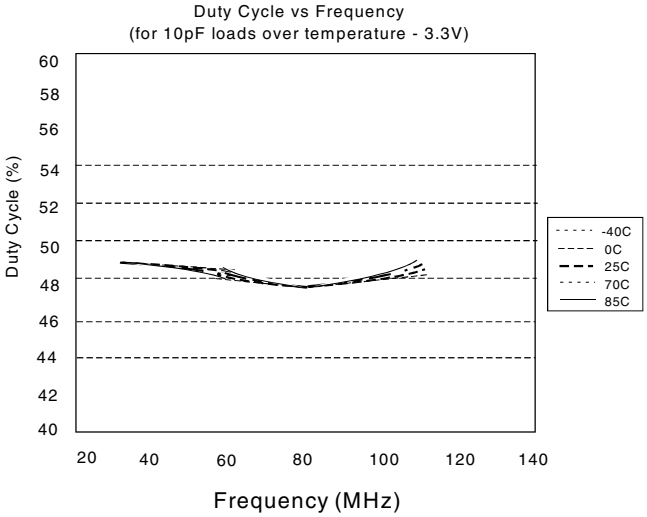
1. Duty Cycle is taken from typical chip measured at 1.4V.
2. IDD data is calculated from IDD = ICORE + nCVf, where ICORE is the unloaded current. (n = Number of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = Frequency (Hz))

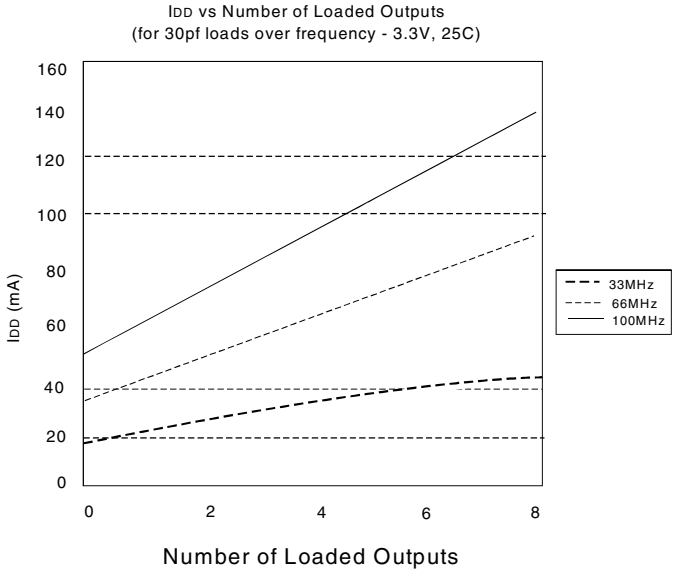
TYPICAL DUTY CYCLE(1) AND IDD TRENDS(2) FOR IDT2309-1H

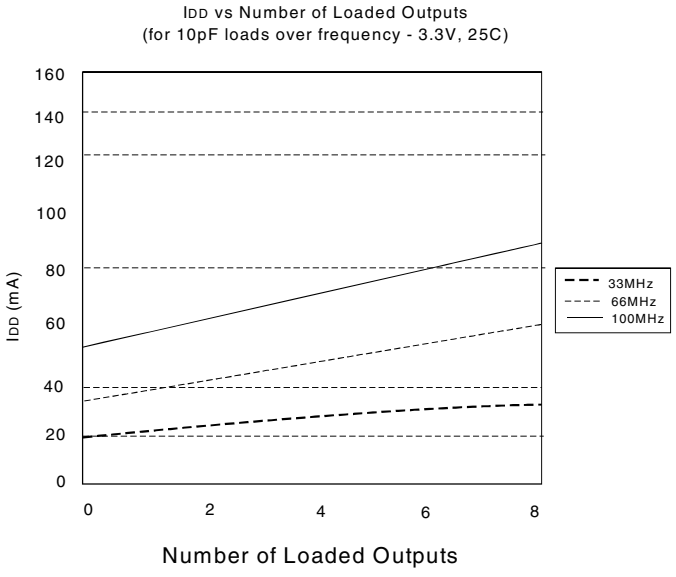








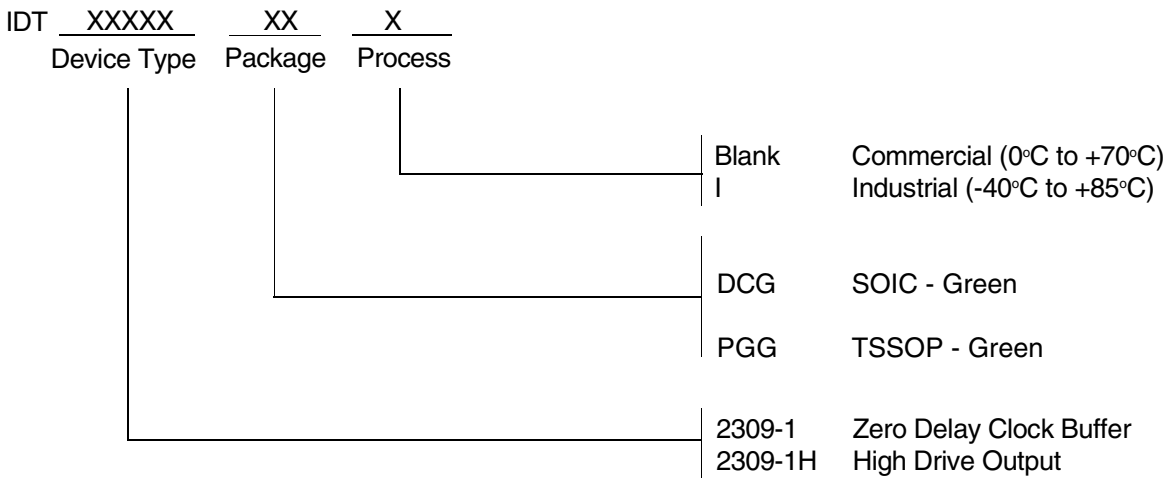




NOTES:

1. Duty Cycle is taken from typical chip measured at 1.4V.
2. IDD data is calculated from IDD = ICORE + nCVf, where ICORE is the unloaded current. (n = Number of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = Frequency (Hz))

ORDERING INFORMATION



Ordering Code	Package Type	Operating Range
IDT2309-1DCG	16-Pin SOIC	Commercial
IDT2309-1DCGI	16-Pin SOIC	Industrial
IDT2309-1HDCG	16-Pin SOIC	Commercial
IDT2309-1HDCGI	16-Pin SOIC	Industrial
IDT2309-1HPG	16-Pin TSSOP	Commercial
IDT2309-1HPGG	16-Pin TSSOP	Commercial
IDT2309-1HPGI	16-Pin TSSOP	Industrial
IDT2309-1HPGGI	16-Pin TSSOP	Industrial

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Renesas Electronics:

2309-1HPGG 2309-1HDCG 2309-1DCGI8 2309-1HDCG8 2309-1HPGG8 2309-1HDCGI8 2309-1DCGI 2309-1HDCGI 2309-1DCG 2309-1HPGGI 2309-1DCG8 2309-1HPGGI8 2309M-1 2309M-1T