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# FDMA1028NZ

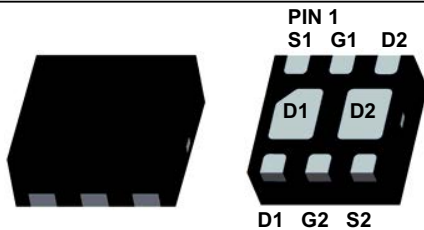
## Dual N-Channel PowerTrench® MOSFET

### General Description

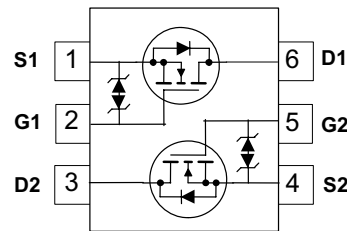
This device is designed specifically as a single package solution for dual switching requirements in cellular handset and other ultra-portable applications. It features two independent N-Channel MOSFETs with low on-state resistance for minimum conduction losses. The MicroFET 2x2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

### Features

- 3.7 A, 20V.  $R_{DS(ON)} = 68\text{ m}\Omega @ V_{GS} = 4.5\text{V}$   
 $R_{DS(ON)} = 86\text{ m}\Omega @ V_{GS} = 2.5\text{V}$
- Low profile – 0.8 mm maximum – in the new package MicroFET 2x2 mm
- HBM ESD protection level > 2kV (Note 3)
- RoHS Compliant
- Free from halogenated compounds and antimony oxides



MicroFET 2x2



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DS</sub>	Drain-Source Voltage	20	V
V <sub>GS</sub>	Gate-Source Voltage	±12	V
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	3.7	A
	– Pulsed	6	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a) (Note 1b)	1.4	W
		0.7	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	–55 to +150	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	86 (Single Operation)	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1b)	173 (Single Operation)	
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1c)	69 (Dual Operation)	
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1d)	151 (Dual Operation)	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
028	FDMA1028NZ	7"	8mm	3000 units

### Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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#### Off Characteristics

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		15		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate–Body Leakage	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

#### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		–4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 3.7\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 3.3\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 3.7\text{ A}, T_J = 125^\circ\text{C}$		37 50 53	68 86 90	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 3.7\text{ A}$		16		S

#### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		340		pF
$C_{oss}$	Output Capacitance			80		pF
$C_{rss}$	Reverse Transfer Capacitance			60		pF
$R_g$	Gate Resistance				25	$\Omega$

#### Switching Characteristics (Note 2)

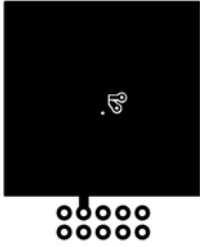
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		8	16	ns
$t_r$	Turn–On Rise Time			8	16	ns
$t_{d(off)}$	Turn–Off Delay Time			14	26	ns
$t_f$	Turn–Off Fall Time			3	6	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 3.7\text{ A},$ $V_{GS} = 4.5\text{ V}$		4	6	nC
$Q_{gs}$	Gate–Source Charge			0.7		nC
$Q_{gd}$	Gate–Drain Charge			1.1		nC

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

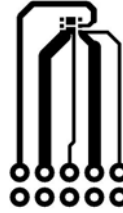
### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.

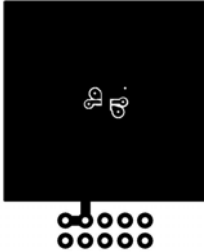
- (a)  $R_{\theta JA} = 86\text{ }^\circ\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For single operation.
- (b)  $R_{\theta JA} = 173\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper. For single operation.
- (c)  $R_{\theta JA} = 69\text{ }^\circ\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For dual operation.
- (d)  $R_{\theta JA} = 151\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper. For dual operation.



a. 86 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 173 °C/W when mounted on a minimum pad of 2 oz copper



c. 69 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



d. 151 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

## Typical Characteristics

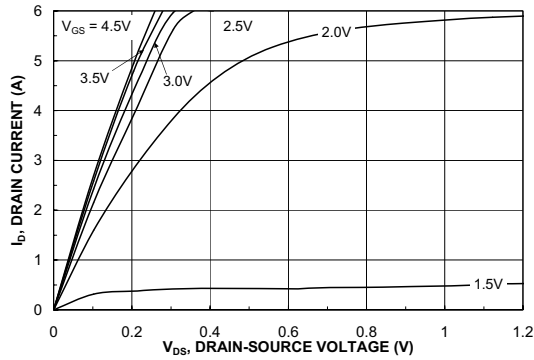


Figure 1. On-Region Characteristics.

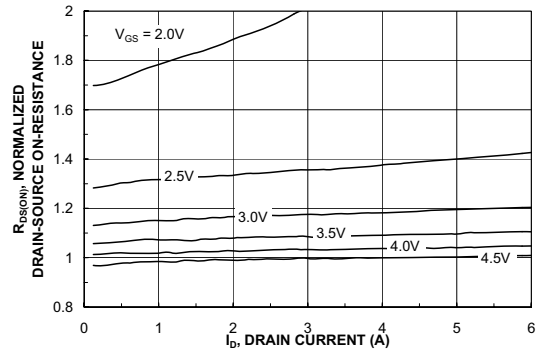


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

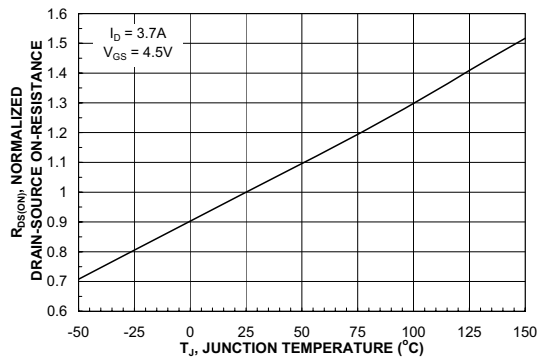


Figure 3. On-Resistance Variation with Temperature.

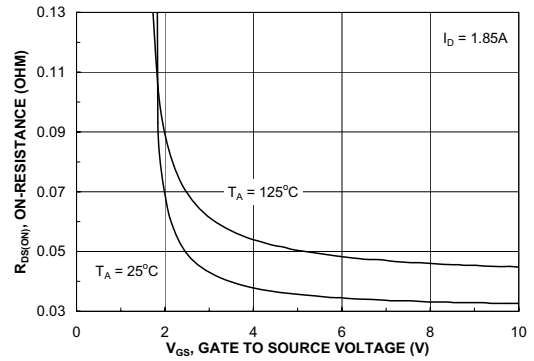


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

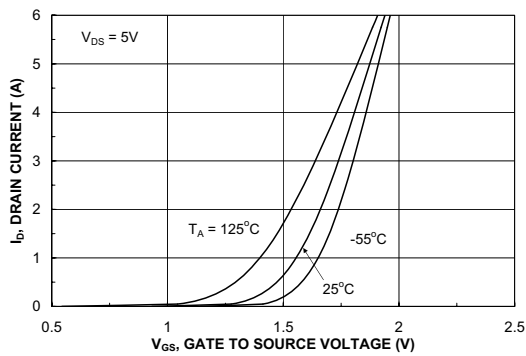


Figure 5. Transfer Characteristics.

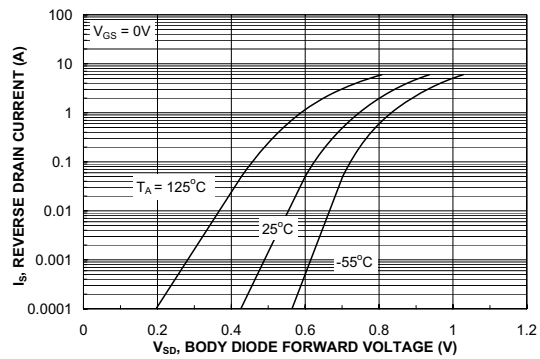


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics

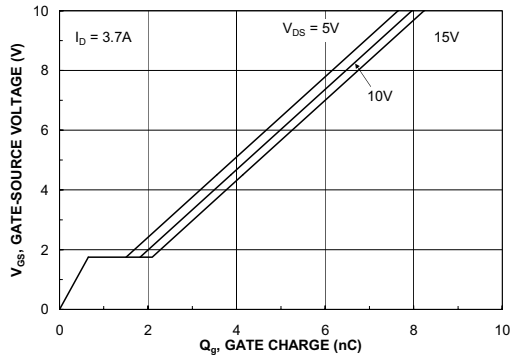


Figure 7. Gate Charge Characteristics.

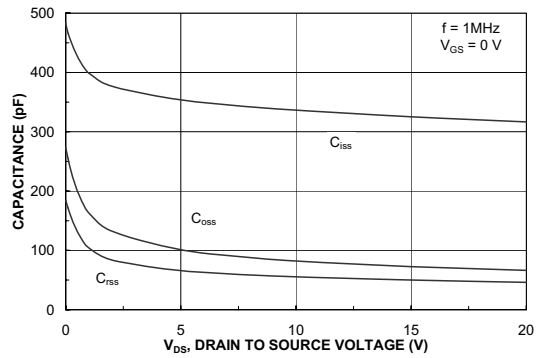


Figure 8. Capacitance Characteristics.

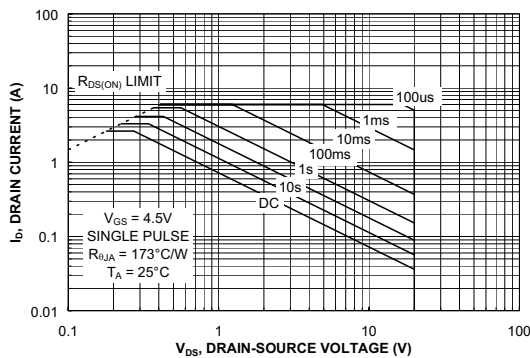


Figure 9. Maximum Safe Operating Area.

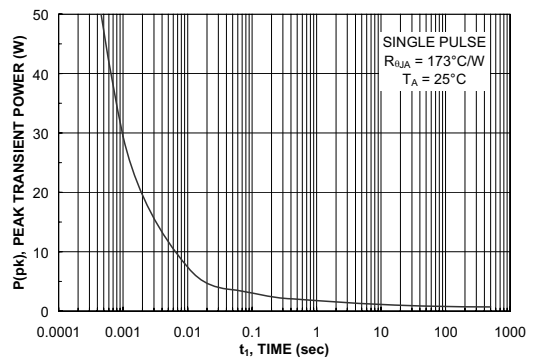


Figure 10. Single Pulse Maximum Power Dissipation.

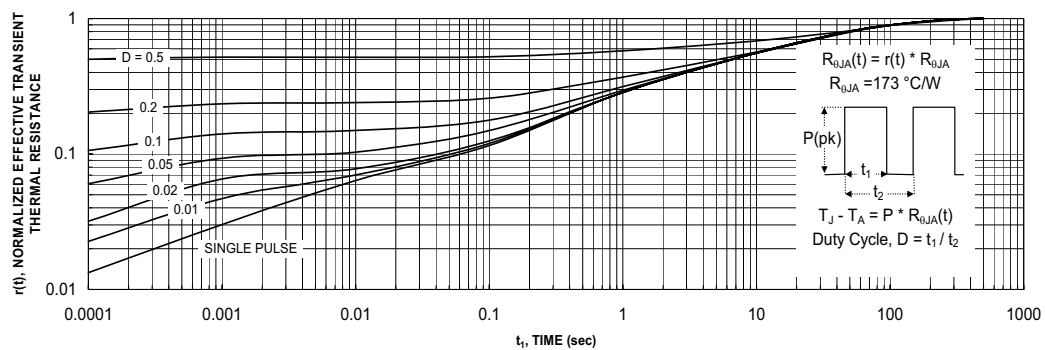
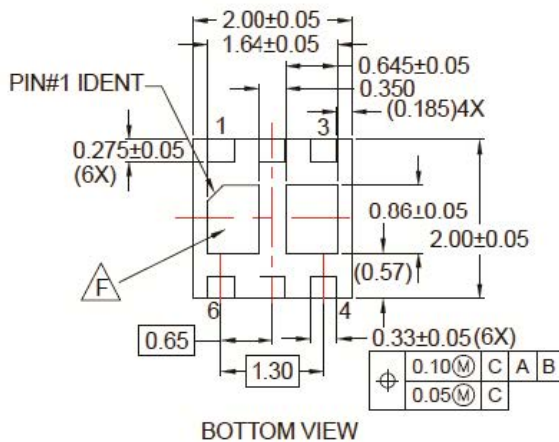
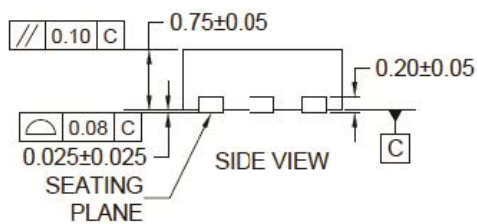
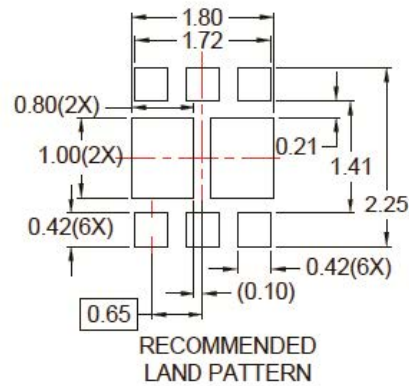
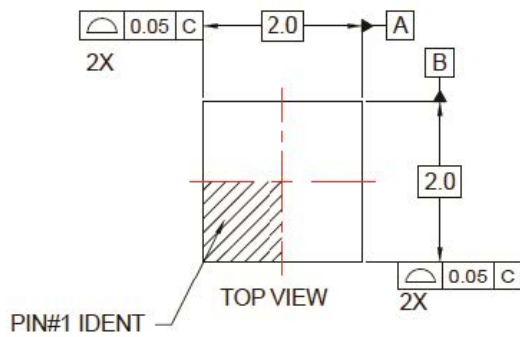


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

## Dimensional Outline and Pad Layout



### NOTES:

- A. CONFORM TO JEDEC REGISTRATIONS MO-229, VARIATION VCCC, EXCEPT WHERE NOTED.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
  - D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
  - E. DRAWING FILENAME: MKT-UMLP16Erev4
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