# 16-Bit, 5V Digital Signal Controllers with PWM, SENT, Op Amps and Advanced Analog Features 

## Operating Conditions

- 4.5 V to $5.5 \mathrm{~V},-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}, \mathrm{DC}$ to 70 MIPS
- 4.5 V to $5.5 \mathrm{~V},-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$, DC to 60 MIPS
- 4.5 V to $5.5 \mathrm{~V},-40^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$, DC to 40 MIPS


## Core: 16-Bit dsPIC33E CPU

- Code-Efficient (C and Assembly) Architecture
- 16-Bit Wide Data Path
- Two 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle, Mixed-Sign MUL plus Hardware Divide
- 32-Bit Multiply Support
- Intermediate Security for Memory:
- Provides a Boot Flash Segment in addition to the existing General Flash Segment
- Error Code Correction (ECC) for Flash
- Added Two Alternate Register Sets for Fast Context Switching


## Clock Management

- Internal, 15\% Low-Power RC (LPRC) - 32 kHz
- Internal, $1 \%$ Fast RC (FRC) - 7.37 MHz
- Internal, 10\% Backup RC (BFRC) - 7.37 MHz
- Programmable PLLs and Oscillator Clock Sources
- Fail-Safe Clock Monitor (FSCM)
- Additional FSCM Source (BFRC), Intended to Provide a Clock Fail Switch Source for the System Clock
- Independent Watchdog Timer (WDT)
- System Windowed Watchdog Timer (DMT)
- Fast Wake-up and Start-up


## Power Management

- Low-Power Management modes (Sleep, Idle and Doze)
- Power Consumption Minimized Executing nop String
- Integrated Power-on Reset (POR) and Brown-out Reset (BOR)
- $0.5 \mathrm{~mA} / \mathrm{MHz}$ Dynamic Current (typical)
- $50 \mu \mathrm{~A}$ at $+25^{\circ} \mathrm{C}$ IPD Current (typical)


## PWM

- Up to Six Pulse-Width Modulation (PWM) Outputs (three generators)
- Primary Master Time Base Inputs allow Time Base Synchronization from Internal/External Sources
- Dead Time for Rising and Falling Edges
- 7.14 ns PWM Resolution
- PWM Support for:
- DC/DC, AC/DC, inverters, Power Factor Correction (PFC) and lighting
- Brushless Direct Current (BLDC), Permanent Magnet Synchronous Motor (PMSM), AC Induction Motor (ACIM), Switched Reluctance Motor (SRM)
- Programmable Fault inputs
- Flexible trigger configurations for Analog-to-Digital conversion
- Supports PWM lock, PWM output chopping and dynamic phase shifting


## Advanced Analog Features

- ADC module:
- Configurable as $10-$ bit, 1.1 Msps with four S\&H or 12-bit, 500 ksps with one S\&H
- Up to 36 analog inputs
- Flexible and Independent ADC Trigger Sources
- Up to Four Op Amp/Comparators with Direct Connection to the ADC module:
- Additional dedicated comparator and 7-bit Digital-to-Analog Converter (DAC)
- Two comparator voltage reference outputs
- Programmable references with 128 voltage points
- Programmable blanking and filtering
- Charge Time Measurement Unit (CTMU):
- Supports mTouch ${ }^{\text {TM }}$ capacitive touch sensing
- Provides high-resolution time measurement (1 ns)
- On-chip temperature measurement
- Temperature sensor diode
- Nine sources of edge input triggers (CTED1, CTED2, OCPWM, TMR1, SYSCLK, OSCLK, FRC, BFRC and LPRC)


## Timers/Output Compare/Input Capture

- Nine General Purpose Timers:
- Five 16-bit and up to two 32-bit timers/counters; Timer3 can provide ADC trigger
- Four Output Capture modules Configurable as Timers/Counters
- Four Input Capture modules


## Communication Interfaces

- Two Enhanced Addressable Universal Asynchronous Receiver/Transmitter (UART) modules ( 6.25 Mbps ):
- With support for LIN/J2602 bus support and IrDA ${ }^{\circledR}$
- High and low speed (SCI)
- Two SPI modules (15 Mbps):
- 25 Mbps data rate without using PPS
- One $I^{2} C^{\top M}$ module (up to 1 Mbaud) with SMBus Support
- Two SENT J2716 (Single-Edge Nibble Transmission-Transmit/Receive) module for Automotive Applications
- One CAN module:
- 32 buffers, 16 filters and three masks


## Direct Memory Access (DMA)

- 4-Channel DMA with User-Selectable Priority Arbitration
- UART, Serial Peripheral Interface (SPI), ADC, Input Capture, Output Compare and Controller Area Network (CAN)


## Input/Output

- GPI/O Registers to Support Selectable Slew Rate I/O
- Peripheral Pin Select (PPS) to allow Function Remap
- Sink/Source: 8 mA or 12 mA , Pin-Specific for Standard Voh/Vol
- Selectable Open-Drain, Pull-ups and Pull-Downs
- Change Notice Interrupts on All I/O Pins


## Qualification and Class B Support

- AEC-Q100 REVG (Grade 1: $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ ) Completed
- AEC-Q100 REVG (Grade 0: $-40^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ ) Planned
- Class B Safety Library, IEC 60730


## Class B Fault Handling Support

- Backup FRC
- Windowed WDT uses LPRC
- Windowed Deadman Timer (DMT) uses System Clock (System Windowed Watchdog Timer)
- H/W Clock Monitor Circuit
- Oscillator Frequency Monitoring through CTMU (OSCI, SYSCLK, FRC, BFRC, LPRC)
- Dedicated PWM Fault Pin
- Lockable Clock Configuration


## Debugger Development Support

- In-Circuit and In-Application Programming
- Three Complex and Five Simple Breakpoints
- Trace and Run-Time Watch
dsPIC33EVXXXGM00X/10X PRODUCT FAMILIES
The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. The following pages show the devices' pinout diagrams.



## Pin Diagrams



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See Section 11.5 "Peripheral Pin Select (PPS)" for available peripherals and information on limitations.
2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See Section 11.0 "I/O Ports" for more information.
3: If the op amp is selected when OPAEN $(C M x C O N<10>)=1$, the $O A x$ input is used; otherwise, the ANx input is used.

## Pin Diagrams (Continued)



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See Section 11.5 "Peripheral Pin Select (PPS)" for available peripherals and information on limitations.
2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See Section 11.0 "I/O Ports" for more information.
3: If the op amp is selected when OPAEN $(C M x C O N<10>)=1$, the OAx input is used; otherwise, the ANx input is used.
4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

## Pin Diagrams (Continued)



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See Section 11.5 "Peripheral Pin Select (PPS)" for available peripherals and information on limitations.
2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See Section 11.0 "I/O Ports" for more information.
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## Pin Diagrams (Continued)

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## Pin Diagrams (Continued)



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See Section 11.5 "Peripheral Pin Select (PPS)" for available peripherals and information on limitations.
2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See Section 11.0 "I/O Ports" for more information.
3: If the op amp is selected when OPAEN $(C M x C O N<10>)=1$, the OAx input is used; otherwise, the ANx input is used.
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## Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

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## Referenced Sources

This device data sheet is based on the following individual chapters of the "dsPIC33/PIC24 Family Reference Manual", which are available from the Microchip web site (www.microchip.com). The following documents should be considered as the general reference for the operation of a particular module or device feature:

- "Introduction" (DS70573)
- "CPU" (DS70359)
- "Data Memory" (DS70595)
- "Program Memory" (DS70613)
- "Flash Programming" (DS70609)
- "Interrupts" (DS70000600)
- "Oscillator" (DS70580)
- "Reset" (DS70602)
- "Watchdog Timer and Power-Saving Modes" (DS70615)
- "I/O Ports" (DS70000598)
- "Timers" (DS70362)
- "CodeGuard ${ }^{\text {TM }}$ Intermediate Security" (DS70005182)
- "Deadman Timer (DMT)" (DS70005155)
- "Input Capture" (DS70000352)
- "Output Compare" (DS70005157)
- "High-Speed PWM"(DS70645)
- "Analog-to-Digital Converter (ADC)" (DS70621)
- "Universal Asynchronous Receiver Transmitter (UART)" (DS70000582)
- "Serial Peripheral Interface (SPI)" (DS70005185)
- "Inter-Integrated Circuit ${ }^{T M}\left(I^{2} C^{\text {TM }}\right) "$ " (DS70000195)
- "Enhanced Controller Area Network (ECAN ${ }^{\text {TM }}$ )"(DS70353)
- "Direct Memory Access (DMA)" (DS70348)
- "Programming and Diagnostics" (DS70608)
- "Op Amp/Comparator" (DS70000357)
- "Device Configuration" (DS70000618)
- "Charge Time Measurement Unit (CTMU)" (DS70661)
- "Single-Edge Nibble Transmission (SENT) Module" (DS70005145)


### 1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EVXXXGM00X/10X family Digital Signal Controller (DSC) devices.
dsPIC33EVXXXGM00X/10X family devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.
Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33EVXXXGM00X/10X FAMILY BLOCK DIAGRAM


TABLE 1-1: PINOUT I/O DESCRIPTIONS

| Pin Name | $\begin{gathered} \text { Pin } \\ \text { Type } \end{gathered}$ | Buffer Type | PPS | Description |
| :---: | :---: | :---: | :---: | :---: |
| AN0-AN35 | 1 | Analog | No | Analog input channels. |
| $\begin{aligned} & \text { CLKI } \\ & \text { CLKO } \end{aligned}$ | 1 0 | ST/ CMOS - | No | External clock source input. Always associated with OSC1 pin function. <br> Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function. |
| $\begin{aligned} & \text { OSC1 } \\ & \text { OSC2 } \end{aligned}$ | I | ST/ CMOS - | No <br> No | Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. <br> Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. |
| REFCLKO | O | - | Yes | Reference clock output. |
| IC1-IC4 | 1 | ST | Yes | Capture Inputs 1 to 4. |
| $\begin{aligned} & \text { OCFA } \\ & \text { OC1-OC4 } \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \end{aligned}$ | ST | Yes Yes | Compare Fault A input (for compare channels). Compare Outputs 1 to 4. |
| $\begin{aligned} & \hline \text { INT0 } \\ & \text { INT1 } \\ & \text { INT2 } \end{aligned}$ | $\begin{aligned} & \text { I } \\ & \text { । } \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { ST } \\ & \text { ST } \\ & \text { ST } \end{aligned}$ | No <br> Yes <br> Yes | External Interrupt 0. <br> External Interrupt 1. <br> External Interrupt 2. |
| RA0-RA4, RA7-RA12 | I/O | ST | Yes | PORTA is a bidirectional I/O port. |
| RB0-RB15 | I/O | ST | Yes | PORTB is a bidirectional I/O port. |
| RC0-RC13, RC15 | I/O | ST | Yes | PORTC is a bidirectional I/O port. |
| RD5-RD6, RD8 | I/O | ST | Yes | PORTD is a bidirectional I/O port. |
| RE12-RE15 | I/O | ST | Yes | PORTE is a bidirectional I/O port. |
| RF0-RF1 | I/O | ST | No | PORTF is a bidirectional I/O port. |
| RG6-RG9 | I/O | ST | Yes | PORTG is a bidirectional I/O port. |
| $\begin{aligned} & \hline \text { T1CK } \\ & \text { T2CK } \\ & \text { T3CK } \\ & \text { T4CK } \\ & \text { T5CK } \end{aligned}$ | $\begin{aligned} & \text { I } \\ & \text { I } \\ & \text { I } \end{aligned}$ | $\begin{aligned} & \text { ST } \\ & \text { ST } \\ & \text { ST } \\ & \text { ST } \\ & \text { ST } \end{aligned}$ | No Yes No No No | Timer1 external clock input. Timer2 external clock input. Timer3 external clock input. Timer4 external clock input. Timer5 external clock input. |
|  | $\begin{aligned} & \mathrm{O} \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & \text { ST } \\ & \text { ST } \\ & \text { ST } \end{aligned}$ | $\begin{aligned} & \text { No } \\ & \text { No } \\ & \text { No } \end{aligned}$ | CTMU pulse output. CTMU External Edge Input 1. CTMU External Edge Input 2. |
| $\begin{aligned} & \hline \hline \text { U1CTS } \\ & \hline \text { U1RTS } \\ & \text { U1RX } \\ & \text { U1TX } \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \\ & 1 \\ & 0 \end{aligned}$ | ST <br> $\overline{\text { ST }}$ <br> - | Yes <br> Yes <br> Yes <br> Yes | UART1 Clear-to-Send. UART1 Ready-to-Send. UART1 receive. UART1 transmit. |
| $\begin{aligned} & \hline \overline{\mathrm{U} 2 \mathrm{CTS}} \\ & \hline \mathrm{U} 2 R T S \\ & \text { U2RX } \\ & \text { U2TX } \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \\ & 1 \\ & 0 \end{aligned}$ | $\frac{S T}{-}$ - | Yes <br> Yes <br> Yes <br> Yes | UART2 Clear-to-Send. UART2 Ready-to-Send. UART2 receive. UART2 transmit. |
| $\begin{aligned} & \hline \text { SCK1 } \\ & \text { SDI1 } \\ & \frac{\text { SDO1 }}{\text { SS1 }} \end{aligned}$ | $\begin{gathered} \text { I/O } \\ 1 \\ 0 \\ 1 / \mathrm{O} \end{gathered}$ | $\begin{aligned} & \text { ST } \\ & \text { ST } \\ & \hline- \end{aligned}$ | No <br> No <br> No <br> No | Synchronous serial clock input/output for SPI1. SPI1 data in. <br> SPI1 data out. <br> SPI1 slave synchronization or frame pulse I/O. |

Legend: $\mathrm{CMOS}=\mathrm{CMOS}$ compatible input or output ST = Schmitt Trigger input with CMOS levels PPS = Peripheral Pin Select

| Analog = Analog input | $\mathrm{P}=$ Power |
| :--- | :--- |
| $\mathrm{O}=$ Output | $\mathrm{I}=$ Input |

TTL = TTL input buffer

## TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)



TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

| Pin Name | Pin Type | Buffer Type | PPS |  | Descriptio |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| AVDD | P | P | No | Positive s times. | for analog modules. Th | must be conn |
| AVss | P | P | No | Ground re | ce for analog modules. |  |
| Vdd | P | - | No | Positive | for peripheral logic and |  |
| VCAP | P | - | No | CPU logic | capacitor connection. |  |
| Vss | P | - | No | Ground re | ce for logic and I/O pins |  |
| Legend: CMOS = CMOS compatible input or output <br> ST = Schmitt Trigger input with CMOS levels PPS = Peripheral Pin Select <br> Analog = Analog input $\mathrm{O}=$ Output TTL = TTL input buffer |  |  |  |  |  | $\begin{aligned} & \text { P = Power } \\ & \mathrm{I}=\text { Input } \end{aligned}$ |

### 2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

### 2.1 Basic Connection Requirements

Getting started with the dsPIC33EVXXXGM00X/10X family of 16 -bit microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All Vdd and Vss pins (see Section 2.2 "Decoupling Capacitors")
- All AVDD and AVss pins (regardless if ADC module is not used)
(see Section 2.2 "Decoupling Capacitors")
- Vcap
(see Section 2.3 "CPU Logic Filter Capacitor Connection (VcAP)")
- MCLR pin
(see Section 2.4 "Master Clear (MCLR) Pin")
- PGECx/PGEDx pins used for In-Circuit Serial Programming ${ }^{\text {TM }}$ (ICSP ${ }^{\text {TM }}$ ) and debugging purposes (see Section 2.5 "ICSP Pins")
- OSC1 and OSC2 pins when external oscillator source is used
(see Section 2.6 "External Oscillator Pins")
Note: The AVDD and AVss pins must be connected, regardless of the ADC voltage reference source.


### 2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, Vss, AVDd and AVss, is required.
Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A value of $0.1 \mu \mathrm{~F}$ ( 100 nF ), $10 \mathrm{~V}-20 \mathrm{~V}$ is recommended. This capacitor should be a Low Equivalent Series Resistance (low-ESR), and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- Placement on the Printed Circuit Board (PCB): The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch ( 6 mm ) in length.
- Handling high-frequency noise: If the board is experiencing high-frequency noise, above tens of MHz , add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of $0.01 \mu \mathrm{~F}$ to $0.001 \mu \mathrm{~F}$. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, $0.1 \mu \mathrm{~F}$ in parallel with $0.001 \mu \mathrm{~F}$.
- Maximizing performance: On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing the PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION


Note 1: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than $1 \Omega$ and the inductor capacity greater than 10 mA .

Where:

$$
\begin{aligned}
& f=\frac{F C N V}{2} \quad \text { (i.e., ADC Conversion Rate/2) } \\
& f=\frac{1}{(2 \pi \sqrt{L C})} \\
& L=\left(\frac{1}{(2 \pi f \sqrt{C})}\right)^{2}
\end{aligned}
$$

### 2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from $4.7 \mu \mathrm{~F}$ to $47 \mu \mathrm{~F}$.

### 2.3 CPU Logic Filter Capacitor Connection (VcAP)

A low-ESR (<1 Ohms) capacitor is required on the Vcap pin, which is used to stabilize the internal voltage regulator output. The Vcap pin must not be connected to VDD, and must have a capacitor greater than $4.7 \mu \mathrm{~F}(10 \mu \mathrm{~F}$ is recommended), with at least a 16 V rating connected to the ground. The type can be ceramic or tantalum. See Section 30.0 "Electrical Characteristics" for additional information.

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length should not exceed one-quarter inch ( 6 mm ).

### 2.4 Master Clear (MCLR) Pin

The $\overline{M C L R}$ pin provides two specific device functions:

- Device Reset
- Device Programming and Debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\mathrm{MCLR}}$ pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of $R$ and $C$ will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-1, it is recommended that the capacitor, C , be isolated from the $\overline{M C L R}$ pin during programming and debugging operations.
Place the components as shown in Figure 2-2 within one-quarter inch ( 6 mm ) from the $\overline{M C L R}$ pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS

dsPIC33EV

Note 1: $R \leq 10 k \Omega$ is recommended. A suggested starting value is $10 \mathrm{k} \Omega$. Ensure that the $\overline{\mathrm{MCLR}}$ pin VIH and VIL specifications are met.
2: R1 $\leq 470 \Omega$ will limit any current flow into MCLR from the external capacitor, C , in the event of $\overline{\mathrm{MCLR}}$ pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{M C L R}$ pin VIH and VIL specifications are met.

### 2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not exceeding 100 Ohms.
Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High $(\mathrm{VIH})$ and Voltage Input Low (VIL) requirements.
Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB ${ }^{\circledR}$ PICkit $^{\text {TM }}$ 3, MPLAB ICD 3 or MPLAB REAL ICE ${ }^{\text {TM }}$.

For more information on MPLAB ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site (www.microchip.com).

- "Using MPLAB ${ }^{\circledR}$ ICD 3" (poster) (DS51765)
- "MPLAB ${ }^{\circledR}$ ICD 3 Design Advisory" (DS51764)
- "MPLAB ${ }^{\circledR}$ REAL ICE ${ }^{\text {TM }}$ In-Circuit Emulator User's Guide" (DS51616)
- "Using MPLAB ${ }^{\circledR}$ REAL ICE ${ }^{\text {TM }}$ In-Circuit Emulator" (poster) (DS51749)


### 2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator. For more information, see Section 9.0 "Oscillator Configuration".
The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed as shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT


### 2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 5 MHz < FIN < 13.6 MHz to comply with device PLL start-up conditions. This intends that, if the external oscillator frequency is outside this range, the application must start up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.
Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLFBD, to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source.
Note: Clock switching must be enabled in the device Configuration Word.

### 2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.
Alternatively, connect a 1 k to 10 k resistor between Vss and unused pins, and drive the output to logic low.

## dsPIC33EVXXXGM00X/10X FAMILY

NOTES:

### 3.0 CPU

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "CPU" (DS70359) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to $4 \mathrm{M} \times 24$ bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

### 3.1 Registers

The dsPIC33EVXXXGM00X/10X family devices have sixteen, 16-bit Working registers in the programmer's model. Each of the Working registers can act as a Data, Address or Address Offset register. The sixteenth Working register (W15) operates as a Software Stack Pointer for interrupts and calls.
In addition, the dsPIC33EVXXXGM00X/10X devices include two alternate Working register sets, which consist of W0 through W14. The alternate registers can be made persistent to help reduce the saving and restoring of register content during Interrupt Service Routines (ISRs). The alternate Working registers can be assigned to a specific Interrupt Priority Level (IPL1 through IPL6) by configuring the CTXTx<2:0> bits in the FALTREG Configuration register.

The alternate Working registers can also be accessed manually by using the CTXTSWP instruction.
The CCTXI<2:0> and MCTXI<2:0> bits in the CTXTSTAT register can be used to identify the current, and most recent, manually selected Working register sets.

### 3.2 Instruction Set

The device instruction set has two classes of instructions: the MCU class of instructions and the DSP class of instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

### 3.3 Data Space Addressing

The Base Data Space can be addressed as 4K words or 8 Kbytes and is split into two blocks, referred to as X and $Y$ data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EV devices, certain DSP instructions operate through the $X$ and $Y$ AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Space boundary is device-specific.
The upper 32 Kbytes of the Data Space (DS) memory map can optionally be mapped into Program Space (PS) at any 16K program word boundary. The Program-toData Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Data Space Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8 M words or 16 Mbytes. For more information on EDS, PSV and table accesses, refer to "Data Memory" (DS70595) and "Program Memory" (DS70613) in the "dsPIC33/PIC24 Family Reference Manual".
On dsPIC33EV devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The $X$ AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms. Figure 3-1 illustrates the block diagram of the dsPIC33EVXXXGM00X/10X family devices.

### 3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

FIGURE 3-1: dsPIC33EVXXXGM00X/10X FAMILY CPU BLOCK DIAGRAM


### 3.5 Programmer's Model

The programmer's model for the dsPIC33EVXXXGM00X/ 10X family is shown in Figure 3-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EVXXXGM00X/10X family devices contain control registers for Modulo Addressing and Bit-Reversed Addressing, and interrupts. These registers are described in subsequent sections of this document.
All registers associated with the programmer's model are memory-mapped, as shown in Table 4-1.

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

| Register(s) Name | Description |
| :---: | :---: |
| W0 through W15 ${ }^{(1)}$ | Working Register Array |
| W0 through W14 ${ }^{(1)}$ | Alternate Working Register Array 1 |
| W0 through W14 ${ }^{(1)}$ | Alternate Working Register Array 2 |
| ACCA, ACCB | 40-Bit DSP Accumulators |
| PC | 23-Bit Program Counter |
| SR | ALU and DSP Engine STATUS Register |
| SPLIM | Stack Pointer Limit Value Register |
| TBLPAG | Table Memory Page Address Register |
| DSRPAG | Extended Data Space (EDS) Read Page Register |
| RCOUNT | REPEAT Loop Count Register |
| DCOUNT | Do Loop Count Register |
| DOSTARTH ${ }^{(2)}$, DOSTARTL ${ }^{(2)}$ | DO Loop Start Address Register (High and Low) |
| DOENDH, DOENDL | Do Loop End Address Register (High and Low) |
| CORCON | Contains DSP Engine, DO Loop Control and Trap Status bits |

Note 1: Memory-mapped W0 through W14 represents the value of the register in the currently active CPU context.
2: The DOSTARTH and DOSTARTL registers are read-only.

FIGURE 3-2: PROGRAMMER'S MODEL


### 3.6 CPU Control Registers

## REGISTER 3-1: SR: CPU STATUS REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/C-0 | R/C-0 | R-0 | R/W-0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OA | OB | $\mathrm{SA}^{(3)}$ | $\mathrm{SB}^{(3)}$ | OAB | SAB | DA | DC |
| bit 15 |  |  | bit 8 |  |  |  |  |


| R/W-0 | R/W-0 | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{IPL2}^{(1,2)}$ | $\mathrm{IPL1}^{(1,2)}$ | $\mathrm{IPLO}^{(1,2)}$ | RA | N | OV | Z | C |
| bit 7 |  |  |  |  |  |  |  |


| Legend: | C = Clearable bit |  |
| :--- | :--- | :--- |
| $R=$ Readable bit | $\mathrm{W}=$ Writable bit | $\mathrm{U}=$ Unimplemented bit, read as ' 0 ' |
| $-\mathrm{n}=$ Value at POR | $' 1$ ' = Bit is set | 0 ' = Bit is cleared |

bit 15 OA: Accumulator A Overflow Status bit
1 = Accumulator A has overflowed
$0=$ Accumulator A has not overflowed
bit $14 \quad$ OB: Accumulator B Overflow Status bit
$1=$ Accumulator $B$ has overflowed
$0=$ Accumulator B has not overflowed
bit 13
SA: Accumulator A Saturation 'Sticky' Status bit ${ }^{(3)}$
$1=$ Accumulator $A$ is saturated or has been saturated at some time
$0=$ Accumulator $A$ is not saturated
bit 12
SB: Accumulator B Saturation 'Sticky' Status bit ${ }^{(3)}$
1 = Accumulator $B$ is saturated or has been saturated at some time
$0=$ Accumulator $B$ is not saturated
bit $11 \quad \mathrm{OAB}: \mathrm{OA}| | \mathrm{OB}$ Combined Accumulator Overflow Status bit
1 = Accumulator A or B has overflowed
$0=$ Accumulator $A$ and $B$ have not overflowed
bit 10
SAB: SA || SB Combined Accumulator 'Sticky' Status bit
$1=$ Accumulator $A$ or $B$ is saturated or has been saturated at some time
$0=$ Accumulator $A$ and $B$ have not been saturated
bit 9 DA: DO Loop Active bit
1 = DO loop is in progress
$0=$ DO loop is not in progress
bit 8
DC: MCU ALU Half Carry/Borrow bit
$1=$ A carry-out from the $4^{\text {th }}$ low-order bit (for byte-sized data) or $8^{\text {th }}$ low-order bit (for word-sized data) of the result occurred
$0=$ No carry-out from the $4^{\text {th }}$ low-order bit (for byte-sized data) or $8^{\text {th }}$ low-order bit (for word-sized data) of the result occurred

Note 1: The IPL<2:0> bits are concatenated with the IPL3 bit (CORCON $<3>$ ) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL3 = 1 . User interrupts are disabled when IPL3 $=1$.
2: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1 .
3: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using the bit operations.

## REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5 IPL<2:0>: CPU Interrupt Priority Level Status bits ${ }^{(1,2)}$
111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
$110=$ CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
$010=$ CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
$000=$ CPU Interrupt Priority Level is 0 ( 8 )
bit 4 RA: REPEAT Loop Active bit
1 = REPEAT loop is in progress
$0=$ REPEAT loop is not in progress
bit $3 \quad \mathbf{N}$ : MCU ALU Negative bit
1 = Result was negative
$0=$ Result was non-negative (zero or positive)
bit $2 \quad$ OV: MCU ALU Overflow bit
This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state.
1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
$0=$ Overflow has not occurred for signed arithmetic
bit 1
Z: MCU ALU Zero bit
1 = An operation that affects the $Z$ bit has set it at some time in the past
$0=$ The most recent operation that affects the $Z$ bit has cleared it (i.e., a non-zero result)
bit $0 \quad$ C: MCU ALU Carry/ $\overline{\text { Borrow }}$ bit
1 = A carry-out from the Most Significant bit (MSb) of the result occurred
$0=$ No carry-out from the Most Significant bit of the result occurred
Note 1: The IPL<2:0> bits are concatenated with the IPL3 bit (CORCON $<3>$ ) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL3 = 1 . User interrupts are disabled when IPL3 $=1$.
2: The IPL<2:0> Status bits are read-only when the NSTDIS bit $($ INTCON1<15>) $=1$.
3: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using the bit operations.

## REGISTER 3-2: CORCON: CORE CONTROL REGISTER

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VAR | - | US1 | US0 | EDT $^{(1)}$ | DL2 | DL1 | DL0 |
| bit 15 |  |  |  | bit 8 |  |  |  |


| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/C-0 | R-0 | R/W-0 | R/W-0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SATA | SATB | SATDW | ACCSAT | IPL3 $^{(2)}$ | SFA | RND | IF |
| bit 7 |  |  | bit 0 |  |  |  |  |


| Legend: | $C=$ Clearable bit |  |
| :--- | :--- | :--- |
| $R=$ Readable bit | $\mathrm{W}=$ Writable bit | $\mathrm{U}=$ Unimplemented bit, read as ' 0 ' |
| $-\mathrm{n}=$ Value at POR | $' 1 '=$ Bit is set | $' 0$ ' = Bit is cleared |

bit 15 VAR: Variable Exception Processing Latency Control bit
1 = Variable exception processing latency is enabled
$0=$ Fixed exception processing latency is enabled
bit 14 Unimplemented: Read as ' 0 '
bit 13-12 US<1:0>: DSP Multiply Unsigned/Signed Control bits
11 = Reserved
$10=$ DSP engine multiplies are mixed-sign
01 = DSP engine multiplies are unsigned
$00=$ DSP engine multiplies are signed
bit 11
EDT: Early DO Loop Termination Control bit ${ }^{(1)}$
$1=$ Terminates executing DO loop at the end of current loop iteration
$0=$ No effect
bit 10-8 DL<2:0>: DO Loop Nesting Level Status bits
$111=7$ DO loops are active
-
-
-
$001=1$ DO loop is active
$000=0$ DO loops are active
bit 7
SATA: ACCA Saturation Enable bit
1 = Accumulator A saturation is enabled
$0=$ Accumulator $A$ saturation is disabled
bit 6
SATB: ACCB Saturation Enable bit
1 = Accumulator $B$ saturation is enabled
$0=$ Accumulator $B$ saturation is disabled
bit 5 SATDW: Data Space Write from DSP Engine Saturation Enable bit
1 = Data Space write saturation is enabled
$0=$ Data Space write saturation is disabled
bit 4 ACCSAT: Accumulator Saturation Mode Select bit
$1=9.31$ saturation (super saturation)
$0=1.31$ saturation (normal saturation)
Note 1: This bit is always read as ' 0 '.
2: The IPL3 bit is concatenated with the IPL<2:0> bits ( $\mathrm{SR}<7: 5>$ ) to form the CPU Interrupt Priority Level.

## REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

| bit 3 | IPL3: CPU Interrupt Priority Level Status bit 3 ${ }^{(2)}$ |
| :---: | :---: |
|  | 1 = CPU Interrupt Priority Level is greater than 7 <br> $0=$ CPU Interrupt Priority Level is less than 7 |
| bit 2 | SFA: Stack Frame Active Status bit <br> 1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values <br> $0=$ Stack frame is not active; W14 and W15 address of EDS or Base Data Space |
| bit 1 | RND: Rounding Mode Select bit <br> 1 = Biased (conventional) rounding is enabled <br> $0=$ Unbiased (convergent) rounding is enabled |
| bit 0 | IF: Integer or Fractional Multiplier Mode Select bit <br> 1 = Integer mode is enabled for DSP multiply <br> $0=$ Fractional mode is enabled for DSP multiply |

Note 1: This bit is always read as ' 0 '.
2: The IPL3 bit is concatenated with the IPL<2:0> bits $(S R<7: 5>)$ to form the CPU Interrupt Priority Level.

## REGISTER 3-3: CTXTSTAT: CPU W REGISTER CONTEXT STATUS REGISTER

| U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| - | - | - | - | - | CCTXI2 | CCTXI1 | CCTXIO |
| bit 15 |  |  |  |  | bit 8 |  |  |


| U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R/W-0 | R/W-0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| - | - | - | - | - | MCTXI2 | MCTXI1 | MCTXIO |
| bit 7 |  |  |  |  | bit 0 |  |  |

## Legend:

| $\mathrm{R}=$ Readable bit | $\mathrm{W}=$ Writable bit | $\mathrm{U}=$ Unimplemented bit, read as ' 0 ' |
| :--- | :--- | :--- |
| $-\mathrm{n}=$ Value at POR | $' 1$ ' = Bit is set | $' 0$ ' $=$ Bit is cleared |


| bit 15-11 | Unimplemented: Read as ' 0 ' |
| :--- | :--- |
| bit 10-8 | CCTXI<2:0>: Current (W Register) Context Identifier bits |
|  | $111=$ Reserved |
|  | - |
|  | $011=$ Reserved |
|  | $010=$ Alternate Working Register Set 2 is currently in use |
|  | $001=$ Alternate Working Register Set 1 is currently in use |
|  | $000=$ Default register set is currently in use |
| bit 7-3 | Unimplemented: Read as ' 0 ' |
| bit 2-0 | MCTXI<2:0>: Manual (W Register) Context Identifier bits |
|  | $111=$ Reserved |
|  | - |
|  | - |
|  | $011=$ Reserved |
|  | $010=$ Alternate Working Register Set 2 was most recently manually selected |
|  | $001=$ Alternate Working Register Set 1 was most recently manually selected |
|  | $000=$ Default register set was most recently manually selected |

### 3.7 Arithmetic Logic Unit (ALU)

The dsPIC33EVXXXGM00X/10X family ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and $\overline{\text { Digit Borrow }}$ bits, respectively, for subtraction operations.
The ALU can perform 8 -bit or 16 -bit operations, depending on the mode of the instruction that is used. The data for the ALU operation can come from the W register array or from the data memory, depending on the addressing mode of the instruction. Similarly, the output data from the ALU can be written to the W register array or a data memory location.
For information on the SR bits affected by each instruction, refer to the "16-bit MCU and DSC Programmer's Reference Manual" (DS70157).
The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16 -bit divisor division.

### 3.7.1 MULTIPLIER

Using the high-speed, 17-bit x 17-bit multiplier, the ALU supports unsigned, signed or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16 -bit signed
- 16 -bit x 16 -bit unsigned
- 16 -bit signed $\times 5$-bit (literal) unsigned
- 16 -bit signed $\times 16$-bit unsigned
- 16-bit unsigned x 5 -bit (literal) unsigned
- 16 -bit unsigned $\times 16$-bit signed
- 8 -bit unsigned x 8 -bit unsigned


### 3.7.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16 -bit signed and unsigned DIV instructions can specify any W register for both the 16 -bit divisor ( Wn ) and any W register (aligned) pair $(\mathrm{W}(\mathrm{m}+1): \mathrm{Wm})$ for the 32-bit dividend. The divide algorithm takes the single-cycle per bit of the divisor, so both 32 -bit/16-bit and 16 -bit/16-bit instructions take the same number of cycles to execute.

### 3.8 DSP Engine

The DSP engine consists of a high-speed, 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/ subtracter (with two target accumulators, round and saturation logic).
The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are ADD, SUB and NEG.
The DSP engine has options selected through bits in the CPU Core Control register (CORCON) as follows:

- Fractional or Integer DSP Multiply (IF)
- Signed, Unsigned or Mixed-Sign DSP Multiply (US)
- Conventional or Convergent Rounding (RND)
- Automatic Saturation On/Off for ACCA (SATA)
- Automatic Saturation On/Off for ACCB (SATB)
- Automatic Saturation On/Off for Writes to Data Memory (SATDW)
- Accumulator Saturation mode Selection (ACCSAT)

TABLE 3-2: DSP INSTRUCTIONS SUMMARY

| Instruction | Algebraic <br> Operation | ACC Write <br> Back |
| :--- | :--- | :---: |
| CLR | $A=0$ | Yes |
| ED | $A=(x-y)^{2}$ | No |
| EDAC | $A=A+(x-y)^{2}$ | No |
| MAC | $A=A+(x \bullet y)$ | Yes |
| MAC | $A=A+x^{2}$ | No |
| MOVSAC | No change in A | Yes |
| MPY | $A=x \bullet y$ | No |
| MPY | $A=x^{2}$ | No |
| MPY.N | $A=-x \bullet y$ | No |
| MSC | $A=A-x \bullet y$ | Yes |

### 4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Program Memory" (DS70613) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

The dsPIC33EVXXXGM00X/10X family architecture features separate program and data memory spaces and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

### 4.1 Program Address Space

The program address memory space of the dsPIC33EVXXXGM00X/10X family devices is 4M instructions. The space is addressable by a 24 -bit value derived either from the 23 -bit PC, during program execution or from table operation, or from DS remapping, as described in Section 4.7 "Interfacing Program and Data Memory Spaces".
User application access to the program memory space is restricted to the lower half of the address range ( $0 \times 000000$ to $0 \times 02 \mathrm{ABFF}$ ). The exception is the use of the TBLRD operations, which use TBLPAG<7> to read Device ID sections of the configuration memory space and the TBLWT operations, which are used to set up the write latches located in configuration memory space.
The program memory maps, which are presented by the device family and memory size, are shown in Figure 4-1 through Figure 4-3.

FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EV64GM00X/10X DEVICES ${ }^{(1)}$


Note 1: Memory areas are not shown to scale.

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EV128GM00X/10X DEVICES ${ }^{(1)}$


Note 1: Memory areas are not shown to scale.

FIGURE 4-3: PROGRAM MEMORY MAP FOR dsPIC33EV256GM00X/10X DEVICES ${ }^{(1)}$


Note 1: Memory areas are not shown to scale.

### 4.1.1 PROGRAM MEMORY <br> ORGANIZATION

The program memory space is organized in wordaddressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (see Figure 4-4).
Program memory addresses are always word-aligned on the lower word and addresses are incremented or decremented by two during the code execution. This arrangement provides compatibility with the Data Memory Space Addressing and makes data in the program memory space accessible.

### 4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EVXXXGM00X/10X family devices reserve the addresses between $0 \times 000000$ and $0 \times 000200$ for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address, $0 \times 000000$ of Flash memory, with the actual address for the start of code at address, 0x000002 of Flash memory.
For more information on the Interrupt Vector Tables, see Section 7.1 "Interrupt Vector Table".

## FIGURE 4-4: PROGRAM MEMORY ORGANIZATION



### 4.2 Data Address Space

The dsPIC33EVXXXGM00X/10X family CPU has a separate, 16 -bit wide data memory space. The Data Space (DS) is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory maps, which are presented by device family and memory size, are shown in Figure 4-5 and Figure 4-6.
All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the DS. This arrangement gives a Base Data Space address range of 64 Kbytes or 32 K words.
The Base Data Space address is used in conjunction with a Data Space Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS), which has a total address range of 16 Mbytes.
dsPIC33EVXXXGM00X/10X family devices implement up to 20 Kbytes of data memory (4 Kbytes of data memory for Special Function Registers and up to 16 Kbytes of data memory for RAM). If an EA points to a location outside of this area, an all zero word or byte is returned.

### 4.2.1 DATA SPACE WIDTH

The data memory space is organized in byteaddressable, 16 -bit wide blocks. Data is aligned in data memory and registers as 16 -bit words, but all DS EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

### 4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with $\mathrm{PIC}^{\circledR} \mathrm{MCU}$ devices and improve Data Space memory usage efficiency, the dsPIC33EVXXXGM00X/10X family instruction set supports both word and byte operations. As a consequence of byte accessibility, all the Effective Address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws +2 for word operations.
A data byte read, reads the complete word that contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode, but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, therefore, care must be taken when mixing byte and word operations or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB; the MSB is not modified.
A Sign-Extend (SE) instruction is provided to allow user applications to translate 8 -bit signed data to 16 -bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

### 4.2.3 SFR SPACE

The first 4 Kbytes of the Near Data Space, from 0x0000 to $0 x 0 F F F$, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33EVXXXGM00X/10X family core and peripheral modules for controlling the operation of the device.
SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as ' 0 '.

$$
\begin{array}{ll}
\text { Note: } & \text { The actual set of peripheral features and } \\
\text { interrupts varies by the device. Refer to the } \\
& \text { corresponding device tables and pinout } \\
\text { diagrams for device-specific information. }
\end{array}
$$

### 4.2.4 NEAR DATA SPACE

The 8 -Kbyte area, between $0 \times 0000$ and $0 \times 1 \mathrm{FFF}$, is referred to as the Near Data Space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole DS is addressable using MOV instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a Working register as an Address Pointer.

FIGURE 4-5: DATA MEMORY MAP FOR 64-KBYTE/128-KBYTE DEVICES ${ }^{(1)}$


FIGURE 4-6: DATA MEMORY MAP FOR 256-KBYTE DEVICES ${ }^{(1)}$


### 4.2.5 X AND Y DATA SPACES

The dsPIC33EVXXXGM00X/10X family core has two Data Spaces: X and Y . These Data Spaces can be considered either separate (for some DSP instructions) or as one unified, linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).
The X DS is used by all instructions and supports all addressing modes. The $X$ DS has separate read and write data buses. The X read data bus is the read data path for all instructions that view the DS as combined $X$ and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y DS is used in concert with the X DS by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY.N and MSC) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to the X Data Space.
All data memory writes, including in DSP instructions, view Data Space as combined $X$ and $Y$ address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

## Special Function Register Maps <br> 4.3 TAB

| $\begin{gathered} \text { SFR } \\ \text { Name } \end{gathered}$ | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| W0 | 0000 | W0 (WREG) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| W1 | 0002 | W1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| W2 | 0004 | W2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| W3 | 0006 | W3 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| W4 | 0008 | W4 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| W5 | 000A | W5 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| W6 | 000C | W6 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| W7 | 000E | W7 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| W8 | 0010 | W8 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| W9 | 0012 | W9 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| W10 | 0014 | W10 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| W11 | 0016 | W11 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| W12 | 0018 | W12 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| W13 | 001A | W13 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| W14 | 001C | W14 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| W15 | 001E | W15 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0800 |
| SPLIM | 0020 | SPLIM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| ACCAL | 0022 | ACCAL |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $x \times x x$ |
| ACCAH | 0024 | ACCAH |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $x \times x x$ |
| ACCAU | 0026 | Sign Extension of ACCA<39> |  |  |  |  |  |  |  | ACCAU |  |  |  |  |  |  |  | xxxx |
| ACCBL | 0028 | ACCBL |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| ACCBH | 002A | ACCBH |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| ACCBU | 002C | Sign Extension of ACCB<39> ACCBU |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| PCL | 002E | Program Counter Low Word Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  | - | 0000 |
| PCH | 0030 | - | - | - | - | - | - | - | - | - | Program Counter High Word Register |  |  |  |  |  |  | 0000 |
| DSRPAG | 0032 | - | - | - | - | - | - | Data Space Read Page Register |  |  |  |  |  |  |  |  |  | 0001 |
| DSWPAG | 0034 | - | - | - | - | - | - | - | Data Space Write Page Register |  |  |  |  |  |  |  |  | 0001 |
| RCOUNT | 0036 | Repeat Loop Count Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 | xxxx |
| DCOUNT | 0038 | DCOUNT<15:1> |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 | xxxx |
| DOSTARTL | 003A | DOSTARTL<15:1> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| DOSTARTH | 003C | - | - | - | - | - | - | - | - | - | - | DOSTARTH<5:0> |  |  |  |  |  | 00xx |
| DOENDL | 003E | DOENDL<15:1> |  |  |  |  |  |  |  |  |  |  |  |  |  |  | - | xxxx |

Legend: $\mathrm{x}=$ unknown value on Reset; - = unimplemented, read as ' 0 '. Reset values are shown in hexadecimal.

| $\begin{gathered} \text { SFR } \\ \text { Name } \end{gathered}$ | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\underset{\text { Resets }}{\text { All }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DOENDH | 0040 | - | - | - | - | - | - | - | - | - | - | DOENDH<5:0> |  |  |  |  |  | 00xx |
| SR | 0042 | OA | OB | SA | SB | OAB | SAB | DA | DC | IPL2 | IPL1 | IPL0 | RA | N | OV | z | C | 0000 |
| CORCON | 0044 | VAR | - | US1 | USO | EDT | DL2 | DL1 | DLO | SATA | SATB | SATDW | ACCSAT | IPL3 | SFA | RND | IF | 0020 |
| MODCON | 0046 | XMODEN | YMODEN | - | - | BWM3 | BWM2 | BWM1 | BWM0 | YWM3 | YWM2 | YWM1 | YWM0 | xWM3 | xWM2 | XWM1 | xwm0 | 0000 |
| XMODSRT | 0048 | XMODSRT<15:1> |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 | xxxx |
| XMODEND | 004A | XMODEND<15:1> |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 | xxxx |
| YMODSRT | 004C | YMODSRT<15:1> |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 | $x \times x x$ |
| YMODEND | 004E | YMODEND<15:1> |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 | xxxx |
| XBREV | 0050 | BREN | XBREV14 | XBREV13 | XBREV12 | XBREV11 | XBREV10 | XBREV9 | XBREV8 | XBREV7 | XBREV6 | XBREV5 | XBREV4 | XBREV3 | XBREV2 | XBREV1 | XBREV0 | 8xxx |
| DISICNT | 0052 | - | - | DISICNT<13:0> |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| TBLPAG | 0054 | - | - | - | - | - | - | - | - | TBLPAG<7:0> |  |  |  |  |  |  |  | 0000 |
| MSTRPR | 0058 | MSTRPR<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| CTXTSTAT | 005A | - | - | - | - | - | CCTX12 | CCTX11 | CCTXIO | - | - | - | - | - | MCTXI2 | MCTXI1 | MCTXIO | 0000 |

TABLE 4-2: TIMERS REGISTER MAP

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TMR1 | 0100 | Timer1 Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| PR1 | 0102 | Period Register 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | FFFF |
| T1CON | 0104 | TON | - | TSIDL | - | - | - | - | - | - | TGATE | TCKPS1 | TCKPSO | - | TSYNC | TCS | - | 0000 |
| TMR2 | 0106 | Timer2 Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| TMR3HLD | 0108 | Timer3 Holding Register (For 32-bit timer operations only) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| TMR3 | 010A | Timer3 Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| PR2 | 010C | Period Register 2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | FFFF |
| PR3 | 010E | Period Register 3 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | FFFF |
| T2CON | 0110 | TON | - | TSIDL | - | - | - | - | - | - | TGATE | TCKPS 1 | TCKPSO | T32 | - | TCS | - | 0000 |
| T3CON | 0112 | TON | - | TSIDL | - | - | - | - | - | - | TGATE | TCKPS1 | TCKPSO | - | - | TCS | - | 0000 |
| TMR4 | 0114 | Timer4 Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| TMR5HLD | 0116 | Timer5 Holding Register (For 32-bit operations only) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| TMR5 | 0118 | Timer5 Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| PR4 | 011A | Period Register 4 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | FFFF |
| PR5 | 011C | Period Register 5 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | FFFF |
| T4CON | 011E | TON | - | TSIDL | - | - | - | - | - | - | TGATE | TCKPS 1 | TCKPSO | T32 | - | TCS | - | 0000 |
| T5CON | 0120 | TON | - | TSIDL | - | - | - | - | - | - | TGATE | TCKPS1 | TCKPS0 | - | - | TCS | - | 0000 |

Legend: - = unimplemented, read as ' 0 '. Reset values are shown in hexadecimal.
TABLE 4-3: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 4 REGISTER MAP

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IC1CON1 | 0140 | - | - | ICSIDL | ICTSEL2 | ICTSEL1 | ICTSELO | - | - | - | ICI1 | ICIO | ICOV | ICBNE | ICM2 | ICM1 | ICM0 | 0000 |
| IC1CON2 | 0142 | - | - | - | - | - | - | - | IC32 | ICTRIG | TRIGSTAT | - | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSELO | 000D |
| IC1BUF | 0144 | Input Capture 1 Buffer Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| IC1TMR | 0146 | Input Capture 1 Timer Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| IC2CON1 | 0148 | - | - | ICSIDL | ICTSEL2 | ICTSEL1 | ICTSELO | - | - | - | ICI1 | ICIO | ICOV | ICBNE | ICM2 | ICM1 | ICM0 | 0000 |
| IC2CON2 | 014A | - | - | - | - | - | - | - | IC32 | ICTRIG | TRIGSTAT | - | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSELO | 000D |
| IC2BUF | 014C | Input Capture 2 Buffer Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| IC2TMR | 014E | Input Capture 2 Timer Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| IC3CON1 | 0150 | - | - | ICSIDL | ICTSEL2 | ICTSEL1 | ICTSELO | - | - | - | ICI1 | ICIO | ICOV | ICBNE | ICM2 | ICM1 | ICM0 | 0000 |
| IC3CON2 | 0152 | - | - | - | - | - | - | - | IC32 | ICTRIG | TRIGSTAT | - | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSELO | 000D |
| IC3BUF | 0154 | Input Capture 3 Buffer Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| IC3TMR | 0156 | Input Capture 3 Timer Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| IC4CON1 | 0158 | - | - | ICSIDL | ICTSEL2 | ICTSEL1 | ICTSELO | - | - | - | ICI1 | ICIO | ICOV | ICBNE | ICM2 | ICM1 | ICM0 | 0000 |
| IC4CON2 | 015A | - | - | - | - | - | - | - | IC32 | ICTRIG | TRIGSTAT | - | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSELO | 000D |
| IC4BUF | 015C | Input Capture 4 Buffer Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| IC4TMR | 015E | Input Capture 4 Timer Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |

Legend: $\mathrm{x}=$ unknown value on Reset; $-=$ unimplemented, read as ' 0 '. Reset values are shown in hexadecimal.
TABLE 4-4: I2C1 REGISTER MAP

| $\begin{gathered} \text { SFR } \\ \text { Name } \end{gathered}$ | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{gathered} \text { All } \\ \text { Resets } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| I2C1CON1 | 0200 | I2CEN | - | I2CSIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 |
| I2C1CON2 | 0202 | - | - | - | - | - | - | - | - | - | PCIE | SCIE | boen | SDAHT | SBCDE | AHEN | DHEN | 1000 |
| I2C1STAT | 0204 | ACKSTAT | TRSTAT | ACKTIM | - | - | BCL | GCSTAT | ADD10 | IWCOL | 12COV | D_A | P | S | R_W | RBF | TBF | 0000 |
| I2C1ADD | 0206 | - | - | - | - | - | - | I2C1 Address Register |  |  |  |  |  |  |  |  |  | 0000 |
| I2C1MSK | 0208 | - | - | - | - | - | - | I2C1 Address Mask Register |  |  |  |  |  |  |  |  |  | 0000 |
| I2C1BRG | 020A | Baud Rate Generator Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| I2C1TRN | 020C | - | - | - | - | - | - | - | - | I2C1 Transmit Register |  |  |  |  |  |  |  | 00FF |
| I2C1RCV | 020E | - | - | - | - | - | - | - | - | 12C1 Receive Register |  |  |  |  |  |  |  | 0000 |

TABLE 4-5: UART1 AND UART2 REGISTER MAP

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| U1MODE | 0220 | UARTEN | - | USIDL | IREN | RTSMD | - | UEN1 | UENO | WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL1 | PDSELO | STSEL | 0000 |
| U1STA | 0222 | UTXISEL1 | UTXINV | UTXISELO | - | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL1 | URXISELO | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| U1TXREG | 0224 | - | - | - | - | - | - | - |  |  |  | UART1 | Transmit R | gister |  |  |  | xxxx |
| U1RXREG | 0226 | - | - | - | - | - | - | - |  |  |  | UART1 | Receive Re | gister |  |  |  | 0000 |
| U1BRG | 0228 | Baud Rate Generator Prescaler Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| U2MODE | 0230 | UARTEN | - | USIDL | IREN | RTSMD | - | UEN1 | UENO | WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL1 | PDSELO | STSEL | 0000 |
| U2STA | 0232 | UTXISEL1 | UTXINV | UTXISELO | - | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL1 | URXISELO | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| U2TXREG | 0234 | - | - | - | - | - | - | - | UART2 Transmit Register |  |  |  |  |  |  |  |  | xxxx |
| U2RXREG | 0236 | - | - | - | - | - | - | - | UART2 Receive Register |  |  |  |  |  |  |  |  | 0000 |
| U2BRG | 0238 | Baud Rate Generator Prescaler Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |

\footnotetext{
TABLE 4-6: SPI1 AND SPI2 REGISTER MAP

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{array}{\|c} \text { All } \\ \text { Resets } \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SPI1STAT | 0240 | SPIEN | - | SPISIDL | - | - | SPIBEC2 | SPIBEC1 | SPIBECO | SRMPT | SPIROV | SRXMPT | SISEL2 | SISEL1 | SISELO | SPITBF | SPIRBF | 0000 |
| SPI1CON1 | 0242 | - | - | - | DISSCK | DISSDO | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | SPRE2 | SPRE1 | SPRE0 | PPRE1 | PPRE0 | 0000 |
| SPI1CON2 | 0244 | FRMEN | SPIFSD | FRMPOL | - | - | - | - | - | - | - | - | - | - | - | FRMDLY | SPIBEN | 0000 |
| SPI1BUF | 0248 | SPI1 Transmit and Receive Buffer Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| SPI2STAT | 0260 | SPIEN | - | SPISIDL | - | - | SPIBEC2 | SPIBEC1 | SPIBECO | SRMPT | SPIROV | SRXMPT | SISEL2 | SISEL1 | SISELO | SPITBF | SPIRBF | 0000 |
| SPI2CON1 | 0262 | - | - | - | DISSCK | DISSDO | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | SPRE2 | SPRE1 | SPREO | PPRE1 | PPRE0 | 0000 |
| SPI2CON2 | 0264 | FRMEN | SPIFSD | FRMPOL | - | - | - | - | - | - | - | - | - | - | - | FRMDLY | SPIBEN | 0000 |
| SPI2BUF | 0268 | SPI2 Transmit and Receive Buffer Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |

TABLE 4-7: ADC1 REGISTER MAP

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{array}{\|c\|} \text { All } \\ \text { Resets } \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ADC1BUF0 | 0300 |  |  |  |  |  |  |  | ADC1 Dat | ta Buffer 0 |  |  |  |  |  |  |  | xxxx |
| ADC1BUF1 | 0302 |  |  |  |  |  |  |  | ADC1 Dat | ata Buffer 1 |  |  |  |  |  |  |  | $x \mathrm{xxx}$ |
| ADC1BUF2 | 0304 |  |  |  |  |  |  |  | ADC1 Data | ata Buffer 2 |  |  |  |  |  |  |  | xxxx |
| ADC1BUF3 | 0306 |  |  |  |  |  |  |  | ADC1 Data | ata Buffer 3 |  |  |  |  |  |  |  | xxxx |
| ADC1BUF4 | 0308 |  |  |  |  |  |  |  | ADC1 Dat | ata Buffer 4 |  |  |  |  |  |  |  | xxxx |
| ADC1BUF5 | 030A |  |  |  |  |  |  |  | ADC1 Dat | ata Buffer 5 |  |  |  |  |  |  |  | xxxx |
| ADC1BUF6 | 030C |  |  |  |  |  |  |  | ADC1 Dat | ata Buffer 6 |  |  |  |  |  |  |  | xxxx |
| ADC1BUF7 | 030E |  |  |  |  |  |  |  | ADC1 Dat | ata Buffer 7 |  |  |  |  |  |  |  | xxxx |
| ADC1BUF8 | 0310 |  |  |  |  |  |  |  | ADC1 Dat | ata Buffer 8 |  |  |  |  |  |  |  | xxxx |
| ADC1BUF9 | 0312 |  |  |  |  |  |  |  | ADC1 Data | ata Buffer 9 |  |  |  |  |  |  |  | xxxx |
| ADC1BUFA | 0314 |  |  |  |  |  |  |  | ADC1 Data | ta Buffer 10 |  |  |  |  |  |  |  | xxxx |
| ADC1BUFB | 0316 |  |  |  |  |  |  |  | ADC1 Dat | ta Buffer 1 |  |  |  |  |  |  |  | xxxx |
| ADC1BUFC | 0318 |  |  |  |  |  |  |  | ADC1 Data | ta Buffer 12 |  |  |  |  |  |  |  | $x \times x x^{\text {a }}$ |
| ADC1BUFD | 031A |  |  |  |  |  |  |  | ADC1 Data | ta Buffer 13 |  |  |  |  |  |  |  | $x \times x x$ |
| ADC1BUFE | 031C |  |  |  |  |  |  |  | ADC1 Data | ta Buffer 14 |  |  |  |  |  |  |  | xxxx |
| ADC1BUFF | 031E |  |  |  |  |  |  |  | ADC1 Data | ta Buffer 15 |  |  |  |  |  |  |  | xxxx |
| AD1CON1 | 0320 | ADON | - | ADSIDL | ADDMABM | - | AD12B | FORM1 | FORM0 | SSRC2 | SSRC1 | SSRCO | SSRCG | SIMSAM | ASAM | SAMP | DONE | 0000 |
| AD1CON2 | 0322 | VCFG2 | VCFG1 | VCFG0 | - | - | CSCNA | CHPS1 | CHPSO | BUFS | SMPI4 | SMPI3 | SMPI2 | SMP11 | SMPIO | BUFM | ALTS | 0000 |
| AD1CON3 | 0324 | ADRC | - | - | SAMC4 | SAMC3 | SAMC2 | SAMC1 | SAMC0 | ADCS7 | ADCS6 | ADCS5 | ADCS4 | ADCS3 | ADCS2 | ADCS1 | ADCSO | 0000 |
| AD1CHS123 | 0326 | - | - | - | CH123SB2 | CH123SB1 | CH123NB1 | CH123NB0 | CH123SB0 | - | - | - | CH123SA2 | CH123SA1 | CH123NA1 | CH123NA0 | CH123SA0 | 0000 |
| AD1CHS0 | 0328 | CHONB | - | CH0SB5 | CHOSB4 | CHOSB3 | CHOSB2 | CHOSB1 | CHOSB0 | CHONA | - | CHOSA5 | CHOSA4 | CHOSA3 | CHOSA2 | CHOSA1 | CHOSAO | 0000 |
| AD1CSSH | 032E |  |  |  |  | CSS<31:24> |  |  |  | - | - | - | - |  | CsS | 19:16> |  | 0000 |
| AD1CSSL | 0330 |  |  |  |  |  |  |  | CSS< | <15:0> |  |  |  |  |  |  |  | 0000 |
| AD1CON4 | 0332 | - | - | - | - | - | - | - | ADDMAEN | - | - | - | - | - | DMABL2 | DMABL1 | DMABLO | 0000 |

TABLE 4-8: CTMU REGISTER MAP

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CTMUCON1 | 033A | CTMUEN | - | CTMUSIDL | TGEN | EDGEN | EDGSEQEN | IDISSEN | CTTRIG | - | - | - | - | - | - | - | - | 0000 |
| CTMUCON2 | 033C | EDG1MOD | EDG1POL | EDG1SEL3 | EDG1SEL2 | EDG1SEL1 | EDG1SEL0 | EDG2STAT | EDG1STAT | EDG2MOD | EDG2POL | EDG2SEL3 | EDG2SEL2 | EDG2SEL1 | EDG2SELO | - | - | 0000 |
| CTMUICON | 033E | ITRIM5 | ITRIM4 | ITRIM3 | ITRIM2 | ITRIM1 | ITRIM0 | IRNG1 | IRNGO | - | - | - | - | - | - | - | - | 0000 |


| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{array}{\|c} \text { All } \\ \text { Resets } \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| C1CTRL1 | 0400 | - | - | CSIDL | ABAT | CANCKS | REQOP2 | REQOP1 | REQOPO | OPMODE2 | OPMODE1 | OPMODEO | - | CANCAP | - | - | WIN | 0480 |
| C1CTRL2 | 0402 | - | - | - | - | - | - | - | - | - | - | - | DNCNT<4:0> |  |  |  |  | 0000 |
| C1VEC | 0404 | - | - | - | FILHIT4 | FILHIT3 | FILHIT2 | FILHIT1 | FILHIT0 | - | ICODE6 | ICODE5 | ICODE4 | ICODE3 | ICODE2 | ICODE1 | ICODEO | 0000 |
| C1FCTRL | 0406 | DMABS2 | DMABS1 | DMABSO | - | - | - | - | - | - | - | FSA5 | FSA4 | FSA3 | FSA2 | FSA1 | FSAO | 0000 |
| C1FIFO | 0408 | - | - | FBP5 | FBP4 | FBP3 | FBP2 | FBP1 | FBPO | - | - | FNRB5 | FNRB4 | FNRB3 | FNRB2 | FNRB1 | FNRBO | 0000 |
| C1INTF | 040A | - | - | TXBO | TXBP | RXBP | TXWAR | RXWAR | EWARN | IVRIF | WAKIF | ERRIF | - | FIFOIF | RBOVIF | RBIF | TBIF | 0000 |
| C1INTE | 040C | - | - | - | - | - | - | - | - | IVRIE | WAKIE | ERRIE | - | FIFOIE | RBOVIE | RBIE | TBIE | 0000 |
| C1EC | 040E | TERRCNT7 | TERRCNT6 | TERRCNT5 | TERRCNT4 | TERRCNT3 | TERRCNT2 | TERRCNT1 | TERRCNTO | RERRCNT7 | RERRCNT6 | RERRCNT5 | RERRCNT4 | RERRCNT3 | RERRCNT2 | RERRCNT1 | RERRCNTO | 0000 |
| C1CFG1 | 0410 | - | - | - | - | - | - | - | - | SJW1 | SJW0 | BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 | 0000 |
| C1CFG2 | 0412 | - | WAKFIL | - | - | - | SEG2PH2 | SEG2PH1 | SEG2PH0 | SEG2PHTS | SAM | SEG1PH2 | SEG1PH1 | SEG1PH0 | PRSEG2 | PRSEG1 | PRSEG0 | 0000 |
| C1FEN1 | 0414 | FLTEN<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | FFFF |
| C1FMSKSEL1 | 0418 | F7MSK1 | F7MSK0 | F6MSK1 | F6MSK0 | F5MSK1 | F5MSK0 | F4MSK1 | F4MSK0 | F3MSK1 | F3MSK0 | F2MSK1 | F2MSK0 | F1MSK1 | F1MSK0 | FOMSK1 | FOMSK0 | 0000 |
| C1FMSKSEL2 | 041A | F15MSK1 | F15MSK0 | F14MSK1 | F14MSK0 | F13MSK1 | F13MSK0 | F12MSK1 | F12MSK0 | F11MSK1 | F11MSK0 | F10MSK1 | F10MSK0 | F9MSK1 | F9MSK0 | F8MSK1 | F8MSK0 | 0000 |

TABLE 4-10: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 FOR dsPIC33EVXXXGM10X DEVICES

| $\begin{gathered} \text { SFR } \\ \text { Name } \end{gathered}$ | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{array}{\|c} \text { All } \\ \text { Resets } \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 0400- 041E | See definition when WIN $=x$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C1RXFUL1 | 0420 | RXFUL<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| C1RXFUL2 | 0422 | RXFUL<31:16> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| C1RXOVF1 | 0428 | RXOVF<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| C1RXOVF2 | 042A | RXOVF<31:16> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| C1TR01CON | 0430 | TXEN1 | TXABT1 | TXLARB1 | TXERR1 | TXREQ1 | RTREN1 | TX1PRI1 | TX1PRI0 | TXENO | TXABATO | TXLARB0 | TXERRO | TXREQ0 | RTRENO | TXOPRI1 | TXOPRIO | 0000 |
| C1TR23CON | 0432 | TXEN3 | TXABT3 | TXLARB3 | TXERR3 | TXREQ3 | RTREN3 | TX3PRI1 | TX3PRIO | TXEN2 | TXABAT2 | TXLARB2 | TXERR2 | TXREQ2 | RTREN2 | TX2PR11 | TX2PRIO | 0000 |
| C1TR45CON | 0434 | TXEN5 | TXABT5 | TXLARB5 | TXERR5 | TXREQ5 | RTREN5 | TX5PR11 | TX5PRI0 | TXEN4 | TXABAT4 | TXLARB4 | TXERR4 | TXREQ4 | RTREN4 | TX4PR11 | TX4PRIO | 0000 |
| C1TR67CON | 0436 | TXEN7 | TXABT7 | TXLARB7 | TXERR7 | TXREQ7 | RTREN7 | TX7PR11 | TX7PRIO | TXEN6 | TXABAT6 | TXLARB6 | TXERR6 | TXREQ6 | RTREN6 | TX6PRI1 | TX6PRIO | xxxx |
| C1RXD | 0440 |  |  |  |  |  |  | CAN 1 | Receive D | Word | gister |  |  |  |  |  |  | xxxx |
| C1TXD | 0442 |  |  |  |  |  |  | CAN1 | Transmit D | a Word | gister |  |  |  |  |  |  | xx |

TABLE 4-11: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EVXXXGM10X DEVICES

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{array}{\|c} \text { All } \\ \text { Resets } \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\begin{aligned} & \text { 0400- } \\ & 041 \mathrm{E} \end{aligned}$ | See definition when WIN $=x$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C1BUFPNT1 | 0420 | F3BP3 | F3BP2 | F3BP1 | F3BP0 | F2BP3 | F2BP2 | F2BP1 | F2BP0 | F1BP3 | F1BP2 | F1BP1 | F1BP0 | F0BP3 | FOBP2 | FOBP1 | FOBPO | 0000 |
| C1BUFPNT2 | 0422 | F7BP3 | F7BP2 | F7BP1 | F7BP0 | F6BP3 | F6BP2 | F6BP1 | F6BP0 | F5BP3 | F5BP2 | F5BP1 | F5BP0 | F4BP3 | F4BP2 | F4BP1 | F4BP0 | 0000 |
| C1BUFPNT3 | 0424 | F11BP3 | F11BP2 | F11BP1 | F11BP0 | F10BP3 | F10BP2 | F10BP1 | F10BP0 | F9BP3 | F9BP2 | F9BP1 | F9BP0 | F8BP3 | F8BP2 | F8BP1 | F8BP0 | 0000 |
| C1BUFPNT4 | 0426 | F15BP3 | F15BP2 | F15BP1 | F15BP0 | F14BP3 | F14BP2 | F14BP1 | F14BP0 | F13BP3 | F13BP2 | F13BP1 | F13BP0 | F12BP3 | F12BP2 | F12BP1 | F12BP0 | 0000 |
| C1RXMOSID | 0430 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | - | MIDE | - | EID17 | EID16 | xxxx |
| C1RXMOEID | 0432 | EID<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| C1RXM1SID | 0434 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SIDO | - | MIDE | - | EID17 | EID16 | xxxx |
| C1RXM1EID | 0436 | EID<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| C1RXM2SID | 0438 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | - | MIDE | - | EID17 | EID16 | $x \mathrm{xxx}$ |
| C1RXM2EID | 043A | EID<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| C1RXFOSID | 0440 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | - | EXIDE | - | EID17 | EID16 | $x \times x x$ |
| C1RXFOEID | 0442 | EID<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| C1RXF1SID | 0444 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SIDO | - | EXIDE | - | EID17 | EID16 | xxxx |
| C1RXF1EID | 0446 | EID<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| C1RXF2SID | 0448 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | - | EXIDE | - | EID17 | EID16 | $x \times x{ }^{\text {x }}$ |
| C1RXF2EID | 044A | EID<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| C1RXF3SID | 044C | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SIDO | - | EXIDE | - | EID17 | EID16 | $x \mathrm{xxx}$ |
| C1RXF3EID | 044E | EID<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| C1RXF4SID | 0450 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SIDO | - | EXIDE | - | EID17 | EID16 | $x \times x \times$ |
| C1RXF4EID | 0452 | EID<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| C1RXF5SID | 0454 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | - | EXIDE | - | EID17 | EID16 | $x \times x x$ |
| C1RXF5EID | 0456 | EID<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| C1RXF6SID | 0458 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | - | EXIDE | - | EID17 | EID16 | xxxx |
| C1RXF6EID | 045A | EID<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $x \times x x$ |
| C1RXF7SID | 045C | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SIDO | - | EXIDE | - | EID17 | EID16 | $x \times x x$ |
| C1RXF7EID | 045E | EID<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| C1RXF8SID | 0460 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SIDO | - | EXIDE | - | EID17 | EID16 | xxxx |
| C1RXF8EID | 0462 | EID<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| C1RXF9SID | 0464 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SIDO | - | EXIDE | - | EID17 | EID16 | xxxx |
| C1RXF9EID | 0466 | EID<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| C1RXF10SID | 0468 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SIDO | - | EXIDE | - | EID17 | EID16 | xxxx |
| C1RXF10EID | 046A | EID<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |




TABLE 4-13: SENT2 RECEIVER REGISTER MAP

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SENT2CON1 | 0520 | SNTEN | - | SNTSIDL | - | RCVEN | TXM | TXPOL | CRCEN | PPP | SPCEN | - | PS | - | NIBCNT2 | NIBCNT1 | NIBCNT0 | 0000 |
| SENT2CON2 | 0524 | TICKTIME<15:0> (Transmit modes) or SYNCMAX<15:0> (Receive mode) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | FFFF |
| SENT2CON3 | 0528 | FRAMETIME<15:0> (Transmit modes) or SYNCMIN <15:0> (Receive mode) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | FFFF |
| SENT2STAT | 052C | - | - | - | - | - | - | - | - | PAUSE | NIB2 | NIB1 | NIB0 | CRCERR | FRMERR | RXIDLE | SYNCTXEN | 0000 |
| SENT2SYNC | 0530 | Synchronization Time Period Register (Transmit mode) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| SENT2DATL | 0534 | DATA4<3:0> |  |  |  | DATA5<3:0> |  |  |  | DATA6<3:0> |  |  |  | CRC<3:0> |  |  |  | 0000 |
| SENT2DATH | 0536 | STAT<3:0> |  |  |  | DATA1<3:0> |  |  |  | DATA2<3:0> |  |  |  | DATA3<3:0> |  |  |  | 0000 |
| Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

TABLE 4-14: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EVXXXGM002/102 DEVICES

| $\begin{gathered} \text { SFR } \\ \text { Name } \end{gathered}$ | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{array}{\|c\|} \text { All } \\ \text { Resets } \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| RPOR0 | 0670 | - | - | RP35R5 | RP35R4 | RP35R3 | RP35R2 | RP35R1 | RP35R0 | - | - | RP20R5 | RP20R4 | RP20R3 | RP20R2 | RP20R1 | RP20R0 | 0000 |
| RPOR1 | 0672 | - | - | RP37R5 | RP37R4 | RP37R3 | RP37R2 | RP37R1 | RP37R0 | - | - | RP36R5 | RP36R4 | RP36R3 | RP36R2 | RP36R1 | RP36R0 | 0000 |
| RPOR2 | 0674 | - | - | RP39R5 | RP39R4 | RP39R3 | RP39R2 | RP39R1 | RP39R0 | - | - | RP38R5 | RP38R4 | RP38R3 | RP38R2 | RP38R1 | RP38R0 | 0000 |
| RPOR3 | 0676 | - | - | RP41R5 | RP41R4 | RP41R3 | RP41R2 | RP41R1 | RP41R0 | - | - | RP40R5 | RP40R4 | RP40R3 | RP40R2 | RP40R1 | RP40R0 | 0000 |
| RPOR4 | 0678 | - | - | RP43R5 | RP43R4 | RP43R3 | RP43R2 | RP43R1 | RP43R0 | - | - | RP42R5 | RP42R4 | RP42R3 | RP42R2 | RP42R1 | RP42R0 | 0000 |
| RPOR10 | 0684 | - | - | RP176R5 | RP176R4 | RP176R3 | RP176R2 | RP176R1 | RP176R0 | - | - | - | - | - | - | - | - | 0000 |
| RPOR11 | 0686 | - | - | RP178R5 | RP178R4 | RP178R3 | RP178R2 | RP178R1 | RP178R0 | - | - | RP177R5 | RP177R4 | RP177R3 | RP177R2 | RP177R1 | RP177R0 | 0000 |
| RPOR12 | 0688 | - | - | RP180R5 | RP180R4 | RP180R3 | RP180R2 | RP180R1 | RP180R0 | - | - | RP179R5 | RP179R4 | RP179R3 | RP179R2 | RP179R1 | RP179R0 | 0000 |
| RPOR13 | 068A | - | - | - | - | - | - | - | - | - | - | RP181R5 | RP181R4 | RP181R3 | RP181R2 | RP181R1 | RP181R0 | 0000 |

Legend: $-=$ unimplemented, read as ' 0 '. Reset values are shown in hexadecimal.
TABLE 4-16: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EVXXXGM006/106 DEVICES

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| RPORO | 0670 | - | - | RP35R5 | RP35R4 | RP35R3 | RP35R2 | RP35R1 | RP35R0 | - | - | RP20R5 | RP20R4 | RP20R3 | RP20R2 | RP20R1 | RP20R0 | 0000 |
| RPOR1 | 0672 | - | - | RP37R5 | RP37R4 | RP37R3 | RP37R2 | RP37R1 | RP37R0 | - | - | RP36R5 | RP36R4 | RP36R3 | RP36R2 | RP36R1 | RP36R0 | 000 |
| RPOR2 | 0674 | - | - | RP39R5 | RP39R4 | RP39R3 | RP39R2 | RP39R1 | RP39R0 | - | - | RP38R5 | RP38R4 | RP38R3 | RP38R2 | RP38R1 | RP38R0 | 0000 |
| RPOR3 | 0676 | - | - | RP41R5 | RP41R4 | RP41R3 | RP41R2 | RP41R1 | RP41R0 | - | - | RP40R5 | RP40R4 | RP40R3 | RP40R2 | RP40R1 | RP40R0 | 0000 |
| RPOR4 | 0678 | - | - | RP43R5 | RP43R4 | RP43R3 | RP43R2 | RP43R1 | RP43R0 | - | - | RP42R5 | RP42R4 | RP42R3 | RP42R2 | RP42R1 | RP42R0 | 0000 |
| RPOR5 | 067A | - | - | RP49R5 | RP49R4 | RP49R3 | RP49R2 | RP49R1 | RP49R0 | - | - | RP48R5 | RP48R4 | RP48R3 | RP48R2 | RP48R1 | RP48R0 | 0000 |
| RPOR6 | 067C | - | - | RP55R5 | RP55R4 | RP55R3 | RP55R2 | RP55R1 | RP55R0 | - | - | RP54R5 | RP54R4 | RP54R3 | RP54R2 | RP54R1 | RP54R0 | 0000 |
| RPOR7 | 067E | - | - | RP57R5 | RP57R4 | RP57R3 | RP57R2 | RP57R1 | RP57R0 | - | - | RP56R5 | RP56R4 | RP56R3 | RP56R2 | RP56R1 | RP56R0 | 0000 |
| RPOR8 | 0680 | - | - | RP70R5 | RP70R4 | RP70R3 | RP70R2 | RP70R1 | RP70R0 | - | - | RP69R5 | RP69R4 | RP69R3 | RP69R2 | RP69R1 | RP69R0 | 0000 |
| RPOR9 | 0682 | - | - | RP118R5 | RP118R4 | RP118R3 | RP118R2 | RP118R1 | RP118R0 | - | - | RP97R5 | RP97R4 | RP97R3 | RP97R2 | RP97R1 | RP97R0 | 0000 |
| RPOR10 | 0684 | - | - | RP176R5 | RP176R4 | RP176R3 | RP176R2 | RP176R1 | RP176R0 | - | - | RP120R5 | RP120R4 | RP120R3 | RP120R2 | RP120R1 | RP120R0 | 0000 |
| RPOR11 | 0686 | - | - | RP178R5 | RP178R4 | RP178R3 | RP178R2 | RP178R1 | RP178R0 | - | - | RP177R5 | RP177R4 | RP177R3 | RP177R2 | RP177R1 | RP177R0 | 0000 |
| RPOR12 | 0688 | - | - | RP180R5 | RP180R4 | RP180R3 | RP180R2 | RP180R1 | RP180R0 | - | - | RP179R5 | RP179R4 | RP179R3 | RP179R2 | RP179R1 | RP179R0 | 0000 |
| RPOR13 | 068A | - | - | - | - | - | - | - | - | - | - |  |  | RP181 | R<5:0> |  |  | 0000 |

TABLE 4-17: PERIPHERAL INPUT REMAP REGISTER MAP

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{array}{\|c} \text { All } \\ \text { Resets } \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| RPINRO | 06A0 | INT1R<7:0> |  |  |  |  |  |  |  | - | - | - | - | - | - | - | - | 0000 |
| RPINR1 | 06A2 | - | - | - | - | - | - | - | - | INT2R<7:0> |  |  |  |  |  |  |  | 0000 |
| RPINR3 | 06A6 | - | - | - | - | - | - | - | - | T2CKR<7:0> |  |  |  |  |  |  |  | 0000 |
| RPINR7 | 06AE | IC2R7 | IC2R6 | IC2R5 | IC2R4 | IC2R3 | IC2R2 | IC2R1 | IC2R0 | IC1R7 | IC1R6 | IC1R5 | IC1R4 | IC1R3 | IC1R2 | IC1R1 | IC1R0 | 0000 |
| RPINR8 | 06B0 | IC4R7 | IC4R6 | IC4R5 | IC4R4 | IC4R3 | IC4R2 | IC4R1 | IC4R0 | IC3R7 | IC3R6 | IC3R5 | IC3R4 | IC3R3 | IC3R2 | IC3R1 | IC3R0 | 0000 |
| RPINR11 | 06B6 | - | - | - | - | - | - | - | - | OCFAR<7:0> |  |  |  |  |  |  |  | 0000 |
| RPINR12 | 06B8 | FLT2R7 | FLT2R6 | FLT2R5 | FLT2R4 | FLT2R3 | FLT2R2 | FLT2R1 | FLT2R0 | FLT1R7 | FLT1R6 | FLT1R5 | FLT1R4 | FLT1R3 | FLT1R2 | FLT1R1 | FLT1R0 | 0000 |
| RPINR18 | 06C4 | - | - | - | - | - | - | - | - | U1RXR<7:0> |  |  |  |  |  |  |  | 0000 |
| RPINR19 | 06C6 | - | - | - | - | - | - | - | - | U2RXR<7:0> |  |  |  |  |  |  |  | 0000 |
| RPINR22 | 06CC | SCK2R7 | SCK2R6 | SCK2R5 | SCK2R4 | SCK2R3 | SCK2R2 | SCK2R1 | SCK2R0 | SDI2R7 | SDI2R6 | SDI2R5 | SDI2R4 | SDI2R3 | SDI2R2 | SDI2R1 | SDI2R0 | 0000 |
| RPINR23 | 06CE | - | - | - | - | - | - | - | - | SS2R<7:0> |  |  |  |  |  |  |  | 0000 |
| RPINR26 | 06D4 | - | - | - | - | - | - | - | - | C1RXR $<7: 0>$ (1) |  |  |  |  |  |  |  | 0000 |
| RPINR37 | 06EA | SYNC11R<7:0> |  |  |  |  |  |  |  | - | - | - | - | - | - | - | - | 0000 |
| RPINR38 | 06EC | DTCMP1R<7:0> |  |  |  |  |  |  |  | - | - | - | - | - | - | - | - | 0000 |
| RPINR39 | 06EE | DTCMP3R7 | DTCMP3R6 | DTCMP3R5 | DTCMP3R4 | DTCMP3R3 | DTCMP3R2 | DTCMP3R1 | DTCMP3R0 | DTCMP2R7 | DTCMP2R6 | DTCMP2R5 | DTCMP2R4 | DTCMP2R3 | DTCMP2R2 | DTCMP2R1 | DTCMP2R0 | 0000 |
| RPINR44 | 06F8 | SENT1R<7:0> |  |  |  |  |  |  |  | - | - | - | - | - | - | - | - | 0000 |
| RPINR45 | 06FA | - | - | - | - | - | - | - | - | SENT2R<7:0> |  |  |  |  |  |  |  | 0000 |
| Legend: Note 1: | $\begin{aligned} & -=1 \\ & \text { This } 1 \end{aligned}$ | unimplemented eature is avail | ed, read as ' ilable only on | '. Reset valu dsPIC33EV | es are shown XXXGM10X d | in hexadecim devices. |  |  |  |  |  |  |  |  |  |  |  |  |

TABLE 4-19: NVM REGISTER MAP

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{gathered} \text { All } \\ \text { Resets } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| NVMCON | 0728 | WR | WREN | WRERR | NVMSIDL | - | - | RPDF | URERR | - | - | - | - | NVMOP3 | NVMOP2 | NVMOP1 | NVMOPO | 0000 |
| NVMADR | 072A |  |  |  |  |  |  |  |  | VMAD |  |  |  |  |  |  |  | 0000 |
| NVMADRU | 072C | - | - | - | - | - | - | - | - | NVMADRU<23:16> |  |  |  |  |  |  |  | 0000 |
| NVMKEY | 072E | - | - | - | - | - | - | - | - | NVMKEY<7:0> |  |  |  |  |  |  |  | 0000 |
| NVMSRCADRL | 0730 | NVMSRCADR<15:1> |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 | 0000 |
| NVMSRCADRH | 0732 | - | - | - | - | - | - | - | - | NVMSRCADR<23:16> |  |  |  |  |  |  |  | 0000 |

TABLE 4-20: SYSTEM CONTROL REGISTER MAP

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| RCON | 0740 | TRAPR | IOPUWR | - | - | VREGSF | - | СМ | VREGS | EXTR | SWR | SWDTEN | WDTO | SLEEP | IDLE | BOR | POR | Note 1 |
| OSCCON | 0742 | - | cosc2 | cosc1 | cosco | - | NOSC2 | NOSC1 | NOSC0 | CLKLOCK | IOLOCK | LOCK | - | CF | - | - | OSWEN | Note 2 |
| CLKDIV | 0744 | ROI | DOZE2 | DOZE1 | DOZEO | DOZEN | FRCDIV2 | FRCDIV1 | FRCDIV0 | PLLPOST1 | PLLPOST0 | - | PLLPRE4 | PLLPRE3 | PLLPRE2 | PLLPRE1 | PLLPRE0 | 0000 |
| PLLFBD | 0746 | - | - | - | - | - | - | - | PLLDIV<8:0> |  |  |  |  |  |  |  |  | 0000 |
| OSCTUN | 0748 | - | - | - | - | - | - | - | - | - | - | TUN<5:0> |  |  |  |  |  | 0000 |
| Legend: Note 1: 2: | $-=$ unimplemented, read as ' 0 '. Reset values are shown in hexadecimal. RCON register Reset values are dependent on the type of Reset. OSCCON register Reset values are dependent on the Configuration fuses. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

\footnotetext{
TABLE 4-21: REFERENCE CLOCK REGISTER MAP

| $\begin{gathered} \text { SFR } \\ \text { Name } \end{gathered}$ | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{gathered} \text { All } \\ \text { Resets } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| REFOCON | 074E | ROON | - | ROSSLP | ROSEL | RODIV3 | RODIV2 | RODIV1 | RODIV0 | - | - | - | - | - | - | - | - | 0000 |

TABLE 4－22：PMD REGISTER MAP FOR dsPIC33EVXXXGM00X／10X FAMILY DEVICES

| $\overline{<} \overline{\stackrel{n}{\otimes}}$ | $\left\lvert\, \begin{aligned} & \circ \\ & \hline \stackrel{\rightharpoonup}{\circ} \end{aligned}\right.$ | 앙 | $\left\lvert\, \begin{aligned} & \circ \\ & \hline- \\ & \hline- \end{aligned}\right.$ | $\left\|\begin{array}{l\|} \hline 0 \\ 0 \\ 0 \end{array}\right\|$ | $\left\|\begin{array}{l\|} \hline 0 \\ 0 \\ 0 \end{array}\right\|$ | 合 |  | ） |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & 0 \\ & \text { it } \end{aligned}$ | $\stackrel{i}{0}$ | $\left\lvert\, \begin{aligned} & 0 \\ & \sum_{\grave{N}} \\ & 0 \end{aligned}\right.$ | 1 | 1 | 1 | I |  | 1 |
| $\pm$ |  | $\begin{aligned} & \text { N } \\ & \underset{N}{N} \\ & \text { O} \end{aligned}$ | 1 | 1 | ｜ | ｜ |  | ｜ |
| $\underset{\sim}{\sim}$ | 1 | O | $1$ | $\sum_{\substack{0 \\ \sum_{V}^{n} \\ \hline}}$ | 1 | ｜ |  | ｜ |
| $\begin{aligned} & \text { m } \\ & \stackrel{ \pm}{*} \end{aligned}$ | $\underset{\substack{0 \\ \vdots}}{\stackrel{0}{N}}$ | $\begin{aligned} & 0 \\ & \sum_{0}^{0} \\ & 0 \\ & 0 \end{aligned}$ | $1$ |  | 1 | ｜ |  | ｜ |
| $\begin{aligned} & \pm \\ & \pm \\ & \hline \mathbf{D} \end{aligned}$ | $\frac{\underset{N}{N}}{\stackrel{N}{N}}$ | 1 | ｜ | 1 | 1 |  |  | 1 |
| $\begin{aligned} & \text { n } \\ & \stackrel{+}{\mathbf{0}} \end{aligned}$ | $\sum_{\Sigma}^{\circ}$ | 1 | I |  | ｜ | I |  | ｜ |
| $\begin{aligned} & 0 \\ & \text { + } \end{aligned}$ | $\underset{N}{Q}$ | 1 | ｜ | 1 | ｜ | ｜ |  | ｜ |
| $\begin{aligned} & \text { N } \\ & \stackrel{ \pm}{\mathbf{n}} \end{aligned}$ | $\begin{aligned} & \underset{\underset{N}{N}}{N} \\ & \underset{N}{n} \end{aligned}$ | 1 | 1 | 1 | ｜ | I |  | ｜ |
| $\begin{aligned} & \infty \\ & \stackrel{\infty}{\mathbf{n}} \end{aligned}$ | 1 |  | 1 | 1 | $\begin{array}{\|l\|} \hline 0 \\ \sum_{\sum}^{n} \\ \sum \\ \sum \\ \hline \end{array}$ | 1 |  | $\sum_{\text {¢ }}^{0}$ |
| $\begin{aligned} & \text { o } \\ & \stackrel{+}{\mathbf{0}} \end{aligned}$ | $\sum_{i}^{0}$ | $\left\lvert\, \begin{aligned} & \underset{N}{\mathrm{O}} \\ & \hline \end{aligned}\right.$ | 1 | 1 | $\sum_{\sum_{\mathrm{L}}}^{\sum_{N}^{N}}$ | \｜ |  | 1 |
| $\begin{aligned} & \text { 읓 } \\ & \text { ( } \end{aligned}$ | 1 |  | $\mid \sum_{0}^{0}$ | 1 | $\sum_{\sum_{\mathrm{L}}}^{\sum_{\mathrm{m}}^{\mathrm{m}}}$ | \｜ |  | 1 |
| $\begin{aligned} & \text { F } \\ & \stackrel{1}{\infty} \end{aligned}$ |  | $\left\lvert\, \begin{aligned} & 0 \\ & \sum_{\substack{0}} \\ & \hline \end{aligned}\right.$ | 1 | 1 | 1 | ｜ |  | 号 |
| $\begin{aligned} & \text { N } \\ & \underset{\sim}{\mathbf{0}} \end{aligned}$ | $\underset{N}{\underset{N}{N}}$ | 1 | 1 | 1 | ｜ | ｜ |  | － |
| $\begin{aligned} & \text { m } \\ & \vdots \\ & \hline \mathbf{n} \end{aligned}$ | ${\underset{N}{N}}_{\substack{0}}^{0}$ | 1 | 1 | 1 | ｜ | ｜ |  | 1 |
| $\begin{aligned} & \pm \\ & \stackrel{ \pm}{ \pm} \end{aligned}$ | $\sum_{\downarrow}^{\infty}$ | 1 | 1 | 1 | ｜ | ｜ |  | 1 |
| $\begin{aligned} & \text { ח } \\ & \stackrel{1}{幺} \end{aligned}$ | $\underset{\substack{0 \\ 卜}}{0}$ | 1 | ｜ | 1 | 1 | ｜ |  | 1 |
| $$ | $\begin{aligned} & \circ \\ & \stackrel{\circ}{5} \\ & \hline \end{aligned}$ | $\begin{array}{\|c} \text { No } \\ \text { N } \end{array}$ | $\begin{array}{\|l} \hline \mathrm{O} \\ \stackrel{\rightharpoonup}{O} \\ \hline \end{array}$ | $\begin{aligned} & 0 \\ & \stackrel{8}{0} \\ & \hline \end{aligned}$ | $\begin{array}{\|l\|l} \hline \mathbf{0} \\ \stackrel{1}{0} \\ \hline \end{array}$ | $\begin{array}{\|l} \hline 0 \\ 0 \\ \hat{O} \end{array}$ |  | 山 <br> $\stackrel{0}{0}$ <br> 0 |
| $\stackrel{\propto}{\omega}$ | $\sum_{\mathrm{D}}^{\overline{\mathrm{D}}}$ | $\sum_{\mathrm{O}}^{\mathrm{N}}$ | $\sum_{i}^{N}$ | $\sum_{\Lambda}^{ \pm}$ | $\left\lvert\, \begin{aligned} & 0 \\ & \sum_{0}^{\infty} \\ & \hline \end{aligned}\right.$ | $\sum_{i}^{\hat{D}}$ |  | $\sum_{0}^{\infty}$ |

Legend：$\quad-=$ unimplemented，read as＇ 0 ＇．Reset values are shown in hexadecimal．
Note 1：$\quad$ This feature is available only on dsPIC33EVXXXGM10X devices．

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{gathered} \text { All } \\ \text { Resets } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IFSO | 0800 | NVMIF | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI11F | SPI1EIF | T31F | T21F | OC2IF | IC21F | DMAOIF | T11F | OC11F | IC11F | INTOIF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT21F | T5IF | T4IF | OC4IF | OC3IF | DMA21F | - | - | - | INT11F | CNIF | CMPIF | M12C11F | SI2C1IF | 0000 |
| IFS2 | 0804 | - | - | - | - | - | - | - | - | - | IC4IF | IC31F | DMA3IF | C1IF | C1RXIF ${ }^{(1)}$ | SP121F | SPI2EIF | 0000 |
| IFS3 | 0806 | - | - | - | - | - | - | PSEMIF | - | - | - | - | - | - | - | - | - | 0000 |
| IFS4 | 0808 | - | - | CTMUIF | - | - | - | - | - | - | C1TXIF ${ }^{(1)}$ | - | - | - | U2EIF | U1EIF | - | 0000 |
| IFS5 | 080A | PWM21F | PWM11F | - | - | - | - | - | - | - | - | - | - | - | - | - | - | 0000 |
| IFS6 | 080C | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PWM31F | 0000 |
| IFS8 | 0810 | - | ICDIF | - | - | - | - | - | - | - | - | - | - | - | - | - | - | 0000 |
| IFS10 | 0814 | - | - | I2C1BCIF | - |  | - | - | - | - | - | - | - | - | - | - | - | 0000 |
| IFS11 | 0816 | - | - | - | - | - | ECCSBEIF | SENT21F | SENT2EIF | SENT11F | SENT1EIF | - | - | - | - | - | - | 0000 |
| IEC0 | 0820 | NVMIE | DMA1IE | AD1IE | U1TXIE | U1RXIE | SP111E | SPI1EIE | T31E | T21E | OC2IE | IC2IE | DMAOIE | T11E | OC1IE | IC1IE | INTOIE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT21E | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | - | - | - | INT11E | CNIE | CMPIE | M12C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | - | - | - | - | - | - | - | - | - | IC4IE | IC3IE | DMA3IE | C1IE | C1RXIE ${ }^{(1)}$ | SP121E | SPI2EIE | 0000 |
| IEC3 | 0826 | - | - | - | - | - | - | PSEMIE | - | - | - | - | - | - | - | - | - | 0000 |
| IEC4 | 0828 | - | - | CTMUIE | - | - | - | - | - | - | C1TXIE ${ }^{(1)}$ | - | - | - | U2EIE | U1EIE | - | 0000 |
| IEC5 | 082A | PWM2IE | PWM11E | - | - | - | - | - | - | - | - | - | - | - | - | - | - | 0000 |
| IEC6 | 082C | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PWM3IE | 0000 |
| IEC8 | 0830 | - | ICDIE | - | - | - | - | - | - | - | - | - | - | - | - | - | - | 0000 |
| IEC10 | 0834 | - | - | 12C1BCIE | - | - | - | - | - | - | - | - | - | - | - | - | - | 0000 |
| IEC11 | 0836 | - | - | - | - | - | ECCSBEIE | SENT2IE | SENT2EIE | SENT11E | SENT1EIE | - | - | - | - | - | - | 0000 |
| IPC0 | 0840 | - | T11P2 | T11P1 | T11P0 | - | OC11P2 | OC1IP1 | OC11P0 | - | IC11P2 | IC11P1 | IC11P0 | - | INTOP2 | INTOIP1 | INTOPO | 4444 |
| IPC1 | 0842 | - | T21P2 | T21P1 | T21P0 | - | OC21P2 | OC2IP1 | OC2IP0 | - | IC21P2 | IC2IP1 | IC2IP0 | - | DMAOIP2 | DMAOIP1 | DMAOIPO | 4444 |
| IPC2 | 0844 | - | U1RXIP2 | U1RXIP1 | U1RXIP0 | - | SP11P2 | SP11P1 | SP11P0 | - | SP11EIP2 | SPI1EIP1 | SP11EIP0 | - | T31P2 | T3IP1 | T31P0 | 4444 |
| IPC3 | 0846 | - | NVMIP2 | NVMIP1 | NVMIPO | - | DMA11P2 | DMA1IP1 | DMA11P0 | - | AD1IP2 | AD11P1 | AD11P0 | - | U1TXIP2 | U1TXIP1 | U1TXIP0 | 4444 |
| IPC4 | 0848 | - | CNIP2 | CNIP1 | CNIPO | - | CMPIP2 | CMPIP1 | CMPIP0 | - | M12C1IP2 | M12C1IP1 | M12C11P0 | - | SI2C1IP2 | SI2C1IP1 | SI2C11P0 | 4444 |
| IPC5 | 084A | - | - | - | - | - | - | - | - | - | - | - | - | - | INT11P2 | INT11P1 | INT11P0 | 0004 |
| IPC6 | 084C | - | T41P2 | T4IP1 | T4IP0 | - | OC4IP2 | OC4IP1 | OC4IP0 | - | OC3IP2 | OC3IP1 | OC3IP0 | - | DMA21P2 | DMA2IP1 | DMA21P0 | 4444 |
| IPC7 | 084E | - | U2TXIP2 | U2TXIP1 | U2TXIP0 | - | U2RXIP2 | U2RXIP1 | U2RXIP0 | - | INT2\|P2 | INT2\|P1 | INT21P0 | - | TSIP2 | TSIP1 | TSIP0 | 4444 |
| IPC8 | 0850 | - | C11P2 | C1IP1 | C1IP0 | - | C1RXIP2 ${ }^{(1)}$ | C1RXIP1 ${ }^{(1)}$ | C1RXIP(1) | - | SP121P2 | SP121P1 | SP121P0 | - | SPI2EIP2 | SPI2EIP1 | SPI2EIP0 | 4444 |
| IPC9 | 0852 | - | - | - | - | - | IC4IP2 | IC4IP1 | IC4IP0 | - | IC31P2 | IC31P1 | IC31P0 | - | DMA31P2 | DMA31P1 | DMA31P0 | 0444 |
| IPC14 | 085C | - | - | - | - | - | - | - | - | - | PSEMIP2 | PSEMIP1 | PSEMIPO | - | - | - | - | 0040 |
| IPC16 | 0860 | - | - | - | - | - | U2EIP2 | U2EIP1 | U2EIP0 | - | U1EIP2 | U1EIP1 | U1EIP0 | - | - | - | - | 0440 |
| IPC17 | 0862 | - | - | - | - | - | C1TXIP2 ${ }^{(1)}$ | C1TXIP1 ${ }^{(1)}$ | C1TXIP( ${ }^{(1)}$ | - | - | - | - | - | - | - | - | 0400 |

$\begin{array}{lll}\text { Legend: } & -=\text { unimplemented, read as '0' Reset values are shown in hexadecimal. } \\ \text { Note 1: } & \text { This feature is available only on dsPIC33EVXXXGM10X devices. }\end{array}$
TABLE 4-23: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EVXXXGM00X/10X FAMILY DEVICES (CONTINUED)

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IPC19 | 0866 | - | - | - | - | - | - | - | - | - | CTMUIP2 | CTMUIP1 | CTMUIP0 | - | - | - | - | 0040 |
| IPC23 | 086E | - | PWM2IP2 | PWM2IP1 | PWM2IP0 | - | PWM1IP2 | PWM1IP1 | PWM1IP0 | - | - | - | - | - | - | - | - | 4400 |
| IPC24 | 0870 | - | - | - | - | - | - | - | - | - | - | - | - | - | PWM31P2 | PWM3IP1 | PWM3IP0 | 0004 |
| IPC35 | 0886 | - | - | - | - | - | ICDIP2 | ICDIP1 | ICDIP0 | - | - | - | - | - | - | - | - | 0400 |
| IPC43 | 0896 | - | - | - | - | - | - | - | - | - | I2C1BCIP2 | I2C1BCIP1 | I2C1BCIP0 | - | - | - | - | 0040 |
| IPC45 | 089A | - | SENT1IP2 | SENT1IP1 | SENT1IP0 | - | SENT1EIP2 | SENT1EIP1 | SENT1EIP0 | - | - | - | - | - | - | - | - | 4400 |
| IPC46 | 089C | - | - | - | - | - | ECCSBEIP2 | ECCSBEIP1 | ECCSBEIP0 | - | SENT2IP2 | SENT2IP1 | SENT2IP0 | - | SENT2EIP2 | SENT2EIP1 | SENT2EIP0 | 0444 |
| INTCON1 | 08C0 | NSTDIS | OVAERR | OVBERR | COVAERR | COVBERR | OVATE | OVBTE | COVTE | SFTACERR | DIVOERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | - | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | - | - | - | - | AIVTEN | - | - | - | - | - | INT2EP | INT1EP | INTOEP | 0000 |
| INTCON3 | 08C4 | DMT | - | - | - | - | - | - | - | - | - | DAE | DOOVR | - | - | - | - | 0000 |
| INTCON4 | 08C6 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | ECCDBE | SGHT | 0000 |
| INTTREG | 08C8 | - | - | - | - | - | ILR3 | ILR2 | ILR1 | VECNUM7 | VECNUM6 | VECNUM5 | VECNUM4 | VECNUM3 | VECNUM2 | VECNUM1 | VECNUM0 | 0000 |
| Legend: <br> Note 1: | $-=u$ | nimpleme ature is | ted, read a vailable only | '0' Reset on dsPIC3 | values are sh EVXXXGM | wn in hexad OX devices. | cimal. |  |  |  |  |  |  |  |  |  |  |  |

TABLE 4-24: OUTPUT COMPARE REGISTER MAP

| $\begin{gathered} \text { SFR } \\ \text { Name } \end{gathered}$ | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{array}{\|c\|} \text { All } \\ \text { Resets } \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OC1CON1 | 0900 | - | - | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSELO | - | - | ENFLTA | - | - | OCFLTA | TRIGMODE | OCM2 | OCM1 | OCM0 | 0000 |
| OC1CON2 | 0902 | FLTMD | FLTOUT | FLTTRIEN | OCINV | - | - | - | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSELO | 000C |
| OC1RS | 0904 | Output Compare 1 Secondary Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| OC1R | 0906 | Output Compare 1 Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $x \times x x$ |
| OC1TMR | 0908 | Output Compare 1 Timer Value Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| OC2CON1 | 090A | - | - | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSELO | - | - | ENFLTA | - | - | OCFLTA | TRIGMODE | OCM2 | OCM1 | осм0 | 0000 |
| OC2CON2 | 090C | FLTMD | FLTOUT | FLTTRIEN | OCINV | - | - | - | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSELO | 000C |
| OC2RS | 090E | Output Compare 2 Secondary Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| OC2R | 0910 | Output Compare 2 Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $x \times x \times$ |
| OC2TMR | 0912 | Output Compare 2 Timer Value Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $x \times x \times$ |
| OC3CON1 | 0914 | - | - | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSELO | - | - | ENFLTA | - | - | OCFLTA | TRIGMODE | OCM2 | OCM1 | осмо | 0000 |
| OC3CON2 | 0916 | FLTMD | FLTOUT | FLTTRIEN | OCINV | - | - | - | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSELO | 000c |
| OC3RS | 0918 | Output Compare 3 Secondary Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| OC3R | 091A | Output Compare 3 Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| OC3TMR | 091C | Output Compare 3 Timer Value Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $x \times x \times$ |
| OC4CON1 | 091E | - | - | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSELO | - | - | ENFLTA | - | - | OCFLTA | TRIGMODE | OCM2 | OCM1 | осм0 | 0000 |
| OC4CON2 | 0920 | FLTMD | FLTOUT | FLTTRIEN | OCINV | - | - | - | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSELO | 000C |
| OC4RS | 0922 | Output Compare 4 Secondary Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| OC4R | 0924 | Output Compare 4 Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
| OC4TMR | 0926 | Output Compare 4 Timer Value Register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |

[^0]TABLE 4-25: OP AMP/COMPARATOR REGISTER MAP

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{gathered} \text { All } \\ \text { Resets } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CMSTAT | 0A80 | PSIDL | - | - | C5EVT | C4EVT | C3EVT | C2EVT | C1EVT | - | - | - | C50UT | C4OUT | C3OUT | C2OUT | C10UT | 0000 |
| CVR1CON | OA82 | CVREN | CVROE | - | - | CVRSS | VREFSEL | - | - | - | CVR6 | CVR5 | CVR4 | CVR3 | CVR2 | CVR1 | CVRO | 0000 |
| CM1CON | OA84 | CON | COE | CPOL | - | - | OPAEN | CEVT | COUT | EVPOL1 | EVPOLO | - | CREF | - | - | CCH1 | CCHO | 0000 |
| CM1MSKSRC | 0A86 | - | - | - | - | SELSRCC3 | SELSRCC2 | SELSRCC1 | SELSRCC0 | SELSRCB3 | SELSRCB2 | SELSRCB1 | SELSRCB0 | SELSRCA3 | SELSRCA2 | SELSRCA1 | SELSRCA0 | 0000 |
| CM1MSKCON | OA88 | HLMS | - | OCEN | OCNEN | Oben | OBNEN | OAEN | OANEN | NAGS | PAGS | ACEN | ACNEN | ABEN | ABNEN | AAEN | AANEN | 0000 |
| CM1FLTR | OA8A | - | - | - | - | - | - | - | - | - | CFSEL2 | CFSEL1 | CFSELO | CFLTREN | CFDIV2 | CFDIV1 | CFDIV | 0000 |
| CM2CON | OABC | CON | COE | CPOL | - | - | OPAEN | CEVT | COUT | EVPOL1 | EVPOLO | - | CREF | - | - | CCH1 | CCHO | 0000 |
| CM2MSKSRC | OA8E | - | - | - | - | SELSRCC3 | SELSRCC2 | SELSRCC1 | SELSRCC0 | SELSRCB3 | SELSRCB2 | SELSRCB1 | SELSRCBO | SELSRCA3 | SELSRCA2 | SELSRCA1 | SELSRCA0 | 0000 |
| CM2MSKCON | OA90 | HLMS | - | OCEN | OCNEN | OBEN | OBNEN | OAEN | OANEN | NAGS | PAGS | ACEN | ACNEN | Aben | ABNEN | AAEN | AANEN | 0000 |
| CM2FLTR | OA92 | - | - | - | - | - | - | - | - | - | CFSEL2 | CFSEL1 | CFSELO | CFLTREN | CFDIV2 | CFDIV1 | CFDIV0 | 0000 |
| CM3CON | 0A94 | CON | COE | CPOL | - | - | OPAEN | CEVT | COUT | EVPOL1 | EVPOLO | - | CREF | - | - | CCH1 | CCHO | 0000 |
| CM3MSKSRC | OA96 | - | - | - | - | SELSRCC3 | SELSRCC2 | SELSRCC1 | SELSRCC0 | SELSRCB3 | SELSRCB2 | SELSRCB1 | SELSRCBO | SELSRCA3 | SELSRCA2 | SELSRCA1 | SELSRCA0 | 0000 |
| CM3MSKCON | OA98 | HLMS | - | OCEN | OCNEN | OBEN | OBNEN | OAEN | OANEN | NAGS | PAGS | ACEN | ACNEN | ABEN | ABNEN | AAEN | AANEN | 0000 |
| CM3FLTR | OA9A | - | - | - | - | - | - | - | - | - | CFSEL2 | CFSEL1 | CFSELO | CFLTREN | CFDIV2 | CFDIV1 | CFDIV | 0000 |
| CM4CON | OA9C | CON | COE | CPOL | - | - | - | CEVT | COUT | EVPOL1 | EVPOLO | - | CREF | - | - | CCH1 | CCHO | 0000 |
| CM4MSKSRC | OA9E | - | - | - | - | SELSRCC3 | SELSRCC2 | SELSRCC1 | SELSRCC0 | SELSRCB3 | SELSRCB2 | SELSRCB1 | SELSRCB0 | SELSRCA3 | SELSRCA2 | SELSRCA1 | SELSRCA0 | 0000 |
| CM4MSKCON | OAAO | HLMS | - | OCEN | OCNEN | OBEN | OBNEN | OAEN | OANEN | NAGS | PAGS | ACEN | ACNEN | ABEN | ABNEN | AAEN | AANEN | 0000 |
| CM4FLTR | OAA2 | - | - | - | - | - | - | - | - | - | CFSEL2 | CFSEL1 | CFSELO | CFLTREN | CFDIV2 | CFDIV1 | CFDIV | 0000 |
| CM5CON | OAA4 | CON | COE | CPOL | - | - | OPAEN | CEVT | COUT | EVPOL1 | EVPOLO | - | CREF | - | - | CCH1 | CCHO | 0000 |
| CM5MSKSRC | OAA6 | - | - | - | - | SELSRCC3 | SELSRCC2 | SELSRCC1 | SELSRCC0 | SELSRCB3 | SELSRCB2 | SELSRCB1 | SELSRCB0 | SELSRCA3 | SELSRCA2 | SELSRCA1 | SELSRCA0 | 0000 |
| CM5MSKCON | OAA8 | HLMS | - | OCEN | OCNEN | OBEN | OBNEN | OAEN | OANEN | NAGS | PAGS | ACEN | ACNEN | ABEN | ABNEN | AAEN | AANEN | 0000 |
| CM5FLTR | OAAA | - | - | - | - | - | - | - | - | - | CFSEL2 | CFSEL1 | CFSELO | CFLTREN | CFDIV2 | CFDIV1 | CFDIV0 | 0000 |
| CVR2CON | OAB4 | CVREN | CVROE | - | - | CVRSS | VREFSEL | - | - | - | CVR6 | CVR5 | CVR4 | CVR3 | CVR2 | CVR1 | CVRO | 0000 |

TABLE 4-26:

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\underset{\text { Resets }}{\text { All }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DMAOCON | OB00 | CHEN | SIZE | DIR | HALF | NULLW | - | - | - | - | - | AMODE1 | AMODE0 | - | - | MODE1 | MODE0 | 0000 |
| DMAOREQ | OB02 | FORCE | - | - | - | - | - | - | - | IRQSEL7 | IRQSEL6 | IRQSEL5 | IRQSEL4 | IRQSEL3 | IRQSEL2 | IRQSEL1 | IRQSELO | 00FF |
| DMAOSTAL | OB04 |  |  |  |  |  |  |  |  | STA | 15:0> |  |  |  |  |  |  | 0000 |
| DMAOSTAH | 0B06 | - | - | - | - | - | - | - | - | STA<23:16> |  |  |  |  |  |  |  | 0000 |
| DMAOSTBL | OB08 |  |  |  |  |  |  |  |  | STB< | 15:0> |  |  |  |  |  |  | 0000 |
| DMAOSTBH | OBOA | - | - | - | - | - | - | - | - | STB<23:16> |  |  |  |  |  |  |  | 0000 |
| DMAOPAD | OBOC | PAD<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| DMAOCNT | OBOE | - | - | CNT<13:0> |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| DMA1CON | OB10 | CHEN | SIZE | DIR | HALF | NULLW | - | - | - | - | - | AMODE1 | AMODEO | - | - | MODE1 | MODE0 | 0000 |
| DMA1REQ | OB12 | FORCE | - | - | - | - | - | - | - | IRQSEL7 | IRQSEL6 | IRQSEL5 | IRQSEL4 | IRQSEL3 | IRQSEL2 | IRQSEL1 | IRQSELO | 00FF |
| DMA1STAL | OB14 |  |  |  |  |  |  |  |  | STA | STA<15.0> |  |  |  |  |  |  | 0000 |
| DMA1STAH | OB16 | - | - | - | - | - | - | - | - | STA<23:16> |  |  |  |  |  |  |  | 0000 |
| DMA1STBL | OB18 |  |  |  |  |  |  |  |  | STB< | 15:0> |  |  |  |  |  |  | 0000 |
| DMA1STBH | 0B1A | - | - | - | - | - | - | - | - | STB<23:16> |  |  |  |  |  |  |  | 0000 |
| DMA1PAD | OB1C | PAD<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| DMA1CNT | OB1E | - | - |  |  |  |  |  |  | CNT<13:0> |  |  |  |  |  |  |  | 0000 |
| DMARCON | OB20 | CHEN | SIZE | DIR | HALF | NULLW | - | - | - | - | - | AMODE1 | AMODEO | - | - | MODE1 | MODE0 | 0000 |
| DMA2REQ | OB22 | FORCE | - | - | - | - | - | - | - | IRQSEL7 | IRQSEL6 | IRQSEL5 | IRQSEL4 | IRQSEL3 | IRQSEL2 | IRQSEL1 | IRQSELO | 00FF |
| DMA2STAL | OB24 |  |  |  |  |  |  |  |  | STAく | 15:0> |  |  |  |  |  |  | 0000 |
| DMA2STAH | 0B26 | - | - | - | - | - | - | - | - | STA<23:16> |  |  |  |  |  |  |  | 0000 |
| DMA2STBL | OB28 |  |  |  |  |  |  |  |  | STB | 15:0> |  |  |  |  |  |  | 0000 |
| DMA2STBH | 0B2A | - | - | - | - | - | - | - | - | STB<23:16> |  |  |  |  |  |  |  | 0000 |
| DMA2PAD | OB2C | PAD<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| DMA2CNT | OB2E | - | - |  |  |  |  |  |  | CNT<13:0> |  |  |  |  |  |  |  | 0000 |
| DMA3CON | OB30 | CHEN | SIZE | DIR | HALF | NULLW | - | - | - | - | - | AMODE1 | AMODEO | - | - | MODE1 | MODE0 | 0000 |
| DMA3REQ | 0B32 | FORCE | - | - | - | - | - | - | - | IRQSEL7 | IRQSEL6 | IRQSEL5 | IRQSEL4 | IRQSEL3 | IRQSEL2 | IRQSEL1 | IRQSELO | 00FF |
| DMA3STAL | OB34 |  |  |  |  |  |  |  |  | STA<15:0> |  |  |  |  |  |  |  | 0000 |
| DMA3STAH | OB36 | - | - | - | - | - | - | - | - | STA<23:16> |  |  |  |  |  |  |  | 0000 |
| DMA3STBL | OB38 |  |  |  |  |  |  |  |  | STB<15:0> |  |  |  |  |  |  |  | 0000 |
| DMA3STBH | OB3A | - | - | - | - | - | - | - | - | STB<23:16> |  |  |  |  |  |  |  | 0000 |
| DMA3PAD | OB3C | PAD<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| DMA3CNT | OB3E | - | - |  |  |  |  |  |  | CNT<13:0> |  |  |  |  |  |  |  | 0000 |
| DMAPWC | OBFO | - | - | - | - | - | - | - | - | - | - | - | - | PWCOL<3:0> |  |  |  | 0000 |
| DMARQC | OBF2 | - | - | - | - | - | - | - | - | - | - | - | - | RQCOL<3:0> |  |  |  | 0000 |
| DMAPPS | OBF4 | - | - | - | - | - | - | - | - | - | - | - | - | PPST<3:0> |  |  |  | 0000 |

TABLE 4-26: DMAC REGISTER MAP (CONTINUED)

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DMALCA | OBF6 | - | - | - | - | - | - | - | - | - | - | - | - |  |  | 3:0> |  | 000F |
| DSADRL | OBF8 | DSADR<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| DSADRH | OBFA |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |

TABLE 4-27: PWM REGISTER MAP

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PTCON | OC00 | PTEN | - | PTSIDL | SESTAT | SEIEN | EIPU | SYNCPOL | SYNCOEN | SYNCEN | SYNCSRC2 | SYNCSRC1 | SYNCSRCO | SEVTPS3 | SEVTPS2 | SEVTPS1 | SEVTPSO | 0000 |
| PTCON2 | OC02 | - | - | - | - | - | - | - | - | - | - | - | - | - |  | PCLKDIV<2:0> |  | 0000 |
| PTPER | 0C04 | PTPER<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | FFF8 |
| SEVTCMP | OC06 | SEVTCMP<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| MDC | OCOA | MDC<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| CHOP | 0C1A | CHPCLKEN | - | - | - | - | - | CHOPCLK9 | CHOPCLK8 | CHOPCLK7 | CHOPCLK6 | CHOPCLK5 | CHOPCLK4 | CHOPCLK3 | CHOPCLK2 | CHOPCLK1 | CHOPCLKO | 0000 |
| PWMKEY | OC1E | PWMKEY<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |

Legend: — = unimplemented, read as ' 0 '. Reset values are shown in hexadecimal.

TABLE 4-28: PWM GENERATOR 1 REGISTER MAP

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{array}{\|c} \text { All } \\ \text { Resets } \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PWMCON1 | OC20 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC1 | DTC0 | DTCP | - | - | CAM | XPRES | IUE | 0000 |
| IOCON1 | OC22 | PENH | PENL | POLH | POLL | PMOD1 | PMODO | OVRENH | OVRENL | OVRDAT1 | OVRDATO | FLTDAT1 | FLTDATO | CLDAT1 | CLDATO | SWAP | OSYNC | 0000 |
| FCLCON1 | OC24 | - | CLSRC4 | CLSRC3 | CLSRC2 | CLSRC1 | CLSRC0 | CLPOL | CLMOD | FLTSRC4 | FLTSRC3 | FLTSRC2 | FLTSRC1 | FLTSRC0 | FLTPOL | FLTMOD1 | FLTMODO | 0000 |
| PDC1 | OC26 | PDC1<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| PHASE1 | OC28 | PHASE1<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| DTR1 | OC2A | - | - | DTR1<13:0> |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| ALTDTR1 | 0C2C | - | - | ALTDTR1<13:0> |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| TRIG1 | OC32 | TRGCMP<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| TRGCON1 | OC34 | TRGDIV3 | TRGDIV2 | TRGDIV1 | TRGDIV0 | - | - | - | - | - | - | TRGSTRT5 | TRGSTRT4 | TRGSTRT3 | TRGSTRT2 | TRGSTRT1 | TRGSTRT0 | 0000 |
| PWMCAP1 | OC38 | PWMCAP1<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| LEBCON1 | 0C3A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | - | - | - | - | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY1 | 0С3C | - | - | - | - | LEB<11:0> |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| AUXCON1 | 0С3E | - | - | - | - | BLANKSEL3 | BLANKSEL2 | BLANKSEL1 | BLANKSELO | - | - | CHOPSEL3 | CHOPSEL2 | CHOPSEL1 | CHOPSELO | CHOPHEN | CHOPLEN | 0000 |

TABLE 4-29: PWM GENERATOR 2 REGISTER MAP

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{gathered} \text { All } \\ \text { Resets } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PWMCON2 | OC40 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC1 | DTCO | DTCP | - | - | CAM | XPRES | IUE | 0000 |
| IOCON2 | OC42 | PENH | PENL | POLH | POLL | PMOD1 | PMODO | OVRENH | OVRENL | OVRDAT1 | OVRDATO | FLTDAT1 | FLTDAT0 | CLDAT1 | CLDAT0 | SWAP | OSYNC | 0000 |
| FCLCON2 | OC44 | - | CLSRC4 | CLSRC3 | CLSRC2 | CLSRC1 | CLSRC0 | CLPOL | CLMOD | FLTSRC4 | FLTSRC3 | FLTSRC2 | FLTSRC1 | FLTSRCO | FLTPOL | FLTMOD1 | FLTMODO | 0000 |
| PDC2 | 0C46 | PDC2<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| PHASE2 | OC48 | PHASE2<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| DTR2 | 0C4A | - | - | DTR2<13:0> |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| ALTDTR2 | OC4C | - | - | ALTDTR2<13:0> |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| TRIG2 | OC52 | TRGCMP<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| TRGCON2 | OC54 | TRGDIV3 | TRGDIV2 | TRGDIV1 | TRGDIV0 | - | - | - | - | - | - | TRGSTRT5 | TRGSTRT4 | TRGSTRT3 | TRGSTRT2 | TRGSTRT1 | TRGSTRT0 | 0000 |
| PWMCAP2 | OC58 | PWMCAP2<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| LEBCON2 | 0C5A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | - | - | - | - | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY2 | 0C5C | - | - | - | - | LEB<11:0> |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| AUXCON2 | OC5E | - | - | - | - | BLANKSEL3 | BLANKSEL2 | BLANKSEL1 | BLANKSELO | - | - | CHOPSEL3 | CHOPSEL2 | CHOPSEL1 | CHOPSELO | CHOPHEN | CHOPLEN | 0000 |

[^1]TABLE 4-30: PWM GENERATOR 3 REGISTER MAP

| $\begin{gathered} \text { SFR } \\ \text { Name } \end{gathered}$ | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{array}{\|c} \text { All } \\ \text { Resets } \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PWMCON3 | OC60 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC1 | DTC0 | DTCP | - | - | CAM | XPRES | IUE | 0000 |
| IOCON3 | OC62 | PENH | PENL | POLH | POLL | PMOD1 | PMODO | OVRENH | OVRENL | OVRDAT1 | OVRDATO | FLTDAT1 | FLTDAT0 | CLDAT1 | CLDAT0 | SWAP | OSYNC | 0000 |
| FCLCON3 | OC64 | - | CLSRC4 | CLSRC3 | CLSRC2 | CLSRC1 | CLSRC0 | CLPOL | CLMOD | FLTSRC4 | FLTSRC3 | FLTSRC2 | FLTSRC1 | FLTSRC0 | FLTPOL | FLTMOD1 | FLTMODO | 0000 |
| PDC3 | OC66 | PDC3<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| PHASE3 | OC68 | PHASE3<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| DTR3 | OC6A | - | - | DTR3<13:0> |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| ALTDTR3 | 0C6C | - | - | ALTDTR3<13:0> |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| TRIG3 | OC72 | TRGCMP<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| TRGCON3 | 0 C 74 | TRGDIV3 | TRGDIV2 | TRGDIV1 | TRGDIV0 | - | - | - | - | - | - | TRGSTRT5 | TRGSTRT4 | TRGSTRT3 | TRGSTRT2 | TRGSTRT1 | TRGSTRT0 | 0000 |
| PWMCAP3 | 0 C 78 | PWMCAP3<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| LEBCON3 | 0C7A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | - | - | - | - | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY3 | 0C7C | - | - | - | - | LEB<11:0> |  |  |  |  |  |  |  |  |  |  |  | 0000 |
| AUXCON3 | 0C7E | - | - | - | - | BLANKSEL3 | BLANKSEL2 | BLANKSEL1 | BLANKSELO | - | - | CHOPSEL3 | CHOPSEL2 | CHOPSEL1 | CHOPSELO | CHOPHEN | CHOPLEN | 0000 |



TABLE 4-31: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES
TABLE 4-33: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX02 DEVICES

| SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TRISA | 0E00 | - | - | - | - | - | - | - | - | - | - | - | TRISA<4:0> |  |  |  |  | DF9F |
| PORTA | 0E02 | - | - | - | - | - | - | - | - | - | - | - | RA<4:0> |  |  |  |  | 0000 |
| LATA | 0E04 | - | - | - | - | - | - | - | - | - | - | - | LATA<4:0> |  |  |  |  | 0000 |
| ODCA | 0E06 | - | - | - | - | - | - | - | - | - | - | - | ODCA<4:0> |  |  |  |  | 0000 |
| CNENA | 0E08 | - | - | - | - | - | - | - | - | - | - | - | CNIEA<4:0> |  |  |  |  | 0000 |
| CNPUA | OEOA | - | - | - | - | - | - | - | - | - | - | - | CNPUA<4:0> |  |  |  |  | 0000 |
| CNPDA | OEOC | - | - | - | - | - | - | - | - | - | - | - | CNPDA<4:0> |  |  |  |  | 0000 |
| ANSELA | OEOE | - | - | - | - | - | - | - | - | - | - | - | ANSA4 | - | ANSA<2:0> |  |  | 1813 |
| SR1A | 0E10 | - | - | - | - | - | - | - | - | - | - | - | SR1A4 | - | - | - | - | 0000 |
| SROA | 0E12 | - | - | - | - | - | - | - | - | - | - | - | SROA4 | - | - | - | - | 0000 |

[^2]``` \\
\hline Wx & \[
\begin{aligned}
& \text { X Data Space Prefetch Address register for DSP instructions } \\
& \in\{[\mathrm{W} 8]+=6,[\mathrm{~W} 8]+=4,[\mathrm{~W} 8]+=2,[\mathrm{~W} 8],[\mathrm{W} 8]-=6,[\mathrm{~W} 8]-=4,[\mathrm{~W} 8]-=2, \\
& \quad[\mathrm{W} 9]+=6,[\mathrm{~W} 9]+=4,[\mathrm{~W} 9]+=2,[\mathrm{~W} 9],[\mathrm{W} 9]-=6,[\mathrm{~W} 9]-=4,[\mathrm{~W} 9]-=2, \\
& \\
& [\mathrm{~W} 9+\mathrm{W} 12], \text { none }\}
\end{aligned}
\] \\
\hline Wxd & X Data Space Prefetch Destination register for DSP instructions \(\in\{\) W44...W7\} \\
\hline Wy & ```
Y Data Space Prefetch Address register for DSP instructions
\in{[W10] + = 6,[W10] + = 4,[W10] + = 2,[W10],[W10] - = 6,[W10] - = 4,[W10] - = 2,
    [W11] + = 6,[W11] + = 4,[W11] + = 2,[W11],[W11] - = 6,[W11] - = 4,[W11] - = 2,
    [W11 + W12], none}
``` \\
\hline Wyd & Y Data Space Prefetch Destination register for DSP instructions \(\in\{\) W44...W7\} \\
\hline
\end{tabular}

TABLE 28-2: INSTRUCTION SET OVERVIEW
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \begin{tabular}{l}
Base \\
Instr \\
\#
\end{tabular} & Assembly Mnemonic & & Assembly Syntax & Description & \# of Words & \# of Cycles & Status Flags Affected \\
\hline \multirow[t]{7}{*}{1} & \multirow[t]{7}{*}{ADD} & ADD & Acc & Add Accumulators & 1 & 1 & \[
\begin{gathered}
\mathrm{OA}, \mathrm{OB}, \mathrm{SA}, \\
\mathrm{SB}
\end{gathered}
\] \\
\hline & & ADD & f & \(\mathrm{f}=\mathrm{f}+\mathrm{W}\) WEG & 1 & 1 & C,DC,N,OV,Z \\
\hline & & ADD & f,WREG & WREG = \(\mathrm{f}+\) WREG & 1 & 1 & C,DC,N,OV,Z \\
\hline & & ADD & \#lit10,Wn & \(\mathrm{Wd}=\mathrm{lit} 10+\mathrm{Wd}\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & ADD & Wb,Ws,Wd & \(\mathrm{Wd}=\mathrm{Wb}+\mathrm{Ws}\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & ADD & Wb, \#lit5,Wd & \(\mathrm{Wd}=\mathrm{Wb}+\mathrm{lit5}\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & ADD & Wso,\#Slit4, Acc & 16-bit Signed Add to Accumulator & 1 & 1 & \[
\begin{gathered}
\mathrm{OA}, \mathrm{OB}, \mathrm{SA}, \\
\text { SB }
\end{gathered}
\] \\
\hline \multirow[t]{5}{*}{2} & \multirow[t]{5}{*}{ADDC} & ADDC & f & \(\mathrm{f}=\mathrm{f}+\) WREG + (C) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & ADDC & f,WREG & WREG = f + WREG + (C) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & ADDC & \#lit10,Wn & Wd \(=\) lit10 + Wd + (C) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & ADDC & Wb,Ws,Wd & \(\mathrm{Wd}=\mathrm{Wb}+\mathrm{Ws}+(\mathrm{C})\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & ADDC & Wb, \#lit5,Wd & \(\mathrm{Wd}=\mathrm{Wb}+\mathrm{lit5}+(\mathrm{C})\) & 1 & 1 & C,DC,N,OV,Z \\
\hline \multirow[t]{5}{*}{3} & \multirow[t]{5}{*}{AND} & And & f & \(\mathrm{f}=\mathrm{f}\). AND. WREG & 1 & 1 & N,Z \\
\hline & & AND & f,WREG & WREG = f.AND. WREG & 1 & 1 & N,Z \\
\hline & & AND & \#lit10,Wn & Wd = lit10.AND. Wd & 1 & 1 & N,Z \\
\hline & & AND & Wb,Ws,Wd & \(\mathrm{Wd}=\mathrm{Wb}\). AND. Ws & 1 & 1 & N,Z \\
\hline & & AND & Wb, \#lit5,Wd & Wd = Wb .AND. lit5 & 1 & 1 & N,Z \\
\hline \multirow[t]{5}{*}{4} & \multirow[t]{5}{*}{ASR} & ASR & f & \(\mathrm{f}=\) Arithmetic Right Shift f & 1 & 1 & C,N,OV,Z \\
\hline & & ASR & f,WREG & WREG = Arithmetic Right Shift f & 1 & 1 & C,N,OV,Z \\
\hline & & ASR & Ws,wd & Wd = Arithmetic Right Shift Ws & 1 & 1 & C,N,OV,Z \\
\hline & & ASR & Wb,Wns, Wnd & Wnd = Arithmetic Right Shift Wb by Wns & 1 & 1 & N,Z \\
\hline & & ASR & Wb, \#lit5, Wnd & Wnd = Arithmetic Right Shift Wb by lit5 & 1 & 1 & N,Z \\
\hline \multirow[t]{2}{*}{5} & \multirow[t]{2}{*}{BCLR} & BCLR & f,\#bit4 & Bit Clear f & 1 & 1 & None \\
\hline & & BCLR & Ws,\#bit4 & Bit Clear Ws & 1 & 1 & None \\
\hline \multirow[t]{22}{*}{6} & \multirow[t]{22}{*}{BRA} & BRA & C, Expr & Branch if Carry & 1 & 1 (4) & None \\
\hline & & BRA & GE, Expr & Branch if greater than or equal & 1 & 1 (4) & None \\
\hline & & BRA & GEU, Expr & Branch if unsigned greater than or equal & 1 & 1 (4) & None \\
\hline & & BRA & GT, Expr & Branch if greater than & 1 & 1 (4) & None \\
\hline & & BRA & GTU, Expr & Branch if unsigned greater than & 1 & 1 (4) & None \\
\hline & & BRA & LE, Expr & Branch if less than or equal & 1 & 1 (4) & None \\
\hline & & BRA & LEU, Expr & Branch if unsigned less than or equal & 1 & 1 (4) & None \\
\hline & & BRA & LT, Expr & Branch if less than & 1 & 1 (4) & None \\
\hline & & BRA & LTU, Expr & Branch if unsigned less than & 1 & 1 (4) & None \\
\hline & & BRA & N, Expr & Branch if Negative & 1 & 1 (4) & None \\
\hline & & BRA & NC, Expr & Branch if Not Carry & 1 & 1 (4) & None \\
\hline & & BRA & NN, Expr & Branch if Not Negative & 1 & 1 (4) & None \\
\hline & & BRA & NOV, Expr & Branch if Not Overflow & 1 & 1 (4) & None \\
\hline & & BRA & NZ, Expr & Branch if Not Zero & 1 & 1 (4) & None \\
\hline & & BRA & OA, Expr & Branch if Accumulator A overflow & 1 & 1 (4) & None \\
\hline & & BRA & OB, Expr & Branch if Accumulator B overflow & 1 & 1 (4) & None \\
\hline & & BRA & OV, Expr & Branch if Overflow & 1 & 1 (4) & None \\
\hline & & BRA & SA, Expr & Branch if Accumulator A saturated & 1 & 1 (4) & None \\
\hline & & BRA & SB, Expr & Branch if Accumulator B saturated & 1 & 1 (4) & None \\
\hline & & BRA & Expr & Branch Unconditionally & 1 & 4 & None \\
\hline & & BRA & Z, Expr & Branch if Zero & 1 & 1 (4) & None \\
\hline & & BRA & Wn & Computed Branch & 1 & 4 & None \\
\hline \multirow[t]{2}{*}{7} & \multirow[t]{2}{*}{BSET} & BSET & f,\#bit4 & Bit Set f & 1 & 1 & None \\
\hline & & BSET & Ws, \#bit4 & Bit Set Ws & 1 & 1 & None \\
\hline
\end{tabular}

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

\section*{TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)}
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Base Instr \# & Assembly Mnemonic & & Assembly Syntax & Description & \# of Words & \# of Cycles & Status Flags Affected \\
\hline \multirow[t]{2}{*}{8} & \multirow[t]{2}{*}{BSW} & BSW.C & Ws, Wb & Write C bit to Ws<Wb> & 1 & 1 & None \\
\hline & & BSW. z & Ws, Wb & Write Z bit to Ws<Wb> & 1 & 1 & None \\
\hline \multirow[t]{2}{*}{9} & \multirow[t]{2}{*}{BTG} & BTG & f,\#bit4 & Bit Toggle f & 1 & 1 & None \\
\hline & & BTG & Ws,\#bit4 & Bit Toggle Ws & 1 & 1 & None \\
\hline \multirow[t]{2}{*}{10} & \multirow[t]{2}{*}{BTSC} & BTSC & f,\#bit4 & Bit Test f, Skip if Clear & 1 & \[
\begin{gathered}
1 \\
(2 \text { or } 3)
\end{gathered}
\] & None \\
\hline & & BTSC & Ws,\#bit4 & Bit Test Ws, Skip if Clear & 1 & \[
\begin{gathered}
1 \\
(2 \text { or } 3)
\end{gathered}
\] & None \\
\hline \multirow[t]{2}{*}{11} & \multirow[t]{2}{*}{BTSS} & BTSS & f,\#bit4 & Bit Test f, Skip if Set & 1 & \[
\begin{gathered}
1 \\
(2 \text { or } 3) \\
\hline
\end{gathered}
\] & None \\
\hline & & BTSS & Ws,\#bit4 & Bit Test Ws, Skip if Set & 1 & \[
\begin{gathered}
1 \\
(2 \text { or } 3)
\end{gathered}
\] & None \\
\hline \multirow[t]{5}{*}{12} & \multirow[t]{5}{*}{BTST} & BTST & f,\#bit4 & Bit Test f & 1 & 1 & Z \\
\hline & & BTST.C & Ws,\#bit4 & Bit Test Ws to C & 1 & 1 & C \\
\hline & & BTST.Z & Ws,\#bit4 & Bit Test Ws to Z & 1 & 1 & Z \\
\hline & & BTST.C & Ws, Wb & Bit Test Ws<Wb> to C & 1 & 1 & C \\
\hline & & BTST.z & Ws,wb & Bit Test Ws<Wb> to Z & 1 & 1 & Z \\
\hline \multirow[t]{3}{*}{13} & \multirow[t]{3}{*}{BTSTS} & BTSTS & f,\#bit4 & Bit Test then Set f & 1 & 1 & Z \\
\hline & & BTSTS.C & Ws,\#bit4 & Bit Test Ws to C, then Set & 1 & 1 & C \\
\hline & & BTSTS. 2 & Ws,\#bit4 & Bit Test Ws to Z, then Set & 1 & 1 & Z \\
\hline \multirow[t]{3}{*}{14} & \multirow[t]{3}{*}{CALL} & CALL & lit23 & Call subroutine & 2 & 4 & SFA \\
\hline & & CALL & Wn & Call indirect subroutine & 1 & 4 & SFA \\
\hline & & CALL.L & Wn & Call indirect subroutine (long address) & 1 & 4 & SFA \\
\hline \multirow[t]{4}{*}{15} & \multirow[t]{4}{*}{CLR} & CLR & f & \(\mathrm{f}=0 \times 0000\) & 1 & 1 & None \\
\hline & & CLR & WREG & WREG \(=0 \times 0000\) & 1 & 1 & None \\
\hline & & CLR & Ws & Ws = 0x0000 & 1 & 1 & None \\
\hline & & CLR & Acc, Wx, Wxd, Wy, Wyd, AWB & Clear Accumulator & 1 & 1 & \[
\begin{gathered}
\mathrm{OA}, \mathrm{OB}, \mathrm{SA}, \\
\mathrm{SB}
\end{gathered}
\] \\
\hline 16 & CLRWDT & CLRWDT & & Clear Watchdog Timer & 1 & 1 & WDTO,Sleep \\
\hline \multirow[t]{3}{*}{17} & \multirow[t]{3}{*}{COM} & COM & f & \(\mathrm{f}=\overline{\mathrm{f}}\) & 1 & 1 & N,Z \\
\hline & & Com & f,WREG & WREG = \(\bar{f}\) & 1 & 1 & N,Z \\
\hline & & COM & Ws, Wd & \(\mathrm{Wd}=\overline{\mathrm{Ws}}\) & 1 & 1 & N,Z \\
\hline \multirow[t]{3}{*}{18} & \multirow[t]{3}{*}{CP} & CP & f & Compare f with WREG & 1 & 1 & C,DC,N,OV,Z \\
\hline & & CP & Wb,\#lit8 & Compare Wb with lit8 & 1 & 1 & C,DC,N,OV,Z \\
\hline & & CP & Wb, Ws & Compare Wb with Ws (Wb - Ws) & 1 & 1 & C,DC,N,OV,Z \\
\hline \multirow[t]{2}{*}{19} & \multirow[t]{2}{*}{CPO} & CP0 & f & Compare f with 0x0000 & 1 & 1 & C,DC,N,OV,Z \\
\hline & & CPO & Ws & Compare Ws with 0x0000 & 1 & 1 & C,DC,N,OV,Z \\
\hline \multirow[t]{3}{*}{20} & \multirow[t]{3}{*}{CPB} & CPB & f & Compare f with WREG, with Borrow & 1 & 1 & C,DC,N,OV,Z \\
\hline & & CPB & Wb,\#lit8 & Compare Wb with lit8, with Borrow & 1 & 1 & C,DC,N,OV,Z \\
\hline & & CPB & Wb, Ws & Compare Wb with Ws, with Borrow
\[
(\mathrm{Wb}-\mathrm{Ws}-\overline{\mathrm{C}})
\] & 1 & 1 & C,DC,N,OV,Z \\
\hline \multirow[t]{2}{*}{21} & CPSEQ & CPSEQ & Wb, Wn & Compare Wb with Wn, skip if \(=\) & 1 & \[
\begin{gathered}
1 \\
(2 \text { or } 3) \\
\hline
\end{gathered}
\] & None \\
\hline & CPBEQ & CPBEQ & Wb, Wn, Expr & Compare Wb with Wn, branch if = & 1 & 1 (5) & None \\
\hline \multirow[t]{2}{*}{22} & CPSGT & CPSGT & Wb, Wn & Compare Wb with Wn, skip if > & 1 & \[
\begin{gathered}
1 \\
(2 \text { or } 3)
\end{gathered}
\] & None \\
\hline & CPBGT & CPBGT & Wb, Wn, Expr & Compare Wb with Wn, branch if > & 1 & 1 (5) & None \\
\hline \multirow[t]{2}{*}{23} & CPSLT & CPSLT & Wb, Wn & Compare Wb with Wn, skip if < & 1 & \[
\begin{gathered}
1 \\
(2 \text { or } 3)
\end{gathered}
\] & None \\
\hline & CPBLT & CPBLT & Wb, Wn, Expr & Compare Wb with Wn, branch if < & 1 & 1 (5) & None \\
\hline \multirow[t]{2}{*}{24} & CPSNE & CPSNE & Wb, Wn & Compare Wb with Wn, skip if \(\neq\) & 1 & \[
\begin{gathered}
1 \\
(2 \text { or } 3)
\end{gathered}
\] & None \\
\hline & CPBNE & CPBNE & Wb, Wn, Expr & Compare Wb with Wn, branch if \(\neq\) & 1 & 1 (5) & None \\
\hline
\end{tabular}

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Base Instr \# & Assembly Mnemonic & & Assembly Syntax & Description & \# of Words & \# of Cycles & Status Flags Affected \\
\hline \multirow[t]{2}{*}{25} & \multirow[t]{2}{*}{CTXTSWP} & CTXTSWP & \#lit3 & Switch CPU register context to context defined by lit3 & 1 & 2 & None \\
\hline & & CTXTSWP & Wn & Switch CPU register context to context defined by Wn & 1 & 2 & None \\
\hline 26 & DAW & DAW & Wn & \(\mathrm{W} \mathrm{n}=\) decimal adjust W & 1 & 1 & C \\
\hline \multirow[t]{3}{*}{27} & \multirow[t]{3}{*}{DEC} & DEC & f & \(\mathrm{f}=\mathrm{f}-1\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & DEC & f,WREG & WREG \(=\mathrm{f}-1\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & DEC & Ws,wd & \(\mathrm{Wd}=\mathrm{Ws}-1\) & 1 & 1 & C,DC,N,OV,Z \\
\hline \multirow[t]{3}{*}{28} & \multirow[t]{3}{*}{DEC2} & DEC2 & f & \(\mathrm{f}=\mathrm{f}-2\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & DEC2 & f,WREG & WREG \(=\mathrm{f}-2\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & DEC2 & Ws,wd & \(\mathrm{Wd}=\mathrm{Ws}-2\) & 1 & 1 & C,DC,N,OV,Z \\
\hline 29 & DISI & DISI & \#lit14 & Disable Interrupts for k instruction cycles & 1 & 1 & None \\
\hline \multirow[t]{4}{*}{30} & \multirow[t]{4}{*}{DIV} & DIV.S & Wm, Wn & Signed 16/16-bit Integer Divide & 1 & 18 & N,Z,C,OV \\
\hline & & DIV.SD & Wm, Wn & Signed 32/16-bit Integer Divide & 1 & 18 & N,Z,C,OV \\
\hline & & DIV.U & Wm, Wn & Unsigned 16/16-bit Integer Divide & 1 & 18 & N,Z,C,OV \\
\hline & & DIV.UD & Wm, Wn & Unsigned 32/16-bit Integer Divide & 1 & 18 & N,Z,C,OV \\
\hline 31 & DIVF & DIVF & Wm, Wn & Signed 16/16-bit Fractional Divide & 1 & 18 & N,Z,C,OV \\
\hline \multirow[t]{2}{*}{32} & \multirow[t]{2}{*}{DO} & DO & \#lit15, Expr & Do code to PC + Expr, lit15 + 1 times & 2 & 2 & None \\
\hline & & DO & Wn, Expr & Do code to PC + Expr, (Wn) + 1 times & 2 & 2 & None \\
\hline 33 & ED & ED & Wm*Wm, Acc, Wx, Wy, Wxd & Euclidean Distance (no accumulate) & 1 & 1 & OA,OB,OAB, SA,SB,SAB \\
\hline 34 & EDAC & EDAC & Wm*Wm, Acc, Wx, Wy, Wxd & Euclidean Distance & 1 & 1 & OA,OB,OAB, SA,SB,SAB \\
\hline 35 & EXCH & EXCH & Wns, Wnd & Swap Wns with Wnd & 1 & 1 & None \\
\hline 36 & FBCL & FBCL & Ws, Wnd & Find Bit Change from Left (MSb) Side & 1 & 1 & C \\
\hline 37 & FF1L & FF1L & Ws, Wnd & Find First One from Left (MSb) Side & 1 & 1 & C \\
\hline 38 & FF1R & FF1R & Ws, Wnd & Find First One from Right (LSb) Side & 1 & 1 & C \\
\hline \multirow[t]{3}{*}{39} & \multirow[t]{3}{*}{GOTO} & GOTO & Expr & Go to address & 2 & 4 & None \\
\hline & & GOTO & Wn & Go to indirect & 1 & 4 & None \\
\hline & & GOTO.L & Wn & Go to indirect (long address) & 1 & 4 & None \\
\hline \multirow[t]{3}{*}{40} & \multirow[t]{3}{*}{INC} & INC & f & \(\mathrm{f}=\mathrm{f}+1\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & INC & f,WREG & WREG \(=\mathrm{f}+1\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & INC & Ws,wd & \(\mathrm{Wd}=\mathrm{Ws}+1\) & 1 & 1 & C,DC,N,OV,Z \\
\hline \multirow[t]{3}{*}{41} & \multirow[t]{3}{*}{INC2} & INC2 & f & \(\mathrm{f}=\mathrm{f}+2\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & INC2 & f, WREG & WREG = f +2 & 1 & 1 & C,DC,N,OV,Z \\
\hline & & INC2 & Ws,wd & \(W \mathrm{~d}=\mathrm{Ws}+2\) & 1 & 1 & C,DC,N,OV,Z \\
\hline \multirow[t]{5}{*}{42} & \multirow[t]{5}{*}{IOR} & IOR & f & \(\mathrm{f}=\mathrm{f}\). IOR. WREG & 1 & 1 & N,Z \\
\hline & & IOR & f, WREG & WREG = f.IOR. WREG & 1 & 1 & N,Z \\
\hline & & IOR & \#lit10,Wn & \(\mathrm{Wd}=\) lit10 .IOR. Wd & 1 & 1 & N,Z \\
\hline & & IOR & Wb,Ws,Wd & \(\mathrm{Wd}=\mathrm{Wb}\).IOR. Ws & 1 & 1 & N,Z \\
\hline & & IOR & Wb, \#lit5,Wd & \(\mathrm{Wd}=\mathrm{Wb}\).IOR. lit5 & 1 & 1 & N,Z \\
\hline 43 & LAC & LAC & Wso,\#Slit4,Acc & Load Accumulator & 1 & 1 & \[
\begin{aligned}
& \text { OA,OB,OAB, } \\
& \text { SA,SB,SAB }
\end{aligned}
\] \\
\hline 44 & LNK & LNK & \#lit14 & Link Frame Pointer & 1 & 1 & SFA \\
\hline \multirow[t]{5}{*}{45} & \multirow[t]{5}{*}{LSR} & LSR & f & \(\mathrm{f}=\) Logical Right Shift f & 1 & 1 & C,N,OV,Z \\
\hline & & LSR & f,WREG & WREG = Logical Right Shift f & 1 & 1 & C,N,OV,Z \\
\hline & & LSR & Ws,wd & Wd = Logical Right Shift Ws & 1 & 1 & C,N,OV,Z \\
\hline & & LSR & Wb, Wns, Wnd & Wnd = Logical Right Shift Wb by Wns & 1 & 1 & N,Z \\
\hline & & LSR & Wb, \#lit5,Wnd & Wnd = Logical Right Shift Wb by lit5 & 1 & 1 & N,Z \\
\hline
\end{tabular}

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Base Instr \# & Assembly Mnemonic & & Assembly Syntax & Description & \# of Words & \# of Cycles & Status Flags Affected \\
\hline \multirow[t]{2}{*}{46} & \multirow[t]{2}{*}{MAC} & MAC & Wm*Wn, Acc, Wx, Wxd, Wy, Wyd, AWB & Multiply and Accumulate & 1 & 1 & OA,OB,OAB, SA,SB,SAB \\
\hline & & MAC & Wm*Wm, Acc, Wx, Wxd, Wy, Wyd & Square and Accumulate & 1 & 1 & OA,OB,OAB, SA,SB,SAB \\
\hline \multirow[t]{10}{*}{47} & \multirow[t]{10}{*}{MOV} & MOV & f,Wn & Move f to Wn & 1 & 1 & None \\
\hline & & MOV & f & Move f to f & 1 & 1 & None \\
\hline & & MOV & f, WREG & Move f to WREG & 1 & 1 & None \\
\hline & & Mov & \#lit16,Wn & Move 16-bit literal to Wn & 1 & 1 & None \\
\hline & & MOV.b & \#lit8,Wn & Move 8-bit literal to Wn & 1 & 1 & None \\
\hline & & MOV & Wn, f & Move Wn to f & 1 & 1 & None \\
\hline & & MOV & Wso, Wdo & Move Ws to Wd & 1 & 1 & None \\
\hline & & mov & WREG, f & Move WREG to f & 1 & 1 & None \\
\hline & & MOV. D & Wns, Wd & Move Double from W(ns):W(ns + 1) to Wd & 1 & 2 & None \\
\hline & & MOV. D & Ws, Wnd & Move Double from Ws to W(nd + 1):W(nd) & 1 & 2 & None \\
\hline \multirow[t]{6}{*}{48} & \multirow[t]{6}{*}{MOVPAG} & MOVPAG & \#lit10, DSRPAG & Move 10-bit literal to DSRPAG & 1 & 1 & None \\
\hline & & MOVPAG & \#lit9, DSWPAG & Move 9-bit literal to DSWPAG & 1 & 1 & None \\
\hline & & MOVPAG & \#lit8, TBLPAG & Move 8-bit literal to TBLPAG & 1 & 1 & None \\
\hline & & MOVPAGW & Ws, DSRPAG & Move Ws<9:0> to DSRPAG & 1 & 1 & None \\
\hline & & MOVPAGW & Ws, DSWPAG & Move Ws \(<8: 0>\) to DSWPAG & 1 & 1 & None \\
\hline & & MOVPAGW & Ws, TBLPAG & Move Ws<7:0> to TBLPAG & 1 & 1 & None \\
\hline 49 & MOVSAC & MOVSAC & Acc, Wx, Wxd, Wy, Wyd, AWB & Prefetch and store accumulator & 1 & 1 & None \\
\hline \multirow[t]{2}{*}{50} & \multirow[t]{2}{*}{MPY} & MPY & Wm*Wn, Acc, Wx, Wxd, Wy, Wyd & Multiply Wm by Wn to Accumulator & 1 & 1 & \[
\begin{aligned}
& \text { OA,OB,OAB, } \\
& \text { SA,SB,SAB }
\end{aligned}
\] \\
\hline & & MPY & Wm*Wm, Acc , Wx, Wxd, Wy, Wyd & Square Wm to Accumulator & 1 & 1 & OA,OB,OAB, SA,SB,SAB \\
\hline 51 & MPY.N & MPY.N & Wm*Wn, Acc , Wx, Wxd, Wy, Wyd & -(Multiply Wm by Wn) to Accumulator & 1 & 1 & None \\
\hline 52 & MSC & MSC & Wm*Wm, Acc, Wx, Wxd, Wy, Wyd, AWB & Multiply and Subtract from Accumulator & 1 & 1 & \[
\begin{aligned}
& \text { OA,OB,OAB, } \\
& \text { SA,SB,SAB }
\end{aligned}
\] \\
\hline
\end{tabular}

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Base Instr \# & Assembly Mnemonic & & Assembly Syntax & Description & \# of Words & \# of Cycles & Status Flags Affected \\
\hline \multirow[t]{19}{*}{53} & \multirow[t]{19}{*}{MUL} & MUL.SS & Wb,Ws, Wnd & \[
\begin{aligned}
& \{\mathrm{Wnd}+1, \mathrm{Wnd}\}=\operatorname{signed}(\mathrm{Wb})^{*} \\
& \text { signed }(\mathrm{Ws})
\end{aligned}
\] & 1 & 1 & None \\
\hline & & MUL.SS & Wb, Ws, Acc & Accumulator \(=\) signed \((\mathrm{Wb})^{*}\) signed \((\mathrm{Ws})\) & 1 & 1 & None \\
\hline & & MUL. SU & Wb,Ws, Wnd & \[
\begin{aligned}
& \{\mathrm{Wnd}+1, \mathrm{Wnd}\}=\text { signed }(\mathrm{Wb})^{*} \\
& \text { unsigned }(\mathrm{Ws})
\end{aligned}
\] & 1 & 1 & None \\
\hline & & MUL. SU & Wb, Ws, Acc & Accumulator \(=\operatorname{signed}(\mathrm{Wb})\) * unsigned(Ws) & 1 & 1 & None \\
\hline & & MUL. SU & Wb, \#lit5, Acc & Accumulator \(=\) signed(Wb) * unsigned(lit5) & 1 & 1 & None \\
\hline & & MUL.US & Wb,Ws, Wnd & ```
{Wnd + 1,Wnd} = unsigned(Wb)*
signed(Ws)
``` & 1 & 1 & None \\
\hline & & MUL.US & Wb, Ws, Acc & ```
Accumulator = unsigned(Wb) *
signed(Ws)
``` & 1 & 1 & None \\
\hline & & MUL.UU & Wb, Ws, Wnd & \[
\begin{aligned}
& \{\mathrm{Wnd}+1, \mathrm{Wnd}\}=\text { unsigned }(\mathrm{Wb})^{*} \\
& \text { unsigned }(\mathrm{Ws})
\end{aligned}
\] & 1 & 1 & None \\
\hline & & MUL.UU & Wb,\#lit5, Acc & ```
Accumulator = unsigned(Wb) *
unsigned(lit5)
``` & 1 & 1 & None \\
\hline & & MUL.UU & Wb, Ws, Acc & ```
Accumulator = unsigned(Wb) *
unsigned(Ws)
``` & 1 & 1 & None \\
\hline & & MULW.SS & Wb,Ws,Wnd & Wnd = signed(Wb) * signed(Ws) & 1 & 1 & None \\
\hline & & MULW.SU & Wb,Ws, Wnd & Wnd = signed(Wb) * unsigned(Ws) & 1 & 1 & None \\
\hline & & MULW.US & Wb, Ws, Wnd & Wnd = unsigned(Wb) * signed(Ws) & 1 & 1 & None \\
\hline & & MULW.UU & Wb,Ws, Wnd & Wnd = unsigned( Wb ) * unsigned(Ws) & 1 & 1 & None \\
\hline & & MUL. SU & Wb, \#lit5,Wnd & \[
\begin{aligned}
& \{\mathrm{Wnd}+1, \mathrm{Wnd}\}=\operatorname{signed}(\mathrm{Wb})^{*} \\
& \text { unsigned(lit5) }
\end{aligned}
\] & 1 & 1 & None \\
\hline & & MUL. SU & Wb, \#lit5, Wnd & Wnd \(=\operatorname{signed}(\mathrm{Wb})^{*}\) unsigned(lit5) & 1 & 1 & None \\
\hline & & MUL.UU & Wb, \#lit5, Wnd & \(\{\mathrm{Wnd}+1\), Wnd \(\}=\) unsigned \((\mathrm{Wb})\) * unsigned(lit5) & 1 & 1 & None \\
\hline & & MUL.UU & Wb, \#lit5,Wnd & Wnd = unsigned(Wb) * unsigned(lit5) & 1 & 1 & None \\
\hline & & MUL & f & W3:W2 = f * WREG & 1 & 1 & None \\
\hline \multirow[t]{4}{*}{54} & \multirow[t]{4}{*}{NEG} & NEG & Acc & Negate Accumulator & 1 & 1 & \[
\begin{aligned}
& \text { OA,OB,OAB, } \\
& \text { SA,SB,SAB }
\end{aligned}
\] \\
\hline & & NEG & f & \(\mathrm{f}=\overline{\mathrm{f}}+1\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & NEG & f,WREG & WREG \(=\overline{\mathrm{f}}+1\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & NEG & Ws,Wd & \(\mathrm{Wd}=\overline{\mathrm{Ws}}+1\) & 1 & 1 & C,DC,N,OV,Z \\
\hline \multirow[t]{2}{*}{55} & \multirow[t]{2}{*}{NOP} & NOP & & No Operation & 1 & 1 & None \\
\hline & & NOPR & & No Operation & 1 & 1 & None \\
\hline \multirow[t]{4}{*}{56} & \multirow[t]{4}{*}{POP} & POP & f & Pop f from Top-of-Stack (TOS) & 1 & 1 & None \\
\hline & & POP & Wdo & Pop from Top-of-Stack (TOS) to Wdo & 1 & 1 & None \\
\hline & & POP.D & Wnd & Pop from Top-of-Stack (TOS) to W(nd):W(nd +1) & 1 & 2 & None \\
\hline & & POP.S & & Pop Shadow Registers & 1 & 1 & All \\
\hline \multirow[t]{4}{*}{57} & \multirow[t]{4}{*}{PUSH} & PUSH & f & Push f to Top-of-Stack (TOS) & 1 & 1 & None \\
\hline & & PUSH & Wso & Push Wso to Top-of-Stack (TOS) & 1 & 1 & None \\
\hline & & PUSH.D & Wns & Push W(ns):W(ns + 1) to Top-of-Stack (TOS) & 1 & 2 & None \\
\hline & & PUSH.S & & Push Shadow Registers & 1 & 1 & None \\
\hline 58 & PWRSAV & PWRSAV & \#lit1 & Go into Sleep or Idle mode & 1 & 1 & WDTO,Sleep \\
\hline \multirow[t]{2}{*}{59} & \multirow[t]{2}{*}{RCALL} & RCALL & Expr & Relative Call & 1 & 4 & SFA \\
\hline & & RCALL & Wn & Computed Call & 1 & 4 & SFA \\
\hline \multirow[t]{2}{*}{60} & \multirow[t]{2}{*}{Repeat} & REPEAT & \#lit15 & Repeat Next Instruction lit15 + 1 times & 1 & 1 & None \\
\hline & & REPEAT & Wn & Repeat Next Instruction (Wn) + 1 times & 1 & 1 & None \\
\hline 61 & RESET & RESET & & Software device Reset & 1 & 1 & None \\
\hline 62 & RETFIE & RETFIE & & Return from interrupt & 1 & 6 (5) & SFA \\
\hline
\end{tabular}

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

\section*{TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)}
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \begin{tabular}{l}
Base \\
Instr \\
\#
\end{tabular} & Assembly Mnemonic & & Assembly Syntax & Description & \# of Words & \# of Cycles & Status Flags Affected \\
\hline 63 & RETLW & RETLW & \#lit10,Wn & Return with literal in Wn & 1 & 6 (5) & SFA \\
\hline 64 & RETURN & \multicolumn{2}{|l|}{RETURN} & Return from Subroutine & 1 & 6 (5) & SFA \\
\hline \multirow[t]{3}{*}{65} & \multirow[t]{3}{*}{RLC} & RLC & f & \(\mathrm{f}=\) Rotate Left through Carry f & 1 & 1 & C,N,Z \\
\hline & & RLC & f,WREG & WREG = Rotate Left through Carry f & 1 & 1 & C,N,Z \\
\hline & & RLC & Ws,wd & Wd = Rotate Left through Carry Ws & 1 & 1 & C,N,Z \\
\hline \multirow[t]{3}{*}{66} & \multirow[t]{3}{*}{RLNC} & RLNC & f & \(\mathrm{f}=\) Rotate Left (No Carry) f & 1 & 1 & N,Z \\
\hline & & RLNC & f,WREG & WREG = Rotate Left (No Carry) f & 1 & 1 & N,Z \\
\hline & & RLNC & Ws,wd & Wd = Rotate Left (No Carry) Ws & 1 & 1 & N, Z \\
\hline \multirow[t]{3}{*}{67} & \multirow[t]{3}{*}{RRC} & RRC & f & \(\mathrm{f}=\) Rotate Right through Carry f & 1 & 1 & C,N,Z \\
\hline & & RRC & f,WREG & WREG = Rotate Right through Carry f & 1 & 1 & C,N,Z \\
\hline & & RRC & Ws,wd & Wd = Rotate Right through Carry Ws & 1 & 1 & C,N,Z \\
\hline \multirow[t]{3}{*}{68} & \multirow[t]{3}{*}{RRNC} & RRNC & f & \(\mathrm{f}=\) Rotate Right (No Carry) f & 1 & 1 & N,Z \\
\hline & & RRNC & f, WREG & WREG = Rotate Right (No Carry) f & 1 & 1 & N,Z \\
\hline & & RRNC & Ws,wd & Wd = Rotate Right (No Carry) Ws & 1 & 1 & N,Z \\
\hline \multirow[t]{2}{*}{69} & \multirow[t]{2}{*}{SAC} & SAC & Acc,\#Slit4,Wdo & Store Accumulator & 1 & 1 & None \\
\hline & & SAC.R & Acc,\#Slit4,Wdo & Store Rounded Accumulator & 1 & 1 & None \\
\hline 70 & SE & SE & Ws, Wnd & Whd = sign-extended Ws & 1 & 1 & C,N,Z \\
\hline \multirow[t]{3}{*}{71} & \multirow[t]{3}{*}{SETM} & SETM & f & \(\mathrm{f}=0 \times \mathrm{FFFF}\) & 1 & 1 & None \\
\hline & & SETM & WREG & WREG = 0xFFFFF & 1 & 1 & None \\
\hline & & SETM & Ws & Ws = 0xFFFF & 1 & 1 & None \\
\hline \multirow[t]{2}{*}{72} & \multirow[t]{2}{*}{SFTAC} & SFTAC & Acc, Wn & Arithmetic Shift Accumulator by (Wn) & 1 & 1 & OA,OB,OAB, SA,SB,SAB \\
\hline & & SFTAC & Acc,\#Slit6 & Arithmetic Shift Accumulator by Slit6 & 1 & 1 & OA,OB,OAB, SA,SB,SAB \\
\hline \multirow[t]{5}{*}{73} & \multirow[t]{5}{*}{SL} & SL & f & \(\mathrm{f}=\) Left Shift f & 1 & 1 & C,N,OV,Z \\
\hline & & SL & f, WREG & WREG = Left Shift f & 1 & 1 & C,N,OV,Z \\
\hline & & SL & Ws,Wd & Wd = Left Shift Ws & 1 & 1 & C,N,OV,Z \\
\hline & & SL & Wb, Wns, Wnd & Wnd = Left Shift Wb by Wns & 1 & 1 & N,Z \\
\hline & & SL & Wb, \#lit5, Wnd & Wnd = Left Shift Wb by lit5 & 1 & 1 & N,Z \\
\hline \multirow[t]{6}{*}{74} & \multirow[t]{6}{*}{SUB} & SUB & Acc & Subtract Accumulators & 1 & 1 & OA,OB,OAB, SA,SB,SAB \\
\hline & & SUB & f & \(\mathrm{f}=\mathrm{f}-\) WREG & 1 & 1 & C,DC,N,OV,Z \\
\hline & & SUB & f, WREG & WREG = \(\mathrm{f}-\) WREG & 1 & 1 & C,DC,N,OV,Z \\
\hline & & SUB & \#lit10,Wn & \(\mathrm{Wn}=\mathrm{Wn}-\mathrm{lit} 10\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & SUB & Wb, Ws, Wd & \(\mathrm{Wd}=\mathrm{Wb}-\mathrm{Ws}\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & SUB & Wb, \#lit5,Wd & \(\mathrm{Wd}=\mathrm{Wb}-\mathrm{lit5}\) & 1 & 1 & C,DC,N,OV,Z \\
\hline \multirow[t]{5}{*}{75} & \multirow[t]{5}{*}{SUBB} & SUBB & f & \(\mathrm{f}=\mathrm{f}-\mathrm{WREG}-(\overline{\mathrm{C}})\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & SUBB & f, WREG & WREG \(=\mathrm{f}-\mathrm{WREG}-(\overline{\mathrm{C}})\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & SUBB & \#lit10,Wn & Wn \(=\mathrm{W} \mathrm{n}-\mathrm{lit} 10-(\overline{\mathrm{C}})\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & SUBB & Wb,Ws, Wd & \(\mathrm{Wd}=\mathrm{Wb}-\mathrm{Ws}-(\overline{\mathrm{C}})\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & SUBB & Wb, \#lit5,Wd & \(\mathrm{Wd}=\mathrm{Wb}-\mathrm{lit5}-(\overline{\mathrm{C}})\) & 1 & 1 & C,DC,N,OV,Z \\
\hline \multirow[t]{4}{*}{76} & \multirow[t]{4}{*}{SUBR} & SUBR & f & \(\mathrm{f}=\) WREG -f & 1 & 1 & C,DC,N,OV,Z \\
\hline & & SUBR & f, WREG & WREG = WREG - f & 1 & 1 & C,DC,N,OV,Z \\
\hline & & SUBR & Wb, Ws, Wd & \(\mathrm{Wd}=\mathrm{Ws}-\mathrm{Wb}\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & SUBR & Wb, \#lit5, Wd & \(\mathrm{Wd}=\) lit5 -Wb & 1 & 1 & C,DC,N,OV,Z \\
\hline \multirow[t]{4}{*}{77} & \multirow[t]{4}{*}{SUBBR} & SUBBR & f & \(\mathrm{f}=\) WREG \(-\mathrm{f}-(\overline{\mathrm{C}})\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & SUBBR & f, WREG & WREG = WREG - \(\mathrm{f}-(\overline{\mathrm{C}})\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & SUBBR & Wb,Ws,Wd & \(W \mathrm{~d}=\mathrm{Ws}-\mathrm{Wb}-(\overline{\mathrm{C}})\) & 1 & 1 & C,DC,N,OV,Z \\
\hline & & SUBBR & Wb, \#lit5, Wd & \(\mathrm{Wd}=\) lit5 \(-\mathrm{Wb}-(\overline{\mathrm{C}})\) & 1 & 1 & C, DC,N,OV,Z \\
\hline
\end{tabular}

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Base Instr \# & Assembly Mnemonic & & Assembly Syntax & Description & \# of Words & \# of Cycles & Status Flags Affected \\
\hline \multirow[t]{2}{*}{78} & \multirow[t]{2}{*}{SWAP} & SWAP.b & Wn & Wn = nibble swap Wn & 1 & 1 & None \\
\hline & & SWAP & Wn & Wn = byte swap Wn & 1 & 1 & None \\
\hline 79 & TBLRDH & TBLRDH & Ws,wd & Read Prog<23:16> to Wd<7:0> & 1 & 5 & None \\
\hline 80 & TBLRDL & TBLRDL & Ws,wd & Read Prog<15:0> to Wd & 1 & 5 & None \\
\hline 81 & TBLWTH & TBLWTH & Ws, Wd & Write Ws<7:0> to Prog<23:16> & 1 & 2 & None \\
\hline 82 & TBLWTL & TBLWTL & Ws,Wd & Write Ws to Prog<15:0> & 1 & 2 & None \\
\hline 83 & ULNK & ULNK & & Unlink Frame Pointer & 1 & 1 & SFA \\
\hline \multirow[t]{5}{*}{84} & \multirow[t]{5}{*}{XOR} & XOR & f & \(\mathrm{f}=\mathrm{f} . \mathrm{XOR}\). WREG & 1 & 1 & N,Z \\
\hline & & XOR & f,WREG & WREG = f.XOR. WREG & 1 & 1 & N,Z \\
\hline & & XOR & \#lit10,Wn & \(\mathrm{Wd}=\) lit10. \(\mathrm{XOR} . \mathrm{Wd}\) & 1 & 1 & N, Z \\
\hline & & XOR & Wb,Ws,Wd & \(\mathrm{Wd}=\mathrm{Wb}\). XOR. Ws & 1 & 1 & N,Z \\
\hline & & XOR & Wb,\#lit5,Wd & Wd = Wb . XOR. lit5 & 1 & 1 & N,Z \\
\hline 85 & ZE & ZE & Ws, Wnd & Wnd = Zero-extend Ws & 1 & 1 & C,Z,N \\
\hline
\end{tabular}

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

\subsection*{29.0 DEVELOPMENT SUPPORT}

The \(\mathrm{PIC}^{\circledR}\) microcontrollers (MCU) and dsPIC \({ }^{\circledR}\) digital signal controllers (DSC) are supported with a full range of software and hardware development tools:
- Integrated Development Environment
- MPLAB \({ }^{\circledR}\) XIDE Software
- Compilers/Assemblers/Linkers
- MPLAB XC Compiler
- MPASM \({ }^{\text {TM }}\) Assembler
- MPLINK \({ }^{\text {TM }}\) Object Linker/ MPLIB \({ }^{\text {M }}\) Object Librarian
- MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
- MPLAB X SIM Software Simulator
- Emulators
- MPLAB REAL ICE \({ }^{\text {TM }}\) In-Circuit Emulator
- In-Circuit Debuggers/Programmers
- MPLAB ICD 3
- PICkit \({ }^{\text {TM }} 3\)
- Device Programmers
- MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

\subsection*{29.1 MPLAB X Integrated Development Environment Software}

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows \({ }^{\circledR}\), Linux and Mac OS \({ }^{\circledR}\) X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for highperformance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.
With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.
Feature-Rich Editor:
- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:
- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:
- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:
- Local file history feature
- Built-in support for Bugzilla issue tracker

\section*{dsPIC33EVXXXGM00X/10X FAMILY}

\subsection*{29.2 MPLAB XC Compilers}

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.
The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.
MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:
- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

\subsection*{29.3 MPASM Assembler}

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.
The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel \({ }^{\circledR}\) standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.
The MPASM Assembler features include:
- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

\subsection*{29.4 MPLINK Object Linker/ MPLIB Object Librarian}

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.
The object linker/library features include:
- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

\subsection*{29.5 MPLAB Assembler, Linker and Librarian for Various Device Families}

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:
- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

\subsection*{29.6 MPLAB X SIM Software Simulator}

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.
The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

\subsection*{29.7 MPLAB REAL ICE In-Circuit Emulator System}

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, LowVoltage Differential Signal (LVDS) interconnection (CAT5).
The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

\subsection*{29.8 MPLAB ICD 3 In-Circuit Debugger System}

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.
The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a highspeed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

\subsection*{29.9 PICkit 3 In-Circuit Debugger/ Programmer}

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a fullspeed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming \({ }^{\text {TM }}\) (ICSP \({ }^{\text {TM }}\) ).

\subsection*{29.10 MPLAB PM3 Device Programmer}

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display ( \(128 \times 64\) ) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

\subsection*{29.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits}

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.
The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.
The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM \(^{\text {TM }}\) and dsPICDEM \({ }^{\text {TM }}\) demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ \({ }^{\circledR}\) security ICs, CAN, IrDA \({ }^{\circledR}\), PowerSmart battery management, SEEVAL \({ }^{\circledR}\) evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.
Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

\subsection*{29.12 Third-Party Development Tools}

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.
- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent \({ }^{\circledR}\) and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika \({ }^{\circledR}\)

\subsection*{30.0 ELECTRICAL CHARACTERISTICS}

This section provides an overview of dsPIC33EVXXXGM00X/10X family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.
Absolute maximum ratings for the dsPIC33EVXXXGM00X/10X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.
Absolute Maximum Ratings \({ }^{(1)}\)Ambient temperature under bias\(-40^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
Storage temperature ..... \(-65^{\circ} \mathrm{C}\) to \(+160^{\circ} \mathrm{C}\)
Voltage on VdD with respect to Vss ..... -0.3 V to +6.0 V
Voltage on Vcap with respect to Vss ..... 1.62 V to 1.98 V
Maximum current out of Vss pin ..... 350 mA
Maximum current into VDD pin \({ }^{(2)}\) ..... 350 mA
Maximum current sunk by any I/O pin ..... 20 mA
Maximum current sourced by I/O pin ..... 18 mA
Maximum current sourced/sunk by all ports \({ }^{(2)}\) ..... 200 mA

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

\subsection*{30.1 DC Characteristics}

TABLE 30-1: OPERATING MIPS vs. VOLTAGE
\begin{tabular}{|l|c|c|c|}
\hline \multirow{2}{*}{ Characteristic } & \begin{tabular}{c} 
Vod Range \\
(in Volts)
\end{tabular} & \multirow{2}{T}{\begin{tabular}{c} 
Temperature Range \\
(in \({ }^{\circ} \mathrm{C}\) )
\end{tabular}} & Maximum MIPS \\
\cline { 4 - 4 } & & dsPIC33EVXXXGM00X/10X Family \\
\hline \hline I-Temp & 4.5 V to \(5.5 \mathrm{~V}^{(1,2)}\) & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) & 70 \\
\hline E-Temp & 4.5 V to \(5.5 \mathrm{~V}^{(1,2)}\) & \(-40^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) & 60 \\
\hline
\end{tabular}

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, op amp/comparator and comparator voltage reference will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.
2: When BOR is enabled, the device will work from 4.7 V to 5.5 V .

Note 1: Customer operating voltage range is specified as: 4.5 V to 5.5 V .

TABLE 30-2: THERMAL OPERATING CONDITIONS


TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS
\begin{tabular}{|l|c|c|c|c|l|}
\hline \multicolumn{1}{|c|}{ Characteristic } & Symbol & Typ. & Max. & \multicolumn{1}{c|}{ Unit } & Notes \\
\hline \hline Package Thermal Resistance, 64-Pin QFN & \(\theta \mathrm{JA}\) & 28.0 & - & \({ }^{\circ} \mathrm{C} / \mathrm{W}\) & \(\mathbf{1}\) \\
\hline Package Thermal Resistance, 64-Pin TQFP, 10x10 mm & \(\theta \mathrm{JA}\) & 48.3 & - & \({ }^{\circ} \mathrm{C} / \mathrm{W}\) & \(\mathbf{1}\) \\
\hline Package Thermal Resistance, 44-Pin QFN & \(\theta \mathrm{JA}\) & 29.0 & - & \({ }^{\circ} \mathrm{C} / \mathrm{W}\) & \(\mathbf{1}\) \\
\hline Package Thermal Resistance, 44-Pin TQFP, 10x10 mm & \(\theta \mathrm{JA}\) & 49.8 & - & \({ }^{\circ} \mathrm{C} / \mathrm{W}\) & \(\mathbf{1}\) \\
\hline Package Thermal Resistance, 28-Pin QFN-S & \(\theta \mathrm{JA}\) & 30.0 & - & \({ }^{\circ} \mathrm{C} / \mathrm{W}\) & \(\mathbf{1}\) \\
\hline Package Thermal Resistance, 28-Pin SOIC & \(\theta \mathrm{JA}\) & 69.7 & - & \({ }^{\circ} \mathrm{C} / \mathrm{W}\) & \(\mathbf{1}\) \\
\hline Package Thermal Resistance, 28-Pin SPDIP & \(\theta \mathrm{JA}\) & 60.0 & - & \({ }^{\circ} \mathrm{C} / \mathrm{W}\) & \(\mathbf{1}\) \\
\hline
\end{tabular}

Note 1: Junction to ambient thermal resistance, Theta-JA ( \(\theta \mathrm{JA}\) ) numbers are achieved by package simulations.

TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions (see Note 3): 4.5V to 5.5 V (unless otherwise stated) \\
Operating temperature \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic & Min. & Typ. \({ }^{(1)}\) & Max. & Units & Conditions \\
\hline \multicolumn{8}{|l|}{Operating Voltage} \\
\hline DC10 & VDD & Supply Voltage \({ }^{(3)}\) & VBOR & - & 5.5 & V & \\
\hline DC12 & VDR & RAM Data Retention Voltage \({ }^{(2)}\) & 1.8 & - & - & V & \\
\hline DC16 & VPOR & Vdd Start Voltage to Ensure Internal Power-on Reset Signal & - & - & Vss & V & \\
\hline DC17 & SVDD & Vdd Rise Rate to Ensure Internal Power-on Reset Signal & 1.0 & - & - & V/ms & \(0 \mathrm{~V}-5.0 \mathrm{~V}\) in 5 ms \\
\hline DC18 & VCore & Vdd Core Internal Regulator Voltage & 1.62 & 1.8 & 1.98 & V & Voltage is dependent on load, temperature and VDD \\
\hline
\end{tabular}

Note 1: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
2: This is the limit to which VDD may be lowered without losing RAM data.
3: VDD voltage must remain at Vss for a minimum of \(200 \mu s\) to ensure POR.
TABLE 30-5: FILTER CAPACITOR (CeFC) SPECIFICATIONS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{8}{|l|}{Standard Operating Conditions (unless otherwise stated) Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended} \\
\hline Param No. & Symbol & Characteristics & Min. & Typ. & Max. & Units & Comments \\
\hline & Cefc & External Filter Capacitor Value \({ }^{(1)}\) & 4.7 & 10 & - & \(\mu \mathrm{F}\) & Capacitor must have a low series resistance (<1 \()\) \\
\hline
\end{tabular}

Note 1: Typical VCAP voltage \(=1.8\) volts when VDD \(\geq\) VDDMIN.

TABLE 30-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{4}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5 V to 5.5 V \\
(unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param. & Typ. \({ }^{(2)}\) & Max. & Units & \multicolumn{3}{|c|}{Conditions} \\
\hline \multicolumn{7}{|l|}{Operating Current (IDD) \({ }^{(1)}\)} \\
\hline DC20d & 4.5 & 5.5 & mA & \(-40^{\circ} \mathrm{C}\) & \multirow{4}{*}{5.0V} & \multirow{4}{*}{10 MIPS} \\
\hline DC20a & 4.65 & 5.6 & mA & \(+25^{\circ} \mathrm{C}\) & & \\
\hline DC20b & 4.85 & 6.0 & mA & \(+85^{\circ} \mathrm{C}\) & & \\
\hline DC20c & 5.6 & 7.2 & mA & \(+125^{\circ} \mathrm{C}\) & & \\
\hline DC22d & 8.6 & 10.6 & mA & \(-40^{\circ} \mathrm{C}\) & \multirow{4}{*}{5.0V} & \multirow{4}{*}{20 MIPS} \\
\hline DC22a & 8.8 & 10.8 & mA & \(+25^{\circ} \mathrm{C}\) & & \\
\hline DC22b & 9.1 & 11.1 & mA & \(+85^{\circ} \mathrm{C}\) & & \\
\hline DC22c & 9.8 & 12.6 & mA & \(+125^{\circ} \mathrm{C}\) & & \\
\hline DC23d & 16.8 & 18.5 & mA & \(-40^{\circ} \mathrm{C}\) & \multirow{4}{*}{5.0V} & \multirow{4}{*}{40 MIPS} \\
\hline DC23a & 17.2 & 19.0 & mA & \(+25^{\circ} \mathrm{C}\) & & \\
\hline DC23b & 17.55 & 19.2 & mA & \(+85^{\circ} \mathrm{C}\) & & \\
\hline DC23c & 18.3 & 21.0 & mA & \(+125^{\circ} \mathrm{C}\) & & \\
\hline DC24d & 25.15 & 28.0 & mA & \(-40^{\circ} \mathrm{C}\) & \multirow{4}{*}{5.0V} & \multirow{4}{*}{60 MIPS} \\
\hline DC24a & 25.5 & 28.0 & mA & \(+25^{\circ} \mathrm{C}\) & & \\
\hline DC24b & 25.5 & 28.0 & mA & \(+85^{\circ} \mathrm{C}\) & & \\
\hline DC24c & 25.55 & 28.5 & mA & \(+125^{\circ} \mathrm{C}\) & & \\
\hline DC25d & 29.0 & 31.0 & mA & \(-40^{\circ} \mathrm{C}\) & \multirow{3}{*}{5.0V} & \multirow{3}{*}{70 MIPS} \\
\hline DC25a & 28.5 & 31.0 & mA & \(+25^{\circ} \mathrm{C}\) & & \\
\hline DC25b & 28.3 & 31.0 & mA & \(+85^{\circ} \mathrm{C}\) & & \\
\hline
\end{tabular}

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:
- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- \(\overline{\mathrm{MCLR}}=\mathrm{VDD}, \mathrm{WDT}\) and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- CPU executing
while(1)
\{
NOP () ;
\}
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.

TABLE 30-7: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{4}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V \\
(unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Parameter No. & Typ. \({ }^{(2)}\) & Max. & Units & \multicolumn{3}{|c|}{Conditions} \\
\hline \multicolumn{7}{|l|}{Idie Current (IIDLE) \({ }^{(1)}\)} \\
\hline DC40d & 1.25 & 1.45 & mA & \(-40^{\circ} \mathrm{C}\) & \multirow{4}{*}{5.0 V} & \multirow{4}{*}{10 MIPS} \\
\hline DC40a & 1.25 & 1.45 & mA & \(+25^{\circ} \mathrm{C}\) & & \\
\hline DC40b & 1.5 & 2.6 & mA & \(+85^{\circ} \mathrm{C}\) & & \\
\hline DC40c & 1.5 & 2.6 & mA & \(+125^{\circ} \mathrm{C}\) & & \\
\hline DC42d & 2.3 & 2.6 & mA & \(-40^{\circ} \mathrm{C}\) & \multirow{4}{*}{5.0 V} & \multirow{4}{*}{20 MIPS} \\
\hline DC42a & 2.3 & 2.6 & mA & \(+25^{\circ} \mathrm{C}\) & & \\
\hline DC42b & 2.6 & 3.45 & mA & \(+85^{\circ} \mathrm{C}\) & & \\
\hline DC42c & 2.6 & 3.85 & mA & \(+125^{\circ} \mathrm{C}\) & & \\
\hline DC44d & 6.9 & 7.5 & mA & \(-40^{\circ} \mathrm{C}\) & \multirow{3}{*}{5.0 V} & \multirow{3}{*}{70 MIPS} \\
\hline DC44a & 6.9 & 7.5 & mA & \(+25^{\circ} \mathrm{C}\) & & \\
\hline DC44b & 7.25 & 8.6 & mA & \(+85^{\circ} \mathrm{C}\) & & \\
\hline
\end{tabular}

Note 1: Base Idle current (IIDLE) is measured as follows:
- CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- \(\overline{\mathrm{MCLR}}=\mathrm{VDD}, \mathrm{WDT}\) and FSCM are disabled
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit \((\) RCON<11> \()=0\) (i.e., Flash regulator is set to standby while the device is in Sleep mode)
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.

TABLE 30-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{4}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V \\
(unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Parameter No. & Typ. \({ }^{(2)}\) & Max. & Units & & & Conditions \\
\hline \multicolumn{7}{|l|}{Power-Down Current (IPD) - dsPIC33EVXXXGM00X/10X \({ }^{(1)}\)} \\
\hline DC60d & 9.25 & 30 & \(\mu \mathrm{A}\) & \(-40^{\circ} \mathrm{C}\) & \multirow{4}{*}{5.0V} & \multirow{4}{*}{Base Power-Down Current} \\
\hline DC60a & 15.75 & 35 & \(\mu \mathrm{A}\) & \(+25^{\circ} \mathrm{C}\) & & \\
\hline DC60b & 67.75 & 250 & \(\mu \mathrm{A}\) & \(+85^{\circ} \mathrm{C}\) & & \\
\hline DC60c & 270 & 750 & \(\mu \mathrm{A}\) & \(+125^{\circ} \mathrm{C}\) & & \\
\hline DC61d & 1 & 7 & \(\mu \mathrm{A}\) & \(-40^{\circ} \mathrm{C}\) & \multirow{4}{*}{5.0V} & \multirow{4}{*}{Watchdog Timer Current: \(\Delta \mathrm{IWDT} T^{(3)}\)} \\
\hline DC61a & 1.25 & 8 & \(\mu \mathrm{A}\) & \(+25^{\circ} \mathrm{C}\) & & \\
\hline DC61b & 3.5 & 12 & \(\mu \mathrm{A}\) & \(+85^{\circ} \mathrm{C}\) & & \\
\hline DC61c & 5 & 15 & \(\mu \mathrm{A}\) & \(+125^{\circ} \mathrm{C}\) & & \\
\hline
\end{tabular}

Note 1: IPD (Sleep) current is measured as follows:
- CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- \(\overline{\mathrm{MCLR}}=\mathrm{VDD}, \mathrm{WDT}\) and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all ones)
- The VREGS bit \((\) RCON \(<8>)=0\) (i.e., core regulator is set to standby while the device is in Sleep mode)
- The VREGSF bit \((\) RCON<11> \()=0\) (i.e., Flash regulator is set to standby while the device is in Sleep mode)
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
3: The \(\Delta\) current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

TABLE 30-9: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{5}{|l|}{\[
\begin{array}{|l}
\hline \text { Standard Operating Conditions: } 4.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \\
\text { (unless otherwise stated) } \\
\begin{array}{ll}
\text { Operating temperature } & -40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C} \text { for Industrial } \\
& -40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C} \text { for Extended }
\end{array}
\end{array}
\]} \\
\hline Parameter No. & Typ. \({ }^{(2)}\) & Max. & \begin{tabular}{l}
Doze \\
Ratio
\end{tabular} & Units & \multicolumn{3}{|c|}{Conditions} \\
\hline \multicolumn{8}{|l|}{Doze Current (IDoze) \({ }^{(1)}\)} \\
\hline DC73a & 16.0 & 17.7 & 1:2 & mA & \multirow[b]{2}{*}{\(-40^{\circ} \mathrm{C}\)} & \multirow[b]{2}{*}{5.0V} & \multirow[b]{2}{*}{70 MIPS} \\
\hline DC73g & 7.1 & 7.57 & 1:128 & mA & & & \\
\hline DC70a & 16.25 & 17.95 & 1:2 & mA & \multirow{2}{*}{\(+25^{\circ} \mathrm{C}\)} & \multirow{2}{*}{5.0V} & \multirow{2}{*}{70 MIPS} \\
\hline DC70g & 7.3 & 7.77 & 1:128 & mA & & & \\
\hline DC71a & 17.0 & 18.7 & 1:2 & mA & \multirow[b]{2}{*}{\(+85^{\circ} \mathrm{C}\)} & \multirow[b]{2}{*}{5.0 V} & \multirow[b]{2}{*}{70 MIPS} \\
\hline DC71g & 7.5 & 8.1 & 1:128 & mA & & & \\
\hline DC72a & 17.75 & 19.95 & 1:2 & mA & \multirow[b]{2}{*}{\(+125^{\circ} \mathrm{C}\)} & \multirow[b]{2}{*}{5.0V} & \multirow[b]{2}{*}{60 MIPS} \\
\hline DC72g & 8.25 & 9.32 & 1:128 & mA & & & \\
\hline
\end{tabular}

Note 1: IDOZE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDOZE measurements are as follows:
- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- \(\overline{\mathrm{MCLR}}=\) VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- CPU executing
while(1)
\{
NOP () ;
\}
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.

TABLE 30-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5 V to 5.5 V (unless otherwise stated) \\
\(\begin{array}{ll}\text { Operating temperature } & -40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C} \text { for Industrial } \\ & -40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C} \text { for Extended }\end{array}\)
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic & Min. & Typ. \({ }^{(1)}\) & Max. & Units & Conditions \\
\hline DI10 & VIL & Input Low Voltage I/O Pins & Vss & - & 0.2 Vdd & V & \\
\hline DI20 & VIH & Input High Voltage I/O Pins & 0.75 VDD & - & 5.5 & V & \\
\hline DI30 & ICNPU & Change Notification Pull-up Current & 200 & 375 & 600 & \(\mu \mathrm{A}\) & \(\mathrm{V} D \mathrm{~L}=5.0 \mathrm{~V}, \mathrm{~V}\) PIN \(=\mathrm{V}\) Ss \\
\hline DI31 & ICNPD & Change Notification Pull-Down Current \({ }^{(7)}\) & 175 & 400 & 625 & \(\mu \mathrm{A}\) & VDD \(=5.0 \mathrm{~V}, \mathrm{~V}\) PIN \(=\mathrm{V}\) DD \\
\hline \[
\begin{aligned}
& \text { DI50 } \\
& \text { DI55 } \\
& \text { DI56 }
\end{aligned}
\] & IIL & \begin{tabular}{l}
Input Leakage Current \({ }^{(2,3)}\) I/O Pins \\
\(\overline{\text { MCLR }}\) \\
OSC1
\end{tabular} & \[
\begin{aligned}
& -100 \\
& -700 \\
& -200
\end{aligned}
\] & \[
\begin{aligned}
& - \\
& - \\
& -
\end{aligned}
\] & \[
\begin{aligned}
& 100 \\
& 700 \\
& 200
\end{aligned}
\] & \begin{tabular}{l}
nA \\
nA \\
nA
\end{tabular} & Vss \(\leq\) VPIN \(\leq\) VDD, Pin at high-impedance Vss \(\leq\) VPIN \(\leq\) VDD Vss \(\leq\) VPIN \(\leq\) VDD, XT and HS modes \\
\hline DI60a & IICL & Input Low Injection Current & 0 & - & \(-5^{(4,6)}\) & mA & All pins except VDD, Vss, AVdd, AVss, MCLR, Vcap and RB7 \\
\hline DI60b & IICH & Input High Injection Current & 0 & - & \(+5^{(5,6)}\) & mA & All pins except Vdd, Vss, AVDD, AVss, MCLR, VcAP, RB7 and all 5 V tolerant pins \({ }^{(5)}\) \\
\hline DI60c & SIICT & Total Input Injection Current (sum of all I/O and control pins) & \(-20^{(7)}\) & - & \(+20^{(7)}\) & mA & Absolute instantaneous sum of all \(\pm\) input injection currents from all I/O pins
\[
\left(|\mathrm{IICL}+|\mathrm{IICH}|) \leq \sum \mathrm{IICT}\right.
\] \\
\hline
\end{tabular}

Note 1: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
2: The leakage current on the \(\overline{M C L R}\) pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
3: Negative current is defined as current sourced by the pin.
4: VIL source < (Vss - 0.3). Characterized but not tested.
5: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources \(>5.5 \mathrm{~V}\).
6: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
7: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted, provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

TABLE 30-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS
\begin{tabular}{|l|l|l|c|c|c|c|c|}
\hline \multicolumn{3}{|c|}{} & \multicolumn{3}{|c|}{\begin{tabular}{l} 
Standard Operating Conditions: 4.5V to 5.5V \\
(unless otherwise stated)
\end{tabular}} \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\hline\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}

Note 1: Parameters are characterized, but not tested.
2: Includes all I/O pins that are not \(8 x\) sink driver pins (see below).
3: Includes pins, such as RA3, RA4 and RB<15:10> for 28-pin devices, RA3, RA4, RA9 and RB<15:10> for 44-pin devices and RA4, RA7, RA9, RB<15:10> and RC15 for 64-pin devices.

TABLE 30-12: ELECTRICAL CHARACTERISTICS: BOR
\begin{tabular}{|l|l|l|c|c|c|c|c|}
\hline \multicolumn{3}{|c|}{} & \multicolumn{3}{|c|}{\begin{tabular}{l} 
Standard Operating Conditions: 4.5V to 5.5V \\
(unless otherwise stated) \\
Operating temperature \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline \begin{tabular}{c} 
Param \\
No.
\end{tabular} & Symbol & Characteristic & Min. \({ }^{(1)}\) & Typ. & Max. & Units & Conditions \\
\hline \hline BO10 & VBOR & \begin{tabular}{l} 
BOR Event on VDD Transition \\
High-to-Low
\end{tabular} & 4.15 & 4.285 & 4.4 & V & \begin{tabular}{l} 
VDD \\
(See Note 2, Note 3 and \\
Note 4)
\end{tabular} \\
\hline
\end{tabular}

Note 1: Parameters are for design guidance only and are not tested in manufacturing.
2: The VBor specification is relative to the VdD.
3: The device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, op amp/comparator and comparator voltage reference will have degraded performance. Device functionality is tested but not characterized.
4: The start-up VDD must rise above 4.6 V .

TABLE 30-13: DC CHARACTERISTICS: PROGRAM MEMORY
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V (unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic & Min & Typ. \({ }^{(1)}\) & Max & Units & Conditions \\
\hline & & Program Flash Memory & & & & & \\
\hline D130 & Ep & Cell Endurance & 10,000 & - & - & E/W & \(-40^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
\hline D131 & VPR & Vdd for Read & 4.5 & - & 5.5 & V & \\
\hline D132b & Vpew & Vdd for Self-Timed Write & 4.5 & - & 5.5 & V & \\
\hline D134 & TRETD & Characteristic Retention & 20 & - & - & Year & Provided no other specifications are violated, \(-40^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
\hline D135 & IDDP & Supply Current During Programming & - & 10 & - & mA & \\
\hline D136a & TRW & Row Write Cycle Time & 0.657 & - & 0.691 & ms & TRW \(=4965\) FRC cycles, TA \(=+85^{\circ} \mathrm{C}\) (See Note 2) \\
\hline D136b & TRW & Row Write Cycle Time & 0.651 & - & 0.698 & ms & TRW \(=4965\) FRC cycles, \(\mathrm{TA}=+125^{\circ} \mathrm{C}\) (See Note 2) \\
\hline D137a & TPE & Page Erase Time & 19.44 & - & 20.44 & ms & TPE \(=146893\) FRC cycles, TA \(=+85^{\circ} \mathrm{C}\) (See Note 2) \\
\hline D137b & TPE & Page Erase Time & 19.24 & - & 20.65 & ms & TPE \(=146893\) FRC cycles, TA \(=+125^{\circ} \mathrm{C}\) (See Note 2) \\
\hline D138a & Tww & Word Write Cycle Time & 45.78 & - & 48.15 & \(\mu \mathrm{s}\) & Tww \(=346\) FRC cycles, TA \(=+85^{\circ} \mathrm{C}\) (See Note 2) \\
\hline D138b & Tww & Word Write Cycle Time & 45.33 & - & 48.64 & \(\mu \mathrm{s}\) & Tww \(=346\) FRC cycles, TA \(=+125^{\circ} \mathrm{C}\) (See Note 2) \\
\hline
\end{tabular}

Note 1: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
2: Other conditions: \(\mathrm{FRC}=7.3728 \mathrm{MHz}, \mathrm{TUN}\left\langle 5: 0>=\mathrm{b}^{\prime} 011111\right.\) (for Min), TUN \(<5: 0>=\mathrm{b}^{\prime} 100000\) (for Max). This parameter depends on the FRC accuracy (see Table 30-19) and the value of the FRC Oscillator Tuning register.

\subsection*{30.2 AC Characteristics and Timing Parameters}

This section defines the dsPIC33EVXXXGM00X/10X family AC characteristics and timing parameters.
TABLE 30-14: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC
\begin{tabular}{|l|l|}
\hline & \begin{tabular}{l} 
Standard Operating Conditions: 4.5V to 5.5V \\
(unless otherwise stated)
\end{tabular} \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
& \begin{tabular}{l} 
Operating voltage VDD range as described in Section 30.1 " DC \\
Characteristics".
\end{tabular} \\
\hline
\end{tabular}

FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS


TABLE 30-15: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS
\begin{tabular}{|l|l|l|c|c|c|c|l|}
\hline \begin{tabular}{c} 
Param \\
No.
\end{tabular} & Symbol & \multicolumn{1}{|c|}{ Characteristic } & Min. & Typ. & Max. & Units & \multicolumn{1}{c|}{ Conditions } \\
\hline \hline DO50 & Cosco & OSC2 Pin & - & - & 15 & pF & \begin{tabular}{l} 
In XT and HS modes, when \\
external clock is used to drive
\end{tabular} \\
DO56 & CIO & All I/O Pins and OSC2 & - & - & 50 & pF & \begin{tabular}{l} 
EC mode \\
ESC1
\end{tabular} \\
DO58 & CB & SCLx, SDAx & - & - & 400 & pF & In \(\mathrm{I}^{2} \mathrm{C}^{\text {TM }}\) mode
\end{tabular}

FIGURE 30-2: EXTERNAL CLOCK TIMING


TABLE 30-16: EXTERNAL CLOCK TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V \\
(unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param No. & Symb & Characteristic & Min. & Typ. \({ }^{(1)}\) & Max. & Units & Conditions \\
\hline \multirow[t]{2}{*}{OS10} & \multirow[t]{2}{*}{Fin} & External CLKI Frequency (External clocks allowed only in EC and ECPLL modes) & DC & - & 40 & MHz & EC \\
\hline & & Oscillator Crystal Frequency & \[
\begin{gathered}
3.5 \\
10
\end{gathered}
\] & - & \[
\begin{aligned}
& 10 \\
& 25
\end{aligned}
\] & \[
\begin{aligned}
& \mathrm{MHz} \\
& \mathrm{MHz}
\end{aligned}
\] & \[
\begin{aligned}
& \text { XT } \\
& \text { HS }
\end{aligned}
\] \\
\hline OS20 & Tosc & Tosc \(=1 / \mathrm{Fosc}\) & 12.5 & - & DC & ns & \(\mathrm{TA}=+125^{\circ} \mathrm{C}\) \\
\hline OS25 & TcY & Instruction Cycle Time \({ }^{(2)}\) & 25 & - & DC & ns & TA \(=+125^{\circ} \mathrm{C}\) \\
\hline OS30 & TosL, TosH & External Clock in (OSC1) High or Low Time & \(0.375 \times\) Tosc & - & \(0.625 \times\) Tosc & ns & EC \\
\hline OS31 & TosR, TosF & External Clock in (OSC1) Rise or Fall Time & - & - & 20 & ns & EC \\
\hline OS40 & TckR & CLKO Rise Time \({ }^{(3)}\) & - & 5.2 & - & ns & \\
\hline OS41 & TckF & CLKO Fall Time \({ }^{(3)}\) & - & 5.2 & - & ns & \\
\hline \multirow[t]{2}{*}{OS42} & \multirow[t]{2}{*}{Gm} & \multirow[t]{2}{*}{\begin{tabular}{l}
External Oscillator \\
Transconductance \({ }^{(4)}\)
\end{tabular}} & - & 12 & - & mA/V & \[
\begin{aligned}
& \mathrm{HS}, \mathrm{VDD}=5.0 \mathrm{~V}, \\
& \mathrm{TA}=+25^{\circ} \mathrm{C}
\end{aligned}
\] \\
\hline & & & - & 6 & - & mA/V & \[
\begin{aligned}
& \mathrm{XT}, \mathrm{VDD}=5.0 \mathrm{~V}, \\
& \mathrm{TA}=+25^{\circ} \mathrm{C}
\end{aligned}
\] \\
\hline
\end{tabular}

Note 1: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Minimum" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Maximum" cycle time limit is "DC" (no clock) for all devices.
3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.
4: This parameter is characterized, but is not tested in manufacturing.

\section*{TABLE 30-17: PLL CLOCK TIMING SPECIFICATIONS}
\begin{tabular}{|l|l|l|c|c|c|c|c|c|}
\hline \multicolumn{3}{|c|}{} & \multicolumn{3}{|c|}{\begin{tabular}{l} 
Standard Operating Conditions: 4.5V to 5.5V \\
(unless otherwise stated) \\
Operating temperature \(\quad-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline \begin{tabular}{c} 
Param \\
No.
\end{tabular} & Symbol & \multicolumn{1}{|c|}{ Characteristic } & Min. & Typ. \({ }^{(1)}\) & Max. & Units & Conditions \\
\hline \hline OS50 & FPLLI & \begin{tabular}{l} 
PLL Voltage Controlled \\
Oscillator (VCO) Input \\
Frequency Range
\end{tabular} & 0.8 & - & 8.0 & MHz & ECPLL, XTPLL modes \\
\hline OS51 & FSYs & \begin{tabular}{l} 
On-Chip VCO System \\
Frequency
\end{tabular} & 120 & - & 340 & MHz & \\
\hline OS52 & TLOCK & PLL Start-up Time (Lock Time) & 0.9 & 1.5 & 3.1 & ms & \\
\hline OS53 & DCLK & CLKO Stability (Jitter) \({ }^{(2)}\) & -3 & 0.5 & 3 & \(\%\) & \\
\hline
\end{tabular}

Note 1: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated. Parameters are for design guidance only and are not tested.
2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases or communication clocks used by the application, use the following formula:


For example, if Fosc \(=120 \mathrm{MHz}\) and the SPI bit rate \(=10 \mathrm{MHz}\), the effective jitter is as follows:
\[
\text { Effective Jitter }=\frac{D C L K}{\sqrt{\frac{120}{10}}}=\frac{D C L K}{\sqrt{12}}=\frac{D C L K}{3.464}
\]

TABLE 30-18: INTERNAL FRC ACCURACY
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|l|}{AC CHARACTERISTICS} & \multicolumn{6}{|l|}{Standard Operating Conditions: 4.5 V to 5.5 V (unless otherwise stated) Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended} \\
\hline Param No. & Characteristic & Min. & Typ. & Max. & Units & \multicolumn{2}{|c|}{Conditions} \\
\hline \multicolumn{8}{|l|}{Internal FRC Accuracy @ FRC Frequency = 7.37 MHz \({ }^{(1)}\)} \\
\hline F20a & FRC & -1 & 0.5 & +1 & \% & \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) & VDD \(=4.5-5.5 \mathrm{~V}\) \\
\hline F20b & FRC & -2 & 1 & +2 & \% & \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) & \(\mathrm{VDD}=4.5-5.5 \mathrm{~V}\) \\
\hline
\end{tabular}

Note 1: Frequency calibrated at \(+25^{\circ} \mathrm{C}\) and 5.0 V . TUN \(<5: 0>\) bits can be used to compensate for temperature drift.

\section*{TABLE 30-19: INTERNAL LPRC ACCURACY}
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|l|}{AC CHARACTERISTICS} & \multicolumn{6}{|l|}{Standard Operating Conditions: 4.5V to 5.5 V (unless otherwise stated) Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended} \\
\hline Param No. & Characteristic & Min. & Typ. & Max. & Units & Cond & tions \\
\hline \multicolumn{8}{|l|}{LPRC @ \(32.768 \mathrm{kHz}^{(1)}\)} \\
\hline F21a & LPRC & -15 & 5 & +15 & \% & \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) & \(\mathrm{VDD}=4.5-5.5 \mathrm{~V}\) \\
\hline F21b & LPRC & -30 & 10 & +30 & \% & \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) & \(\mathrm{V} D \mathrm{D}=4.5-5.5 \mathrm{~V}\) \\
\hline
\end{tabular}

Note 1: Change of LPRC frequency as VDD changes.

FIGURE 30-3: I/O TIMING CHARACTERISTICS


Note: Refer to Figure 30-1 for load conditions.

TABLE 30-20: I/O TIMING REQUIREMENTS
\begin{tabular}{|l|l|l|c|c|c|c|c|c|}
\hline \multicolumn{3}{|c|}{} & \multicolumn{4}{|c|}{\begin{tabular}{l} 
Standard Operating Conditions: 4.5V to 5.5V \\
(unless otherwise stated) \\
Operating temperature \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline \begin{tabular}{c} 
Param \\
No.
\end{tabular} & Symbol & Characteristic & Min. & Typ. \({ }^{(1)}\) & Max. & Units & Conditions \\
\hline \hline DO31 & TIOR & Port Output Rise Time & - & 5 & 10 & ns & \\
\hline DO32 & TIOF & Port Output Fall Time & - & 5 & 10 & ns & \\
\hline DI35 & TINP & INTx Pin High or Low Time (input) & 20 & - & - & ns & \\
\hline DI40 & TRBP & CNx High or Low Time (input) & 2 & - & - & TCY & \\
\hline
\end{tabular}

Note 1: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.

FIGURE 30-4: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS


FIGURE 30-5: POWER-ON RESET TIMING CHARACTERISTICS
Power-up Timer Disabled - Clock Sources = (FRC, FRCDIVN, FRCDIV16, FRCPLL, EC, ECPLL and LPRC)


Power-up Timer Disabled \(\boldsymbol{-}\) Clock Sources \(=(\) HS, HSPLL, XT and XTPLL)

- - - - - - - - - - - - - - - - - - - - - - - - -

Power-up Timer Enabled - Clock Sources = (FRC, FRCDIVN, FRCDIV16, FRCPLL, EC, ECPLL and LPRC)


Power-up Timer Enabled - Clock Sources = (HS, HSPLL, XT and XTPLL)


Note 1: The power-up period will be extended if the power-up sequence completes before the device exits from BOR (VDD < VBor).
2: The power-up period includes internal voltage regulator stabilization delay.

TABLE 30-21: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\[
\begin{aligned}
& \text { Standard Operating Conditions: } 4.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \\
& \text { (unless otherwise stated) } \\
& \begin{array}{ll}
\text { Operating temperature }-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C} \text { for Industrial } \\
& -40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C} \text { for Extended }
\end{array}
\end{aligned}
\]} \\
\hline Param No. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline SY00 & TPU & Power-up Period & - & 400 & 600 & \(\mu \mathrm{s}\) & \\
\hline SY10 & Tost & Oscillator Start-up Time & - & 1024 Tosc & - & - & Tosc = OSC1 period \\
\hline \multirow[t]{2}{*}{SY12} & TWDT & Watchdog Timer Time-out Period & 0.8 & - & 1.2 & ms & WDTPRE \(=0\), WDTPS \(<3: 0>=0000\), using LPRC tolerances indicated in F21a/F21b (see Table 30-19) at \(+85^{\circ} \mathrm{C}\) \\
\hline & & & 3.2 & - & 4.8 & ms & WDTPRE \(=1\), WDTPS \(<3: 0>=0000\), using LPRC tolerances indicated in F21a/F21b (see Table 30-19) at \(+85^{\circ} \mathrm{C}\) \\
\hline SY13 & TıOz & I/O High-Impedance from MCLR Low or Watchdog Timer Reset & 0.68 & 0.72 & 1.2 & \(\mu \mathrm{s}\) & \\
\hline SY20 & TMCLR & \(\overline{\text { MCLR }}\) Pulse Width (low) & 2 & - & - & \(\mu \mathrm{s}\) & \\
\hline SY30 & TBOR & BOR Pulse Width (low) & 1 & - & - & ms & \\
\hline SY35 & Tfscm & Fail-Safe Clock Monitor Delay & - & 500 & 900 & \(\mu \mathrm{s}\) & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) \\
\hline SY36 & TVREG & Voltage Regulator Standby-to-Active mode Transition Time & - & - & 30 & \(\mu \mathrm{s}\) & \\
\hline SY37 & Toscdfrc & FRC Oscillator Start-up Delay & 46 & 48 & 54 & \(\mu \mathrm{s}\) & \\
\hline SY38 & Toscdiprc & LPRC Oscillator Start-up Delay & - & - & 70 & \(\mu \mathrm{s}\) & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.

FIGURE 30-6: TIMER1-TIMER5 EXTERNAL CLOCK TIMING CHARACTERISTICS


Note: Refer to Figure 30-1 for load conditions.

TABLE 30-22: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS \({ }^{(1)}\)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{4}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V (unless otherwise stated) \\
Operating temperature \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param No. & Symbol & \multicolumn{2}{|l|}{Characteristic \({ }^{(2)}\)} & Min. & Typ. & Max. & Units & Conditions \\
\hline \multirow[t]{2}{*}{TA10} & \multirow[t]{2}{*}{TтXH} & \multirow[t]{2}{*}{T1CK High Time} & Synchronous mode & \[
\begin{aligned}
& \hline \text { Greater of: } \\
& 20 \text { or } \\
& (\mathrm{TCY}+20) / \mathrm{N}
\end{aligned}
\] & - & - & ns & Must also meet Parameter TA15, \(\mathrm{N}=\) Prescaler value (1, 8, 64, 256) \\
\hline & & & Asynchronous mode & 35 & - & - & ns & \\
\hline \multirow[t]{2}{*}{TA11} & \multirow[t]{2}{*}{TtxL} & \multirow[t]{2}{*}{T1CK Low Time} & Synchronous mode & \[
\begin{aligned}
& \text { Greater of: } \\
& \quad 20 \text { or } \\
& (\mathrm{TCY}+20) / \mathrm{N}
\end{aligned}
\] & - & - & ns & Must also meet Parameter TA15, \(\mathrm{N}=\) Prescaler value (1, 8, 64, 256) \\
\hline & & & Asynchronous mode & 10 & - & - & ns & \\
\hline TA15 & TTXP & T1CK Input Period & Synchronous mode & \[
\begin{gathered}
\text { Greater of: } \\
40 \text { or } \\
(2 \mathrm{TcY}+40) / \mathrm{N}
\end{gathered}
\] & - & - & ns & \[
\begin{aligned}
& N=\text { Prescaler value } \\
& (1,8,64,256)
\end{aligned}
\] \\
\hline OS60 & Ft1 & \multicolumn{2}{|l|}{T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS ( \(\mathrm{T} 1 \mathrm{CON}<1>\) ) bit)} & DC & - & 50 & kHz & \\
\hline TA20 & TCKEXTMRL & \multicolumn{2}{|l|}{Delay from External T1CK Clock Edge to Timer Increment} & 0.75 TCY + 40 & - & 1.75 TcY + 40 & ns & \\
\hline \multicolumn{9}{|l|}{\begin{tabular}{l}
Note 1: Timer1 is a Type A. \\
2: These parameters are characterized, but are not tested in manufacturing.
\end{tabular}} \\
\hline
\end{tabular}

TABLE 30-23: TIMER2 AND TIMER4 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{4}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{```
Standard Operating Conditions: 4.5V to 5.5V
(unless otherwise stated)
Operating temperature }-4\mp@subsup{0}{}{\circ}\textrm{C}\leq\textrm{TA}\leq+8\mp@subsup{5}{}{\circ}\textrm{C}\mathrm{ for Industrial
    -40}\mp@subsup{}{}{\circ}\textrm{C}\leq\textrm{TA}\leq+12\mp@subsup{5}{}{\circ}\textrm{C}\mathrm{ for Extended
```} \\
\hline Param No. & Symbol & Charac & teristic \({ }^{(1)}\) & Min. & Typ. & Max. & Units & Conditions \\
\hline TB10 & TtxH & TxCK High Time & Synchronous mode & \[
\begin{aligned}
& \text { Greater of: } \\
& 20 \text { or } \\
& (\mathrm{TcY}+20) / \mathrm{N}
\end{aligned}
\] & - & - & ns & Must also meet Parameter TB15, \(\mathrm{N}=\) Prescaler value (1, 8, 64, 256) \\
\hline TB11 & TtxL & TxCK Low Time & Synchronous mode & \[
\begin{aligned}
& \text { Greater of: } \\
& 20 \text { or } \\
& (\mathrm{TcY}+20) / \mathrm{N}
\end{aligned}
\] & - & - & ns & Must also meet Parameter TB15, \(\mathrm{N}=\) Prescaler value (1, 8, 64, 256) \\
\hline TB15 & TtxP & TxCK Input Period & Synchronous mode & \[
\begin{gathered}
\text { Greater of: } \\
40 \text { or } \\
(2 \mathrm{TcY}+40) / \mathrm{N}
\end{gathered}
\] & - & - & ns & \[
\begin{aligned}
& \mathrm{N}=\text { Prescaler value } \\
& (1,8,64,256)
\end{aligned}
\] \\
\hline TB20 & TCKEXTMRL & Delay from Clock Edge Increment & External TxCK to Timer & 0.75 Tcy + 40 & - & 1.75 TCy + 40 & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.

TABLE 30-24: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{4}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5 V to 5.5 V \\
(unless otherwise stated)
\[
\begin{array}{|ll|}
\hline \text { Operating temperature } & -40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C} \text { for Industrial } \\
& -40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C} \text { for Extended }
\end{array}
\]
\end{tabular}} \\
\hline Param No. & Symbol & Charac & teristic \({ }^{(1)}\) & Min. & Typ. & Max. & Units & Conditions \\
\hline TC10 & TtxH & TxCK High Time & Synchronous & TCY + 20 & - & - & ns & Must also meet Parameter TC15 \\
\hline TC11 & TtxL & TxCK Low Time & Synchronous & TCY + 20 & - & - & ns & Must also meet Parameter TC15 \\
\hline TC15 & TTXP & TxCK Input Period & Synchronous, with Prescaler & 2 TCY + 40 & - & - & ns & \[
\begin{array}{|l}
N=\text { Prescaler value } \\
(1,8,64,256)
\end{array}
\] \\
\hline TC20 & TCKEXTMRL & Delay from Clock Edge Increment & External TxCK to Timer & 0.75 TCY + 40 & - & 1.75 TCY + 40 & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.

FIGURE 30-7: INPUT CAPTURE \(x\) (ICx) TIMING CHARACTERISTICS


Note 1: Refer to Figure 30-1 for load conditions.

TABLE 30-25: INPUT CAPTURE x (ICx) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V \\
(unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param. No. & Symbol & Characteristics \({ }^{(1)}\) & Min. & Max. & Units & \multicolumn{2}{|r|}{Conditions} \\
\hline IC10 & TccL & ICx Input Low Time & \[
\begin{gathered}
\hline \text { Greater of: } \\
12.5+25 \text { or } \\
(0.5 \mathrm{TCY} / \mathrm{N})+25
\end{gathered}
\] & - & ns & Must also meet Parameter IC15 & \multirow{3}{*}{\(N=\) Prescaler value (1, 4, 16)} \\
\hline IC11 & TccH & ICx Input High Time & \[
\begin{gathered}
\text { Greater of: } \\
12.5+25 \text { or } \\
(0.5 \mathrm{TcY} / \mathrm{N})+25
\end{gathered}
\] & - & ns & Must also meet Parameter IC15 & \\
\hline IC15 & TccP & ICx Input Period & \[
\begin{gathered}
\text { Greater of: } \\
25+50 \text { or } \\
(1 \mathrm{TCY} / \mathrm{N})+50 \\
\hline
\end{gathered}
\] & - & ns & & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.

FIGURE 30-8: OUTPUT COMPARE x (OCx) TIMING CHARACTERISTICS


Note: Refer to Figure 30-1 for load conditions.

TABLE 30-26: OUTPUT COMPARE x (OCx) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|c|}{} & \multicolumn{3}{|l|}{\begin{tabular}{l} 
Standard Operating Conditions: 4.5V to 5.5V \\
(unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline \begin{tabular}{c} 
Param \\
No.
\end{tabular} & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. & Max. & Units & Conditions \\
\hline \hline OC10 & TCCF & OCx Output Fall Time & - & - & - & ns & See Parameter DO32 \\
\hline OC11 & TCCR & OCx Output Rise Time & - & - & - & ns & See Parameter DO31 \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.

FIGURE 30-9: OCx/PWMx MODULE TIMING CHARACTERISTICS


TABLE 30-27: OCx/PWMx MODE TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5 V to 5.5 V (unless otherwise stated) \\
Operating temperature \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. & Max. & Units & Conditions \\
\hline OC15 & TFD & Fault Input to PWMx I/O Change & - & - & TCY + 20 & ns & \\
\hline OC20 & Tflt & Fault Input Pulse Width & TCY + 20 & - & - & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 30-10: HIGH-SPEED PWMx MODULE FAULT TIMING CHARACTERISTICS


FIGURE 30-11: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS


Note: Refer to Figure 30-1 for load conditions.

TABLE 30-28: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V (unless otherwise stated) \\
Operating temperature \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. & Max. & Units & Conditions \\
\hline MP10 & TFPWM & PWMx Output Fall Time & - & - & - & ns & See Parameter DO32 \\
\hline MP11 & TRPWM & PWMx Output Rise Time & - & - & - & ns & See Parameter DO31 \\
\hline MP20 & Tfd & Fault Input \(\downarrow\) to PWMx I/O Change & - & - & 15 & ns & \\
\hline MP30 & Tfr & Fault Input Pulse Width & 15 & - & - & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.

TABLE 30-29: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{4}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V \\
(unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Maximum Data Rate & Master Transmit Only (Half-Duplex) & Master Transmit/Receive (Full-Duplex) & Slave Transmit/Receive (Full-Duplex) & CKE & CKP & SMP \\
\hline 15 MHz & Table 30-30 & - & - & 0,1 & 0,1 & 0,1 \\
\hline 9 MHz & - & Table 30-31 & - & 1 & 0,1 & 1 \\
\hline 9 MHz & - & Table 30-32 & - & 0 & 0,1 & 1 \\
\hline 15 MHz & - & - & Table 30-33 & 1 & 0 & 0 \\
\hline 11 MHz & - & - & Table 30-34 & 1 & 1 & 0 \\
\hline 15 MHz & - & - & Table 30-35 & 0 & 1 & 0 \\
\hline 11 MHz & - & - & Table 30-36 & 0 & 0 & 0 \\
\hline
\end{tabular}

FIGURE 30-12: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS


Note: Refer to Figure 30-1 for load conditions.

FIGURE 30-13: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS


Note: Refer to Figure 30-1 for load conditions.

TABLE 30-30: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5 V to 5.5 V \\
(unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline SP10 & FscP & Maximum SCK2 Frequency & - & - & 15 & MHz & See Note 3 \\
\hline SP20 & TscF & SCK2 Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP21 & TscR & SCK2 Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP30 & TdoF & SDO2 Data Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP31 & TdoR & SDO2 Data Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP35 & TscH2doV, TscL2doV & SDO2 Data Output Valid after SCK2 Edge & - & 6 & 20 & ns & \\
\hline SP36 & TdiV2scH, TdiV2scL & SDO2 Data Output Setup to First SCK2 Edge & 30 & - & - & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
3: The minimum clock period for SCK2 is 66.7 ns . Therefore, the clock generated in Master mode must not violate this specification.
4: Assumes 50 pF load on all SPI2 pins.

FIGURE 30-14: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = \(x\), SMP = 1) TIMING CHARACTERISTICS


TABLE 30-31: SPI2 MASTER MODE (FULL-DUPLEX, CKE = \(1, \mathrm{CKP}=\mathrm{x}, \mathrm{SMP}=1\) ) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{```
Standard Operating Conditions: 4.5V to 5.5V
(unless otherwise stated)
Operating temperature }-4\mp@subsup{0}{}{\circ}\textrm{C}\leq\textrm{TA}\leq+8\mp@subsup{5}{}{\circ}\textrm{C}\mathrm{ for Industrial
    -40}\mp@subsup{}{}{\circ}\textrm{C}\leq\textrm{TA}\leq+12\mp@subsup{5}{}{\circ}\textrm{C}\mathrm{ for Extended
```} \\
\hline Param. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline SP10 & FscP & Maximum SCK2 Frequency & - & - & 9 & MHz & See Note 3 \\
\hline SP20 & TscF & SCK2 Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP21 & TscR & SCK2 Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP30 & TdoF & SDO2 Data Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP31 & TdoR & SDO2 Data Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP35 & TscH2doV, TscL2doV & SDO2 Data Output Valid after SCK2 Edge & - & 6 & 20 & ns & \\
\hline SP36 & TdoV2sc, TdoV2scL & SDO2 Data Output Setup to First SCK2 Edge & 30 & - & - & ns & \\
\hline SP40 & TdiV2scH, TdiV2scL & Setup Time of SDI2 Data Input to SCK2 Edge & 30 & - & - & ns & \\
\hline SP41 & TscH2diL, TscL2diL & Hold Time of SDI2 Data Input to SCK2 Edge & 30 & - & - & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
3: The minimum clock period for SCK2 is 111 ns . The clock generated in Master mode must not violate this specification.
4: Assumes 50 pF load on all SPI2 pins.

FIGURE 30-15: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP \(=x\), SMP \(=1\) ) TIMING CHARACTERISTICS


Note: Refer to Figure 30-1 for load conditions.

TABLE 30-32: SPI2 MASTER MODE (FULL-DUPLEX, CKE =0, CKP = x, SMP =1) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V (unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline SP10 & FscP & Maximum SCK2 Frequency & - & - & 9 & MHz & \(-40^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) and see Note 3 \\
\hline SP20 & TscF & SCK2 Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP21 & TscR & SCK2 Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP30 & TdoF & SDO2 Data Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP31 & TdoR & SDO2 Data Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP35 & TscH2doV, TscL2doV & SDO2 Data Output Valid after SCK2 Edge & - & 6 & 20 & ns & \\
\hline SP36 & TdoV2scH, TdoV2scL & SDO2 Data Output Setup to First SCK2 Edge & 30 & - & - & ns & \\
\hline SP40 & TdiV2scH, TdiV2scL & Setup Time of SDI2 Data Input to SCK2 Edge & 30 & - & - & ns & \\
\hline SP41 & TscH2diL, TscL2diL & Hold Time of SDI2 Data Input to SCK2 Edge & 30 & - & - & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
3: The minimum clock period for SCK2 is 111 ns . The clock generated in Master mode must not violate this specification.
4: Assumes 50 pF load on all SPI2 pins.

FIGURE 30-16: SPI2 SLAVE MODE (FULL-DUPLEX, CKE \(=1\), CKP \(=0\), SMP \(=0\) ) TIMING CHARACTERISTICS


TABLE 30-33: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = \(1, C K P=0, S M P=0\) ) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{```
Standard Operating Conditions: 4.5V to 5.5V
(unless otherwise stated)
Operating temperature
    -40}\mp@subsup{}{}{\circ}\textrm{C}\leq\textrm{TA}\leq+8\mp@subsup{5}{}{\circ}\textrm{C}\mathrm{ for Industrial
    -40}\mp@subsup{}{}{\circ}\textrm{C}\leqT\textrm{TA}\leq+12\mp@subsup{5}{}{\circ}\textrm{C}\mathrm{ for Extended
```} \\
\hline Param. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline SP70 & FscP & Maximum SCK2 Input Frequency & - & - & 15 & MHz & See Note 3 \\
\hline SP72 & TscF & SCK2 Input Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP73 & TscR & SCK2 Input Rise Time & - & - & - & ns & See Parameter DO31 and Note Note 4 \\
\hline SP30 & TdoF & SDO2 Data Output Fall Time & - & - & - & ns & See Parameter DO32 and Note Note 4 \\
\hline SP31 & TdoR & SDO2 Data Output Rise Time & - & - & - & ns & See Parameter DO31 and Note Note 4 \\
\hline SP35 & TscH2doV, TscL2doV & SDO2 Data Output Valid after SCK2 Edge & - & 6 & 20 & ns & \\
\hline SP36 & TdoV2scH,
TdoV2scL & SDO2 Data Output Setup to First SCK2 Edge & 30 & - & - & ns & \\
\hline SP40 & TdiV2scH, TdiV2scL & Setup Time of SDI2 Data Input to SCK2 Edge & 30 & - & - & ns & \\
\hline SP41 & TscH2diL, TscL2diL & Hold Time of SDI2 Data Input to SCK2 Edge & 30 & - & - & ns & \\
\hline SP50 & TssL2scH, TssL2scL & \(\overline{\text { SS2 }} \downarrow\) to SCK2 \(\uparrow\) or SCK2 \(\downarrow\) Input & 120 & - & - & ns & \\
\hline SP51 & TssH2doZ & \(\overline{\mathrm{SS} 2} \uparrow\) to SDO2 Output High-Impedance & 10 & - & 50 & ns & See Note 4 \\
\hline SP52 & \begin{tabular}{l}
TscH2ssH \\
TscL2ssH
\end{tabular} & \(\overline{\mathrm{SS} 2} \uparrow\) after SCK2 Edge & \(1.5 \mathrm{TCY}+40\) & - & - & ns & See Note 4 \\
\hline SP60 & TssL2doV & SDO2 Data Output Valid after SS2 Edge & - & - & 50 & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
3: The minimum clock period for SCK2 is 66.7 ns . Therefore, the SCK2 clock generated by the master must not violate this specification.
4: Assumes 50 pF load on all SPI2 pins.

FIGURE 30-17: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS


TABLE 30-34: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = \(1, \mathrm{CKP}=1, \mathrm{SMP}=0\) ) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\[
\begin{array}{|l}
\hline \text { Standard Operating Conditions: } 4.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \\
\text { (unless otherwise stated) } \\
\begin{array}{ll}
\text { Operating temperature } \quad-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C} \text { for Industrial } \\
& -40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C} \text { for Extended }
\end{array}
\end{array}
\]} \\
\hline Param. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline SP70 & FscP & Maximum SCK2 Input Frequency & - & - & 11 & MHz & See Note 3 \\
\hline SP72 & TscF & SCK2 Input Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP73 & TscR & SCK2 Input Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP30 & TdoF & SDO2 Data Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP31 & TdoR & SDO2 Data Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP35 & TscH2doV, TscL2doV & SDO2 Data Output Valid after SCK2 Edge & - & 6 & 20 & ns & \\
\hline SP36 & TdoV2scH, TdoV2scL & SDO2 Data Output Setup to First SCK2 Edge & 30 & - & - & ns & \\
\hline SP40 & TdiV2scH, TdiV2scL & Setup Time of SDI2 Data Input to SCK2 Edge & 30 & - & - & ns & \\
\hline SP41 & TscH2diL, TscL2diL & Hold Time of SDI2 Data Input to SCK2 Edge & 30 & - & - & ns & \\
\hline SP50 & TssL2scH, TssL2scL & \(\overline{\mathrm{SS} 2} \downarrow\) to SCK2 \(\uparrow\) or SCK2 \(\downarrow\) Input & 120 & - & - & ns & \\
\hline SP51 & TssH2doZ & \(\overline{\mathrm{SS} 2} \uparrow\) to SDO2 Output High-Impedance & 10 & - & 50 & ns & See Note 4 \\
\hline SP52 & \begin{tabular}{l}
TscH2ssH \\
TscL2ssH
\end{tabular} & \(\overline{\mathrm{SS} 2} \uparrow\) after SCK2 Edge & 1.5 TCY + 40 & - & - & ns & See Note 4 \\
\hline SP60 & TssL2doV & SDO2 Data Output Valid after SS2 Edge & - & - & 50 & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
3: The minimum clock period for SCK2 is 91 ns . Therefore, the SCK2 clock generated by the master must not violate this specification.
4: Assumes 50 pF load on all SPI2 pins.

FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE \(=0\), CKP \(=1\), SMP \(=0\) ) TIMING CHARACTERISTICS


TABLE 30-35: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = \(0, C K P=1, S M P=0\) ) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V (unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline SP70 & FscP & Maximum SCK2 Input Frequency & - & - & 15 & MHz & See Note 3 \\
\hline SP72 & TscF & SCK2 Input Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP73 & TscR & SCK2 Input Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP30 & TdoF & SDO2 Data Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP31 & TdoR & SDO2 Data Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP35 & TscH2doV, TscL2doV & SDO2 Data Output Valid after SCK2 Edge & - & 6 & 20 & ns & \\
\hline SP36 & TdoV2scH,
TdoV2scL & SDO2 Data Output Setup to First SCK2 Edge & 30 & - & - & ns & \\
\hline SP40 & TdiV2scH, TdiV2scL & Setup Time of SDI2 Data Input to SCK2 Edge & 30 & - & - & ns & \\
\hline SP41 & TscH2diL, TscL2diL & Hold Time of SDI2 Data Input to SCK2 Edge & 30 & - & - & ns & \\
\hline SP50 & TssL2scH, TssL2scL & \(\overline{\text { SS2 }} \downarrow\) to SCK2 \(\uparrow\) or SCK2 \(\downarrow\) Input & 120 & - & - & ns & \\
\hline SP51 & TssH2doZ & \(\overline{\mathrm{SS} 2} \uparrow\) to SDO2 Output High-Impedance & 10 & - & 50 & ns & See Note 4 \\
\hline SP52 & TscH2ssH TscL2ssH & \(\overline{\mathrm{SS} 2} \uparrow\) after SCK2 Edge & 1.5 TCY + 40 & - & - & ns & See Note 4 \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
3: The minimum clock period for SCK2 is 66.7 ns . Therefore, the SCK2 clock generated by the master must not violate this specification.
4: Assumes 50 pF load on all SPI2 pins.

FIGURE 30-19: SPI2 SLAVE MODE (FULL-DUPLEX, CKE \(=0\), CKP \(=0\), SMP \(=0\) ) TIMING CHARACTERISTICS


TABLE 30-36: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = \(0, \mathrm{CKP}=0, \mathrm{SMP}=0\) ) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V (unless otherwise stated) \\
Operating temperature \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline SP70 & FscP & Maximum SCK2 Input Frequency & - & - & 11 & MHz & See Note 3 \\
\hline SP72 & TscF & SCK2 Input Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP73 & TscR & SCK2 Input Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP30 & TdoF & SDO2 Data Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP31 & TdoR & SDO2 Data Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP35 & TscH2doV, TscL2doV & SDO2 Data Output Valid after SCK2 Edge & - & 6 & 20 & ns & \\
\hline SP36 & TdoV2scH, TdoV2scL & SDO2 Data Output Setup to First SCK2 Edge & 30 & - & - & ns & \\
\hline SP40 & TdiV2scH, TdiV2scL & Setup Time of SDI2 Data Input to SCK2 Edge & 30 & - & - & ns & \\
\hline SP41 & TscH2diL, TscL2diL & Hold Time of SDI2 Data Input to SCK2 Edge & 30 & - & - & ns & \\
\hline SP50 & TssL2scH, TssL2scL & \(\overline{\text { SS2 } \downarrow \text { to SCK2 } \uparrow \text { or SCK2 } \downarrow ~}\) Input & 120 & - & - & ns & \\
\hline SP51 & TssH2doZ & \(\overline{\mathrm{SS} 2} \uparrow\) to SDO2 Output High-Impedance & 10 & - & 50 & ns & See Note 4 \\
\hline SP52 & \begin{tabular}{l}
TscH2ssH \\
TscL2ssH
\end{tabular} & \(\overline{\mathrm{SS} 2} \uparrow\) after SCK2 Edge & 1.5 TCY + 40 & - & - & ns & See Note 4 \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
3: The minimum clock period for SCK2 is 91 ns . Therefore, the SCK2 clock generated by the master must not violate this specification.
4: Assumes 50 pF load on all SP12 pins.

TABLE 30-37: SPI1 MAXIMUM DATA/CLOCK RATE SUMMARY
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{4}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5 V to 5.5 V \\
(unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Maximum Data Rate & Master Transmit Only (Half-Duplex) & Master Transmit/Receive (Full-Duplex) & Slave Transmit/Receive (Full-Duplex) & CKE & CKP & SMP \\
\hline 25 MHz & Table 30-38 & - & - & 0,1 & 0,1 & 0,1 \\
\hline 25 MHz & - & Table 30-39 & - & 1 & 0,1 & 1 \\
\hline 25 MHz & - & Table 30-40 & - & 0 & 0,1 & 1 \\
\hline 25 MHz & - & - & Table 30-41 & 1 & 0 & 0 \\
\hline 25 MHz & - & - & Table 30-42 & 1 & 1 & 0 \\
\hline 25 MHz & - & - & Table 30-43 & 0 & 1 & 0 \\
\hline 25 MHz & - & - & Table 30-44 & 0 & 0 & 0 \\
\hline
\end{tabular}

FIGURE 30-20: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS


FIGURE 30-21: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS


Note: Refer to Figure 30-1 for load conditions.

TABLE 30-38: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline SP10 & FscP & Maximum SCK1 Frequency & - & - & 25 & MHz & See Note 3 \\
\hline SP20 & TscF & SCK1 Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP21 & TscR & SCK1 Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP30 & TdoF & SDO1 Data Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP31 & TdoR & SDO1 Data Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP35 & \begin{tabular}{l}
TscH2doV, \\
TscL2doV
\end{tabular} & SDO1 Data Output Valid after SCK1 Edge & - & 6 & 20 & ns & \\
\hline SP36 & TdiV2scH, TdiV2scL & SDO1 Data Output Setup to First SCK1 Edge & 20 & - & - & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.
4: Assumes 50 pF load on all SPI1 pins.

FIGURE 30-22: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = \(x\), SMP = 1) TIMING CHARACTERISTICS


TABLE 30-39: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP \(=\mathrm{x}, \mathrm{SMP}=1\) ) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5 V to 5.5 V (unless otherwise stated) \\
Operating temperature \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline SP10 & FscP & Maximum SCK1 Frequency & - & - & 25 & MHz & See Note 3 \\
\hline SP20 & TscF & SCK1 Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP21 & TscR & SCK1 Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP30 & TdoF & SDO1 Data Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP31 & TdoR & SDO1 Data Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP35 & TscH2doV, TscL2doV & SDO1 Data Output Valid after SCK1 Edge & - & 6 & 20 & ns & \\
\hline SP36 & TdoV2sc, TdoV2scL & SDO1 Data Output Setup to First SCK1 Edge & 20 & - & - & ns & \\
\hline SP40 & TdiV2sch, TdiV2scL & Setup Time of SDI1 Data Input to SCK1 Edge & 20 & - & - & ns & \\
\hline SP41 & TscH2diL, TscL2diL & Hold Time of SDI1 Data Input to SCK1 Edge & 15 & - & - & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
3: The minimum clock period for SCK1 is 100 ns . The clock generated in Master mode must not violate this specification.
4: Assumes 50 pF load on all SPI1 pins.

FIGURE 30-23: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = \(x\), SMP = 1) TIMING CHARACTERISTICS


Note: Refer to Figure 30-1 for load conditions.

TABLE 30-40: SPI1 MASTER MODE (FULL-DUPLEX, CKE = \(0, \mathrm{CKP}=\mathrm{x}, \mathrm{SMP}=1\) ) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5V \\
(unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline SP10 & FscP & Maximum SCK1 Frequency & - & - & 25 & MHz & \(-40^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) and see Note 3 \\
\hline SP20 & TscF & SCK1 Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP21 & TscR & SCK1 Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP30 & TdoF & SDO1 Data Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP31 & TdoR & SDO1 Data Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP35 & TscH2doV, TscL2doV & SDO1 Data Output Valid after SCK1 Edge & - & 6 & 20 & ns & \\
\hline SP36 & TdoV2scH, TdoV2scL & SDO1 Data Output Setup to First SCK1 Edge & 20 & - & - & ns & \\
\hline SP40 & TdiV2scH, TdiV2scL & Setup Time of SDI1 Data Input to SCK1 Edge & 20 & - & - & ns & \\
\hline SP41 & TscH2diL, TscL2diL & Hold Time of SDI1 Data Input to SCK1 Edge & 20 & - & - & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
3: The minimum clock period for SCK1 is 100 ns. The clock generated in Master mode must not violate this specification.
4: Assumes 50 pF load on all SPI1 pins.

FIGURE 30-24: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS


TABLE 30-41: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = \(1, \mathrm{CKP}=0, \mathrm{SMP}=0\) ) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\[
\begin{aligned}
& \text { Standard Operating Conditions: } 4.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \\
& \text { (unless otherwise stated) } \\
& \text { Operating temperature }-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C} \text { for Industrial } \\
& \qquad-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C} \text { for Extended }
\end{aligned}
\]} \\
\hline Param. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline SP70 & FscP & Maximum SCK1 Input Frequency & - & - & 25 & MHz & See Note 3 \\
\hline SP72 & TscF & SCK1 Input Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP73 & TscR & SCK1 Input Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP30 & TdoF & SDO1 Data Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP31 & TdoR & SDO1 Data Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP35 & TscH2doV, TscL2doV & SDO1 Data Output Valid after SCK1 Edge & - & 6 & 20 & ns & \\
\hline SP36 & TdoV2scH, TdoV2scL & SDO1 Data Output Setup to First SCK1 Edge & 20 & - & - & ns & \\
\hline SP40 & TdiV2scH, TdiV2scL & Setup Time of SDIx Data Input to SCK1 Edge & 20 & - & - & ns & \\
\hline SP41 & TscH2diL, TscL2diL & Hold Time of SDI1 Data Input to SCK1 Edge & 15 & - & - & ns & \\
\hline SP50 & TssL2scH, TssL2scL & \(\overline{\text { SS1 }} \downarrow\) to SCK1 \(\uparrow\) or SCK1 \(\downarrow\) Input & 120 & - & - & ns & \\
\hline SP51 & TssH2doZ & \(\overline{\mathrm{SS1}} \uparrow\) to SDO1 Output High-Impedance & 10 & - & 50 & ns & See Note 4 \\
\hline SP52 & TscH2ssH TscL2ssH & \(\overline{\text { SS1 }} \uparrow\) after SCK1 Edge & 1.5 TCY + 40 & - & - & ns & See Note 4 \\
\hline SP60 & TssL2doV & SDO1 Data Output Valid after SS1 Edge & - & - & 50 & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
3: The minimum clock period for SCK1 is 66.7 ns . Therefore, the SCK1 clock generated by the master must not violate this specification.
4: Assumes 50 pF load on all SPI1 pins.

FIGURE 30-25: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS


Note: Refer to Figure 30-1 for load conditions.

TABLE 30-42: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = \(1, \mathrm{CKP}=1, \mathrm{SMP}=0\) ) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\[
\begin{aligned}
& \text { Standard Operating Conditions: } 4.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \\
& \text { (unless otherwise stated) } \\
& \text { Operating temperature }-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C} \text { for Industrial } \\
& \qquad-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C} \text { for Extended }
\end{aligned}
\]} \\
\hline Param. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline SP70 & FscP & Maximum SCK1 Input Frequency & - & - & 25 & MHz & See Note 3 \\
\hline SP72 & TscF & SCK1 Input Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP73 & TscR & SCK1 Input Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP30 & TdoF & SDO1 Data Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP31 & TdoR & SDO1 Data Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP35 & TscH2doV, TscL2doV & SDO1 Data Output Valid after SCK1 Edge & - & 6 & 20 & ns & \\
\hline SP36 & TdoV2scH, TdoV2scL & SDO1 Data Output Setup to First SCK1 Edge & 20 & - & - & ns & \\
\hline SP40 & TdiV2scH, TdiV2scL & Setup Time of SDI1 Data Input to SCK1 Edge & 20 & - & - & ns & \\
\hline SP41 & TscH2diL, TscL2diL & Hold Time of SDI1 Data Input to SCK1 Edge & 15 & - & - & ns & \\
\hline SP50 & TssL2scH, TssL2scL & \(\overline{\text { SS1 }} \downarrow\) to SCK1 \(\uparrow\) or SCK1 \(\downarrow\) Input & 120 & - & - & ns & \\
\hline SP51 & TssH2doZ & \(\overline{\mathrm{SS1}} \uparrow\) to SDO1 Output High-Impedance & 10 & - & 50 & ns & See Note 4 \\
\hline SP52 & TscH2ssH, TscL2ssH & \(\overline{\text { SS1 }} \uparrow\) after SCK1 Edge & 1.5 TCY + 40 & - & - & ns & See Note 4 \\
\hline SP60 & TssL2doV & SDO1 Data Output Valid after SS1 Edge & - & - & 50 & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.
4: Assumes 50 pF load on all SPI1 pins.

FIGURE 30-26: SPI1 SLAVE MODE (FULL-DUPLEX, CKE =0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS


TABLE 30-43: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = \(0, \mathrm{CKP}=1, \mathrm{SMP}=0\) ) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\[
\begin{aligned}
& \text { Standard Operating Conditions: } 4.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \\
& \text { (unless otherwise stated) } \\
& \text { Operating temperature }-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C} \text { for Industrial } \\
& \\
& \\
& \hline-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C} \text { for Extended }
\end{aligned}
\]} \\
\hline Param. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline SP70 & FscP & Maximum SCK1 Input Frequency & - & - & 25 & MHz & See Note 3 \\
\hline SP72 & TscF & SCK1 Input Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP73 & TscR & SCK1 Input Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP30 & TdoF & SDO1 Data Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP31 & TdoR & SDO1 Data Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP35 & TscH2doV, TscL2doV & SDO1 Data Output Valid after SCK1 Edge & - & 6 & 20 & ns & \\
\hline SP36 & TdoV2scH, TdoV2scL & SDO1 Data Output Setup to First SCK1 Edge & 20 & - & - & ns & \\
\hline SP40 & TdiV2sch, TdiV2scL & Setup Time of SDI1 Data Input to SCK1 Edge & 20 & - & - & ns & \\
\hline SP41 & TscH2diL, TscL2diL & Hold Time of SDI1 Data Input to SCK1 Edge & 15 & - & - & ns & \\
\hline SP50 & TssL2scH, TssL2scL & \(\overline{\mathrm{SS} 1} \downarrow\) to SCK1 \(\uparrow\) or SCK1 \(\downarrow\) Input & 120 & - & - & ns & \\
\hline SP51 & TssH2doZ & \(\overline{\mathrm{SS1}} \uparrow\) to SDO1 Output High-Impedance & 10 & - & 50 & ns & See Note 4 \\
\hline SP52 & TscH2ssH, TscL2ssH & \(\overline{\mathrm{SS} 1} \uparrow\) after SCK1 Edge & 1.5 TCY + 40 & - & - & ns & See Note 4 \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
3: The minimum clock period for SCK1 is 66.7 ns . Therefore, the SCK1 clock generated by the master must not violate this specification.
4: Assumes 50 pF load on all SPI1 pins.

FIGURE 30-27: SPI1 SLAVE MODE (FULL-DUPLEX, CKE =0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS


Note: Refer to Figure 30-1 for load conditions.

TABLE 30-44: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = \(0, \mathrm{CKP}=0, \mathrm{SMP}=0\) ) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V \\
(unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline SP70 & FscP & Maximum SCK1 Input Frequency & - & - & 25 & MHz & See Note 3 \\
\hline SP72 & TscF & SCK1 Input Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP73 & TscR & SCK1 Input Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP30 & TdoF & SDO1 Data Output Fall Time & - & - & - & ns & See Parameter DO32 and Note 4 \\
\hline SP31 & TdoR & SDO1 Data Output Rise Time & - & - & - & ns & See Parameter DO31 and Note 4 \\
\hline SP35 & TscH2doV, TscL2doV & SDO1 Data Output Valid after SCK1 Edge & - & 6 & 20 & ns & \\
\hline SP36 & TdoV2scH, TdoV2scL & SDO1 Data Output Setup to First SCK1 Edge & 20 & - & - & ns & \\
\hline SP40 & TdiV2sch, TdiV2scL & Setup Time of SDI1 Data Input to SCK1 Edge & 20 & - & - & ns & \\
\hline SP41 & TscH2diL, TscL2diL & Hold Time of SDI1 Data Input to SCK1 Edge & 15 & - & - & ns & \\
\hline SP50 & TssL2scH, TssL2scL & \(\overline{\mathrm{SS} 1} \downarrow\) to SCK1 \(\uparrow\) or SCK1 \(\downarrow\) Input & 120 & - & - & ns & \\
\hline SP51 & TssH2doZ & \(\overline{\mathrm{SS1}} \uparrow\) to SDO1 Output High-Impedance & 10 & - & 50 & ns & See Note 4 \\
\hline SP52 & TscH2ssH, TscL2ssH & \(\overline{\text { SS1 }} \uparrow\) after SCK1 Edge & 1.5 TCY + 40 & - & - & ns & See Note 4 \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.
4: Assumes 50 pF load on all SPI1 pins.

FIGURE 30-28: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)


Note: Refer to Figure 30-1 for load conditions.

FIGURE 30-29: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)


Note: Refer to Figure 30-1 for load conditions.

TABLE 30-45: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{4}{|l|}{AC CHARACTERISTICS} & \multicolumn{4}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V \\
(unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param No. & Symbol & \multicolumn{2}{|l|}{Characteristic \({ }^{(4)}\)} & Min. \({ }^{(1)}\) & Max. & Units & Conditions \\
\hline \multirow[t]{3}{*}{IM10} & \multirow[t]{3}{*}{TLO:SCL} & \multirow[t]{3}{*}{Clock Low Time} & 100 kHz mode & TCY/2 (BRG + 2) & - & \(\mu \mathrm{S}\) & \\
\hline & & & 400 kHz mode & TCY/2 (BRG + 2) & - & \(\mu \mathrm{s}\) & \\
\hline & & & 1 MHz mode \({ }^{(2)}\) & TCY/2 (BRG + 2) & - & \(\mu \mathrm{S}\) & \\
\hline \multirow[t]{3}{*}{IM11} & \multirow[t]{3}{*}{THI:SCL} & \multirow[t]{3}{*}{Clock High Time} & 100 kHz mode & TCY/2 (BRG + 2) & - & \(\mu \mathrm{s}\) & \\
\hline & & & 400 kHz mode & TCY/2 (BRG + 2) & - & \(\mu \mathrm{S}\) & \\
\hline & & & 1 MHz mode \(^{(2)}\) & TCY/2 (BRG + 2) & - & \(\mu \mathrm{S}\) & \\
\hline \multirow[t]{3}{*}{IM20} & \multirow[t]{3}{*}{TF:SCL} & \multirow[t]{3}{*}{\begin{tabular}{l}
SDAx and SCLx \\
Fall Time
\end{tabular}} & 100 kHz mode & - & 300 & ns & \multirow[t]{3}{*}{CB is specified to be from 10 to 400 pF} \\
\hline & & & 400 kHz mode & \(20+0.1 \mathrm{CB}\) & 300 & ns & \\
\hline & & & 1 MHz mode \({ }^{(2)}\) & - & 100 & ns & \\
\hline \multirow[t]{3}{*}{IM21} & \multirow[t]{3}{*}{TR:SCL} & \multirow[t]{3}{*}{SDAx and SCLx Rise Time} & 100 kHz mode & - & 1000 & ns & \multirow[t]{3}{*}{CB is specified to be from 10 to 400 pF} \\
\hline & & & 400 kHz mode & \(20+0.1\) Cв & 300 & ns & \\
\hline & & & 1 MHz mode \(^{(2)}\) & - & 300 & ns & \\
\hline \multirow[t]{3}{*}{IM25} & \multirow[t]{3}{*}{Tsu:DAT} & \multirow[t]{3}{*}{Data Input Setup Time} & 100 kHz mode & 250 & - & ns & \\
\hline & & & 400 kHz mode & 100 & - & ns & \\
\hline & & & 1 MHz mode \({ }^{(2)}\) & 40 & - & ns & \\
\hline \multirow[t]{3}{*}{IM26} & \multirow[t]{3}{*}{THD:DAT} & \multirow[t]{3}{*}{Data Input Hold Time} & 100 kHz mode & 0 & - & \(\mu \mathrm{S}\) & \\
\hline & & & 400 kHz mode & 0 & 0.9 & \(\mu \mathrm{S}\) & \\
\hline & & & 1 MHz mode \(^{(2)}\) & 0.2 & - & \(\mu \mathrm{S}\) & \\
\hline \multirow[t]{3}{*}{IM30} & \multirow[t]{3}{*}{Tsu:STA} & \multirow[t]{3}{*}{Start Condition Setup Time} & 100 kHz mode & TCY/2 (BRG + 2) & - & \(\mu \mathrm{S}\) & \multirow[t]{3}{*}{Only relevant for Repeated Start condition} \\
\hline & & & 400 kHz mode & TCY/2 (BRG + 2) & - & \(\mu \mathrm{S}\) & \\
\hline & & & 1 MHz mode \({ }^{(2)}\) & TCY/2 (BRG + 2) & - & \(\mu \mathrm{S}\) & \\
\hline \multirow[t]{3}{*}{IM31} & \multirow[t]{3}{*}{THD:STA} & \multirow[t]{3}{*}{Start Condition Hold Time} & 100 kHz mode & TCY/2 (BRG + 2) & - & \(\mu \mathrm{S}\) & \multirow[t]{3}{*}{After this period, the first clock pulse is generated} \\
\hline & & & 400 kHz mode & TCY/2 (BRG +2) & - & \(\mu \mathrm{S}\) & \\
\hline & & & 1 MHz mode \({ }^{(2)}\) & TCY/2 (BRG + 2) & - & \(\mu \mathrm{S}\) & \\
\hline \multirow[t]{3}{*}{IM33} & \multirow[t]{3}{*}{Tsu:sto} & \multirow[t]{3}{*}{Stop Condition Setup Time} & 100 kHz mode & TCY/2 (BRG + 2) & - & \(\mu \mathrm{S}\) & \\
\hline & & & 400 kHz mode & TCY/2 (BRG + 2) & - & \(\mu \mathrm{S}\) & \\
\hline & & & 1 MHz mode \({ }^{(2)}\) & TCY/2 (BRG + 2) & - & \(\mu \mathrm{S}\) & \\
\hline \multirow[t]{3}{*}{IM34} & \multirow[t]{3}{*}{THD:STO} & \multirow[t]{3}{*}{Stop Condition Hold Time} & 100 kHz mode & TCY/2 (BRG + 2) & - & \(\mu \mathrm{S}\) & \\
\hline & & & 400 kHz mode & TCY/2 (BRG + 2) & - & \(\mu \mathrm{S}\) & \\
\hline & & & \(1 \mathrm{MHz} \mathrm{mode}{ }^{(2)}\) & TCY/2 (BRG + 2) & - & \(\mu \mathrm{S}\) & \\
\hline \multirow[t]{3}{*}{IM40} & \multirow[t]{3}{*}{TAA:SCL} & \multirow[t]{3}{*}{Output Valid From Clock} & 100 kHz mode & - & 3500 & ns & \\
\hline & & & 400 kHz mode & - & 1000 & ns & \\
\hline & & & \(1 \mathrm{MHz} \mathrm{mode}{ }^{(2)}\) & - & 400 & ns & \\
\hline \multirow[t]{3}{*}{IM45} & \multirow[t]{3}{*}{TbF:SDA} & \multirow[t]{3}{*}{Bus Free Time} & 100 kHz mode & 4.7 & - & \(\mu \mathrm{S}\) & \multirow[t]{3}{*}{Time the bus must be free before a new transmission can start} \\
\hline & & & 400 kHz mode & 1.3 & - & \(\mu \mathrm{S}\) & \\
\hline & & & \(1 \mathrm{MHz} \mathrm{mode}{ }^{(2)}\) & 0.5 & - & \(\mu \mathrm{S}\) & \\
\hline IM50 & Св & \multicolumn{2}{|l|}{Bus Capacitive Loading} & - & 400 & pF & \\
\hline IM51 & TPGD & \multicolumn{2}{|l|}{Pulse Gobbler Delay} & 65 & 390 & ns & See Note 3 \\
\hline
\end{tabular}

Note 1: \(\quad \mathrm{BRG}\) is the value of the \(\mathrm{I}^{2} \mathrm{C}^{\mathrm{TM}}\) Baud Rate Generator. Refer to "Inter-Integrated Circuit \({ }^{\mathrm{TM}}\left(\mathrm{I}^{2} \mathrm{C}^{\mathrm{TM}}\right)^{\prime \prime}\) (DS70000195) in the "dsPIC33/PIC24 Family Reference Manual". Please see the Microchip web site for the latest "dsPIC33/PIC24 Family Reference Manual" sections.
2: \(\quad\) Maximum pin capacitance \(=10 \mathrm{pF}\) for all I2Cx pins (for 1 MHz mode only).
3: Typical value for this parameter is 130 ns .
4: These parameters are characterized, but are not tested in manufacturing.

FIGURE 30-30: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)


FIGURE 30-31: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)


TABLE 30-46: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{4}{|l|}{AC CHARACTERISTICS} & \multicolumn{4}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5V \\
(unless otherwise stated) \\
\(\begin{array}{ll}\text { Operating temperature } & -40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C} \text { for Industrial } \\ & -40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C} \text { for Extended }\end{array}\)
\end{tabular}} \\
\hline Param. No. & Symbol & \multicolumn{2}{|r|}{Characteristic \({ }^{(3)}\)} & Min. & Max. & Units & Conditions \\
\hline \multirow[t]{3}{*}{IS10} & \multirow[t]{3}{*}{TLO:SCL} & \multirow[t]{3}{*}{Clock Low Time} & 100 kHz mode & 4.7 & - & \(\mu \mathrm{S}\) & \\
\hline & & & 400 kHz mode & 1.3 & - & \(\mu \mathrm{S}\) & \\
\hline & & & 1 MHz mode \(^{(1)}\) & 0.5 & - & \(\mu \mathrm{S}\) & \\
\hline \multirow[t]{3}{*}{IS11} & \multirow[t]{3}{*}{THI:SCL} & \multirow[t]{3}{*}{Clock High Time} & 100 kHz mode & 4.0 & - & \(\mu \mathrm{S}\) & Device must operate at a minimum of 1.5 MHz \\
\hline & & & 400 kHz mode & 0.6 & - & \(\mu \mathrm{S}\) & Device must operate at a minimum of 10 MHz \\
\hline & & & 1 MHz mode \({ }^{(1)}\) & 0.5 & - & \(\mu \mathrm{S}\) & \\
\hline \multirow[t]{3}{*}{IS20} & \multirow[t]{3}{*}{TF:SCL} & \multirow[t]{3}{*}{SDAx and SCLx Fall Time} & 100 kHz mode & - & 300 & ns & \multirow[t]{3}{*}{CB is specified to be from 10 to 400 pF} \\
\hline & & & 400 kHz mode & \(20+0.1\) Св & 300 & ns & \\
\hline & & & \(1 \mathrm{MHz} \mathrm{mode}{ }^{(1)}\) & - & 100 & ns & \\
\hline \multirow[t]{3}{*}{IS21} & \multirow[t]{3}{*}{TR:SCL} & \multirow[t]{3}{*}{SDAx and SCLx Rise Time} & 100 kHz mode & - & 1000 & ns & \multirow[t]{3}{*}{CB is specified to be from 10 to 400 pF} \\
\hline & & & 400 kHz mode & \(20+0.1\) Св & 300 & ns & \\
\hline & & & 1 MHz mode \(^{(1)}\) & - & 300 & ns & \\
\hline \multirow[t]{3}{*}{IS25} & \multirow[t]{3}{*}{Tsu:DAT} & \multirow[t]{3}{*}{Data Input Setup Time} & 100 kHz mode & 250 & - & ns & \\
\hline & & & 400 kHz mode & 100 & - & ns & \\
\hline & & & 1 MHz mode \(^{(1)}\) & 100 & - & ns & \\
\hline \multirow[t]{3}{*}{IS26} & \multirow[t]{3}{*}{THD:DAT} & \multirow[t]{3}{*}{Data Input Hold Time} & 100 kHz mode & 0 & - & \(\mu \mathrm{s}\) & \\
\hline & & & 400 kHz mode & 0 & 0.9 & \(\mu \mathrm{S}\) & \\
\hline & & & 1 MHz mode \({ }^{(1)}\) & 0 & 0.3 & \(\mu \mathrm{S}\) & \\
\hline \multirow[t]{3}{*}{IS30} & \multirow[t]{3}{*}{Tsu:StA} & \multirow[t]{3}{*}{Start Condition Setup Time} & 100 kHz mode & 4.7 & - & \(\mu \mathrm{S}\) & \multirow[t]{3}{*}{Only relevant for Repeated Start condition} \\
\hline & & & 400 kHz mode & 0.6 & - & \(\mu \mathrm{S}\) & \\
\hline & & & 1 MHz mode \({ }^{(1)}\) & 0.25 & - & \(\mu \mathrm{S}\) & \\
\hline \multirow[t]{3}{*}{IS31} & \multirow[t]{3}{*}{THD:STA} & \multirow[t]{3}{*}{Start Condition Hold Time} & 100 kHz mode & 4.0 & - & \(\mu \mathrm{S}\) & \multirow[t]{3}{*}{After this period, the first clock pulse is generated} \\
\hline & & & 400 kHz mode & 0.6 & - & \(\mu \mathrm{S}\) & \\
\hline & & & 1 MHz mode \({ }^{(1)}\) & 0.25 & - & \(\mu \mathrm{S}\) & \\
\hline \multirow[t]{3}{*}{IS33} & \multirow[t]{3}{*}{Tsu:sto} & \multirow[t]{3}{*}{Stop Condition Setup Time} & 100 kHz mode & 4.7 & - & \(\mu \mathrm{s}\) & \\
\hline & & & 400 kHz mode & 0.6 & - & \(\mu \mathrm{s}\) & \\
\hline & & & 1 MHz mode \({ }^{(1)}\) & 0.6 & - & \(\mu \mathrm{S}\) & \\
\hline \multirow[t]{3}{*}{IS34} & \multirow[t]{3}{*}{Thd:sto} & \multirow[t]{3}{*}{Stop Condition Hold Time} & 100 kHz mode & 4 & - & \(\mu \mathrm{S}\) & \\
\hline & & & 400 kHz mode & 0.6 & - & \(\mu \mathrm{S}\) & \\
\hline & & & 1 MHz mode \({ }^{(1)}\) & 0.25 & & \(\mu \mathrm{S}\) & \\
\hline \multirow[t]{3}{*}{IS40} & \multirow[t]{3}{*}{TAA:SCL} & \multirow[t]{3}{*}{Output Valid From Clock} & 100 kHz mode & 0 & 3500 & ns & \\
\hline & & & 400 kHz mode & 0 & 1000 & ns & \\
\hline & & & \(1 \mathrm{MHz} \mathrm{mode}{ }^{(1)}\) & 0 & 350 & ns & \\
\hline \multirow[t]{3}{*}{IS45} & \multirow[t]{3}{*}{TbF:SDA} & \multirow[t]{3}{*}{Bus Free Time} & 100 kHz mode & 4.7 & - & \(\mu \mathrm{S}\) & \multirow[t]{3}{*}{Time the bus must be free before a new transmission can start} \\
\hline & & & 400 kHz mode & 1.3 & - & \(\mu \mathrm{S}\) & \\
\hline & & & \(1 \mathrm{MHz} \mathrm{mode}{ }^{(1)}\) & 0.5 & - & \(\mu \mathrm{S}\) & \\
\hline IS50 & Св & \multicolumn{2}{|l|}{Bus Capacitive Loading} & - & 400 & pF & \\
\hline IS51 & TPGD & \multicolumn{2}{|l|}{Pulse Gobbler Delay} & 65 & 390 & ns & See Note 2 \\
\hline
\end{tabular}

Note 1: Maximum pin capacitance \(=10 \mathrm{pF}\) for all I2Cx pins (for 1 MHz mode only).
2: The typical value for this parameter is 130 ns .
3: These parameters are characterized, but are not tested in manufacturing.

FIGURE 30-32: CANx MODULE I/O TIMING CHARACTERISTICS


TABLE 30-47: CANx MODULE I/O TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V \\
(unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline CA10 & TIOF & Port Output Fall Time & - & - & - & ns & See Parameter DO32 \\
\hline CA11 & TıOR & Port Output Rise Time & - & - & - & ns & See Parameter DO31 \\
\hline CA20 & TcWF & Pulse Width to Trigger CAN Wake-up Filter & 120 & - & - & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 30-33: UARTx MODULE I/O TIMING CHARACTERISTICS


TABLE 30-48: UARTx MODULE I/O TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5 V to 5.5 V (unless otherwise stated) \\
Operating temperature \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\)
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. \({ }^{(2)}\) & Max. & Units & Conditions \\
\hline UA10 & TuAbAUD & UARTx Baud Time & 66.67 & - & - & ns & \\
\hline UA11 & Fbaud & UARTx Baud Frequency & - & - & 15 & Mbps & \\
\hline UA20 & TCWF & Start Bit Pulse Width to Trigger UARTx Wake-up & 500 & - & - & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 30-49: OP AMP/COMPARATOR x SPECIFICATIONS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions (see Note 3): 4.5V to 5.5 V (unless otherwise stated) \\
Operating temperature \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic & Min. & Typ. \({ }^{(1)}\) & Max. & Units & Conditions \\
\hline \multicolumn{8}{|c|}{Comparator AC Characteristics} \\
\hline CM10 & TRESP & Response Time & - & 19 & 80 & ns & \(\mathrm{V}+\) input step of 100 mV , V- input held at VDD/2 \\
\hline CM11 & Tмс20V & Comparator Mode Change to Output Valid & - & - & 10 & \(\mu \mathrm{s}\) & \\
\hline \multicolumn{8}{|c|}{Comparator DC Characteristics} \\
\hline CM30 & VoffSET & Comparator Offset Voltage & -80 & \(\pm 60\) & 80 & mV & \\
\hline CM31 & VHYST & Input Hysteresis Voltage & - & 30 & - & mV & \\
\hline CM32 & TRISE/ TFALL & Comparator Output Rise/Fall Time & - & 20 & - & ns & 1 pF load capacitance on input \\
\hline CM33 & Vgain & Open-Loop Voltage Gain & - & 90 & - & db & \\
\hline CM34 & VICM & Input Common-Mode Voltage & AVss & - & AVDD & V & \\
\hline \multicolumn{8}{|c|}{Op Amp AC Characteristics} \\
\hline CM20 & SR & Slew Rate & - & 9 & - & V/ \(/ \mathrm{s}\) & 10 pF load \\
\hline CM21 & PM & Phase Margin & - & 35 & - & \({ }^{\circ} \mathrm{C}\) & \(\mathrm{G}=100 \mathrm{~V} / \mathrm{V}, 10 \mathrm{pF}\) load \\
\hline CM22 & Gm & Gain Margin & - & 20 & - & db & \(\mathrm{G}=100 \mathrm{~V} / \mathrm{V}, 10 \mathrm{pF}\) load \\
\hline CM23 & GBW & Gain Bandwidth & - & 10 & - & MHz & 10 pF load \\
\hline \multicolumn{8}{|c|}{Op Amp DC Characteristics} \\
\hline CM40 & VCMR & Common-Mode Input Voltage Range & AVss & - & AVDD & V & \\
\hline CM41 & CMRR & Common-Mode Rejection Ratio & - & 45 & - & db & \(\mathrm{Vcm}=\mathrm{AVDD} / 2\) \\
\hline CM42 & Voffset & Op Amp Offset Voltage & -50 & \(\pm 6\) & 50 & mV & \\
\hline CM43 & Vgain & Open-Loop Voltage Gain & - & 90 & - & db & \\
\hline CM44 & los & Input Offset Current & - & - & - & - & See pad leakage currents in Table 30-10 \\
\hline CM45 & IB & Input Bias Current & - & - & - & - & See pad leakage currents in Table 30-10 \\
\hline CM46 & Iout & Output Current & - & - & 420 & \(\mu \mathrm{A}\) & With minimum value of Rfeedback (CM48) \\
\hline CM48 & Rfeedback & Feedback Resistance Value & 8 & - & - & k \(\Omega\) & Note 2 \\
\hline CM49a & Vout & Output Voltage & AVss + 0.075 & - & AVDD - 0.075 & V & IOUT \(=420 \mu \mathrm{~A}\) \\
\hline
\end{tabular}

Note 1: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
2: Resistances can vary by \(\pm 10 \%\) between op amps.
3: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

TABLE 30-50: OP AMP/COMPARATOR x VOLTAGE REFERENCE SETTLING TIME SPECIFICATIONS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions (see Note 2): 4.5 V to 5.5 V (unless otherwise stated) \\
Operating temperature \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param. & Symbol & Characteristic & Min. & Typ. & Max. & Units & Conditions \\
\hline VRD310 & Tset & Settling Time & - & 1 & 10 & \(\mu \mathrm{S}\) & See Note 1 \\
\hline
\end{tabular}

Note 1: Settling time measured while CVRSS \(=1\) and the CVR<6:0> bits transition from ' 0000000 ' to ' 1111111 '.
2: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

TABLE 30-51: OP AMP/COMPARATOR x VOLTAGE REFERENCE SPECIFICATIONS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{5}{|l|}{\[
\begin{aligned}
& \hline \text { Standard Operating Conditions (see Note 1): } 4.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \\
& \text { (unless otherwise stated) } \\
& \text { Operating temperature }-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C} \text { for Industrial } \\
& \qquad-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C} \text { for Extended }
\end{aligned}
\]} \\
\hline Param No. & Symbol & Characteristics & Min. & Typ. & Max. & Units & Conditions \\
\hline VRD311 & CVRAA & Absolute Accuracy of Internal DAC Input to Comparators & - & \(\pm 25\) & - & mV & \(\mathrm{AVDD}=\mathrm{CVRSRC}=5.0 \mathrm{~V}\) \\
\hline VRD312 & CVRAA1 & Absolute Accuracy of CVrefxo Pins & - & - & +35/-65 & mV & \(\mathrm{AVDD}=\mathrm{CVRSRC}=5.0 \mathrm{~V}\) \\
\hline VRD313 & CVRSRC & Input Reference Voltage & 0 & - & AVDD + 0.3 & V & \\
\hline VRD314 & CVRout & Buffer Output Resistance & - & 1.5k & - & \(\Omega\) & \\
\hline VRD315 & CVcl & Permissible Capacitive Load (CVRefxo pins) & - & - & 25 & pF & \\
\hline VRD316 & IocvR & Permissible Current Output (CVrefxo pins) & - & - & 1 & mA & \\
\hline VRD317 & ION & Current Consumed when Module is Enabled & - & - & 500 & \(\mu \mathrm{A}\) & \(\mathrm{AVDD}=5.0 \mathrm{~V}\) \\
\hline VRD318 & IOFF & Current Consumed when Module is Disabled & - & - & 1 & nA & \(\mathrm{AVDD}=5.0 \mathrm{~V}\) \\
\hline
\end{tabular}

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

TABLE 30-52: CTMU CURRENT SOURCE SPECIFICATIONS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V \\
(unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. & Max. & Units & Conditions \\
\hline \multicolumn{8}{|c|}{CTMU Current Source} \\
\hline CTMUI1 & Iout1 & Base Range & - & 550 & - & nA & CTMUICON<9:8> \(=01\) \\
\hline CTMUI2 & IOUT2 & 10x Range & - & 5.5 & - & \(\mu \mathrm{A}\) & CTMUICON<9:8> \(=10\) \\
\hline CTMUI3 & IOUT3 & 100x Range & - & 55 & - & \(\mu \mathrm{A}\) & CTMUICON<9:8> = 11 \\
\hline CTMUI4 & Iout4 & 1000x Range & - & 550 & - & \(\mu \mathrm{A}\) & CTMUICON<9:8> \(=00\) \\
\hline \multirow[t]{3}{*}{CTMUFV1} & \multirow[t]{3}{*}{VF} & \multirow[t]{3}{*}{Temperature Diode Forward Voltage \({ }^{(1,2)}\)} & - & 0.525 & - & V & \[
\begin{aligned}
& \mathrm{T} \mathrm{~A}=+25^{\circ} \mathrm{C}, \\
& \text { CTMUICON }<9: 8>=01
\end{aligned}
\] \\
\hline & & & - & 0.585 & - & V & \[
\begin{aligned}
& \mathrm{TA}=+25^{\circ} \mathrm{C}, \\
& \text { CTMUICON }<9: 8>=10
\end{aligned}
\] \\
\hline & & & - & 0.645 & - & V & \[
\begin{aligned}
& \mathrm{TA}=+25^{\circ} \mathrm{C}, \\
& \text { CTMUICON }<9: 8>=11
\end{aligned}
\] \\
\hline \multirow[t]{3}{*}{CTMUFV2} & \multirow[t]{3}{*}{VFVR} & \multirow[t]{3}{*}{Temperature Diode Rate of Change \({ }^{(1,2)}\)} & - & -1.92 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) & CTMUICON<9.8> \(=01\) \\
\hline & & & - & -1.74 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) & CTMUICON<9:8> \(=10\) \\
\hline & & & - & -1.56 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) & CTMUICON<9:8> \(=11\) \\
\hline
\end{tabular}

Note 1: Nominal value at center point of current trim range (CTMUICON<15:10> \(=000000\) ).
2: Parameters are characterized, but are not tested in manufacturing. Measurements are taken with the following conditions:
- \(\mathrm{VREF}=\mathrm{AVDD}=5.0 \mathrm{~V}\)
- ADC configured for 10-bit mode
- ADC configured for conversion speed of 500 ksps
- All PMDx bits are cleared (PMDx \(=0\) )
- CPU executing
while(1) statement \{
NOP();
\}
- Device operating from the FRC with no PLL

TABLE 30-53: ADC MODULE SPECIFICATIONS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{|l} 
Standard Operating Conditions (see Note 1): 4.5 V to 5.5 V \\
(unless otherwise stated) \\
Operating temperature \(\quad-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\\
\(\qquad-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic & Min. & Typ. & Max. & Units & Conditions \\
\hline \multicolumn{8}{|c|}{Device Supply} \\
\hline AD01 & AVDD & Module VDD Supply & Greater of: VDD - 0.3 or Vbor & - & Lesser of: VDD +0.3 or 5.5 & V & \\
\hline AD02 & AVss & Module Vss Supply & Vss - 0.3 & - & Vss + 0.3 & V & \\
\hline \multicolumn{8}{|c|}{Reference Inputs} \\
\hline AD05 & VREFH & Reference Voltage High & 4.5 & - & 5.5 & V & \[
\begin{aligned}
& \text { VREFH }=\text { AVDD, } \\
& \text { VREFL }=A V S S=0
\end{aligned}
\] \\
\hline AD06 & VREFL & Reference Voltage Low & AVss & - & AVdd - Vbormin & V & See Note 1 \\
\hline AD06a & & & 0 & - & 0 & V & \[
\begin{aligned}
& \text { VREFH }=\text { AVDD, } \\
& \text { VREFL }=A V S S=0
\end{aligned}
\] \\
\hline AD07 & VREF & Absolute Reference Voltage & 4.5 & - & 5.5 & V & VREF = VREFH - Vrefl \\
\hline AD08 & IREF & Current Drain & - & - & \[
\begin{gathered}
\hline 10 \\
600
\end{gathered}
\] & \[
\mu \mathrm{A}
\]
\[
\mu \mathrm{A}
\] & ADC off ADC on \\
\hline AD09 & IAD & Operating Current & -
- & \[
5
\]
\[
2
\] & \[
\begin{aligned}
& - \\
& -
\end{aligned}
\] & \[
\begin{aligned}
& \mathrm{mA} \\
& \mathrm{~mA}
\end{aligned}
\] & ADC operating in 10-bit mode, see Note 1 ADC operating in 12-bit mode, see Note 1 \\
\hline \multicolumn{8}{|c|}{Analog Input} \\
\hline AD12 & VINH & Input Voltage Range VINH & VINL & - & VREFH & V & This voltage reflects Sample-and-Hold Channels 0, 1, 2 and 3 (CH0-CH3), positive input \\
\hline AD13 & VINL & Input Voltage Range VINL & VREFL & - & AVss + 1V & V & This voltage reflects Sample-and-Hold Channels 0, 1, 2 and 3 (CHO-CH3), negative input \\
\hline AD17 & RIN & Recommended Impedance of Analog Voltage Source & - & - & 200 & \(\Omega\) & Impedance to achieve maximum performance of ADC \\
\hline
\end{tabular}

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

TABLE 30-54: ADC MODULE SPECIFICATIONS (12-BIT MODE)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\[
\begin{aligned}
& \text { Standard Operating Conditions (see Note } 1 \text { ): } 4.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \\
& \text { (unless otherwise stated) } \\
& \text { Operating temperature }-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C} \text { for Industrial } \\
& \qquad-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C} \text { for Extended }
\end{aligned}
\]} \\
\hline Param No. & Symbol & Characteristic & Min. & Typ. & Max. & Units & Conditions \\
\hline \multicolumn{8}{|c|}{ADC Accuracy (12-Bit Mode)} \\
\hline AD20a & Nr & Resolution & & data b & & bits & \\
\hline AD21a & INL & Integral Nonlinearity & -2 & - & +2 & LSb & \[
\begin{aligned}
& \text { VINL = AVSS }=\text { VREFL }=0 \mathrm{~V}, \\
& \text { AVDD = VREFH }=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline AD22a & DNL & Differential Nonlinearity & >-1 & - & < 1 & LSb & \[
\begin{aligned}
& \text { VINL = AVSS = VREFL }=0 \mathrm{~V}, \\
& \text { AVDD }=\mathrm{VREFH}=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline AD23a & GERR & Gain Error & -10 & 4 & 10 & LSb & \[
\begin{aligned}
& \text { VINL }=\mathrm{AVSS}=\mathrm{VREFL}=0 \mathrm{~V}, \\
& \text { AVDD }=\mathrm{VREFH}=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline AD24a & EOFF & Offset Error & -10 & 1.75 & 10 & LSb & \[
\begin{aligned}
& \text { VINL }=\mathrm{AVSS}=\mathrm{VREFL}=0 \mathrm{~V}, \\
& \text { AVDD }=\mathrm{VREFH}=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline AD25a & - & Monotonicity \({ }^{(2)}\) & - & - & - & - & Guaranteed \\
\hline \multicolumn{8}{|c|}{Dynamic Performance (12-Bit Mode)} \\
\hline AD30a & THD & Total Harmonic Distortion & - & - & -75 & dB & \\
\hline AD31a & SINAD & Signal to Noise and Distortion & 68.5 & 69.5 & - & dB & \\
\hline AD32a & SFDR & Spurious Free Dynamic Range & 80 & - & - & dB & \\
\hline AD33a & FNYQ & Input Signal Bandwidth & - & - & 250 & kHz & \\
\hline AD34a & ENOB & Effective Number of Bits & 11.09 & 11.3 & - & bits & \\
\hline
\end{tabular}

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.
2: The conversion result never decreases with an increase in the input voltage.

TABLE 30-55: ADC MODULE SPECIFICATIONS (10-BIT MODE)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions (see Note 1): 4.5V to 5.5 V (unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic & Min. & Typ. & Max. & Units & Conditions \\
\hline \multicolumn{8}{|c|}{ADC Accuracy (10-Bit Mode)} \\
\hline AD20b & Nr & Resolution & & data & & bits & \\
\hline AD21b & INL & Integral Nonlinearity & -1.5 & - & +1.5 & LSb & \[
\begin{aligned}
& \text { VINL = AVSS }=\text { VREFL }=0 \mathrm{~V}, \\
& \text { AVDD = VREFH }=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline AD22b & DNL & Differential Nonlinearity & \(\geq 1\) & - & < 1 & LSb & \[
\begin{aligned}
& \text { VINL = AVSS }=\text { VREFL }=0 \mathrm{~V}, \\
& \text { AVDD }=\text { VREFH }=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline AD23b & GERR & Gain Error & 1 & 3 & 6 & LSb & \[
\begin{aligned}
& \text { VINL = AVSS }=\text { VREFL }=0 \mathrm{~V}, \\
& \text { AVDD }=\text { VREFH }=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline AD24b & EofF & Offset Error & 1 & 2 & 4 & LSb & \[
\begin{aligned}
& \text { VINL = AVss = VREFL = 0V, } \\
& \text { AVDD = VREFH }=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline AD25b & - & Monotonicity \({ }^{(2)}\) & - & - & - & - & Guaranteed \\
\hline \multicolumn{8}{|c|}{Dynamic Performance (10-Bit Mode)} \\
\hline AD30b & THD & Total Harmonic Distortion & - & - & -64 & dB & \\
\hline AD31b & SINAD & Signal to Noise and Distortion & 57 & 58.5 & - & dB & \\
\hline AD32b & SFDR & Spurious Free Dynamic Range & 72 & - & - & dB & \\
\hline AD33b & FNYQ & Input Signal Bandwidth & - & - & 550 & kHz & \\
\hline AD34b & ENOB & Effective Number of Bits & 9.16 & 9.4 & - & bits & \\
\hline
\end{tabular}

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.
2: The conversion result never decreases with an increase in the input voltage.

FIGURE 30-34: ADC CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS (ASAM \(=0, S S R C<2: 0>=000, S S R C G=0)\)


TABLE 30-56: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions (see Note 2): 4.5 V to 5.5 V (unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic & Min. & Typ. \({ }^{(4)}\) & Max. & Units & Conditions \\
\hline \multicolumn{8}{|c|}{Clock Parameters} \\
\hline AD50 & TAD & ADC Clock Period & 117.6 & - & - & ns & \\
\hline AD51 & trc & ADC Internal RC Oscillator Period & - & 250 & - & ns & \\
\hline \multicolumn{8}{|c|}{Conversion Rate} \\
\hline AD55 & tconv & Conversion Time & - & 14 & - & TAD & \\
\hline AD56 & FCNV & Throughput Rate & - & - & 500 & ksps & \\
\hline AD57a & Tsamp & Sample Time when Sampling Any ANx Input & 3 & - & - & TAD & \\
\hline AD57b & Tsamp & Sample Time when Sampling the Op Amp Outputs & 3 & - & - & TAD & \\
\hline \multicolumn{8}{|c|}{Timing Parameters} \\
\hline AD60 & tPCs & Conversion Start from Sample Trigger \({ }^{(1)}\) & 2 & - & 3 & TAD & Auto-convert trigger is not selected \\
\hline AD61 & tPSS & Sample Start from Setting Sample (SAMP) bit \({ }^{(1)}\) & 2 & - & 3 & TAD & \\
\hline AD62 & tcss & Conversion Completion to Sample Start (ASAM =1) \({ }^{(1)}\) & - & 0.5 & - & TAD & \\
\hline AD63 & tDPU & Time to Stabilize Analog Stage from ADC Off to ADC On \({ }^{(1)}\) & - & - & 20 & \(\mu \mathrm{s}\) & See Note 3 \\
\hline
\end{tabular}

Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.
2: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.
3: The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (ADxCON1<15>) = 1). During this time, the ADC result is indeterminate.
4: These parameters are characterized, but are not tested in manufacturing.

FIGURE 30-35: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS
(CHPS \(<1: 0>=01\), SIMSAM \(=0\), ASAM \(=0, S S R C<2: 0>=000, S S R C G=0\) )


FIGURE 30-36: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> \(=01\), SIMSAM \(=0\), ASAM \(=1\), SSRC \(<2: 0>=111\), SSRCG \(=0\), SAMC \(<4: 0>=00010\) )


TABLE 30-57: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions (see Note 1): 4.5V to 5.5 V (unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic & Min. & Typ. \({ }^{(4)}\) & Max. & Units & Conditions \\
\hline \multicolumn{8}{|c|}{Clock Parameters} \\
\hline AD50 & TAD & ADC Clock Period & 75 & - & - & ns & \\
\hline AD51 & tRC & ADC Internal RC Oscillator Period & - & 250 & - & ns & \\
\hline \multicolumn{8}{|c|}{Conversion Rate} \\
\hline AD55 & tconv & Conversion Time & - & 12 & - & TAD & \\
\hline AD56 & Fcnv & Throughput Rate & - & - & 1.1 & Msps & Using simultaneous sampling \\
\hline AD57a & Tsamp & Sample Time When Sampling Any ANx Input & 2 & - & - & TAD & \\
\hline AD57b & TSAMP & Sample Time When Sampling the Op Amp Outputs & 4 & - & - & TAD & \\
\hline \multicolumn{8}{|c|}{Timing Parameters} \\
\hline AD60 & tPCS & Conversion Start from Sample Trigger \({ }^{(2)}\) & 2 & - & 3 & TAD & Auto-convert trigger is not selected \\
\hline AD61 & tPSS & Sample Start from Setting Sample (SAMP) bit \({ }^{(2)}\) & 2 & - & 3 & TAD & \\
\hline AD62 & tcss & Conversion Completion to Sample Start (ASAM = 1) \({ }^{(\mathbf{2 )}}\) & - & 0.5 & - & TAD & \\
\hline AD63 & tDPU & Time to Stabilize Analog Stage from ADC Off to ADC On \({ }^{(2)}\) & - & - & 20 & \(\mu \mathrm{S}\) & See Note 3 \\
\hline
\end{tabular}

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.
2: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.
3: The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON \((A D x C O N 1<15>)=1)\). During this time, the ADC result is indeterminate.
4: These parameters are characterized, but are not tested in manufacturing.

TABLE 30-58: DMA MODULE TIMING REQUIREMENTS
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V (unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+85^{\circ} \mathrm{C}\) for Industrial \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+125^{\circ} \mathrm{C}\) for Extended
\end{tabular}} \\
\hline Param No. & Characteristic & Min. & Typ. \({ }^{(1)}\) & Max. & Units & Conditions \\
\hline DM1 & DMA Byte/Word Transfer Latency & \(1 \mathrm{TcY}^{(2)}\) & - & - & ns & \\
\hline
\end{tabular}

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Because DMA transfers use the CPU data bus, this time is dependent on other functions on the bus.

\section*{dsPIC33EVXXXGM00X/10X FAMILY}

NOTES:

\subsection*{31.0 HIGH-TEMPERATURE ELECTRICAL CHARACTERISTICS}

This section provides an overview of dsPIC33EVXXXGM00X/10X family electrical characteristics for devices operating in an ambient temperature range of \(-40^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\).
The specifications between \(-40^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) are identical to those shown in Section \(\mathbf{3 0 . 0}\) "Electrical Characteristics" for operation between \(-40^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\), with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter DC10 in Section 30.0 "Electrical Characteristics" is the Industrial and Extended temperature equivalent of HDC10.
Absolute maximum ratings for the dsPIC33EVXXXGM00X/10X Family high-temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.
Absolute Maximum Ratings \({ }^{(1)}\)
Ambient temperature under bias \({ }^{(2)}\) ..... \(-40^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
Storage temperature ..... \(-65^{\circ} \mathrm{C}\) to \(+160^{\circ} \mathrm{C}\)
Voltage on VdD with respect to Vss ..... -0.3 V to +6.0 V
Maximum current out of Vss pin ..... 350 mA
Maximum current into VDD pin \({ }^{(3)}\) ..... 350 mA
Maximum junction temperature ..... \(+155^{\circ} \mathrm{C}\)
Maximum current sunk by any I/O pin ..... 20 mA
Maximum current sourced by I/O pin ..... 18 mA
Maximum current sunk by all ports combined ..... 200 mA
Maximum current sourced by all ports combined \({ }^{(3)}\) ..... 200 mA

Note 1: Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.
2: AEC-Q100 reliability testing for devices intended to operate at \(+150^{\circ} \mathrm{C}\) is 1,000 hours. Any design in which the total operating time from \(+125^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.
3: Maximum allowable current is a function of device maximum power dissipation (see Table 31-2).

\subsection*{31.1 High-Temperature DC Characteristics}

TABLE 31-1: OPERATING MIPS VS. VOLTAGE
\begin{tabular}{|l|c|c|c|}
\hline \multirow{2}{*}{ Characteristic } & \begin{tabular}{c} 
Vod Range \\
(in Volts)
\end{tabular} & \multirow{2}{*}{\begin{tabular}{c} 
Temperature Range \\
(in \({ }^{\circ} \mathrm{C}\) )
\end{tabular}} & Max MIPS \\
\cline { 4 - 4 } & & dsPIC33EVXXXGM00X/10X Family \\
\hline \hline HDC5 & 4.5 V to \(5.5 \mathrm{~V}^{(1,2)}\) & \(-40^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) & 40 \\
\hline
\end{tabular}

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules, such as the ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Device functionality is tested but is not characterized. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.
2: When BOR is enabled, the device will work from 4.7 V to 5.5 V .

TABLE 31-2: THERMAL OPERATING CONDITIONS


TABLE 31-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{5}{|l|}{Standard Operating Conditions (see Note 3): 4.5V to 5.5V (unless otherwise stated) Operating temperature \(\quad-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\) for High Temperature} \\
\hline \begin{tabular}{l}
Param \\
No.
\end{tabular} & Symbol & Characteristic & Min. & Typ. \({ }^{(1)}\) & Max. & Units & Conditions \\
\hline \multicolumn{8}{|l|}{Operating Voltage} \\
\hline HDC10 & VDD & Supply Voltage \({ }^{(3)}\) & Vbor & - & 5.5 & V & \\
\hline HDC12 & VDR & RAM Data Retention Voltage \({ }^{(2)}\) & 1.8 & - & - & V & \\
\hline HDC16 & VPOR & Vdd Start Voltage to Ensure Internal Power-on Reset Signal & - & - & Vss & V & \\
\hline HDC17 & SVDD & Vdd Rise Rate to Ensure Internal Power-on Reset Signal & 1.0 & - & - & V/ms & 0V-5.0V in 5 ms \\
\hline HDC18 & VCore & Vdd Core Internal Regulator Voltage & 1.62 & 1.8 & 1.98 & V & Voltage is dependent on load, temperature and VDD \\
\hline
\end{tabular}

Note 1: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
2: This is the limit to which VDD may be lowered without losing RAM data.
3: VDD voltage must remain at Vss for a minimum of \(200 \mu\) s to ensure POR.

TABLE 31-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)
\begin{tabular}{|l|c|c|c|c|c|l|}
\hline \multicolumn{3}{|l|}{ DC CHARACTERISTICS } & \multicolumn{4}{|c|}{\begin{tabular}{l} 
Standard Operating Conditions: 4.5V to 5.5 V (unless otherwise stated) \\
Operating temperature \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\) for High Temperature
\end{tabular}} \\
\hline \begin{tabular}{c} 
Parameter \\
No.
\end{tabular} & Typical & Max & Units & & Conditions \\
\hline \hline Power-Down Current (IPD) \\
\hline HDC60e & 1300 & 2500 & \(\mu \mathrm{~A}\) & \(+150^{\circ} \mathrm{C}\) & 5 V & Base Power-Down Current \\
\hline HDC61c & 10 & 50 & \(\mu \mathrm{~A}\) & \(+150^{\circ} \mathrm{C}\) & 5 V & Watchdog Timer Current: \(\Delta\) IWDT \\
\hline
\end{tabular}

\section*{TABLE 31-5: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)}
\begin{tabular}{|l|c|c|c|c|c|c|}
\hline \multicolumn{2}{|l|}{ DC CHARACTERISTICS } & \multicolumn{4}{|c|}{\begin{tabular}{l} 
Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\) for High Temperature
\end{tabular}} \\
\hline \begin{tabular}{c} 
Parameter \\
No.
\end{tabular} & Typical & Max & Units & & \multicolumn{2}{c|}{ Conditions } \\
\hline \hline HDC40e & 2.6 & 5.0 & mA & \(+150^{\circ} \mathrm{C}\) & 5 V & 10 MIPS \\
\hline HDC42e & 3.6 & 7.0 & mA & \(+150^{\circ} \mathrm{C}\) & 5 V & 20 MIPS \\
\hline
\end{tabular}

TABLE 31-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)
\begin{tabular}{|l|c|c|c|c|c|c|}
\hline \multicolumn{2}{|c|}{ DC CHARACTERISTICS } & \multicolumn{3}{|c|}{\begin{tabular}{l} 
Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) \\
Operating temperature \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\) for High Temperature
\end{tabular}} \\
\hline \begin{tabular}{c} 
Parameter \\
No.
\end{tabular} & Typical & Max & Units & & \multicolumn{3}{c|}{ Conditions } \\
\hline \hline HDC20e & 5.9 & 8.0 & mA & \(+150^{\circ} \mathrm{C}\) & 5 V & 10 MIPS \\
\hline HDC22e & 10.3 & 15.0 & mA & \(+150^{\circ} \mathrm{C}\) & 5 V & 20 MIPS \\
\hline HDC23e & 19.0 & 25.0 & mA & \(+150^{\circ} \mathrm{C}\) & 5 V & 40 MIPS \\
\hline
\end{tabular}

TABLE 31-7: DC CHARACTERISTICS: DOZE CURRENT (IDoze)
\begin{tabular}{|l|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|c|}{ DC CHARACTERISTICS } & \multicolumn{3}{|c|}{\begin{tabular}{l} 
Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) \\
Operating temperature \\
\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\) for High Temperature
\end{tabular}} \\
\hline \begin{tabular}{c} 
Parameter \\
No.
\end{tabular} & Typical & Max & Doze Ratio & Units & & \multicolumn{2}{c|}{ Conditions } \\
\hline \hline HDC73a & 18.5 & 22.0 & \(1: 2\) & mA & \(+150^{\circ} \mathrm{C}\) & 5 V & 40 MIPS \\
\hline HDC73g & 8.35 & 12.0 & \(1: 128\) & mA & & 40 \\
\hline
\end{tabular}

\section*{TABLE 31-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS}
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5 V to 5.5 V \\
(unless otherwise stated) \\
Operating temperature \(\quad-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\) for High Temperature
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic & Min. & Typ. \({ }^{(1)}\) & Max. & Units & Conditions \\
\hline DI10 & VIL & Input Low Voltage Any I/O Pins & Vss & - & 0.2 VDD & V & \\
\hline DI20 & VIH & Input High Voltage I/O Pins & 0.75 VDD & - & 5.5 & V & \\
\hline DI30 & ICNPU & Change Notification Pull-up Current & 200 & 375 & 600 & \(\mu \mathrm{A}\) & \(\mathrm{VDD}=5.0 \mathrm{~V}, \mathrm{VPIN}=\mathrm{VsS}\) \\
\hline DI31 & ICNPD & Change Notification Pull-Down Current \({ }^{(7)}\) & 175 & 400 & 625 & \(\mu \mathrm{A}\) & \(\mathrm{VDD}=5.0 \mathrm{~V}, \mathrm{VPIN}=\mathrm{VDD}\) \\
\hline \[
\begin{array}{|l}
\text { DI50 } \\
\text { DI55 } \\
\text { DI56 }
\end{array}
\] & IIL & \begin{tabular}{l}
Input Leakage Current \({ }^{(2,3)}\) I/O Pins \\
\(\overline{\text { MCLR }}\) \\
OSC1
\end{tabular} & \[
\begin{aligned}
& -200 \\
& -1.5 \\
& -300
\end{aligned}
\] & \[
\begin{aligned}
& - \\
& - \\
& -
\end{aligned}
\] & \[
\begin{aligned}
& 200 \\
& \\
& 1.5 \\
& 300
\end{aligned}
\] & \begin{tabular}{l}
nA \\
\(\mu \mathrm{A}\) \\
nA
\end{tabular} & \begin{tabular}{l}
Vss \(\leq\) VPIN \(\leq\) VDD, Pin at high-impedance \\
VsS \(\leq\) VPIN \(\leq\) VDD \\
Vss \(\leq\) VPIN \(\leq\) VDD, \\
XT and HS modes
\end{tabular} \\
\hline DI60a & IICL & Input Low Injection Current & 0 & - & \(-5^{(4,6)}\) & mA & All pins except VdD, Vss, AVdd, AVss, MCLR, VcAP and RB7 \\
\hline DI60b & IICH & Input High Injection Current & 0 & - & \(+5^{(5,6)}\) & mA & All pins except VDD, Vss, AVDd, AVss, MCLR, VcAP, RB7 and all 5 V tolerant pins \({ }^{(5)}\) \\
\hline DI60c & \IICT & Total Input Injection Current (sum of all I/O and control pins) & \(-20^{(7)}\) & - & \(+20^{(7)}\) & mA & Absolute instantaneous sum of all \(\pm\) input injection currents from all I/O pins \(\left(|\mathrm{IICL}+|\mathrm{IICH}|) \leq \sum \mathrm{IICT}\right.\) \\
\hline
\end{tabular}

Note 1: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
2: The leakage current on the \(\overline{M C L R}\) pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
3: Negative current is defined as current sourced by the pin.
4: VIL source < (VSS - 0.3). Characterized but not tested.
5: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources \(>5.5 \mathrm{~V}\).
6: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
7: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted, provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

TABLE 31-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{5}{|l|}{Standard Operating Conditions: 4.5 V to 5.5 V (unless otherwise stated) Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\) for High Temperature} \\
\hline \[
\begin{gathered}
\text { Param } \\
\text { No. }
\end{gathered}
\] & Symbol & Characteristic & Min. \({ }^{(1)}\) & Typ. & Max. & Units & Conditions \\
\hline HDO16 & Vol & Output Low Voltage 4x Sink Driver Pins \({ }^{(2)}\) & - & - & 0.4 & V & \(\mathrm{IOL}=8.8 \mathrm{~mA}, \mathrm{VDD}=5.0 \mathrm{~V}\) \\
\hline HDO10 & Vol & Output Low Voltage 8x Sink Driver Pins \({ }^{(3)}\) & - & - & 0.4 & V & \(\mathrm{IOL}=10.8 \mathrm{~mA}, \mathrm{VDD}=5.0 \mathrm{~V}\) \\
\hline HDO26 & VOH & Output High Voltage \(4 x\) Sink Driver Pins \({ }^{(2)}\) & VDD - 0.6 & - & - & V & \(\mathrm{IOH}=-8.3 \mathrm{~mA}, \mathrm{VDD}=5.0 \mathrm{~V}\) \\
\hline HDO20 & VOH & Output High Voltage 8x Sink Driver Pins & VDD - 0.6 & - & - & V & \(\mathrm{IOH}=-12.3 \mathrm{~mA}, \mathrm{VDD}=5.0 \mathrm{~V}\) \\
\hline
\end{tabular}

Note 1: Parameters are characterized, but are not tested.
2: Includes all I/O pins that are not \(8 x\) sink driver pins (see below).
3: Includes the pins, such as RA3, RA4 and RB<15:10> for 28-pin devices, RA3, RA4, RA9 and RB<15:10> for 44-pin devices and RA4, RA7, RA9, RB<15:10> and RC15 for 64-pin devices.

TABLE 31-10: ELECTRICAL CHARACTERISTICS: BOR
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|c|}{ DC CHARACTERISTICS } & \multicolumn{4}{|c|}{\(\begin{array}{l}\text { Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) } \\
\text { Operating temperature }\end{array}\)} & \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\) for High Temperature
\end{tabular}\(]\)\begin{tabular}{c} 
Conditions
\end{tabular}

Note 1: Parameters are for design guidance only and are not tested in manufacturing.
2: The VBor specification is relative to the VdD.
3: The device is functional at VBORMIN < VDD < VDDmin. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Device functionality is tested but is not characterized.
4: The start-up VDD must rise above 4.6V.

TABLE 31-11: DC CHARACTERISTICS: PROGRAM MEMORY
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{5}{|l|}{Standard Operating Conditions: 4.5 V to 5.5 V (unless otherwise stated) Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\) for High Temperature} \\
\hline Param No. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. & Max. & Units & Conditions \\
\hline \[
\begin{aligned}
& \text { HD130 } \\
& \text { HD134 }
\end{aligned}
\] & Ep
Tretd & \begin{tabular}{l}
Program Flash Memory \\
Cell Endurance Characteristic Retention
\end{tabular} & \[
\begin{gathered}
10,000 \\
20
\end{gathered}
\] & - & - & \[
\begin{aligned}
& \text { E/W } \\
& \text { Year }
\end{aligned}
\] & \begin{tabular}{l}
\[
-40^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C}^{(2)}
\] \\
1000 E/W cycles or less and no other specifications are violated
\end{tabular} \\
\hline
\end{tabular}

Note 1: These parameters are assured by design, but are not characterized or tested in manufacturing.
2: Programming of the Flash memory is allowed up to \(+150^{\circ} \mathrm{C}\).

\subsection*{31.2 AC Characteristics and Timing Parameters}

The information contained in this section defines the dsPIC33EVXXXGM00X/10X family AC characteristics and timing parameters for high-temperature devices. However, all AC timing specifications in this section are the same as those in Section 30.2 "AC Characteristics and Timing Parameters", with the exception of the parameters listed in this section.

Parameters in this section begin with an H , which denotes High temperature. For example, Parameter OS53 in Section 30.2 "AC Characteristics and Timing Parameters" is the Industrial and Extended temperature equivalent of HOS53.

TABLE 31-12: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC
\begin{tabular}{|l|l|}
\hline AC CHARACTERISTICS & \begin{tabular}{l} 
Standard Operating Conditions: 4.5 V to 5.5 V \\
(unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\) \\
Operating voltage VDD range as described in Table 31-1. \\
\hline
\end{tabular} \\
\hline
\end{tabular}

FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS
Load Condition 1 - for All Pins except OSC2 \(\quad\) Load Condition 2 - for OSC2

TABLE 31-13: PLL CLOCK TIMING SPECIFICATIONS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: 4.5V to 5.5 V (unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\)
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic & Min. & Typ. \({ }^{(1)}\) & Max. & Units & Conditions \\
\hline HOS50 & FPLLI & PLL Voltage Controlled Oscillator (VCO) Input Frequency Range & 0.8 & - & 8.0 & MHz & ECPLL, XTPLL modes \\
\hline HOS51 & Fsys & On-Chip VCO System Frequency & 120 & - & 340 & MHz & \\
\hline HOS52 & TLOCK & PLL Start-up Time (Lock Time) & 0.9 & 1.5 & 3.1 & ms & \\
\hline HOS53 & Dclk & CLKO Stability (Jitter) \({ }^{(2)}\) & -3 & 0.5 & 3 & \% & \\
\hline
\end{tabular}

Note 1: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated. Parameters are for design guidance only and are not tested.
2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases or communication clocks used by the application, use the following formula:
\[
\text { Effective Jitter }=\frac{\text { DCLK }}{\sqrt{\frac{\text { FOSC }}{\text { Time Base or Communication Clock }}}}
\]

For example, if Fosc \(=120 \mathrm{MHz}\) and the SPI bit rate \(=10 \mathrm{MHz}\), the effective jitter is as follows:
\[
\text { Effective Jitter }=\frac{D C L K}{\sqrt{\frac{120}{10}}}=\frac{D C L K}{\sqrt{12}}=\frac{D C L K}{3.464}
\]

TABLE 31-14: INTERNAL FRC ACCURACY
\begin{tabular}{|l|l|c|c|c|c|c|c|}
\hline \multicolumn{2}{|c|}{ AC CHARACTERISTICS } & \multicolumn{5}{|c|}{\begin{tabular}{l} 
Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) \\
Operating temperature \\
\hline \multicolumn{7}{|c|}{\(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\)}
\end{tabular}} \\
\hline \begin{tabular}{c} 
Param \\
No.
\end{tabular} & Characteristic & Min & Typ & Max & Units & Conditions \\
\hline \hline Internal FRC Accuracy @ FRC Frequency \(=7.3728 \mathrm{MHz}\) \\
\hline HF20C & FRC & -3 & 1 & +3 & \(\%\) & \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\) & VDD \(=4.5 \mathrm{~V}\) to 5.5 V \\
\hline
\end{tabular}

\section*{TABLE 31-15: INTERNAL LPRC ACCURACY}
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|l|}{AC CHARACTERISTICS} & \multicolumn{6}{|l|}{Standard Operating Conditions: 4.5 V to 5.5 V (unless otherwise stated) Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\)} \\
\hline Param No. & Characteristic & Min & Typ & Max & Units & Cond & tions \\
\hline \multicolumn{8}{|l|}{LPRC @ 32.768 kHz \({ }^{(1,2)}\)} \\
\hline HF21C & LPRC & -30 & 10 & +30 & \% & \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\) & \(\mathrm{V} D \mathrm{D}=4.5 \mathrm{~V}\) to 5.5 V \\
\hline
\end{tabular}

Note 1: Change of LPRC frequency as VDD changes.
2: LPRC accuracy impacts the Watchdog Timer Time-out Period (TWDT1). See Section 27.5 "Watchdog Timer (WDT)" for more information.

TABLE 31-16: CTMU CURRENT SOURCE SPECIFICATIONS
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{5}{|l|}{Standard Operating Conditions: 4.5V to 5.5 V (unless otherwise stated) Operating temperature
\[
-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}
\]} \\
\hline Param No. & Symbol & Characteristic \({ }^{(1)}\) & Min. & Typ. & Max. & Units & Conditions \\
\hline \multicolumn{8}{|c|}{CTMU Current Source} \\
\hline HCTMUI1 & Iout1 & Base Range & - & 550 & - & nA & CTMUICON<9.8> \(=01\) \\
\hline HCTMUI2 & Iout2 & 10x Range & - & 5.5 & - & \(\mu \mathrm{A}\) & CTMUICON<9.8> = 10 \\
\hline HCTMUI3 & Iout3 & 100x Range & - & 55 & - & \(\mu \mathrm{A}\) & CTMUICON<9.8> = 11 \\
\hline HCTMUIO & IouT4 & 1000x Range & - & 550 & - & \(\mu \mathrm{A}\) & CTMUICON<9.8> \(=00\) \\
\hline \multirow[t]{3}{*}{HCTMUFV1} & \multirow[t]{3}{*}{\(V_{F}\)} & \multirow[t]{3}{*}{Temperature Diode Forward Voltage \({ }^{(2)}\)} & - & 0.525 & - & V & \[
\begin{aligned}
& \mathrm{TA}=+25^{\circ} \mathrm{C}, \\
& \mathrm{CTMUICON}<9.8>=01
\end{aligned}
\] \\
\hline & & & - & 0.585 & - & V & \[
\begin{aligned}
& \mathrm{TA}=+25^{\circ} \mathrm{C}, \\
& \text { CTMUICON }<9.8>=10
\end{aligned}
\] \\
\hline & & & - & 0.645 & - & V & \[
\begin{aligned}
& \mathrm{TA}=+25^{\circ} \mathrm{C}, \\
& \mathrm{CTMUICON}<9.8>=11
\end{aligned}
\] \\
\hline
\end{tabular}

Note 1: Normal value at center point of current trim range (CTMUICON<15:10> \(=000000\) ).
2: Parameters are characterized, but are not tested in manufacturing. Measurements are taken with the following conditions:
- \(\mathrm{VREF}=\mathrm{AVDD}=5.0 \mathrm{~V}\)
- ADC module configured for 10-bit mode
- ADC module configured for conversion speed of 500 ksps
- All PMDx bits are cleared ( \(\mathrm{PMDx}=0\) )
- CPU executing
while(1)
\{
NOP(); \}
- Device operating from the FRC with no PLL

\section*{TABLE 31-17: OP AMP/COMPARATOR SPECIFICATIONS}
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{DC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions: (see Note 3) 4.5V to 5.5V (unless otherwise stated) \\
Operating temperature \(-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\)
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic & Min. & Typ. \({ }^{(1)}\) & Max. & Units & Conditions \\
\hline \multicolumn{8}{|c|}{Comparator DC Characteristics} \\
\hline HCM30 & Voffset & Comparator Offset Voltage & -80 & \(\pm 60\) & 80 & mV & \\
\hline HCM31 & VHYST & Input Hysteresis Voltage & - & 30 & - & mV & \\
\hline HCM34 & VICM & Input Common-Mode Voltage & AVss & - & AVDD & V & \\
\hline \multicolumn{8}{|c|}{Op Amp DC Characteristics \({ }^{(2)}\)} \\
\hline HCM40 & VCMR & Common-Mode Input Voltage Range & AVss & - & AVDD & V & \\
\hline HCM42 & Voffset & Op Amp Offset Voltage & -50 & \(\pm 6\) & 50 & mV & \\
\hline
\end{tabular}

Note 1: Data in "Typ." column is at \(5.0 \mathrm{~V},+25^{\circ} \mathrm{C}\) unless otherwise stated.
2: Resistances can vary by +/-10\% between op amps.
3: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter HBO10 in Table 31-10 for the minimum and maximum BOR values.

TABLE 31-18: ADC MODULE SPECIFICATIONS (12-BIT MODE)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{\begin{tabular}{l}
Standard Operating Conditions (see Note 1): 4.5V to 5.5 V (unless otherwise stated) \\
Operating temperature \(\quad-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\)
\end{tabular}} \\
\hline Param No. & Symbol & Characteristic & Min. & Typ. & Max. & Units & Conditions \\
\hline \multicolumn{8}{|c|}{ADC Accuracy (12-Bit Mode)} \\
\hline HAD20a & Nr & Resolution & & data & & bits & \\
\hline HAD21a & INL & Integral Nonlinearity & -2 & - & +2 & LSb & \[
\begin{aligned}
& \text { VINL = AVSS }=\text { VREFL }=0 \mathrm{~V}, \\
& \text { AVDD }=\text { VREFH }=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline HAD22a & DNL & Differential Nonlinearity & >-1 & - & < 1 & LSb & \[
\begin{aligned}
& \mathrm{VINL}=\mathrm{AVSS}=\mathrm{VREFL}=0 \mathrm{~V}, \\
& \mathrm{AVDD}=\mathrm{VREFH}=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline HAD23a & GERR & Gain Error & -10 & 4 & 10 & LSb & \[
\begin{aligned}
& \mathrm{VINL}=\mathrm{AVSS}=\mathrm{VREFL}=0 \mathrm{~V}, \\
& \mathrm{AVDD}=\mathrm{VREFH}=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline HAD24a & Eoff & Offset Error & -10 & 1.75 & 10 & LSb & \[
\begin{aligned}
& \text { VINL }=\mathrm{AVSS}=\mathrm{VREFL}=0 \mathrm{~V}, \\
& \text { AVDD }=\mathrm{VREFH}=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline
\end{tabular}

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

TABLE 31-19: ADC MODULE SPECIFICATIONS (10-BIT MODE)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{AC CHARACTERISTICS} & \multicolumn{5}{|l|}{Standard Operating Conditions (see Note 1): 4.5V to 5.5 V (unless otherwise stated) Operating temperature \(\quad-40^{\circ} \mathrm{C} \leq \mathrm{TA} \leq+150^{\circ} \mathrm{C}\)} \\
\hline Param No. & Symbol & Characteristic & Min. & Typ. & Max. & Units & Conditions \\
\hline \multicolumn{8}{|c|}{ADC Accuracy (10-Bit Mode)} \\
\hline HAD20b & Nr & Resolution & & data & & bits & \\
\hline HAD21b & INL & Integral Nonlinearity & -1.5 & - & +1.5 & LSb & \[
\begin{aligned}
& \text { VINL }=\mathrm{AVSS}=\mathrm{VREFL}=0 \mathrm{~V}, \\
& \text { AVDD }=\mathrm{VREFH}=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline HAD22b & DNL & Differential Nonlinearity & \(\geq 1\) & - & < 1 & LSb & \[
\begin{aligned}
& \text { VINL }=\mathrm{AVSS}=\mathrm{VREFL}=0 \mathrm{~V}, \\
& \text { AVDD }=\mathrm{VREFH}=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline HAD23b & GERR & Gain Error & 1 & 3 & 6 & LSb & \[
\begin{aligned}
& \text { VINL = AVSS }=\text { VREFL }=0 \mathrm{~V}, \\
& \text { AVDD }=\text { VREFH }=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline HAD24b & Eoff & Offset Error & 1 & 2 & 4 & LSb & \[
\begin{aligned}
& \text { VINL = AVSS }=\text { VREFL }=0 \mathrm{~V}, \\
& \text { AVDD }=\text { VREFH }=5.5 \mathrm{~V}
\end{aligned}
\] \\
\hline
\end{tabular}

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter HBO10 in Table 31-10 for the minimum and maximum BOR values.

\subsection*{32.0 PACKAGING INFORMATION}

\subsection*{32.1 Package Marking Information}

\section*{28-Lead SPDIP (.300")}


Example


Example


Example


> \begin{tabular}{|lll|} \hline Legend: & XX...X & Customer-specific information \\ & Y & Year code (last digit of calendar year) \\ & WY & Year code (last 2 digits of calendar year) \\ & WNN & Alpek code (week of January 1 is week '01') \end{tabular}

\section*{dsPIC33EVXXXGM00X/10X FAMILY}

\subsection*{32.1 Package Marking Information (Continued)}

44-Lead TQFP (10×10×1 mm)


Example


44-Lead QFN ( \(8 \times 8 \times 0.9 \mathrm{~mm}\) )


Example


Example


\subsection*{32.2 Package Details}

The following sections give the technical details of the packages.

\section*{28-Lead Skinny Plastic Dual In-Line (SP) - \(\mathbf{3 0 0}\) mil Body [SPDIP]}

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

\begin{tabular}{|l|c|c|c|c|}
\hline \multicolumn{2}{|c|}{ Units } & \multicolumn{3}{|c|}{ INCHES } \\
\hline & Dimension Limits & MIN & NOM & MAX \\
\hline Number of Pins & N & \multicolumn{3}{|c|}{28} \\
\hline Pitch & e & \multicolumn{3}{|c|}{.100 BSC} \\
\hline Top to Seating Plane & A & - & - & .200 \\
\hline Molded Package Thickness & A 2 & .120 & .135 & .150 \\
\hline Base to Seating Plane & A 1 & .015 & - & - \\
\hline Shoulder to Shoulder Width & E & .290 & .310 & .335 \\
\hline Molded Package Width & E 1 & .240 & .285 & .295 \\
\hline Overall Length & D & 1.345 & 1.365 & 1.400 \\
\hline Tip to Seating Plane & L & .110 & .130 & .150 \\
\hline Lead Thickness & c & .008 & .010 & .015 \\
\hline Upper Lead Width & b 1 & .040 & .050 & .070 \\
\hline Lower Lead Width & b & .014 & .018 & .022 \\
\hline Overall Row Spacing § & eB & - & - & .430 \\
\hline
\end{tabular}

\section*{Notes}
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed . 010 " per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

\section*{28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]}

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging


TOP VIEW


VIEW A-A

\section*{28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]}

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

\begin{tabular}{|c|c|c|c|c|}
\hline \multicolumn{2}{|r|}{Units} & \multicolumn{3}{|c|}{MILLIMETERS} \\
\hline \multicolumn{2}{|r|}{Dimension Limits} & MIN & NOM & MAX \\
\hline Number of Pins & N & \multicolumn{3}{|c|}{28} \\
\hline Pitch & e & \multicolumn{3}{|c|}{1.27 BSC} \\
\hline Overall Height & A & - & - & 2.65 \\
\hline Molded Package Thickness & A2 & 2.05 & - & - \\
\hline Standoff § & A1 & 0.10 & - & 0.30 \\
\hline Overall Width & E & \multicolumn{3}{|c|}{10.30 BSC} \\
\hline Molded Package Width & E1 & \multicolumn{3}{|c|}{7.50 BSC} \\
\hline Overall Length & D & \multicolumn{3}{|c|}{17.90 BSC} \\
\hline Chamfer (Optional) & h & 0.25 & - & 0.75 \\
\hline Foot Length & L & 0.40 & - & 1.27 \\
\hline Footprint & L1 & \multicolumn{3}{|c|}{1.40 REF} \\
\hline Lead Angle & \(\bigcirc\) & \(0^{\circ}\) & - & - \\
\hline Foot Angle & \(\varphi\) & \(0^{\circ}\) & - & \(8^{\circ}\) \\
\hline Lead Thickness & c & 0.18 & - & 0.33 \\
\hline Lead Width & b & 0.31 & - & 0.51 \\
\hline Mold Draft Angle Top & \(\alpha\) & \(5^{\circ}\) & - & \(15^{\circ}\) \\
\hline Mold Draft Angle Bottom & \(\beta\) & \(5^{\circ}\) & - & \(15^{\circ}\) \\
\hline
\end{tabular}

\section*{Notes:}
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A \& B to be determined at Datum H .

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging


\section*{RECOMMENDED LAND PATTERN}
\begin{tabular}{|l|c|c|c|c|}
\hline & Units & \multicolumn{3}{|c|}{ MILLIMETERS } \\
\hline \multicolumn{2}{|c|}{ Dimension Limits } & MIN & NOM & MAX \\
\hline Contact Pitch & E & \multicolumn{3}{|c|}{1.27 BSC} \\
\hline Contact Pad Spacing & C & & 9.40 & \\
\hline Contact Pad Width (X28) & X & & & 0.60 \\
\hline Contact Pad Length (X28) & Y & & & 2.00 \\
\hline Distance Between Pads & Gx & 0.67 & & \\
\hline Distance Between Pads & G & 7.40 & & \\
\hline
\end{tabular}

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
Microchip Technology Drawing No. C04-2052A

\section*{28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length}

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging


Microchip Technology Drawing C04-124C Sheet 1 of 2

\section*{28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length}

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging


Notes:
\begin{tabular}{|l|c|c|c|c|}
\hline & Units & \multicolumn{3}{|c|}{ MILLIMETERS } \\
\hline \multicolumn{2}{|c|}{ Dimension Limits } & MIN & NOM & MAX \\
\hline Number of Pins & N & \multicolumn{3}{|c|}{28} \\
\hline Pitch & e & \multicolumn{3}{|c|}{0.65 BSC} \\
\hline Overall Height & A & 0.80 & 0.90 & 1.00 \\
\hline Standoff & A 1 & 0.00 & 0.02 & 0.05 \\
\hline Terminal Thickness & A 3 & \multicolumn{3}{|c|}{0.20 REF} \\
\hline Overall Width & E & \multicolumn{3}{|c|}{6.00 BSC} \\
\hline Exposed Pad Width & E 2 & 3.65 & \multicolumn{3}{|c|}{3.70} & 4.00 BSC \\
\hline Overall Length & D & \multicolumn{3}{|c|}{40} \\
\hline Exposed Pad Length & D 2 & 3.65 & 3.70 & 4.70 \\
\hline Terminal Width & b & 0.23 & 0.30 & 0.35 \\
\hline Terminal Length & L & 0.30 & 0.40 & 0.50 \\
\hline Terminal-to-Exposed Pad & K & 0.20 & - & - \\
\hline
\end{tabular}
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes onlv.

\section*{28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length}

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging


RECOMMENDED LAND PATTERN
\begin{tabular}{|c|c|c|c|c|}
\hline \multicolumn{2}{|r|}{Units} & \multicolumn{3}{|r|}{MILLIMETERS} \\
\hline \multicolumn{2}{|r|}{Dimension Limits} & MIN & NOM & MAX \\
\hline Contact Pitch & E & \multicolumn{3}{|c|}{0.65 BSC} \\
\hline Optional Center Pad Width & W2 & & & 4.70 \\
\hline Optional Center Pad Length & T2 & & & 4.70 \\
\hline Contact Pad Spacing & C1 & & 6.00 & \\
\hline Contact Pad Spacing & C2 & & 6.00 & \\
\hline Contact Pad Width (X28) & X1 & & & 0.40 \\
\hline Contact Pad Length (X28) & Y1 & & & 0.85 \\
\hline Distance Between Pads & G & 0.25 & & \\
\hline
\end{tabular}

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
Microchip Technology Drawing No. C04-2124A

\section*{44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1 mm Body, 2.00 mm [TQFP]}

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

\begin{tabular}{|c|c|c|c|c|}
\hline \multicolumn{2}{|r|}{Units} & \multicolumn{3}{|c|}{MILLIMETERS} \\
\hline \multicolumn{2}{|r|}{Dimension Limits} & MIN & NOM & MAX \\
\hline Number of Leads & N & \multicolumn{3}{|c|}{44} \\
\hline Lead Pitch & e & \multicolumn{3}{|c|}{0.80 BSC} \\
\hline Overall Height & A & - & - & 1.20 \\
\hline Molded Package Thickness & A2 & 0.95 & 1.00 & 1.05 \\
\hline Standoff & A1 & 0.05 & - & 0.15 \\
\hline Foot Length & L & 0.45 & 0.60 & 0.75 \\
\hline Footprint & L1 & \multicolumn{3}{|c|}{1.00 REF} \\
\hline Foot Angle & \(\phi\) & \(0^{\circ}\) & \(3.5{ }^{\circ}\) & \(7^{\circ}\) \\
\hline Overall Width & E & \multicolumn{3}{|c|}{12.00 BSC} \\
\hline Overall Length & D & \multicolumn{3}{|c|}{12.00 BSC} \\
\hline Molded Package Width & E1 & \multicolumn{3}{|c|}{10.00 BSC} \\
\hline Molded Package Length & D1 & \multicolumn{3}{|c|}{10.00 BSC} \\
\hline Lead Thickness & c & 0.09 & - & 0.20 \\
\hline Lead Width & b & 0.30 & 0.37 & 0.45 \\
\hline Mold Draft Angle Top & \(\alpha\) & \(11^{\circ}\) & \(12^{\circ}\) & \(13^{\circ}\) \\
\hline Mold Draft Angle Bottom & \(\beta\) & \(11^{\circ}\) & \(12^{\circ}\) & \(13^{\circ}\) \\
\hline
\end{tabular}

\section*{Notes:}
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
Microchip Technology Drawing C04-076B

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging


RECOMMENDED LAND PATTERN
\begin{tabular}{|l|c|c|c|c|}
\hline & Units & \multicolumn{3}{|c|}{ MILLIMETERS } \\
\hline \multicolumn{2}{|c|}{ Dimension Limits } & MIN & NOM & MAX \\
\hline Contact Pitch & E & \multicolumn{3}{|c|}{0.80 BSC } \\
\hline Contact Pad Spacing & C1 & & 11.40 & \\
\hline Contact Pad Spacing & C2 & & 11.40 & \\
\hline Contact Pad Width (X44) & X1 & & & 0.55 \\
\hline Contact Pad Length (X44) & Y1 & & & 1.50 \\
\hline Distance Between Pads & G & 0.25 & & \\
\hline
\end{tabular}

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
Microchip Technology Drawing No. C04-2076B

\section*{44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]}

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging


Microchip Technology Drawing C04-103C Sheet 1 of 2

\section*{44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]}

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

\begin{tabular}{|l|c|c|c|c|}
\hline & \multicolumn{1}{|c|}{ Units } & \multicolumn{3}{|c|}{ MILLIMETERS } \\
\hline \multicolumn{2}{|c|}{ Dimension Limits } & MIN & NOM & MAX \\
\hline Number of Pins & N & \multicolumn{3}{|c|}{44} \\
\hline Pitch & e & \multicolumn{3}{|c|}{0.65 BSC} \\
\hline Overall Height & A & 0.80 & 0.90 & 1.00 \\
\hline Standoff & A 1 & 0.00 & 0.02 & 0.05 \\
\hline Terminal Thickness & A 3 & \multicolumn{3}{|c|}{0.20 REF} \\
\hline Overall Width & E & \multicolumn{3}{|c|}{8.00 BSC} \\
\hline Exposed Pad Width & E 2 & 6.25 & 6.45 & 6.60 \\
\hline Overall Length & D & \multicolumn{3}{|c|}{8.00 BSC} \\
\hline Exposed Pad Length & D 2 & 6.25 & 6.45 & 6.60 \\
\hline Terminal Width & b & 0.20 & 0.30 & 0.35 \\
\hline Terminal Length & L & 0.30 & 0.40 & 0.50 \\
\hline Terminal-to-Exposed-Pad & K & 0.20 & - & - \\
\hline
\end{tabular}

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension. usuallv without tolerance. for information purboses onlv.
Microchip Technology Drawing C04-103C Sheet 2 of 2

\section*{44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]}

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging


RECOMMENDED LAND PATTERN
\begin{tabular}{|l|c|c|c|c|}
\hline & Units & \multicolumn{3}{|c|}{ MILLIMETERS } \\
\hline \multicolumn{2}{|c|}{ Dimension Limits } & \multicolumn{2}{|c|}{ MIN } & NOM \\
\hline & MAX \\
\hline Contact Pitch & E & \multicolumn{3}{|c|}{0.65 BSC} \\
\hline Optional Center Pad Width & W 2 & & & 6.60 \\
\hline Optional Center Pad Length & T 2 & & & 6.60 \\
\hline Contact Pad Spacing & C 1 & & 8.00 & \\
\hline Contact Pad Spacing & C 2 & & 8.00 & \\
\hline Contact Pad Width (X44) & X 1 & & & 0.35 \\
\hline Contact Pad Length (X44) & Y 1 & & & 0.85 \\
\hline Distance Between Pads & G & 0.25 & & \\
\hline
\end{tabular}

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances
Microchip Technology Drawing No. C04-2103B

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging


TOP VIEW


SIDE VIEW

> \begin{tabular}{|ll} \hline Note: & \(\begin{array}{l}\text { For the most current package drawings, please see the Microchip Packaging Specification located at } \\ \text { http://www.microchip.com/packaging }\end{array}\) \end{tabular}


Notes:
\begin{tabular}{|l|c|c|c|c|c|}
\hline \multicolumn{2}{|c|}{ Units } & \multicolumn{3}{|c|}{ MILLIMETERS } \\
\hline \multicolumn{2}{|c|}{ Dimension Limits } & MIN & NOM & MAX \\
\hline Number of Leads & N & \multicolumn{3}{|c|}{64} \\
\hline Lead Pitch & e & \multicolumn{3}{|c|}{0.50 BSC} \\
\hline Overall Height & A & - & - & 1.20 \\
\hline Molded Package Thickness & A 2 & 0.95 & 1.00 & 1.05 \\
\hline Standoff & A 1 & 0.05 & - & 0.15 \\
\hline Foot Length & L & 0.45 & 0.60 & 0.75 \\
\hline Footprint & L 1 & \multicolumn{3}{|c|}{1.00 REF} \\
\hline Foot Angle & \(\phi\) & \(0^{\circ}\) & \multicolumn{3}{|c|}{\(3.5^{\circ}\)} \\
\hline Overall Width & E & \multicolumn{3}{|c|}{12.00 BSC} \\
\hline Overall Length & D & \multicolumn{3}{|c|}{12.00 BSC} \\
\hline Molded Package Width & E 1 & \multicolumn{3}{|c|}{10.00 BSC} \\
\hline Molded Package Length & D 1 & \multicolumn{3}{|c|}{-} \\
\hline Lead Thickness & C & 0.09 & - & 0.20 \\
\hline Lead Width & b & 0.17 & 0.22 & 0.27 \\
\hline Mold Draft Angle Top & \(\alpha\) & \(11^{\circ}\) & \(12^{\circ}\) & \(13^{\circ}\) \\
\hline Mold Draft Angle Bottom & \(\beta\) & \(11^{\circ}\) & \(12^{\circ}\) & \(13^{\circ}\) \\
\hline
\end{tabular}
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
Microchip Technology Drawing C04-085C Sheet 2 of 2

\section*{64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]}

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging


RECOMMENDED LAND PATTERN
\begin{tabular}{|l|c|c|c|c|}
\hline & Units & \multicolumn{3}{|c|}{ MILLIMETERS } \\
\hline \multicolumn{2}{|c|}{ Dimension Limits } & MIN & NOM & MAX \\
\hline Contact Pitch & E & \multicolumn{3}{|c|}{0.50 BSC } \\
\hline Contact Pad Spacing & C1 & & 11.40 & \\
\hline Contact Pad Spacing & C2 & & 11.40 & \\
\hline Contact Pad Width (X28) & X1 & & & 0.30 \\
\hline Contact Pad Length (X28) & Y1 & & & 1.50 \\
\hline Distance Between Pads & G & 0.20 & & \\
\hline
\end{tabular}

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
Microchip Technology Drawing C04-2085B Sheet 1 of 1

\section*{64-Lead Plastic Quad Flat, No Lead Package (MR) - 9x9x0.9 mm Body [QFN] With \(7.15 \times 7.15\) Exposed Pad [QFN]}

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging


BOTTOM VIEW

Microchip Technology Drawing C04-149C Sheet 1 of 2

\section*{64-Lead Plastic Quad Flat, No Lead Package (MR) - 9x9x0.9 mm Body [QFN] With \(7.15 \times 7.15\) Exposed Pad [QFN]}

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

\begin{tabular}{|l|c|c|c|c|}
\hline & \multicolumn{4}{|c|}{ Units } \\
\multicolumn{6}{|c|}{ Dimension Limits } & \multicolumn{3}{|c|}{ MINLIMETERS } \\
\hline & N & \multicolumn{3}{|c|}{ NOM } \\
\hline & MAX \\
\hline Number of Pins & e & \multicolumn{3}{|c|}{0.50 BSC} \\
\hline Pitch & A & 0.80 & 0.90 & 1.00 \\
\hline Overall Height & A1 & 0.00 & 0.02 & 0.05 \\
\hline Standoff & A3 & \multicolumn{3}{|c|}{0.20 REF } \\
\hline Contact Thickness & E & \multicolumn{3}{|c|}{9.00 BSC} \\
\hline Overall Width & E2 & 7.05 & \multicolumn{3}{|c|}{7.15} & 7.50 \\
\hline Exposed Pad Width & D & \multicolumn{3}{|c|}{9.00 BSC} \\
\hline Overall Length & D2 & 7.05 & 7.15 & 7.50 \\
\hline Exposed Pad Length & b & 0.18 & 0.25 & 0.30 \\
\hline Contact Width & L & 0.30 & 0.40 & 0.50 \\
\hline Contact Length & K & 0.20 & - & - \\
\hline Contact-to-Exposed Pad & & \multicolumn{3}{|c|}{} \\
\hline
\end{tabular}

\section*{Notes:}
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
Microchip Technology Drawing C04-149C Sheet 2 of 2

64-Lead Plastic Quad Flat, No Lead Package (MR) - 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

\begin{tabular}{|l|c|c|c|c|}
\hline & Units & \multicolumn{3}{|c|}{ MILLIMETERS } \\
\hline \multicolumn{7}{|c|}{ Dimension Limits } & \multicolumn{2}{|c|}{ MIN } & NOM & MAX \\
\hline Contact Pitch & E & \multicolumn{3}{|c|}{0.50 BSC} \\
\hline Optional Center Pad Width & W2 & & & 7.35 \\
\hline Optional Center Pad Length & T2 & & & 7.35 \\
\hline Contact Pad Spacing & C1 & & 8.90 & \\
\hline Contact Pad Spacing & C 2 & & 8.90 & \\
\hline Contact Pad Width (X64) & X1 & & & 0.30 \\
\hline Contact Pad Length (X64) & Y1 & & & 0.85 \\
\hline Distance Between Pads & G & 0.20 & & \\
\hline
\end{tabular}

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
Microchip Technology Drawing No. C04-2149A

\section*{APPENDIX A: REVISION HISTORY}

\section*{Revision A (December 2013)}

This is the initial version of this document.

\section*{Revision B (June 2014)}

This revision incorporates the following updates:
- Sections:
- Added Section 31.0, High-Temperature Electrical Characteristics
- Updated the "Power Management"section, the "Input/Output" section, Section 3.3 "Data Space Addressing", Section 4.2 "Data Address Space", Section 4.3.2 "Extended X Data Space", Section 4.6.1 "Bit-Reversed Addressing Implementation", Section 7.4.1 "INTCON1 through INTCON4", Section 11.6 "I/O Helpful Tips"
- Updated note in Section 17.0 "High-Speed PWM Module", Section 18.0 "Serial Peripheral Interface (SPI)", Section 27.8 "Code Protection and CodeGuard \({ }^{\text {TM }}\) Security"
- Updated title of Section 20.0 "Single-Edge Nibble Transmission (SENT)"
- Updated Section 32.0 "Packaging Information". Deleted e3, Pb-free and Industrial (I) temperature range indication throughout the section, and updated the packaging diagrams
- Updated the "Product Identification System" section
- Registers:
- Updated Register 3-2, Register 7-2, Register 7-6, Register 9-2, Register 11-3, Register 14-1, Register 14-3, Register 14-11, Register 15-1, Register 22-4
- Figures:
- Added Figure 4-5, Figure 4-6, Figure 4-12, Figure 4-13, Figure 14-1, Figure 16-1, Figure 17-2, Figure 23-1, Figure 24-1, Figure 30-37
- Tables:
- Updated Table 1, Table 27-1, Table 27-2, Table 30-6, Table 30-7, Table 30-8, Table 30-9, Table 30-10, Table 30-11, Table 30-12, Table 30-49, Table 30-52 and added Table 31-11,
- Changes to text and formatting were incorporated throughout the document

\section*{Revision C (November 2014)}

This revision incorporates the following updates:
- Sections:
- Added note in Section 5.2 "RTSP Operation"
- Updated "Section 5.4 "Error Correcting Code (ECC)"
- Deleted 44-Terminal Very Thin Leadless Array Package (TL) - 6x6x0.9 mm Body With Exposed Pad (VTLA).
- Registers
- Updated Register 7-6
- Figures:
- Updated Figure 4-1, Figure 4-2, Figure 4-3
- Tables:
- Updated Table 27-2, Table 31-13, Table 31-14, Table 31-15
- Added Table 31-16, Table 31-17

\section*{dsPIC33EVXXXGM00X/10X FAMILY}

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\section*{dsPIC33EVXXXGM00X/10X}

NOTES:

\section*{PRODUCT IDENTIFICATION SYSTEM}

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\section*{dsPIC33EVXXXGM00X/10X FAMILY}

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ISBN: 978-1-63276-813-1

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```


[^0]:    Legend: $x=$ unknown value on Reset; — = unimplemented, read as ' 0 '. Reset values are shown in hexadecimal.

[^1]:    Legend: - = unimplemented, read as ' 0 '. Reset values are shown in hexadecimal.

[^2]:    TABLE 4-34: PORTB REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

    | SFR <br> Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | TRISB | 0E14 | TRISB<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | fffr |
    | PORTB | 0E16 | RB<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
    | LATB | 0E18 | LATB<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
    | ODCB | 0E1A | ODCB<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
    | CNENB | 0E1C | CNIEB<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
    | CNPUB | 0E1E | CNPUB<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
    | CNPDB | 0E20 | CNPDB<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
    | ANSELB | 0E22 | - | - | - | - | - | - |  | ANSB<9:7> |  | - | - | - | ANSB<3:0> |  |  |  | 038F |
    | SR1B | 0E24 | - | - | - | - | - | - |  | SR1B<9:7> |  | - | - | SR1B4 | - | - | - | - | 0000 |
    | SROB | 0E26 | - | - | - | - | - | - |  | SROB<9:7> |  | - | - | SROB4 | - | - | - | - | 0000 |

    TABLE 4-35

    | SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | $\begin{gathered} \text { All } \\ \text { Resets } \end{gathered}$ |
    | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
    | TRISB | 0E14 | TRISB<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DF9F |
    | PORTB | 0E16 | RB<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
    | LATB | 0E18 | LATB<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | xxxx |
    | ODCB | 0E1A | ODCB<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
    | CNENB | 0E1C | CNIEB<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
    | CNPUB | OE1E | CNPUB<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
    | CNPDB | 0E20 | CNPDB<15:0> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0000 |
    | ANSELB | 0E22 | - | - | - | - | - | - | ANSB<9:7> |  |  | - | - | - |  |  |  |  | 010F |
    | SR1B | 0E24 | - | - | - | - | - | - | SR1B<9:7> |  |  | - | - | SR1B4 | - | - | - | - | 0000 |
    | SROB | 0E26 | - | - | - | - | - | - | SROB<9:7> |  |  | - | - | SROB4 | - | - | - | - | 0000 |

    0\mathrm{ '
    bit 7-0 OCFAR<7:0>: Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits
    (see Table 11-2 for input pin selection numbers)
    10110101 = Input tied to RPI181
    •
    •
    •
    00000001 = Input tied to CMP1
    00000000= Input tied to Vss

    ```

    REGISTER 11-7: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline FLT2R7 & FLT2R6 & FLT2R5 & FLT2R4 & FLT2R3 & FLT2R2 & FLT2R1 & FLT2R0 \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline FLT1R7 & FLT1R6 & FLT1R5 & FLT1R4 & FLT1R3 & FLT1R2 & FLT1R1 & FLT1R0 \\
    \hline bit 7
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-8 FLT2R<7:0>: Assign PWM Fault 2 (FLT2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
    10110101 = Input tied to RPI181
    -
    -
    -
    \(00000001=\) Input tied to CMP1
    \(00000000=\) Input tied to Vss
    bit 7-0 FLT1R<7:0>: Assign PWM Fault 1 (FLT1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
    10110101 = Input tied to RPI181
    -
    -
    -
    \(00000001=\) Input tied to CMP1
    \(00000000=\) Input tied to Vss

    \section*{REGISTER 11-8: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline- & - & - & - & - & - & - & - \\
    \hline bit 15 &
    \end{tabular}
    \begin{tabular}{|llllllll|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline & & U1RXR<7:0> & & & \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    Legend:
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' \(=\) Bit is set & ' 0 ' \(=\) Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-8 Unimplemented: Read as ' 0 '
    bit 7-0 U1RXR<7:0>: Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits
    (see Table 11-2 for input pin selection numbers)
    10110101 = Input tied to RPI181
    -
    -
    -
    00000001 = Input tied to CMP1
    \(00000000=\) Input tied to Vss

    \section*{REGISTER 11-9: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline- & - & - & - & - & - & - & - \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|llllllll|}
    \hline\(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) \\
    \hline & & U2RXR<7:0> & & & \\
    \hline bit 7 & & & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & & \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared \(\quad x=\) Bit is unknown \\
    \hline
    \end{tabular}
    ```

    bit 15-8 Unimplemented: Read as '0'
    bit 7-0 U2RXR<7:0>: Assign UART2 Receive (U2RX) to the Corresponding RPn Pin bits
    (see Table 11-2 for input pin selection numbers)
    10110101 = Input tied to RPI181
    •
    •
    •
    00000001 = Input tied to CMP1
    000000000= Input tied to Vss

    ```

    REGISTER 11-10: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline SCK2R7 & SCK2R6 & SCK2R5 & SCK2R4 & SCK2R3 & SCK2R2 & SCK2R1 & SCK2R0 \\
    \hline \multicolumn{8}{|l|}{bit 15 bit 8} \\
    \hline
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline SDI2R & SDI2R6 & SDI2R5 & SDI2R4 & SDI2R3 & SDI2R2 & SDI2R1 & SDI2R0 \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & ' 1 ' \(=\) Bit is set & ' 0 ' = Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-8 SCK2R<7:0>: Assign SPI2 Clock Input (SCK2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
    10110101 = Input tied to RPI181
    -
    -
    -
    00000001 = Input tied to CMP1
    \(00000000=\) Input tied to Vss
    bit 7-0 SDI2R<7:0>: Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
    10110101 = Input tied to RPI181
    -
    -
    -
    \(00000001=\) Input tied to CMP1
    \(00000000=\) Input tied to Vss

    REGISTER 11-11: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline - & - & - & - & - & - & - & - \\
    \hline \multicolumn{8}{|l|}{bit 15 bit 8} \\
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{SS2R<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-8 Unimplemented: Read as ' 0 '
    bit 7-0 SS2R<7:0>: Assign SPI2 Slave Select ( \(\overline{\mathrm{SS} 2}\) ) to the Corresponding RPn Pin bits
    (see Table 11-2 for input pin selection numbers)
    10110101 = Input tied to RPI181
    -
    -
    00000001 = Input tied to CMP1
    \(00000000=\) Input tied to Vss

    REGISTER 11-12: RPINR26: PERIPHERAL PIN SELECT INPUT REGISTER 26
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline- & - & - & - & - & - & - & - \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|llllllll|}
    \hline\(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) \\
    \hline & & \(C 1 R X R<7: 0>\) & & & \\
    \hline bit 7 & & & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' = Bit is set & ' 0 ' \(=\) Bit is cleared \\
    \hline
    \end{tabular}
    bit 15-8 Unimplemented: Read as ' 0 '
    bit 7-0 C1RXR<7:0>: Assign CAN1 RX Input (C1RX) to the Corresponding RPn Pin bits
    (see Table 11-2 for input pin selection numbers)
    10110101 = Input tied to RPI181
    -
    -
    -
    \(00000001=\) Input tied to CMP1
    \(00000000=\) Input tied to Vss

    REGISTER 11-13: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37
    
    bit 15-8 SYNCI1R<7:0>: Assign PWM Synchronization Input 1 to the Corresponding RPn Pin bits
    (see Table 11-2 for input pin selection numbers)
    10110101 = Input tied to RPI181
    -
    -
    \(00000001=\) Input tied to CMP1
    \(00000000=\) Input tied to Vss
    bit 7-0
    Unimplemented: Read as ' 0 '

    REGISTER 11-14: RPINR38: PERIPHERAL PIN SELECT INPUT REGISTER 38
    \begin{tabular}{|llllllll|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline & & DTCMP1R<7:0> & & & \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline- & - & - & - & - & - & - & - \\
    \hline bit 7
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & & \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' \(=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared \(\quad x=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-8 DTCMP1R<7:0>: Assign PWM Dead-Time Compensation Input 1 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
    10110101 = Input tied to RPI181
    -
    -
    -
    \(00000001=\) Input tied to CMP1
    \(00000000=\) Input tied to Vss
    bit 7-0 Unimplemented: Read as ' 0 '

    REGISTER 11-15: RPINR39: PERIPHERAL PIN SELECT INPUT REGISTER 39
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline DTCMP3R7 & DTCMP3R6 & DTCMP3R5 & DTCMP3R4 & DTCMP3R3 & DTCMP3R2 & DTCMP3R1 & DTCMP3R0 \\
    \hline \multicolumn{7}{|l|}{bit 15} & bit 8 \\
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline DTCMP2R7 & DTCMP2R6 & DTCMP2R5 & DTCMP2R4 & DTCMP2R3 & DTCMP2R2 & DTCMP2R1 & DTCMP2R0 \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}
    bit 15-8 DTCMP3R<7:0>: Assign PWM Dead-Time Compensation Input 3 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
    10110101 = Input tied to RPI181
    -
    -
    00000001 = Input tied to CMP1
    \(00000000=\) Input tied to Vss
    bit 7-0 DTCMP2R<7:0>: Assign PWM Dead-Time Compensation Input 2 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
    10110101 = Input tied to RPI181
    -
    -
    -
    00000001 = Input tied to CMP1
    \(00000000=\) Input tied to Vss

    REGISTER 11-16: RPINR44: PERIPHERAL PIN SELECT INPUT REGISTER 44
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{SENT1R<7:0>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline - & - & - & - & - & - & - & - \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' \(=\) Bit is set & 0 ' \(=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-8 SENT1R<7:0>: Assign SENT Module Input 1 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
    10110101 = Input tied to RPI181
    -
    -
    -
    \(00000001=\) Input tied to CMP1
    \(00000000=\) Input tied to Vss
    bit 7-0 Unimplemented: Read as ' 0 '

    REGISTER 11-17: RPINR45: PERIPHERAL PIN SELECT INPUT REGISTER 45
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-O & U-0 \\
    \hline- & - & - & - & - & - & - & - \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|lllllll|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0
    \end{tabular} R/W-0 \begin{tabular}{lllll|}
    \hline & & SENT2R<7:0> & & \\
    \hline bit 7 & & & & \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}
    bit 15-8 Unimplemented: Read as ' 0 '
    bit 7-0 SENT2R<7:0>: Assign SENT Module Input 2 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
    10110101 = Input tied to RPI181
    -
    -
    -
    \(00000001=\) Input tied to CMP1
    \(00000000=\) Input tied to Vss

    \section*{REGISTER 11-18: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP35R5 & RP35R4 & RP35R3 & RP35R2 & RP35R1 & RP35R0 \\
    \hline bit 15 &
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP20R5 & RP20R4 & RP20R3 & RP20R2 & RP20R1 & RP20R0 \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}

    Legend:
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' \(=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared \\
    \hline
    \end{tabular}
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13-8 RP35R<5:0>: Peripheral Output Function is Assigned to RP35 Output Pin bits (see Table 11-3 for peripheral function numbers)
    bit 7-6 Unimplemented: Read as ' 0 '
    bit 5-0 RP20R<5:0>: Peripheral Output Function is Assigned to RP20 Output Pin bits (see Table 11-3 for peripheral function numbers)

    REGISTER 11-19: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP37R5 & RP37R4 & RP37R3 & RP37R2 & RP37R1 & RP37R0 \\
    \hline bit 15 & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP36R5 & RP36R4 & RP36R3 & RP36R2 & RP36R1 & RP36R0 \\
    \hline bit 7 & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' \(=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13-8 RP37R<5:0>: Peripheral Output Function is Assigned to RP37 Output Pin bits (see Table 11-3 for peripheral function numbers)
    bit 7-6 Unimplemented: Read as '0'
    bit 5-0 RP36R<5:0>: Peripheral Output Function is Assigned to RP36 Output Pin bits (see Table 11-3 for peripheral function numbers)

    \section*{REGISTER 11-20: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP39R5 & RP39R4 & RP39R3 & RP39R2 & RP39R1 & RP39R0 \\
    \hline bit 15 &
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{9}{|c|}{ U-0 } & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP38R5 & RP38R4 & RP38R3 & RP38R2 & RP38R1 & RP38R0 \\
    \hline bit 7 & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13-8 RP39R<5:0>: Peripheral Output Function is Assigned to RP39 Output Pin bits (see Table 11-3 for peripheral function numbers)
    bit 7-6 Unimplemented: Read as ' 0 '
    bit 5-0 RP38R<5:0>: Peripheral Output Function is Assigned to RP38 Output Pin bits (see Table 11-3 for peripheral function numbers)

    REGISTER 11-21: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP41R5 & RP41R4 & RP41R3 & RP41R2 & RP41R1 & RP41R0 \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP40R5 & RP40R4 & RP40R3 & RP40R2 & RP40R1 & RP40R0 \\
    \hline bit 7 &
    \end{tabular}

    \section*{Legend:}
    \(R=\) Readable bit
    \(-n=\) Value at POR
    \(W=\) Writable bit
    \(' 1\) ' \(=\) Bit is set
    \(\mathrm{U}=\) Unimplemented bit, read as ' 0 '
    ' 0 ' = Bit is cleared
    \(x=\) Bit is unknown
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13-8 RP41R<5:0>: Peripheral Output Function is Assigned to RP41 Output Pin bits (see Table 11-3 for peripheral function numbers)
    bit 7-6 Unimplemented: Read as ' 0 '
    bit 5-0 RP40R<5:0>: Peripheral Output Function is Assigned to RP40 Output Pin bits (see Table 11-3 for peripheral function numbers)

    REGISTER 11-22: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP43R5 & RP43R4 & RP43R3 & RP43R2 & RP43R1 & RP43R0 \\
    \hline bit 15 &
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP42R5 & RP42R4 & RP42R3 & RP42R2 & RP42R1 & RP42R0 \\
    \hline bit 7 & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13-8 RP43R<5:0>: Peripheral Output Function is Assigned to RP43 Output Pin bits (see Table 11-3 for peripheral function numbers)
    bit 7-6 Unimplemented: Read as ' 0 '
    bit 5-0 RP42R<5:0>: Peripheral Output Function is Assigned to RP42 Output Pin bits (see Table 11-3 for peripheral function numbers)

    REGISTER 11-23: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5 \({ }^{(1)}\)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP49R5 & RP49R4 & RP49R3 & RP49R2 & RP49R1 & RP49R0 \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP48R5 & RP48R4 & RP48R3 & RP48R2 & RP48R1 & RP48R0 \\
    \hline bit 7 & & & & & bit 0 \\
    \hline
    \end{tabular}

    Legend:
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared \(\quad x=\) Bit is unknown
    \end{tabular}
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13-8 RP49R<5:0>: Peripheral Output Function is Assigned to RP49 Output Pin bits (see Table 11-3 for peripheral function numbers)
    bit 7-6 Unimplemented: Read as ' 0 '
    bit 5-0 RP48R<5:0>: Peripheral Output Function is Assigned to RP48 Output Pin bits (see Table 11-3 for peripheral function numbers)

    Note 1: This register is present in dsPIC33EVXXXGM004/104/006/106 devices only.

    REGISTER 11-24: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER \(6{ }^{(1)}\)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP55R5 & RP55R4 & RP55R3 & RP55R2 & RP55R1 & RP55R0 \\
    \hline bit 15 \\
    \begin{tabular}{|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline ( & R/W-0 \\
    \hline bit 7 & - & RP54R5 & RP54R4 & RP54R3 & RP54R2 & RP54R1
    \end{tabular} RP54R0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13-8 RP55R<5:0>: Peripheral Output Function is Assigned to RP55 Output Pin bits (see Table 11-3 for peripheral function numbers)
    bit 7-6 Unimplemented: Read as ' 0 '
    bit 5-0 RP54R<5:0>: Peripheral Output Function is Assigned to RP54 Output Pin bits (see Table 11-3 for peripheral function numbers)

    Note 1: This register is present in dsPIC33EVXXXGM004/104/006/106 devices only

    REGISTER 11-25: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7 \({ }^{(1)}\)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP57R5 & RP57R4 & RP57R3 & RP57R2 & RP57R1 & RP57R0 \\
    \hline bit 15 &
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP56R5 & RP56R4 & RP56R3 & RP56R2 & RP56R1 & RP56R0 \\
    \hline bit 7 &
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' \(=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-14 Unimplemented: Read as '0'
    bit 13-8 RP57R<5:0>: Peripheral Output Function is Assigned to RP57 Output Pin bits (see Table 11-3 for peripheral function numbers)
    bit 7-6 Unimplemented: Read as '0'
    bit 5-0 RP56R<5:0>: Peripheral Output Function is Assigned to RP56 Output Pin bits (see Table 11-3 for peripheral function numbers)

    Note 1: This register is present in dsPIC33EVXXXGM004/104/006/106 devices only.

    REGISTER 11-26: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER \(\mathbf{8}^{(1)}\)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP70R5 & RP70R4 & RP70R3 & RP70R2 & RP70R1 & RP70R0 \\
    \hline bit 15 &
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP69R5 & RP69R4 & RP69R3 & RP69R2 & RP69R1 & RP69R0 \\
    \hline bit 7 & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13-8 RP70R<5:0>: Peripheral Output Function is Assigned to RP70 Output Pin bits (see Table 11-3 for peripheral function numbers)
    bit 7-6 Unimplemented: Read as ' 0 '
    bit 5-0 RP69R<5:0>: Peripheral Output Function is Assigned to RP69 Output Pin bits (see Table 11-3 for peripheral function numbers)

    Note 1: This register is present in dsPIC33EVXXXGM004/104/006/106 devices only.

    REGISTER 11-27: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER \(\mathbf{9}^{(1)}\)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP118R5 & RP118R4 & RP118R3 & RP118R2 & RP118R1 & RP118R0 \\
    \hline bit 15 &
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP97R5 & RP97R4 & RP97R3 & RP97R2 & RP97R1 & RP97R0 \\
    \hline bit 7 &
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' \(=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared \(\quad x=\) Bit is unknown
    \end{tabular}
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13-8 RP118R<5:0>: Peripheral Output Function is Assigned to RP118 Output Pin bits (see Table 11-3 for peripheral function numbers)
    bit 7-6 Unimplemented: Read as ' 0 '
    bit 5-0 RP97R<5:0>: Peripheral Output Function is Assigned to RP97 Output Pin bits (see Table 11-3 for peripheral function numbers)

    Note 1: This register is present in dsPIC33EVXXXGM004/106 devices only.

    REGISTER 11-28: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10
    

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13-8 RP176R<5:0>: Peripheral Output Function is Assigned to RP176 Output Pin bits (see Table 11-3 for peripheral function numbers)
    bit 7-6 Unimplemented: Read as ' 0 '
    bit 5-0 \(\quad \mathbf{R P 1 2 0 R}<5: 0>\) : Peripheral Output Function is Assigned to RP120 Output Pin bits \({ }^{(1)}\) (see Table 11-3 for peripheral function numbers)

    Note 1: RP120R<5:0> is present in dsPIC33EVXXXGM006/106 devices only.

    REGISTER 11-29: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11
    

    \section*{Legend:}
    \(R=\) Readable bit
    \(-n=\) Value at POR
    \(W=\) Writable bit
    \(' 1\) ' \(=\) Bit is set
    \(\mathrm{U}=\) Unimplemented bit, read as ' 0 '
    ' 0 ' = Bit is cleared \(\quad x=\) Bit is unknown
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13-8 RP178R<5:0>: Peripheral Output Function is Assigned to RP178 Output Pin bits (see Table 11-3 for peripheral function numbers)
    bit 7-6 Unimplemented: Read as ' 0 '
    bit 5-0 RP177R<5:0>: Peripheral Output Function is Assigned to RP177 Output Pin bits (see Table 11-3 for peripheral function numbers)

    REGISTER 11-30: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP180R5 & RP180R4 & RP180R3 & RP180R2 & RP180R1 & RP180R0 \\
    \hline bit 15 & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & RP179R5 & RP179R4 & RP179R3 & RP179R2 & RP179R1 & RP179R0 \\
    \hline bit 7 & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13-8 RP180R<5:0>: Peripheral Output Function is Assigned to RP180 Output Pin bits (see Table 11-3 for peripheral function numbers)
    bit 7-6 Unimplemented: Read as ' 0 '
    bit 5-0 RP179R<5:0>: Peripheral Output Function is Assigned to RP179 Output Pin bits (see Table 11-3 for peripheral function numbers)

    REGISTER 11-31: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline- & - & - & - & - & - & - & - \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|l|c|cccccc|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & & \(R P 181 R<5: 0>\) & & \\
    \hline bit 7 & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' \(=\) Bit is set & ' 0 ' = Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-6 Unimplemented: Read as ' 0 '
    bit 5-0 RP181R<5:0>: Peripheral Output Function is Assigned to RP181 Output Pin bits
    (see Table 11-3 for peripheral function numbers)

    \section*{dsPIC33EVXXXGM00X/10X FAMILY}

    NOTES:

    \subsection*{12.0 TIMER1}

    Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
    2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

    The Timer1 module is a 16 -bit timer that can operate as a free-running, interval timer/counter.
    The Timer1 module has the following unique features over other timers:
    - Can be Operated in Asynchronous Counter mode from an External Clock Source
    - The Timer1 External Clock Input (T1CK) can Optionally be Synchronized to the Internal Device Clock and the Clock Synchronization is Performed after the Prescaler

    A block diagram of Timer1 is shown in Figure 12-1.

    The Timer1 module can operate in one of the following modes:
    - Timer mode
    - Gated Timer mode
    - Synchronous Counter mode
    - Asynchronous Counter mode

    In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FcY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.
    The Timer modes are determined by the following bits:
    - Timer Clock Source Control bit (TCS): T1CON<1>
    - Timer Synchronization Control bit (TSYNC): T1CON<2>
    - Timer Gate Control bit (TGATE): T1CON<6>

    Timer control bit settings for different operating modes are given in Table 12-1.

    TABLE 12-1: TIMER MODE SETTINGS
    \begin{tabular}{|l|c|c|c|}
    \hline \multicolumn{1}{|c|}{ Mode } & TCS & TGATE & TSYNC \\
    \hline \hline Timer & 0 & 0 & x \\
    \hline Gated Timer & 0 & 1 & x \\
    \hline \begin{tabular}{l} 
    Synchronous \\
    Counter
    \end{tabular} & 1 & x & 1 \\
    \hline \begin{tabular}{l} 
    Asynchronous \\
    Counter
    \end{tabular} & 1 & x & 0 \\
    \hline
    \end{tabular}

    FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM
    

    Note 1: FP is the peripheral clock.

    \subsection*{12.1 Timer1 Control Register}

    REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & U-0 & R/W-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline TON \({ }^{(1)}\) & - & TSIDL & - & - & - & - & - \\
    \hline bit 15 \\
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline U-0 & R/W-0 & R/W-0 & R/W-0 & U-0 & R/W-0 & R/W-0 & U-0 \\
    \hline - & TGATE & TCKPS1 & TCKPS0 & - & TSYNC \({ }^{(1)}\) & TCS \({ }^{(1)}\) & - \\
    \hline bit 7 &
    \end{tabular}
    \end{tabular}\(.\)\begin{tabular}{l} 
    bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared \(\quad x=\) Bit is unknown
    \end{tabular}
    bit \(15 \quad\)\begin{tabular}{ll} 
    TON: Timer1 On bit \({ }^{(1)}\) \\
    & \(1=\) Starts 16-bit Timer1 \\
    & \(0=\) Stops 16-bit Timer1
    \end{tabular}
    bit 14 Unimplemented: Read as ' 0 '
    bit 13 TSIDL: Timer1 Stop in Idle Mode bit
    1 = Discontinues module operation when the device enters Idle mode
    \(0=\) Continues module operation in Idle mode
    bit 12-7 Unimplemented: Read as ' 0 '
    bit 6 TGATE: Timer1 Gated Time Accumulation Enable bit
    When TCS = 1:
    This bit is ignored.
    When TCS = 0 :
    1 = Gated time accumulation is enabled
    \(0=\) Gated time accumulation is disabled
    bit 5-4 TCKPS<1:0>: Timer1 Input Clock Prescale Select bits
    \(11=1: 256\)
    \(10=1: 64\)
    \(01=1: 8\)
    \(00=1: 1\)
    bit 3 Unimplemented: Read as ' 0 '
    bit 2 TSYNC: Timer1 External Clock Input Synchronization Select bit \({ }^{(1)}\)
    When TCS = 1:
    1 = External clock input is synchronized
    \(0=\) External clock input is not synchronized
    When TCS = 0 :
    This bit is ignored.
    bit 1 TCS: Timer1 Clock Source Select bit \({ }^{(1)}\)
    1 = External clock is from pin, T1CK (on the rising edge)
    0 = Internal clock (Fp)
    bit \(0 \quad\) Unimplemented: Read as ' 0 '
    Note 1: When Timer1 is enabled in External Synchronous Counter mode (TCS = 1, TSYNC = 1, TON = 1), any attempts by user software to write to the TMR1 register are ignored.

    \subsection*{13.0 TIMER2/3 AND TIMER4/5}

    Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
    2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

    These modules are 32-bit timers, which can also be configured as four independent, 16-bit timers with selectable operating modes.

    As a 32-bit timer, Timer2/3 and Timer4/5 operate in the following three modes:
    - Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
    - Single 32-Bit Timer
    - Single 32-Bit Synchronous Counter

    They also support these features:
    - Timer Gate Operation
    - Selectable Prescaler Settings
    - Timer Operation during Idle and Sleep modes
    - Interrupt on a 32-Bit Period Register Match
    - Time Base for Input Capture and Output Compare Modules
    - ADC1 Event Trigger (Timer2/3 only)

    Individually, all eight of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON and T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. The T3CON and T5CON registers are shown in Register 13-2.
    For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (Isw). Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.
    Note: For 32-bit operation, the T3CON and T5CON control bits are ignored. Only the T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

    Block diagrams for the Type B and Type C timers are shown in Figure 13-1 and Figure 13-2, respectively.
    A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

    Note: Only Timer2, Timer3, Timer4 and Timer5 can trigger a DMA data transfer.

    FIGURE 13-1: TYPE B TIMER BLOCK DIAGRAM (x = 2 AND 4)
    

    Note 1: FP is the peripheral clock.

    FIGURE 13-2: TYPE C TIMER BLOCK DIAGRAM (x = 3 AND 5)
    

    Note 1: FP is the peripheral clock.
    2: The ADC trigger is available on TMR3 and TMR5 only.

    FIGURE 13-3: TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)
    

    \subsection*{13.1 Timer2/3 and Timer4/5 Control \\ Registers}

    REGISTER 13-1: TxCON (T2CON AND T4CON) CONTROL REGISTER
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & U-0 & R/W-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline TON & - & TSIDL & - & - & - & - & - \\
    \hline \multicolumn{8}{|l|}{bit 15 bit 8} \\
    \hline U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & U-0 & R/W-0 & U-0 \\
    \hline - & TGATE & TCKPS1 & TCKPS0 & T32 & - & TCS \({ }^{(1)}\) & - \\
    \hline \multicolumn{8}{|l|}{\begin{tabular}{|l|l|l|l|l|l|lll} 
    \\
    bit
    \end{tabular}} \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    \begin{tabular}{|c|c|}
    \hline bit 15 & TON: Timerx On bit \\
    \hline & When T32 = 1: \\
    \hline & 1 = Starts 32-bit Timerx/y \\
    \hline & 0 = Stops 32-bit Timerx/y \\
    \hline & When T32 = 0: \\
    \hline & 1 = Starts 16-bit Timerx \\
    \hline & 0 = Stops 16-bit Timerx \\
    \hline
    \end{tabular}
    bit \(14 \quad\) Unimplemented: Read as ' 0 '
    bit 13 TSIDL: Timerx Stop in Idle Mode bit
    1 = Discontinues module operation when the device enters Idle mode
    0 = Continues module operation in Idle mode
    bit 12-7 Unimplemented: Read as ' 0 '
    bit 6 TGATE: Timerx Gated Time Accumulation Enable bit
    When TCS = 1:
    This bit is ignored.
    When TCS = 0:
    1 = Gated time accumulation is enabled
    \(0=\) Gated time accumulation is disabled
    bit 5-4 TCKPS<1:0>: Timerx Input Clock Prescale Select bits
    \(11=1: 256\)
    \(10=1: 64\)
    \(01=1: 8\)
    \(00=1: 1\)
    bit \(3 \quad\) T32: 32-Bit Timer Mode Select bit
    1 = Timerx and Timery form a single 32-bit timer
    \(0=\) Timerx and Timery act as two 16-bit timers
    bit 2 Unimplemented: Read as ' 0 '
    bit \(1 \quad\) TCS: Timerx Clock Source Select bit \({ }^{(1)}\)
    1 = External clock is from pin, TxCK (on the rising edge)
    0 = Internal clock (Fp)
    bit \(0 \quad\) Unimplemented: Read as ' 0 '
    Note 1: The TxCK pin is not available on all timers. Refer to the "Pin Diagrams" section for the available pins.

    REGISTER 13-2: TyCON (T3CON AND T5CON) CONTROL REGISTER
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & U-0 & R/W-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline TON \({ }^{(1)}\) & - & TSIDL \({ }^{(2)}\) & - & - & - & - & - \\
    \hline \multicolumn{8}{|l|}{bit 15 bit 8} \\
    \hline U-0 & R/W-0 & R/W-0 & R/W-0 & U-0 & U-0 & R/W-0 & U-0 \\
    \hline - & TGATE \({ }^{(1)}\) & TCKPS1 \({ }^{(1)}\) & TCKPS0 \({ }^{(1)}\) & - & - & TCS \({ }^{(1,3)}\) & - \\
    \hline \multicolumn{8}{|l|}{bit \(7 \times\) bit 0} \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & 0 ' \(=\) Bit is cleared
    \end{tabular}
    bit \(15 \quad\) TON: Timery On bit \({ }^{(1)}\)
    1 = Starts 16-bit Timery
    0 = Stops 16-bit Timery
    bit 14 Unimplemented: Read as ' 0 '
    bit 13 TSIDL: Timery Stop in Idle Mode bit \({ }^{(2)}\)
    1 = Discontinues module operation when the device enters an Idle mode
    \(0=\) Continues module operation in an Idle mode
    bit 12-7 Unimplemented: Read as ' 0 '
    bit 6 TGATE: Timery Gated Time Accumulation Enable bit \({ }^{(1)}\)
    When TCS = 1:
    This bit is ignored.
    When TCS = 0:
    1 = Gated time accumulation is enabled
    \(0=\) Gated time accumulation is disabled
    bit 5-4 \(\quad\) TCKPS<1:0>: Timery Input Clock Prescale Select bits \({ }^{(1)}\)
    \(11=1: 256\)
    \(10=1: 64\)
    \(01=1: 8\)
    \(00=1: 1\)
    bit 3-2 Unimplemented: Read as ' 0 '
    bit 1 TCS: Timery Clock Source Select bit \({ }^{(1,3)}\)
    1 = External clock is from pin, TyCK (on the rising edge)
    0 = Internal clock (Fp)
    bit \(0 \quad\) Unimplemented: Read as ' 0 '
    Note 1: When 32-bit operation is enabled ( \(\mathrm{T} 2 \mathrm{CON}<3>=1\) ), these bits have no effect on Timery operation; all timer functions are set through TxCON.
    2: When 32 -bit timer operation is enabled \((\mathrm{T} 32=1)\) in the Timerx Control register \((\mathrm{TxCON}<3>)\), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.
    3: The TyCK pin is not available on all timers. See the "Pin Diagrams" section for the available pins.

    \section*{dsPIC33EVXXXGM00X/10X FAMILY}

    NOTES:

    \subsection*{14.0 DEADMAN TIMER (DMT)}

    Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Deadman Timer (DMT)" (DS70005155) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
    2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

    The primary function of the Deadman Timer (DMT) is to reset the processor in the event of a software malfunction. The DMT, which works on the system clock, is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs, until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.
    DMT can be enabled in the Configuration fuse or by software in the DMTCON register by setting the ON bit. The DMT consists of a 32-bit counter with a time-out count match value, as specified by the two 16 -bit Configuration Fuse registers: FDMTCNTL and FDMTCNTH.

    A DMT is typically used in mission-critical, and safetycritical applications, where any single failure of the software functionality and sequencing must be detected.
    Figure \(14-1\) shows a block diagram of the Deadman Timer module.

    FIGURE 14-1: DEADMAN TIMER BLOCK DIAGRAM
    

    Note 1: DMT Max Count is controlled by the initial value of the FDMTCNTL and FDMTCNTH Configuration registers.
    2: DMT window interval is controlled by the value of the FDMTINTVL and FDMTINTVH Configuration registers.

    \subsection*{14.1 Deadman Timer Control Registers}

    \section*{REGISTER 14-1: DMTCON: DEADMAN TIMER CONTROL REGISTER}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline ON \({ }^{(1)}\) & - & - & - & - & - & - & - \\
    \hline \multicolumn{8}{|l|}{bit \(15 \times\) bit 8} \\
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline - & - & - & - & - & - & - & - \\
    \hline \multicolumn{8}{|l|}{bit \(7 \times\) bit 0} \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' \(=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15 ON: DMT Module Enable bit \({ }^{(1)}\)
    1 = Deadman Timer module is enabled
    0 = Deadman Timer module is not enabled
    bit 14-0 Unimplemented: Read as ' 0 '
    Note 1: This bit has control only when DMTEN \(=0\) in the FDMT register.

    REGISTER 14-2: DMTPRECLR: DEADMAN TIMER PRECLEAR REGISTER
    \begin{tabular}{|lllllll|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0
    \end{tabular}\(\quad\) R/W-0 \begin{tabular}{llll|}
    \hline & STEP1<7:0> & & \\
    \hline bit 15 & & & \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline - & - & - & - & - & - & - & - \\
    \hline \multicolumn{8}{|l|}{bit \(7 \times\) bit 0} \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & ' 1 ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-8
    STEP1<7:0>: DMT Preclear Enable bits
    01000000 = Enables the Deadman Timer preclear (Step 1)
    All Other
    Write Patterns \(=\) Sets the BAD1 flag; these bits are cleared when a DMT Reset event occurs. STEP1<7:0> bits are also cleared if the STEP2<7:0> bits are loaded with the correct value in the correct sequence.
    bit 7-0 Unimplemented: Read as ' 0 '

    \section*{REGISTER 14-3: DMTCLR: DEADMAN TIMER CLEAR REGISTER}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline- & - & - & - & - & - & - & - \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|lllllll|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0
    \end{tabular} R/W-0 \begin{tabular}{llll|}
    \hline & STEP2<7:0> & & \\
    \hline bit 7 & & & \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    \begin{tabular}{|c|c|}
    \hline bit 15-8 & Unimplemented: Read as ' 0 ' \\
    \hline \multirow[t]{4}{*}{bit 7-0} & STEP2<7:0>: DMT Clear Timer bits \\
    \hline & \(00001000=\) Clears STEP1<7:0>, STEP2<7:0> and the Deadman Timer if preceded by the correct loading of the STEP1<7:0> bits in the correct sequence. The write to these bits may be verified by reading the DMTCNTL/H register and observing the counter being reset. \\
    \hline & All Other \\
    \hline & Write Patterns \(=\) Sets the BAD2 bit; the value of STEP1<7:0> will remain unchanged and the new value being written to STEP2<7:0> will be captured. These bits are cleared when a DMT Reset event occurs. \\
    \hline
    \end{tabular}

    \section*{REGISTER 14-4: DMTSTAT: DEADMAN TIMER STATUS REGISTER}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline- & - & - & - & - & - & - & - \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R-0, HC & R-0, HC & R-0, HC & U-0 & U-0 & U-0 & U-0 & R-0 \\
    \hline BAD1 & BAD2 & DMTEVENT & - & - & - & - & WINOPN \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & \(H C=\) Hardware Clearable bit & \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared \(\quad \mathrm{x}=\) Bit is unknown \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|}
    \hline bit 15-8 & Unimplemented: Read as '0' \\
    \hline \multirow[t]{3}{*}{bit 7} & BAD1: Deadman Timer Bad STEP1<7:0> Value Detect bit \\
    \hline & \(1=\) Incorrect STEP1<7:0> value was detected \\
    \hline & \(0=\) Incorrect STEP1<7:0> value was not detected \\
    \hline \multirow[t]{3}{*}{bit 6} & BAD2: Deadman Timer Bad STEP2<7:0> Value Detect bit \\
    \hline & 1 = Incorrect STEP2<7:0> value was detected \\
    \hline & \(0=\) Incorrect STEP2<7:0> value was not detected \\
    \hline \multirow[t]{3}{*}{bit 5} & DMTEVENT: Deadman Timer Event bit \\
    \hline & \(1=\) Deadman Timer event was detected (counter expired, or bad STEP1<7:0> or STEP2<7:0> value was entered prior to counter increment) \\
    \hline & \(0=\) Deadman Timer event was not detected \\
    \hline
    \end{tabular}
    bit 4-1 Unimplemented: Read as ' 0 '
    bit \(0 \quad\) WINOPN: Deadman Timer Clear Window bit
    1 = Deadman Timer clear window is open
    \(0=\) Deadman Timer clear window is not open

    \section*{REGISTER 14-5: DMTCNTL: DEADMAN TIMER COUNT REGISTER LOW}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{COUNTER<15:8>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{COUNTER<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' \(=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-0
    COUNTER<15:0>: Read Current Contents of Lower DMT Counter bits

    \section*{REGISTER 14-6: DMTCNTH: DEADMAN TIMER COUNT REGISTER HIGH}
    \begin{tabular}{|llllllll|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline & & & COUNTER<31:24> & & & \\
    \hline bit 15 & & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|llllllll|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline & & COUNTER<23:16> & & & \\
    \hline bit 7 & & & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & & \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown 0
    bit 15-0
    COUNTER<31:16>: Read Current Contents of Higher DMT Counter bits

    \section*{REGISTER 14-7: DMTPSCNTL: DMT POST CONFIGURE COUNT STATUS REGISTER LOW}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{PSCNT<15:8>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{PSCNT<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-0 PSCNT<15:0>: Lower DMT Instruction Count Value Configuration Status bits This is always the value of the FDMTCNTL Configuration register.

    \section*{REGISTER 14-8: DMTPSCNTH: DMT POST CONFIGURE COUNT STATUS REGISTER HIGH}
    \begin{tabular}{|llllllll|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline & & & \(P S C N T<31: 24>\) & & & \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|llllllll|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline & & & \(P S C N T<23: 16>\) & & & \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-0
    PSCNT<31:16>: Higher DMT Instruction Count Value Configuration Status bits
    This is always the value of the FDMTCNTH Configuration register.

    \section*{REGISTER 14-9: DMTPSINTVL: DMT POST CONFIGURE INTERVAL STATUS REGISTER LOW}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{PSINTV<15:8>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{PSINTV<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-0 PSINTV<15:0>: Lower DMT Window Interval Configuration Status bits This is always the value of the FDMTINTVL Configuration register.

    \section*{REGISTER 14-10: DMTPSINTVH: DMT POST CONFIGURE INTERVAL STATUS REGISTER HIGH}
    \begin{tabular}{|llllllll|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline & & & PSINTV<31:24> & & & \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|llllllll|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline & & & PSINTV<23:16> & & & \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{4}{|l|}{Legend:} \\
    \hline \(\mathrm{R}=\) Readable bit & W = Writable bit & \(\mathrm{U}=\) Unimplemente & as '0' \\
    \hline \(-\mathrm{n}=\) Value at POR & ' 1 ' = Bit is set & ' 0 ' = Bit is cleared & \(x=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-0 PSINTV<31:16>: Higher DMT Window Interval Configuration Status bits
    This is always the value of the FDMTINTVH Configuration register.

    REGISTER 14-11: DMTHOLDREG: DMT HOLD REGISTER \({ }^{(1)}\)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{UPRCNT<15:8>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{UPRCNT<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll}
    \hline Legend: & & \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' \(=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-0 UPRCNT<15:0>: Value of the DMTCNTH register when DMTCNTL and DMTCNTH were Last Read bits
    Note 1: The DMTHOLDREG register is initialized to ' 0 ' on Reset, and is only loaded when the DMTCNTL and DMTCNTH registers are read.

    \subsection*{15.0 INPUT CAPTURE}

    Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Input Capture" (DS70000352) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
    2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

    The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33EVXXXGM00X/10X family devices support 4 input capture channels.
    Key features of the input capture module include:
    - Hardware-Configurable for 32-Bit Operation in All Modes by Cascading Two Adjacent modules
    - Synchronous and Trigger Modes of Output Compare Operation, with up to 31 User-Selectable Trigger/Sync Sources Available
    - A 4-Level FIFO Buffer for Capturing and Holding Timer Values for Several Events
    - Configurable Interrupt Generation
    - Up to Six Clock Sources Available for Each Module, Driving a Separate Internal 16-Bit Counter

    Figure 15-1 shows a block diagram of the Input capture module.

    FIGURE 15-1: INPUT CAPTURE x MODULE BLOCK DIAGRAM
    

    Note 1: The trigger/sync source is enabled by default and is set to Timer3 as a source. This timer must be enabled for proper ICx module operation or the trigger/sync source must be changed to another source option.

    \subsection*{15.1 Input Capture Control Registers}

    \section*{REGISTER 15-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & U-0 & U-0 \\
    \hline- & - & ICSIDL & ICTSEL2 & ICTSEL1 & ICTSEL0 & - & - \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline U-0 & R/W-0 & R/W-0 & R/HC/HS-0 & R/HC/HS-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & ICI1 & ICIO & ICOV & ICBNE & ICM2 & ICM1 & ICM0 \\
    \hline bit 7 & \multicolumn{7}{|l|}{} & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & HC = Hardware Clearable bit & HS = Hardware Settable bit \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared \(\quad \mathrm{x}=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13 ICSIDL: Input Capture \(x\) Stop in Idle Mode Control bit
    1 = Input Capture \(x\) will halt in CPU Idle mode
    \(0=\) Input Capture \(x\) will continue to operate in CPU Idle mode
    bit 12-10
    ICTSEL<2:0>: Input Capture x Timer Select bits
    \(111=\) Peripheral clock (FP) is the clock source of the ICx
    110 = Reserved
    \(101=\) Reserved
    \(100=\) T1CLK is the clock source of the ICx (only the synchronous clock is supported)
    011 = T5CLK is the clock source of the ICx
    \(010=\) T4CLK is the clock source of the ICx
    \(001=\) T2CLK is the clock source of the ICx
    \(000=\) T3CLK is the clock source of the ICx
    bit 9-7 Unimplemented: Read as ' 0 '
    bit 6-5 \(\quad|C|<1: 0>\) : Number of Captures per Interrupt Select bits (this field is not used if \(I C M<2: 0>=001\) or 111)
    \(11=\) Interrupt on every fourth capture event
    \(10=\) Interrupt on every third capture event
    01 = Interrupt on every second capture event
    00 = Interrupt on every capture event
    bit 4 ICOV: Input Capture \(\times\) Overflow Status Flag bit (read-only)
    1 = Input Capture x buffer overflow has occurred
    \(0=\) Input Capture x buffer overflow has not occurred
    bit 3 ICBNE: Input Capture \(x\) Buffer Not Empty Status bit (read-only)
    \(1=\) Input Capture \(\times\) buffer is not empty, at least one more capture value can be read
    \(0=\) Input Capture \(x\) buffer is empty
    bit 2-0 ICM<2:0>: Input Capture \(\times\) Mode Select bits
    \(111=\) Input Capture \(x\) functions as an interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
    \(110=\) Unused (module is disabled)
    101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
    \(100=\) Capture mode, every 4th rising edge (Prescaler Capture mode)
    011 = Capture mode, every rising edge (Simple Capture mode)
    010 = Capture mode, every falling edge (Simple Capture mode)
    001 = Capture mode, every edge, rising and falling (Edge Detect mode ( \(\mathrm{ICl}<1: 0>\) ) is not used in this mode)
    \(000=\) Input Capture x module is turned off

    \section*{REGISTER 15-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & R/W-0 \\
    \hline - & - & - & - & - & - & - & IC32 \({ }^{(1)}\) \\
    \hline \multicolumn{8}{|l|}{bit 15 bit 8} \\
    \hline R/W-0 & R/W/HS-0 & U-0 & R/W-0 & R/W-1 & R/W-1 & R/W-0 & R/W-1 \\
    \hline ICTRIG \({ }^{(2)}\) & TRIGSTAT \({ }^{(3)}\) & - & SYNCSEL4 \({ }^{(4)}\) & SYNCSEL3 \({ }^{(4)}\) & SYNCSEL2 \({ }^{(4)}\) & SYNCSEL1 \({ }^{(4)}\) & SYNCSEL0 \({ }^{(4)}\) \\
    \hline \multicolumn{8}{|l|}{bit \(7 \times 0\)} \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & HS = Hardware Settable bit & \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & ' 0 ' = Bit is cleared \\
    \hline
    \end{tabular}
    bit 15-9 Unimplemented: Read as ' 0 '
    bit \(8 \quad\) IC32: Input Capture \(\times 32\)-Bit Timer Mode Select bit (Cascade mode) \({ }^{(1)}\)
    1 = Odd ICx and even ICx form a single 32-bit input capture module
    0 = Cascade module operation is disabled
    bit \(7 \quad\) ICTRIG: Input Capture \(\times\) Trigger Operation Select bit \({ }^{(2)}\)
    1 = Input source is used to trigger the input capture timer (Trigger mode)
    \(0=\) Input source is used to synchronize the input capture timer to the timer of another module (Synchronization mode)
    bit 6 TRIGSTAT: Timer Trigger Status bit \({ }^{(3)}\)
    1 = ICxTMR has been triggered and is running
    \(0=\) ICxTMR has not been triggered and is being held clear
    bit \(5 \quad\) Unimplemented: Read as ' 0 '
    Note 1: The IC32 bit in both the odd and even ICx must be set to enable Cascade mode.
    2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
    3: This bit is set by the selected input source (selected by the SYNCSEL<4:0> bits); it can be read, set and cleared in software.
    4: Do not use the ICx module as its own sync or trigger source.
    5: This option should only be selected as a trigger source and not as a synchronization source.
    6: When the source ICx timer rolls over, then in the next clock cycle, trigger or synchronization occurs.

    \section*{REGISTER 15-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)}
    bit 4-0 SYNCSEL<4:0>: Input Source Select for Synchronization and Trigger Operation bits \({ }^{(4)}\)
    ```

    11111 = Reserved
    11110 = Reserved
    11101 = Reserved
    11100 = CTMU trigger is the source for the capture timer synchronization
    1 1 0 1 1 ~ = ~ A D C 1 ~ i n t e r r u p t ~ i s ~ t h e ~ s o u r c e ~ f o r ~ t h e ~ c a p t u r e ~ t i m e r ~ s y n c h r o n i z a t i o n ~ ( 5 )
    1 1 0 1 0 = A n a l o g ~ C o m p a r a t o r ~ 3 ~ i s ~ t h e ~ s o u r c e ~ f o r ~ t h e ~ c a p t u r e ~ t i m e r ~ s y n c h r o n i z a t i o n ( 5 )
    1 1 0 0 1 ~ = ~ A n a l o g ~ C o m p a r a t o r ~ 2 ~ i s ~ t h e ~ s o u r c e ~ f o r ~ t h e ~ c a p t u r e ~ t i m e r ~ s y n c h r o n i z a t i o n ~ ( 5 )
    11000 = Analog Comparator 1 is the source for the capture timer synchronization (5)
    1 0 1 1 1 ~ = ~ A n a l o g ~ C o m p a r a t o r ~ 5 ~ i s ~ t h e ~ s o u r c e ~ f o r ~ t h e ~ c a p t u r e ~ t i m e r ~ s y n c h r o n i z a t i o n ( 5 )
    10110 = Analog Comparator 4 is the source for the capture timer synchronization (5)
    10101 = Reserved
    10100 = Reserved
    1 0 0 1 1 ~ = ~ I n p u t ~ C a p t u r e ~ 4 ~ i n t e r r u p t ~ i s ~ t h e ~ s o u r c e ~ f o r ~ t h e ~ c a p t u r e ~ t i m e r ~ s y n c h r o n i z a t i o n
    1 0 0 1 0 = ~ I n p u t ~ C a p t u r e ~ 3 ~ i n t e r r u p t ~ i s ~ t h e ~ s o u r c e ~ f o r ~ t h e ~ c a p t u r e ~ t i m e r ~ s y n c h r o n i z a t i o n
    10001 = Input Capture 2 interrupt is the source for the capture timer synchronization
    10000= Input Capture 1 interrupt is the source for the capture timer synchronization
    01111 = GP Timer5 is the source for the capture timer synchronization
    0 1 1 1 0 = G P ~ T i m e r 4 ~ i s ~ t h e ~ s o u r c e ~ f o r ~ t h e ~ c a p t u r e ~ t i m e r ~ s y n c h r o n i z a t i o n
    0 1 1 0 1 = G P ~ T i m e r 3 ~ i s ~ t h e ~ s o u r c e ~ f o r ~ t h e ~ c a p t u r e ~ t i m e r ~ s y n c h r o n i z a t i o n
    01100 = GP Timer2 is the source for the capture timer synchronization
    01011 = GP Timer1 is the source for the capture timer synchronization
    01010 = Reserved
    01001 = Reserved
    01000 = Input Capture 4 is the source for the capture timer synchronization(6)
    0 0 1 1 1 = I n p u t ~ C a p t u r e ~ 3 ~ i s ~ t h e ~ s o u r c e ~ f o r ~ t h e ~ c a p t u r e ~ t i m e r ~ s y n c h r o n i z a t i o n ( 6 )
    0 0 1 1 0 = ~ I n p u t ~ C a p t u r e ~ 2 ~ i s ~ t h e ~ s o u r c e ~ f o r ~ t h e ~ c a p t u r e ~ t i m e r ~ s y n c h r o n i z a t i o n ( 6 )
    00101 = Input Capture 1 is the source for the capture timer synchronization (6)
    00100 = Output Compare 4 is the source for the capture timer synchronization
    00011 = Output Compare 3 is the source for the capture timer synchronization
    00010=Output Compare 2 is the source for the capture timer synchronization
    00001 = Output Compare 1 is the source for the capture timer synchronization
    00000=Reserved

    ```

    Note 1: The IC32 bit in both the odd and even ICx must be set to enable Cascade mode.
    2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
    3: This bit is set by the selected input source (selected by the SYNCSEL<4:0> bits); it can be read, set and cleared in software.
    4: Do not use the ICx module as its own sync or trigger source.
    5: This option should only be selected as a trigger source and not as a synchronization source.
    6: When the source ICx timer rolls over, then in the next clock cycle, trigger or synchronization occurs.

    \subsection*{16.0 OUTPUT COMPARE}

    Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Output Compare" (DS70005157) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

    2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

    The dsPIC33EVXXXGM00X/10X family devices support up to 4 output compare modules. The output compare module can select one of eight available clock
    sources for its time base. The module compares the value of the timer with the value of one or two Compare registers, depending on the operating mode selected. The state of the output pin changes when the timer value matches the Compare register value. The output compare module generates either a single output pulse, or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.
    Figure 16-1 shows a block diagram of the output compare module.

    Note: For more information on OCxR and OCxRS register restrictions, refer to the "Output Compare" (DS70005157) section in the "dsPIC33/PIC24 Family Reference Manual".

    FIGURE 16-1: OUTPUT COMPARE x MODULE BLOCK DIAGRAM
    

    Note 1: The trigger/sync source is enabled by default and is set to Timer2 as a source. This timer must be enabled for proper OCx module operation or the trigger/sync source must be changed to another source option.

    \subsection*{16.1 Output Compare Control Registers}

    REGISTER 16-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & U-0 & U-0 \\
    \hline- & - & OCSIDL & OCTSEL2 & OCTSEL1 & OCTSEL0 & - & - \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline \multicolumn{10}{|c|}{ R/W-0 } & U-0 & U-0 & R/W-0, HSC & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline ENFLTA & - & - & OCFLTA & TRIGMODE & OCM2 & OCM1 & OCM0 \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|}
    \hline Legend: & \multicolumn{3}{|l|}{HSC = Hardware Settable/Clearable bit} \\
    \hline \(\mathrm{R}=\) Readable bit & W = Writable bit & \(\mathrm{U}=\) Unimplemente & as '0' \\
    \hline -n = Value at POR & ' 1 ' = Bit is set & ' 0 ' = Bit is cleared & \(x=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13 OCSIDL: Output Compare \(\times\) Stop in Idle Mode Control bit
    1 = Output Compare \(x\) halts in CPU Idle mode
    \(0=\) Output Compare \(x\) continues to operate in CPU Idle mode
    bit 12-10
    OCTSEL<2:0>: Output Compare x Clock Select bits
    111 = Peripheral clock (FP)
    \(110=\) Reserved
    101 = Reserved
    \(100=\) T1CLK is the clock source of the OCx (only the synchronous clock is supported)
    \(011=\) T5CLK is the clock source of the OCx
    \(010=\) T4CLK is the clock source of the OCx
    \(001=\) T3CLK is the clock source of the OCx
    \(000=\) T2CLK is the clock source of the OCx
    bit 9-8 Unimplemented: Read as ' 0 '
    bit 7 ENFLTA: Output Compare \(x\) Fault A Input Enable bit
    1 = Output Compare Fault A (OCFA) input is enabled
    \(0=\) Output Compare Fault A (OCFA) input is disabled
    bit 6-5 Unimplemented: Read as '0'
    bit 4 OCFLTA: PWM Fault A Condition Status bit
    1 = PWM Fault A condition on the OCFA pin has occurred
    \(0=\) PWM Fault A condition on the OCFA pin has not occurred
    bit 3 TRIGMODE: Trigger Status Mode Select bit
    1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software
    \(0=\) TRIGSTAT is cleared only by software
    Note 1: OCxR and OCxRS are double-buffered in PWM mode only.

    \section*{REGISTER 16-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1 (CONTINUED)}
    bit 2-0 \(\quad \mathbf{O C M}<\mathbf{2 : 0}\) : Output Compare \(\times\) Mode Select bits
    111 = Center-Aligned PWM mode: Output sets high when OCxTMR \(=\) OCxR and sets low when OCxTMR \(=\) OCxRS \({ }^{(1)}\)
    \(110=\) Edge-Aligned PWM mode: Output sets high when OCxTMR \(=0\) and sets low when OCxTMR = OCxR \({ }^{(1)}\)
    101 = Double Compare Continuous Pulse mode: Initializes OCx pin low, toggles OCx state continuously on alternate matches of OCxR and OCxRS
    \(100=\) Double Compare Single-Shot mode: Initializes OCx pin low, toggles OCx state on matches of OCxR and OCxRS for one cycle
    011 = Single Compare mode: Compare event with OCxR, continuously toggles OCx pin
    010 = Single Compare Single-Shot mode: Initializes OCx pin high, compare event with OCxR, forces OCx pin low
    001 = Single Compare Single-Shot mode: Initializes OCx pin low, compare event with OCxR, forces OCx pin high
    \(000=\) Output compare channel is disabled
    Note 1: OCxR and OCxRS are double-buffered in PWM mode only.

    \section*{REGISTER 16-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & U-0 & U-0 & U-0 & R/W-0 \\
    \hline FLTMD & FLTOUT & FLTTRIEN & OCINV & - & - & - & OC32 \\
    \hline bit 15 \\
    \begin{tabular}{|c|c|c|cc|c|c|c|}
    \hline R/W-0 & R/W-0, HS & R/W-0 & R/W-0 & R/W-1 & R/W-1 & R/W-0 & R/W-0 \\
    \hline OCTRIG & TRIGSTAT & OCTRIS & SYNCSEL4 & SYNCSEL3 & SYNCSEL2 & SYNCSEL1 & SYNCSEL0 \\
    \hline bit 7 &
    \end{tabular}
    \end{tabular}\(.\)\begin{tabular}{ll} 
    bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & HS = Hardware Settable bit & \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared \(\quad \mathrm{x}=\) Bit is unknown \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|}
    \hline \multirow[t]{2}{*}{bit 15} & FLTMD: Fault Mode Select bit \\
    \hline & \[
    \begin{aligned}
    & 1=\text { Fault mode is maintained until the Fault source is removed; the OCFLTA bit is cleared in software } \\
    & \text { and a new PWM period starts } \\
    & 0=\text { Fault mode is maintained until the Fault source is removed and a new PWM period starts }
    \end{aligned}
    \] \\
    \hline \multirow[t]{2}{*}{bit 14} & FLTOUT: Fault Out bit \\
    \hline & \begin{tabular}{l}
    1 = PWM output is driven high on a Fault \\
    \(0=\) PWM output is driven low on a Fault
    \end{tabular} \\
    \hline \multirow[t]{2}{*}{bit 13} & FLTTRIEN: Fault Output State Select bit \\
    \hline & \begin{tabular}{l}
    \(1=\mathrm{OCx}\) pin is tri-stated on a Fault condition \\
    \(0=\) OCx pin I/O state is defined by the FLTOUT bit on a Fault condition
    \end{tabular} \\
    \hline \multirow[t]{3}{*}{bit 12} & OCINV: Output Compare x Invert bit \\
    \hline & \(1=\) OCx output is inverted \\
    \hline & \(0=\) OCx output is not inverted \\
    \hline bit 11-9 & Unimplemented: Read as ' 0 ' \\
    \hline \multirow[t]{3}{*}{bit 8} & OC32: Cascade Two OCx Modules Enable bit (32-bit operation) \\
    \hline & 1 = Cascade module operation is enabled \\
    \hline & \(0=\) Cascade module operation is disabled \\
    \hline \multirow[t]{3}{*}{bit 7} & OCTRIG: Output Compare x Trigger/Sync Select bit \\
    \hline & 1 = Triggers OCx from the source designated by the SYNCSELx bits \\
    \hline & \(0=\) Synchronizes OCx with the source designated by the SYNCSELx bits \\
    \hline \multirow[t]{3}{*}{bit 6} & TRIGSTAT: Timer Trigger Status bit \\
    \hline & \(1=\) Timer source has been triggered and is running \\
    \hline & \(0=\) Timer source has not been triggered and is being held clear \\
    \hline \multirow[t]{3}{*}{bit 5} & OCTRIS: Output Compare \(\times\) Output Pin Direction Select bit \\
    \hline & 1 = Output Compare x is tri-stated \\
    \hline & \(0=\) Output Compare x module drives the OCx pin \\
    \hline
    \end{tabular}

    Note 1: Do not use the OCx module as its own synchronization or trigger source.
    2: When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.

    \section*{REGISTER 16-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)}
    bit 4-0 SYNCSEL<4:0>: Trigger/Synchronization Source Selection bits
    \(11111=\) OCxRS compare event is used for synchronization
    \(11110=\) INT2 is the source for compare timer synchronization
    \(11101=\) INT1 is the source for compare timer synchronization
    \(11100=\) CTMU Trigger is the source for compare timer synchronization
    11011 = ADC1 interrupt is the source for compare timer synchronization
    \(11010=\) Analog Comparator 3 is the source for compare timer synchronization
    \(11001=\) Analog Comparator 2 is the source for compare timer synchronization
    \(11000=\) Analog Comparator 1 is the source for compare timer synchronization
    10111 = Analog Comparator 5 is the source for compare timer synchronization
    10110 = Analog Comparator 4 is the source for compare timer synchronization
    10101 = Capture timer is unsynchronized
    \(10100=\) Capture timer is unsynchronized
    10011 = Input Capture 4 interrupt is the source for compare timer synchronization
    \(10010=\) Input Capture 3 interrupt is the source for compare timer synchronization
    \(10001=\) Input Capture 2 interrupt is the source for compare timer synchronization
    \(10000=\) Input Capture 1 interrupt is the source for compare timer synchronization
    01111 = GP Timer5 is the source for compare timer synchronization
    \(01110=\) GP Timer4 is the source for compare timer synchronization
    \(01101=\) GP Timer3 is the source for compare timer synchronization
    \(01100=\) GP Timer2 is the source for compare timer synchronization
    01011 = GP Timer1 is the source for compare timer synchronization
    \(01010=\) Compare timer is unsynchronized
    01001 = Compare timer is unsynchronized
    \(01000=\) Capture timer is unsynchronized
    00101 = Compare timer is unsynchronized
    \(00100=\) Output Compare 4 is the source for compare timer synchronization \({ }^{(1,2)}\)
    \(00011=\) Output Compare 3 is the source for compare timer synchronization \({ }^{(1,2)}\)
    \(00010=\) Output Compare 2 is the source for compare timer synchronization \({ }^{(1,2)}\)
    \(00001=\) Output Compare 1 is the source for compare timer synchronization \({ }^{(1,2)}\)
    \(00000=\) Compare timer is unsynchronized
    Note 1: Do not use the OCx module as its own synchronization or trigger source.
    2: When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.

    \section*{dsPIC33EVXXXGM00X/10X FAMILY}

    NOTES:

    \subsection*{17.0 HIGH-SPEED PWM MODULE}

    Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "High-Speed PWM" (DS70645) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
    2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

    The dsPIC33EVXXXGM00X/10X family devices support a dedicated Pulse-Width Modulation (PWM) module with up to 6 outputs.
    The high-speed PWMx module consists of the following major features:
    - Three PWM Generators
    - Two PWM Outputs per PWM Generator
    - Individual Period and Duty Cycle for each PWM Pair
    - Duty Cycle, Dead Time, Phase Shift and

    Frequency Resolution of 8.32 ns
    - Independent Fault and Current-Limit Inputs for Six PWM Outputs
    - Redundant Output
    - Center-Aligned PWM mode
    - Output Override Control
    - Chop mode (also known as Gated mode)
    - Special Event Trigger
    - Prescaler for Input Clock
    - PWMxL and PWMxH Output Pin Swapping
    - Independent PWM Frequency, Duty Cycle and Phase-Shift Changes for each PWM Generator
    - Dead-Time Compensation
    - Enhanced Leading-Edge Blanking (LEB) Functionality
    - Frequency Resolution Enhancement
    - PWM Capture Functionality

    \section*{Note: In Edge-Aligned PWM mode, the duty cycle, dead time, phase shift and frequency resolution are 8.32 ns at 60 MIPS.}

    The high-speed PWMx module contains up to three PWM generators. Each PWM generator provides two PWM outputs: PWMxH and PWMxL. The master time base generator provides a synchronous signal as a common time base to synchronize the various PWM outputs. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limit signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known "safe" state.
    Each PWMx can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWMx module also generates a Special Event Trigger to the ADC module based on the master time base.

    The high-speed PWMx module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNCI1 input pin, that utilizes PPS, can synchronize the high-speed PWMx module with an external signal. The SYNCO1 pin is an output pin that provides a synchronous signal to an external device.
    Figure 17-1 illustrates an architectural overview of the high-speed PWMx module and its interconnection with the CPU and other peripherals.

    \subsection*{17.1 PWM Faults}

    The PWMx module incorporates multiple external Fault inputs as follows:
    - FLT1 and FLT2, available on 28-pin, 44-pin and 64-pin packages, which are remappable using the PPS feature
    - FLT3, available on 44-pin and 64-pin packages, which is available as a fixed pin
    - FLT4-FLT8, available on 64-pin packages, which are available as fixed pins
    - FLT32 is available on a fixed pin on all devices

    These Faults provide a safe and reliable way to safely shut down the PWM outputs when the Fault input is asserted.

    \subsection*{17.1.1 PWM FAULTS AT RESET}

    During any Reset event, the PWMx module maintains ownership of the Class B Fault, FLT32. At Reset, this Fault is enabled in Latched mode to ensure the fail-safe power-up of the application. The application software must clear the PWM Fault before enabling the highspeed motor control PWMx module. To clear the Fault condition, the FLT32 pin must first be pulled low externally or the internal pull-down resistor in the CNPDx register can be enabled.

    > Note: The Fault mode may be changed using the FLTMOD<1:0> bits (FCLCONx<1:0>), regardless of the state of FLT32.

    \subsection*{17.1.2 WRITE-PROTECTED REGISTERS}

    On dsPIC33EVXXXGM00X/10X family devices, write protection is implemented for the IOCONx and FCLCONx registers. The write protection feature prevents any inadvertent writes to these registers. This protection feature can be controlled by the PWMLOCK Configuration bit (FDEVOPT<0>). The default state of the write protection feature is enabled (PWMLOCK = 1). The write protection feature can be disabled by configuring PWMLOCK \(=0\).

    To gain write access to these locked registers, the user application must write two consecutive values (0xABCD and \(0 \times 4321\) ) to the PWMKEY register to perform the unlock operation. The write access to the IOCONx or FCLCONx registers must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. To write to both the IOCONx and FCLCONx registers requires two unlock operations.

    The correct unlocking sequence is described in Example 17-1.

    \section*{EXAMPLE 17-1: PWM1 WRITE-PROTECTED REGISTER UNLOCK SEQUENCE}
    ```

    ; FLT32 pin must be pulled low externally in order to clear and disable the fault
    ; Writing to FCLCON1 register requires unlock sequence
    mov \#0xabcd, w10 ; Load first unlock key to w10 register
    mov \#0x4321, w11 ; Load second unlock key to w11 register
    mov \#0x0000, w0 ; Load desired value of FCLCON1 register in w0
    mov w10, PWMKEY ; Write first unlock key to PWMKEY register
    mov w11, PWMKEY ; Write second unlock key to PWMKEY register
    mov w0, FCLCON1 ; Write desired value to FCLCON1 register
    ; Set PWM ownership and polarity using the IOCON1 register
    ; Writing to IOCON1 register requires unlock sequence
    mov \#0xabcd, w10 ; Load first unlock key to w10 register
    mov \#0x4321, w11 ; Load second unlock key to w11 register
    mov \#0xF000, w0 ; Load desired value of IOCON1 register in w0
    mov w10, PWMKEY ; Write first unlock key to PWMKEY register
    mov w11, PWMKEY ; Write second unlock key to PWMKEY register
    mov w0, IOCON1 ; Write desired value to IOCON1 register

    ```

    FIGURE 17-1: HIGH-SPEED PWMx MODULE ARCHITECTURAL OVERVIEW
    

    Note 1: The PWM interrupts are generated by logically ORing the FLTSTAT, CLSTAT and TRGSTAT status bits for the given PWM generator. For more information, refer to "High-Speed PWM" (DS70645) in the "dsPIC33/PIC24 Family Reference Manual".

    FIGURE 17-2: HIGH-SPEED PWMx MODULE REGISTER INTERCONNECTION DIAGRAM
    

    \subsection*{17.2 PWM Resources}

    Many useful resources are provided on the main product page on the Microchip web site (www.microchip.com) for the devices listed in this data sheet. This product page contains the latest updates and additional information.

    Note: In case the above link is not accessible, enter this URL in your browser: http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

    \subsection*{17.2.1 KEY RESOURCES}
    - "High-Speed PWM" (DS70645) in the "dsPIC33/ PIC24 Family Reference Manual"
    - Code Samples
    - Application Notes
    - Software Libraries
    - Webinars
    - All Related"dsPIC33/PIC24 Family Reference Manual" Sections
    - Development Tools

    \subsection*{17.3 PWMx Control Registers}

    REGISTER 17-1: PTCON: PWMx TIME BASE CONTROL REGISTER
    
    \begin{tabular}{|lll|}
    \hline Legend: & HC = Hardware Clearable bit & \(H S=\) Hardware Settable bit \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared \(\quad x=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15 PTEN: PWMx Module Enable bit
    1 = PWMx module is enabled
    \(0=\mathrm{PWMx}\) module is disabled
    bit 14 Unimplemented: Read as ' 0 '
    bit 13 PTSIDL: PWMx Time Base Stop in Idle Mode bit
    1 = PWMx time base halts in CPU Idle mode
    \(0=\) PWMx time base runs in CPU Idle mode
    bit 12 SESTAT: Special Event Interrupt Status bit
    1 = Special event interrupt is pending
    \(0=\) Special event interrupt is not pending
    bit 11 SEIEN: Special Event Interrupt Enable bit
    1 = Special event interrupt is enabled
    \(0=\) Special event interrupt is disabled
    bit 10 EIPU: Enable Immediate Period Updates bit \({ }^{(1)}\)
    1 = Active Period register is updated immediately
    \(0=\) Active Period register updates occur on PWMx cycle boundaries
    bit 9 SYNCPOL: Synchronize Input and Output Polarity bit \({ }^{(1)}\)
    1 = SYNCI1/SYNCO1 polarity is inverted (active-low)
    \(0=\) SYNCI1/SYNCO1 is active-high
    bit 8 SYNCOEN: Primary Time Base Sync Enable bit \({ }^{(1)}\)
    1 = SYNCO1 output is enabled
    \(0=\) SYNCO1 output is disabled
    bit \(7 \quad\) SYNCEN: External Time Base Synchronization Enable bit \({ }^{(1)}\)
    1 = External synchronization of primary time base is enabled
    \(0=\) External synchronization of primary time base is disabled
    Note 1: These bits should be changed only when PTEN \(=0\). In addition, when using the SYNCI1 feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

    \section*{REGISTER 17-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)}
    bit 6-4 SYNCSRC<2:0>: Synchronous Source Selection bits \({ }^{(1)}\)
    111 = Reserved
    -
    -
    -
    \(100=\) Reserved
    011 = Reserved
    010 = Reserved
    001 = Reserved
    \(000=\) SYNCI 1 input from PPS
    bit 3-0 SEVTPS<3:0>: Special Event Trigger Output Postscaler Select bits \({ }^{(1)}\)
    \(1111=1: 16\) postscaler generates a Special Event Trigger on every sixteenth compare match event
    -
    -
    -
    \(0001=1: 2\) postscaler generates a Special Event Trigger on every second compare match event \(0000=1: 1\) postscaler generates a Special Event Trigger on every compare match event

    Note 1: These bits should be changed only when PTEN \(=0\). In addition, when using the SYNCI1 feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

    REGISTER 17-2: PTCON2: PWMx PRIMARY MASTER CLOCK DIVIDER SELECT REGISTER
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline- & - & - & - & - & - & - & - \\
    \hline bit 15 & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|cc|}
    \hline \multicolumn{9}{|c|}{\(\mathrm{U}-0\)} & U-0 & U-0 & U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & - & - & - & & PCLKDIV<2:0>(1) & \\
    \hline bit 7
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & & \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared \(\quad x=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-3 Unimplemented: Read as ' 0 '
    bit 2-0 PCLKDIV<2:0>: PWMx Input Clock Prescaler (Divider) Select bits \({ }^{(1)}\)
    111 = Reserved
    \(110=\) Divide-by-64
    101 = Divide-by-32
    100 = Divide-by-16
    011 = Divide-by-8
    \(010=\) Divide-by-4
    001 = Divide-by-2
    000 = Divide-by-1, maximum PWMx timing resolution (power-on default)
    Note 1: These bits should be changed only when PTEN \(=0\). Changing the clock selection during operation will yield unpredictable results.

    \section*{REGISTER 17-3: PTPER: PWMx PRIMARY MASTER TIME BASE PERIOD REGISTER}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-1 \\
    \hline \multicolumn{8}{|c|}{PTPER<15:8>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{PTPER<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}
    \[
    \begin{array}{|lll}
    \hline \text { Legend: } & & \\
    R=\text { Readable bit } & W=\text { Writable bit } & U=\text { Unimplemented bit, read as ' } 0 \text { ' } \\
    -n=\text { Value at POR } & ' 1 '=\text { Bit is set } & ' 0 \text { ' = Bit is cleared } \quad x=\text { Bit is unknown } \\
    \hline
    \end{array}
    \]

    PTPER<15:0>: Primary Master Time Base (PMTMR) Period Value bits

    \section*{REGISTER 17-4: SEVTCMP: PWMx PRIMARY SPECIAL EVENT COMPARE REGISTER}
    \begin{tabular}{|llllllll|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline & & SEVTCMP<15:8> & & & \\
    \hline bit 15 & & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|llllllll|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline & & SEVTCMP<7:0> & & & \\
    \hline bit 7 & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{|c|c|c|c|}
    \hline \(\mathrm{R}=\) Readable bit & W = Writable bit & \(\mathrm{U}=\) Unimplement & as '0' \\
    \hline -n = Value at POR & ' 1 ' = Bit is set & ' 0 ' = Bit is cleared & \(x=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-0
    SEVTCMP<15:0>: Special Event Compare Count Value bits

    \section*{REGISTER 17-5: CHOP: PWMx CHOP CLOCK GENERATOR REGISTER}
    \begin{tabular}{|l|c|c|c|c|c|c|r|}
    \hline \multicolumn{1}{|c}{ R/W-0 } & U-0 & U-0 & U-0 & U-0 & U-0 & R/W-0 & R/W-0 \\
    \hline CHPCLKEN & - & - & - & - & - & CHOPCLK9 & CHOPCLK8 \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline \multicolumn{1}{|c}{ R/W-0 } & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline CHOPCLK7 & CHOPCLK6 & CHOPCLK5 & CHOPCLK4 & CHOPCLK3 & CHOPCLK2 & CHOPCLK1 & CHOPCLK0 \\
    \hline bit 7 & & & & & & bit 0 \\
    \hline
    \end{tabular}

    Legend:
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}
    bit 15 CHPCLKEN: Enable Chop Clock Generator bit
    1 = Chop clock generator is enabled
    \(0=\) Chop clock generator is disabled
    bit 14-10 Unimplemented: Read as ' 0 '
    bit 9-0 CHOPCLK<9:0>: Chop Clock Divider bits
    The frequency of the chop clock signal is given by the following expression:
    Chop Frequency \(=(\) FP/PCLKDIV<2:0>)/(CHOPCLK<9:0> + 1)

    REGISTER 17-6: MDC: PWMx MASTER DUTY CYCLE REGISTER
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{MDC<15:8>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{MDC<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll}
    \hline Legend: & & \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(\prime 0\) ' \(=\) Bit is cleared \\
    \hline
    \end{tabular}
    bit 15-0
    MDC<15:0>: PWMx Master Duty Cycle Value bits

    \section*{REGISTER 17-7: PWMCONx: PWMx CONTROL REGISTER}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline HS/HC-0 & HS/HC-0 & HS/HC-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline FLTSTAT \(^{(1)}\) & CLSTAT \(^{(1)}\) & TRGSTAT & FLTIEN & CLIEN & TRGIEN & ITB \(^{(2)}\) & MDCS \(^{(2)}\) \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline DTC1 & DTC0 & DTCP \({ }^{(3)}\) & - & - & \(\mathrm{CAM}^{(2,4)}\) & XPRES \({ }^{(5)}\) & IUE \({ }^{(2)}\) \\
    \hline \multicolumn{8}{|l|}{bit \(7 \times\) bit 0} \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & HC = Hardware Clearable bit & HS = Hardware Settable bit \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared \(\quad \mathrm{x}=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit \(15 \quad\) FLTSTAT: Fault Interrupt Status bit \({ }^{(1)}\)
    1 = Fault interrupt is pending
    \(0=\) Fault interrupt is not pending
    This bit is cleared by setting FLTIEN \(=0\).
    bit 14 CLSTAT: Current-Limit Interrupt Status bit \({ }^{(1)}\)
    1 = Current-limit interrupt is pending
    \(0=\) Current-limit interrupt is not pending
    This bit is cleared by setting CLIEN \(=0\).
    bit 13 TRGSTAT: Trigger Interrupt Status bit
    \(1=\) Trigger interrupt is pending
    \(0=\) Trigger interrupt is not pending
    This bit is cleared by setting TRGIEN \(=0\).
    bit 12 FLTIEN: Fault Interrupt Enable bit
    1 = Fault interrupt is enabled
    \(0=\) Fault interrupt is disabled and the FLTSTAT bit is cleared
    bit 11 CLIEN: Current-Limit Interrupt Enable bit
    1 = Current-limit interrupt is enabled
    \(0=\) Current-limit interrupt is disabled and the CLSTAT bit is cleared
    bit 10 TRGIEN: Trigger Interrupt Enable bit
    1 = Trigger event generates an interrupt request
    \(0=\) Trigger event interrupts are disabled and the TRGSTAT bit is cleared
    bit 9
    ITB: Independent Time Base Mode bit \({ }^{(2)}\)
    1 = PHASEx register provides time base period for this PWM generator
    \(0=\) PTPER register provides timing for this PWM generator
    bit \(8 \quad\) MDCS: Master Duty Cycle Register Select bit \({ }^{(\mathbf{2})}\)
    1 = MDC register provides duty cycle information for this PWM generator
    \(0=\) PDCx register provides duty cycle information for this PWM generator
    Note 1: Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
    2: These bits should not be changed after the PWMx is enabled (PTEN = 1).
    3: \(D T C<1: 0>=11\) for DTCP to be effective; else, DTCP is ignored.
    4: The Independent Time Base (ITB=1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
    5: To operate in External Period Reset mode, the ITB bit must be ' 1 ' and the CLMOD bit in the FCLCONx register must be ' 0 '.

    \section*{REGISTER 17-7: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)}
    bit 7-6 DTC<1:0>: Dead-Time Control bits
    11 = Dead-Time Compensation mode
    \(10=\) Dead-time function is disabled
    01 = Negative dead time is actively applied for Complementary Output mode
    \(00=\) Positive dead time is actively applied for all Output modes
    bit 5 DTCP: Dead-Time Compensation Polarity bit \({ }^{(3)}\)
    When Set to ' 1 ':
    If DTCMPx \(=0, P W M x L\) is shortened and PWMxH is lengthened.
    If DTCMPx = 1, PWMxH is shortened and PWMxL is lengthened.
    When Set to ' 0 ':
    If DTCMPx \(=0, \mathrm{PWMxH}\) is shortened and PWMxL is lengthened.
    If DTCMPx \(=1, P W M x L\) is shortened and PWMxH is lengthened.
    bit 4-3 Unimplemented: Read as ' 0 '
    bit 2 CAM: Center-Aligned Mode Enable bit \({ }^{(2,4)}\)
    1 = Center-Aligned mode is enabled
    \(0=\) Edge-Aligned mode is enabled
    bit 1
    XPRES: External PWMx Reset Control bit \({ }^{(5)}\)
    1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
    \(0=\) External pins do not affect PWMx time base
    bit 0
    IUE: Immediate Update Enable bit \({ }^{(2)}\)
    1 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are immediate
    \(0=\) Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are synchronized to the PWMx period boundary

    Note 1: Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
    2: These bits should not be changed after the PWMx is enabled (PTEN = 1).
    3: \(D T C<1: 0>=11\) for DTCP to be effective; else, DTCP is ignored.
    4: The Independent Time Base (ITB=1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
    5: To operate in External Period Reset mode, the ITB bit must be ' 1 ' and the CLMOD bit in the FCLCONx register must be ' 0 '.

    REGISTER 17-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{PDCx<15:8>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{PDCx<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \(R=\) Readable bit
    \(-n=\) Value at POR
    W = Writable bit
    \(\mathrm{U}=\) Unimplemented bit, read as ' 0 '
    ' 1 ' = Bit is set
    ' 0 ' = Bit is cleared
    \(x=\) Bit is unknown
    bit 15-0
    PDCx<15:0>: PWMx Generator Duty Cycle Value bits

    \section*{REGISTER 17-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{PHASEx<15:8>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{PHASEx<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}
    bit 15-0
    PHASEx<15:0>: PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

    Note 1: If ITB (PWMCONx<9>) = 0 , the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output modes (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs.

    2: If ITB (PWMCON \(x<9>\) ) \(=1\), the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output modes (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent Time Base period value for PWMxH and PWMxL.

    REGISTER 17-10: DTRx: PWMx DEAD-TIME REGISTER
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline - & - & \multicolumn{6}{|c|}{DTRx<13:8>} \\
    \hline \multicolumn{7}{|l|}{bit 15} & bit 8 \\
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{DTRx<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13-0 DTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

    \section*{REGISTER 17-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER}
    \begin{tabular}{|c|c|cccccc|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & & \(A L T D T R x<13: 8>\) & & \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|llllllll|}
    \hline\(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) \\
    \hline & & & ALTDTR \(x<7: 0>\) & & & \\
    \hline bit 7 & & & & & & bit 0 \\
    \hline
    \end{tabular}

    Legend:
    \(\begin{array}{lll}R=\text { Readable bit } & W=\text { Writable bit } & U=\text { Unimplemented bit, read as ' } 0 \text { ' } \\ -n=\text { Value at POR } & ' 1 '=\text { Bit is set } & ' 0 '=\text { Bit is cleared }\end{array}\)
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13-0 ALTDTRx<13:0>: Unsigned 14-Bit Alternate Dead-Time Value for PWMx Dead-Time Unit bits

    REGISTER 17-12: TRGCONx: PWMx TRIGGER CONTROL REGISTER
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline TRGDIV3 & TRGDIV2 & TRGDIV1 & TRGDIV0 & - & - & - & - \\
    \hline \multicolumn{8}{|l|}{bit \(15 \times\) bit 8} \\
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline - & - & TRGSTRT5 \({ }^{(1)}\) & TRGSTRT4 \({ }^{(1)}\) & TRGSTRT3 \({ }^{(1)}\) & TRGSTRT2 \({ }^{(1)}\) & TRGSTRT1 \({ }^{(1)}\) & TRGSTRT0 \({ }^{(1)}\) \\
    \hline \multicolumn{8}{|l|}{bit 7 bit 0} \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-12 TRGDIV<3:0>: Trigger Output Divider bits
    1111 = Triggers output for every 16th trigger event
    \(1110=\) Triggers output for every 15th trigger event
    1101 = Triggers output for every 14th trigger event
    \(1100=\) Triggers output for every 13th trigger event
    1011 = Triggers output for every 12th trigger event
    1010 = Triggers output for every 11th trigger event
    1001 = Triggers output for every 10th trigger event
    \(1000=\) Triggers output for every 9th trigger event
    0111 = Triggers output for every 8th trigger event
    \(0110=\) Triggers output for every 7th trigger event
    0101 = Triggers output for every 6th trigger event
    \(0100=\) Triggers output for every 5th trigger event
    0011 = Triggers output for every 4th trigger event
    \(0010=\) Triggers output for every 3rd trigger event
    0001 = Triggers output for every 2nd trigger event
    \(0000=\) Triggers output for every trigger event
    bit 11-6 Unimplemented: Read as ' 0 '
    bit 5-0 TRGSTRT<5:0>: Trigger Postscaler Start Enable Select bits \({ }^{(1)}\)
    111111 = Waits 63 PWM cycles before generating the first trigger event after the module is enabled
    -
    -

    000010 = Waits 2 PWM cycles before generating the first trigger event after the module is enabled
    000001 = Waits 1 PWM cycle before generating the first trigger event after the module is enabled
    \(000000=\) Waits 0 PWM cycles before generating the first trigger event after the module is enabled
    Note 1: The secondary PWM generator cannot generate PWMx trigger interrupts.

    REGISTER 17-13: IOCONx: PWMx I/O CONTROL REGISTER \({ }^{(2)}\)
    \(\left\lvert\,\)\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline R/W-1 & R/W-1 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline PENH & PENL & POLH & POLL & PMOD1 \({ }^{(1)}\) & PMOD0 \({ }^{(1)}\) & OVRENH & OVRENL \\
    \hline bit 15 \\
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline OVRDAT1 & OVRDAT0 & FLTDAT1 & FLTDAT0 & CLDAT1 & CLDAT0 & SWAP & OSYNC \\
    \hline bit 7 &
    \end{tabular}
    \end{tabular}\(.\)\begin{tabular}{l} 
    bit 0 \\
    \hline
    \end{tabular}\right.

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}
    bit 15 PENH: PWMxH Output Pin Ownership bit
    1 = PWMx module controls the PWMxH pin
    \(0=\) GPIO module controls the PWMxH pin
    bit 14 PENL: PWMxL Output Pin Ownership bit
    1 = PWMx module controls the PWMxL pin
    \(0=\) GPIO module controls the PWMxL pin
    bit 13 POLH: PWMxH Output Pin Polarity bit
    \(1=\mathrm{PWMxH}\) pin is active-low
    \(0=\mathrm{PWMxH}\) pin is active-high
    bit 12 POLL: PWMxL Output Pin Polarity bit
    \(1=\mathrm{PWMxL}\) pin is active-low
    \(0=P W M x L\) pin is active-high
    bit 11-10
    PMOD<1:0>: PWMx I/O Pin Mode bits \({ }^{(1)}\)
    11 = Reserved; do not use
    \(10=\) PWMx I/O pin pair is in the Push-Pull Output mode
    \(01=\) PWMx I/O pin pair is in the Redundant Output mode
    \(00=\) PWMx I/O pin pair is in the Complementary Output mode
    bit 9 OVRENH: Override Enable for PWMxH Pin bit
    1 = OVRDAT1 controls the output on the PWMxH pin
    \(0=\) PWMx generator controls the PWMxH pin
    bit 8 OVRENL: Override Enable for PWMxL Pin bit
    1 = OVRDAT0 controls the output on the PWMxL pin
    \(0=\) PWMx generator controls the PWMxL pin
    bit 7-6 OVRDAT<1:0>: Data for PWMxH, PWMxL Pins if Override is Enabled bits If OVERENH \(=1, \mathrm{PWMxH}\) is driven to the state specified by OVRDAT1. If OVERENL \(=1, \mathrm{PWMxL}\) is driven to the state specified by OVRDAT0.
    bit 5-4 FLTDAT<1:0>: Data for PWMxH and PWMxL Pins if FLTMOD is Enabled bits If Fault is active, PWMxH is driven to the state specified by FLTDAT1. If Fault is active, PWMxL is driven to the state specified by FLTDAT0.
    bit 3-2 CLDAT<1:0>: Data for PWMxH and PWMxL Pins if CLMOD is Enabled bits If current limit is active, PWMxH is driven to the state specified by CLDAT1. If current limit is active, PWMxL is driven to the state specified by CLDAT0.

    Note 1: These bits should not be changed after the PWMx module is enabled ( \(\mathrm{PTEN}=1\) ).
    2: If the PWMLOCK Configuration bit (FDEVOPT<0>) is a ' 1 ', the IOCONx register can only be written after the unlock sequence has been executed.

    \section*{REGISTER 17-13: IOCONx: PWMx I/O CONTROL REGISTER \({ }^{(2)}\) (CONTINUED)}

    SWAP: SWAP PWMxH and PWMxL Pins bit
    \(1=\mathrm{PWMxH}\) output signal is connected to the PWMxL pin; PWMxL output signal is connected to the PWMxH pin
    \(0=\) PWMxH and PWMxL pins are mapped to their respective pins
    bit 0
    OSYNC: Output Override Synchronization bit
    1 = Output overrides through the OVRDAT \(<1: 0>\) bits are synchronized to the PWMx time base
    \(0=\) Output overrides through the OVRDAT<1:0> bits occur on the next CPU clock boundary
    Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).
    2: If the PWMLOCK Configuration bit (FDEVOPT<0>) is a ' 1 ', the IOCONx register can only be written after the unlock sequence has been executed.

    REGISTER 17-14: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER
    \begin{tabular}{|lllllllll|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline & & & TRGCMP<15:8> & & & \\
    \hline bit 15 & & & & & & \\
    \hline & & & & & & & \\
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline & & & TRGCMP<7:0> & & & \\
    \hline bit 7 & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}
    bit 15-0 TRGCMP<15:0>: Trigger Control Value bits
    When the primary PWMx functions in the local time base, this register contains the compare values that can trigger the ADC module.

    REGISTER 17-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER \({ }^{(1)}\)
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & CLSRC4 & CLSRC3 & CLSRC2 & CLSRC1 & CLSRC0 & CLPOL \({ }^{(2)}\) & CLMOD \\
    \hline bit 15 \\
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-0 & R/W-0 & R/W-0 \\
    \hline FLTSRC4 & FLTSRC3 & FLTSRC2 & FLTSRC1 & FLTSRC0 & FLTPOL \({ }^{(2)}\) & FLTMOD1 & FLTMOD0 \\
    \hline bit 7
    \end{tabular}
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared \\
    \hline
    \end{tabular}
    bit 15 Unimplemented: Read as ' 0 '
    bit 14-10 CLSRC<4:0>: Current-Limit Control Signal Source Select for PWM Generator x bits
    11111 = Fault 32
    11110 = Reserved
    -
    -

    01100 = Op Amp/Comparator 5
    01011 = Comparator 4
    01010 = Op Amp/Comparator 3
    01001 = Op Amp/Comparator 2
    \(01000=\) Op Amp/Comparator 1
    00111 = Fault 8
    \(00110=\) Fault 7
    \(00101=\) Fault 6
    \(00100=\) Fault 5
    \(00011=\) Fault 4
    \(00010=\) Fault 3
    \(00001=\) Fault 2
    \(00000=\) Fault 1 (default)
    bit 9 CLPOL: Current-Limit Polarity for PWM Generator \(x\) bit \({ }^{(\mathbf{2})}\)
    \(1=\) The selected current-limit source is active-low
    \(0=\) The selected current-limit source is active-high
    bit 8 CLMOD: Current-Limit Mode Enable for PWM Generator x bit
    1 = Current-Limit mode is enabled
    \(0=\) Current-Limit mode is disabled
    Note 1: If the PWMLOCK Configuration bit (FDEVOPT<0>) is a ' 1 ', the FCLCONx register can only be written after the unlock sequence has been executed.
    2: These bits should be changed only when \(\mathrm{PTEN}=0\). Changing the clock selection during operation will yield unpredictable results.

    \section*{REGISTER 17-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER \({ }^{(1)}\)}
    bit 7-3 FLTSRC<4:0>: Fault Control Signal Source Select for PWM Generator x bits
    11111 = Fault 32 (default)
    11110 = Reserved
    -
    -
    -
    \(01100=\) Op Amp/Comparator 5
    01011 = Comparator 4
    \(01010=\) Op Amp/Comparator 3
    01001 = Op Amp/Comparator 2
    \(01000=\) Op Amp/Comparator 1 \(00111=\) Fault 8
    \(00110=\) Fault 7
    \(00101=\) Fault 6
    \(00100=\) Fault 5
    \(00011=\) Fault 4
    \(00010=\) Fault 3
    \(00001=\) Fault 2
    00000 = Fault 1
    bit 2
    FLTPOL: Fault Polarity for PWM Generator x bit \({ }^{(2)}\)
    \(1=\) The selected Fault source is active-low
    \(0=\) The selected Fault source is active-high
    bit 1-0 FLTMOD<1:0>: Fault Mode for PWM Generator \(x\) bits
    \(11=\) Fault input is disabled
    10 = Reserved
    01 = The selected Fault source forces the PWMxH, PWMxL pins to FLTDAT<1:0> values (cycle)
    \(00=\) The selected Fault source forces the PWMxH, PWMxL pins to FLTDAT \(<1: 0>\) values (latched condition)
    Note 1: If the PWMLOCK Configuration bit (FDEVOPT<0>) is a ' 1 ', the FCLCONx register can only be written after the unlock sequence has been executed.
    2: These bits should be changed only when \(\operatorname{PTEN}=0\). Changing the clock selection during operation will yield unpredictable results.

    REGISTER 17-16: LEBCONx: PWMx LEADING-EDGE BLANKING CONTROL REGISTER
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & U-0 & U-0 \\
    \hline PHR & PHF & PLR & PLF & FLTLEBEN & CLLEBEN & - & - \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{9}{|c|}{\(\mathrm{U}-0\)} & \(\mathrm{U}-0\) & \(\mathrm{R} / \mathrm{W}-0\) & \(\mathrm{R} / \mathrm{W}-0\) & \(\mathrm{R} / \mathrm{W}-0\) & \(\mathrm{R} / \mathrm{W}-0\) & \(\mathrm{R} / \mathrm{W}-0\) & \(\mathrm{R} / \mathrm{W}-0\) \\
    \hline- & - & \(\mathrm{BCH}^{(1)}\) & \(\mathrm{BCL}^{(1)}\) & BPH & BPHL & BPLH & BPLL \\
    \hline bit 7 &
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}
    bit 15 PHR: PWMxH Rising Edge Trigger Enable bit
    1 = Rising edge of PWMxH will trigger the Leading-Edge Blanking counter
    0 = Leading-Edge Blanking ignores the rising edge of PWMxH
    bit 14 PHF: PWMxH Falling Edge Trigger Enable bit
    1 = Falling edge of PWMxH will trigger the Leading-Edge Blanking counter
    0 = Leading-Edge Blanking ignores the falling edge of PWMxH
    bit 13 PLR: PWMxL Rising Edge Trigger Enable bit
    1 = Rising edge of PWMxL will trigger the Leading-Edge Blanking counter
    \(0=\) Leading-Edge Blanking ignores the rising edge of PWMxL
    bit \(12 \quad\) PLF: PWMxL Falling Edge Trigger Enable bit
    1 = Falling edge of PWMxL will trigger the Leading-Edge Blanking counter
    \(0=\) Leading-Edge Blanking ignores the falling edge of PWMxL
    bit 11 FLTLEBEN: Fault Input Leading-Edge Blanking Enable bit
    1 = Leading-Edge Blanking is applied to the selected Fault input
    0 = Leading-Edge Blanking is not applied to the selected Fault input
    bit 10
    CLLEBEN: Current-Limit Leading-Edge Blanking Enable bit
    1 = Leading-Edge Blanking is applied to the selected current-limit input
    \(0=\) Leading-Edge Blanking is not applied to the selected current-limit input
    bit 9-6 Unimplemented: Read as ' 0 '
    bit 5
    BCH: Blanking in Selected Blanking Signal High Enable bit \({ }^{(1)}\)
    1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is high
    \(0=\) No blanking when the selected blanking signal is high
    bit \(4 \quad\) BCL: Blanking in Selected Blanking Signal Low Enable bit \({ }^{(1)}\)
    1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low
    \(0=\) No blanking when the selected blanking signal is low
    bit \(3 \quad\) BPHH: Blanking in PWMxH High Enable bit
    1 = State blanking (of current-limit and/or Fault input signals) when the PWMxH output is high
    \(0=\) No blanking when the PWMxH output is high
    bit \(2 \quad\) BPHL: Blanking in PWMxH Low Enable bit
    1 = State blanking (of current-limit and/or Fault input signals) when the PWMxH output is low
    \(0=\) No blanking when the PWMxH output is low
    bit 1
    BPLH: Blanking in PWMxL High Enable bit
    1 = State blanking (of current-limit and/or Fault input signals) when the PWMxL output is high
    \(0=\) No blanking when the PWMxL output is high
    bit 0
    BPLL: Blanking in PWMxL Low Enable bit
    1 = State blanking (of current-limit and/or Fault input signals) when the PWMxL output is low
    \(0=\) No blanking when the PWMxL output is low
    Note 1: The blanking signal is selected through the BLANKSEL<3:0> bits in the AUXCONx register.

    REGISTER 17-17: LEBDLYx: PWMx LEADING-EDGE BLANKING DELAY REGISTER
    \begin{tabular}{|l|c|c|c|cccc|}
    \hline U-0 & U-0 & U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & - & - & & LEB<11:8> & \\
    \hline bit 15 &
    \end{tabular}
    \begin{tabular}{|llllllll|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline & & LEB<7:0> & & & \\
    \hline bit 7 & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}
    bit 15-12 Unimplemented: Read as ' 0 '
    bit 11-0 LEB<11:0>: Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits

    \section*{REGISTER 17-18: AUXCONx: PWMx AUXILIARY CONTROL REGISTER}
    \begin{tabular}{|c|c|c|c|c|c|c|r|}
    \hline U-0 & U-0 & U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & - & - & BLANKSEL3 & BLANKSEL2 & BLANKSEL1 & BLANKSEL0 \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|l|l|c|c|c|cc|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & CHOPSEL3 & CHOPSEL2 & CHOPSEL1 & CHOPSEL0 & CHOPHEN & CHOPLEN \\
    \hline bit 7 & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' \(=\) Bit is set & ' 0 ' \(=\) Bit is cleared
    \end{tabular}
    \begin{tabular}{|c|c|}
    \hline bit 15-12 & Unimplemented: Read as '0' \\
    \hline \multirow[t]{2}{*}{bit 11-8} & BLANKSEL<3:0>: PWMx State Blank Source Select bits \\
    \hline & \begin{tabular}{l}
    The selected state blank signal will block the current-limit and/or Fault input signals (if enabled through the BCH and BCL bits in the LEBCONx register). \\
    1001 = Reserved \\
    \(0100=\) Reserved \\
    \(0011=\) PWM3H is selected as the state blank source \\
    \(0010=\) PWM2H is selected as the state blank source \\
    \(0001=\) PWM1H is selected as the state blank source \\
    \(0000=\) No state blanking
    \end{tabular} \\
    \hline bit 7-6 & Unimplemented: Read as ' 0 ' \\
    \hline \multirow[t]{7}{*}{bit 5-2} & CHOPSEL<3:0>: PWMx Chop Clock Source Select bits \\
    \hline & The selected signal will enable and disable (Chop) the selected PWMx outputs. 1001 = Reserved \\
    \hline & 0100 Reserved \\
    \hline & \(0011=\) PWM3H is selected as the chop clock source \\
    \hline & \(0010=\) PWM2H is selected as the chop clock source \\
    \hline & 0001 = PWM1H is selected as the chop clock source \\
    \hline & \(0000=\) Chop clock generator is selected as the chop clock source \\
    \hline \multirow[t]{2}{*}{bit 1} & CHOPHEN: PWMxH Output Chopping Enable bit \\
    \hline & \(1=\) PWMxH chopping function is enabled \(0=\) PWMxH chopping function is disabled \\
    \hline \multirow[t]{2}{*}{bit 0} & CHOPLEN: PWMxL Output Chopping Enable bit \\
    \hline & \begin{tabular}{l}
    \(1=P W M x L\) chopping function is enabled \\
    \(0=P W M x L\) chopping function is disabled
    \end{tabular} \\
    \hline
    \end{tabular}

    \section*{dsPIC33EVXXXGM00X/10X FAMILY}

    NOTES:

    \subsection*{18.0 SERIAL PERIPHERAL INTERFACE (SPI)}

    Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Serial Peripheral Interface (SPI)" (DS70005185) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
    2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

    The Serial Peripheral Interface (SPI) module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with the Motorola \({ }^{\circledR}\) SPI and SIOP interfaces.
    The dsPIC33EVXXXGM00X/10X device family offers two SPI modules on a single device, SPI1 and SPI2, that are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

    Note: In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 and SPI2 modules.

    The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of these modules, but results in a lower maximum speed. See Section 30.0 "Electrical Characteristics" for more information.
    The SPIx serial interface consists of the following four pins:
    - SDIx: Serial Data Input
    - SDOx: Serial Data Output
    - SCKx: Shift Clock Input or Output
    - \(\overline{S S x} / F S Y N C x\) : Active-Low Slave Select or Frame Synchronization I/O Pulse

    Note: All of the 4 pins of the SPIx serial interface must be configured as digital in the ANSELx registers.

    The SPlx module can be configured to operate with two, three or four pins. In 3-pin mode, \(\overline{\mathrm{SSx}}\) is not used. In 2-pin mode, neither SDOx nor \(\overline{S S x}\) is used.
    Figure 18-1 illustrates the block diagram of the SPIx module in Standard and Enhanced modes.

    FIGURE 18-1: SPIx MODULE BLOCK DIAGRAM
    

    Note 1: In Standard mode, the FIFO is only one level deep.

    \subsection*{18.1 SPI Helpful Tips}
    1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
    a) If FRMPOL (SPIxCON2<13>) \(=1\), use a pull-down resistor on SSx.
    b) If \(\mathrm{FRMPOL}=0\), use a pull-up resistor on \(\overline{\mathrm{SSx}}\).
    Note: This insures that the first frame transmission after initialization is not shifted or corrupted.
    2. In Non-Framed 3-Wire mode (i.e., not using \(\overline{\mathrm{SSx}}\) from a master):
    a) If CKP (SPIxCON1<6>) = 1 , always place a pull-up resistor on \(\overline{\text { SSx. }}\)
    b) If \(C K P=0\), always place a pull-down resistor on \(\overline{\text { SSx. }}\)
    Note: This will insure that during power-up and initialization, the master/slave will not lose sync due to an errant SCKx transition that would cause the slave to accumulate data shift errors, for both transmit and receive, appearing as corrupted data.
    3. FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the \(\overline{\mathrm{SSx}}\) pin, which indicates the start of a data frame.
    Note: Not all third-party devices support Frame mode timing. For more information, refer to the SPI specifications in Section 30.0 "Electrical Characteristics".
    4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a ' 1 ' for the fastest SPI data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPlxCON1<5>) is set.
    To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

    \subsection*{18.2 SPI Control Registers}

    \section*{REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline R/W-0 & U-0 & R/W-0 & U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline SPIEN & - & SPISIDL & - & - & SPIBEC2 & SPIBEC1 & SPIBEC0 \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/C-0, HS & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R-0, HS, HC & R-0, HS, HC \\
    \hline SRMPT & SPIROV & SRXMPT & SISEL2 & SISEL1 & SISEL0 & SPITBF & SPIRBF \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll}
    \hline Legend: & \(C=\) Clearable bit & HS = Hardware Settable bit \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared \(\quad x=\) Bit is unknown \\
    \(H C=\) Hardware Clearable bit & &
    \end{tabular}
    \begin{tabular}{|c|c|}
    \hline \multirow[t]{2}{*}{bit 15} & SPIEN: SPIx Enable bit \\
    \hline & 1 = Enables the SPIx module and configures SCKx, SDOx, SDIx and \(\overline{\text { SSx }}\) as serial port pins \(0=\) Disables the SPIx module \\
    \hline bit 14 & Unimplemented: Read as '0' \\
    \hline \multirow[t]{2}{*}{bit 13} & SPISIDL: SPIx Stop in Idle Mode bit \\
    \hline & \begin{tabular}{l}
    1 = Discontinues the SPIx module operation when the device enters Idle mode \\
    \(0=\) Continues the SPIx module operation in Idle mode
    \end{tabular} \\
    \hline bit 12-11 & Unimplemented: Read as '0' \\
    \hline \multirow[t]{5}{*}{bit 10-8} & SPIBEC<2:0>: SPIx Buffer Element Count bits (valid in Enhanced Buffer mode) \\
    \hline & Master mode: \\
    \hline & Number of SPIx transfers are pending. \\
    \hline & Slave mode: \\
    \hline & Number of SPIx transfers are unread. \\
    \hline \multirow[t]{2}{*}{bit 7} & SRMPT: SPIx Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode) \\
    \hline & 1 = The SPIx Shift register is empty and ready to send or receive the data \(0=\) The SPIx Shift register is not empty \\
    \hline \multirow[t]{2}{*}{bit 6} & SPIROV: SPIx Receive Overflow Flag bit \\
    \hline & ```
    1 = A new byte/word is completely received and discarded; the user application has not read the
    previous data in the SPIxBUF register
    \(0=\) Overflow has not occurred
    ``` \\
    \hline
    \end{tabular}
    bit 5 SRXMPT: SPIx Receive FIFO Empty bit (valid in Enhanced Buffer mode)
    1 = RX FIFO is empty
    \(0=\) RX FIFO is not empty
    bit 4-2 SISEL<2:0>: SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)
    111 = Interrupt when the SPIx transmit buffer is full (SPITBF bit is set)
    \(110=\) Interrupt when the last bit is shifted into SPIxSR, and as a result, the TX FIFO is empty
    101 = Interrupt when the last bit is shifted out of SPIxSR and the transmit is complete
    \(100=\) Interrupt when one data is shifted into SPIxSR, and as a result, the TX FIFO has one open memory location
    011 = Interrupt when the SPIx receive buffer is full (SPIRBF bit is set)
    \(010=\) Interrupt when the SPIx receive buffer is \(3 / 4\) or more full
    001 = Interrupt when data is available in the SPIx receive buffer (SRMPT bit is set)
    \(000=\) Interrupt when the last data in the SPIx receive buffer is read, and as a result, the buffer is empty (SRXMPT bit is set)

    \section*{REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)}
    bit 1

    \section*{SPITBF: SPIx Transmit Buffer Full Status bit}
    \(1=\) Transmit has not yet started, the SPIxTXB bit is full
    \(0=\) Transmit has started, the SPIxTXB bit is empty

    \section*{Standard Buffer mode:}

    Automatically set in hardware when the core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.
    Enhanced Buffer mode:
    Automatically set in the hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.
    SPIRBF: SPIx Receive Buffer Full Status bit
    1 = Receive is complete, the SPIxRXB bit is full
    \(0=\) Receive is incomplete, the SPIxRXB bit is empty
    Standard Buffer mode:
    Automatically set in the hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.
    Enhanced Buffer mode:
    Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

    \section*{REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & - & DISSCK & DISSDO & MODE16 & SMP & CKE \(^{(1)}\) \\
    \hline bit 15 &
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline \multicolumn{1}{|c|}{ R/W-0 } & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline SSEN \(^{(2)}\) & CKP & MSTEN & SPRE2 \(^{(3)}\) & SPRE1 \(^{(3)}\) & SPRE0 \(^{(3)}\) & PPRE1 \(^{(3)}\) & PPRE0 \(^{(3)}\) \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-13 Unimplemented: Read as ' 0 '
    bit 12 DISSCK: Disable SCKx Pin bit (SPI Master modes only)
    1 = Internal SPI clock is disabled, pin functions as I/O
    \(0=\) Internal SPI clock is enabled
    bit 11 DISSDO: Disable SDOx Pin bit
    1 = SDOx pin is not used by the module; pin functions as I/O
    \(0=\) SDOx pin is controlled by the module
    bit 10 MODE16: Word/Byte Communication Select bit
    1 = Communication is word-wide (16 bits)
    \(0=\) Communication is byte-wide ( 8 bits )
    bit 9 SMP: SPIx Data Input Sample Phase bit
    Master mode:
    1 = Input data is sampled at the end of data output time
    \(0=\) Input data is sampled at the middle of data output time
    Slave mode:
    SMP must be cleared when SPIx is used in Slave mode.
    bit \(8 \quad\) CKE: Clock Edge Select bit \({ }^{(1)}\)
    1 = Serial output data changes on transition from active clock state to Idle clock state (refer to bit 6)
    \(0=\) Serial output data changes on transition from Idle clock state to active clock state (refer to bit 6)
    bit \(7 \quad\) SSEN: Slave Select Enable bit (Slave mode) \({ }^{(2)}\)
    \(1=\overline{S S x}\) pin is used for Slave mode
    \(0=\overline{\mathrm{SSx}}\) pin is not used by the module; pin is controlled by port function
    bit \(6 \quad\) CKP: Clock Polarity Select bit
    1 = Idle state for clock is a high level; active state is a low level
    \(0=\) Idle state for clock is a low level; active state is a high level
    bit 5 MSTEN: Master Mode Enable bit
    1 = Master mode
    0 = Slave mode
    Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to ' 0 ' for Framed SPI modes (FRMEN = 1).
    2: \(\quad\) This bit must be cleared when FRMEN \(=1\).
    3: Do not set both primary and secondary prescalers to the value of 1:1.

    \section*{REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)}
    bit 4-2 SPRE<2:0>: Secondary Prescale bits (Master mode) \({ }^{(3)}\)
    111 = Secondary prescale 1:1
    \(110=\) Secondary prescale 2:1
    -
    -
    -
    \(000=\) Secondary prescale 8:1
    bit 1-0 PPRE<1:0>: Primary Prescale bits (Master mode) \({ }^{(3)}\)
    11 = Primary prescale 1:1
    \(10=\) Primary prescale 4:1
    01 = Primary prescale 16:1
    \(00=\) Primary prescale 64:1
    Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to ' 0 ' for Framed SPI modes (FRMEN = 1).
    2: \(\quad\) This bit must be cleared when FRMEN \(=1\).
    3: Do not set both primary and secondary prescalers to the value of \(1: 1\).

    \section*{REGISTER 18-3: SPIxCON2: SPIx CONTROL REGISTER 2}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline FRMEN & SPIFSD & FRMPOL & - & - & - & - & - \\
    \hline \multicolumn{2}{|l|}{bit 15} & & & & & & bit 8 \\
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & R/W-0 & R/W-0 \\
    \hline - & - & - & - & - & - & FRMDLY & SPIBEN \\
    \hline \multicolumn{2}{|l|}{bit 7} & & & & & & bit 0 \\
    \hline \multicolumn{8}{|l|}{Legend:} \\
    \hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{\(\mathrm{R}=\) Readable bit -n = Value at POR}} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{\[
    \begin{aligned}
    & \text { W }=\text { Writable bit } \\
    & \prime 1 \text { ' Bit is set }
    \end{aligned}
    \]}} & \multicolumn{4}{|l|}{\(\mathrm{U}=\) Unimplemented bit, read as ' 0 '} \\
    \hline & & & & '0' = Bit & & = Bit is un & \\
    \hline
    \end{tabular}
    bit 15 FRMEN: Framed SPIx Support bit
    1 = Framed SPIx support is enabled ( \(\overline{\mathrm{SSx}}\) pin is used as the Frame Sync pulse input/output)
    0 = Framed SPIx support is disabled
    bit 14 SPIFSD: SPIx Frame Sync Pulse Direction Control bit
    1 = Frame Sync pulse input (slave)
    \(0=\) Frame Sync pulse output (master)
    bit 13 FRMPOL: Frame Sync Pulse Polarity bit
    1 = Frame Sync pulse is active-high
    \(0=\) Frame Sync pulse is active-low
    bit 12-2
    Unimplemented: Read as '0'
    bit 1
    FRMDLY: Frame Sync Pulse Edge Select bit
    1 = Frame Sync pulse coincides with the first bit clock
    0 = Frame Sync pulse precedes the first bit clock
    bit \(0 \quad\) SPIBEN: SPIx Enhanced Buffer Enable bit
    1 = Enhanced buffer is enabled
    \(0=\) Enhanced buffer is disabled (Standard mode)

    \subsection*{19.0 INTER-INTEGRATED CIRCUIT \({ }^{\text {TM }}\left(\mathbf{I}^{2} \mathrm{C}^{\text {TM }}\right.\) )}

    Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Inter-Integrated Circuit \({ }^{T M}\) ( \(\mathbf{I}^{2} \mathbf{C}^{\text {TM }}\) )" (DS70000195) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
    2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

    The dsPIC33EVXXXGM00X/10X family of devices contains one Inter-Integrated Circuit ( \(\left.I^{2} \mathrm{C}\right)\) module, I2C1.
    The \(I^{2} \mathrm{C}\) module provides complete hardware support for both Slave and Multi-Master modes of the \(I^{2} \mathrm{C}\) serial communication standard, with a 16-bit interface.
    The \(\mathrm{I}^{2} \mathrm{C}\) module has the following 2-pin interface:
    - The SCLx pin is clock.
    - The SDAx pin is data.

    The \(I^{2} \mathrm{C}\) module offers the following key features:
    - \(1^{2} \mathrm{C}\) Interface Supporting Both Master and Slave modes of Operation
    - \(I^{2} \mathrm{C}\) Slave mode Supports 7 and \(10-\) Bit Addressing
    - \(I^{2} C\) Master mode Supports 7 and \(10-B i t\) Addressing
    - \(I^{2} \mathrm{C}\) Port allows Bidirectional Transfers between Master and Slaves
    - Serial Clock Synchronization for \(I^{2} \mathrm{C}\) Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control)
    - \(I^{2} \mathrm{C}\) Supports Multi-Master Operation, Detects Bus Collision and Arbitrates Accordingly
    - Support for Address Bit Masking up to Lower 7 Bits
    - \(I^{2} \mathrm{C}\) Slave Enhancements:
    - SDAx hold time selection of SMBus (300 ns or 150 ns )
    - Start/Stop bit interrupt enables

    Figure \(19-1\) shows a block diagram of the \(\mathrm{I}^{2} \mathrm{C}\) module.

    \section*{\(19.1 \quad I^{2} \mathrm{C}\) Baud Rate Generator}

    The Baud Rate Generator (BRG) used for \(I^{2} C\) mode operation is used to set the SCL clock frequency for \(100 \mathrm{kHz}, 400 \mathrm{kHz}\) and 1 MHz . The BRG reload value is contained in the I2CxBRG register. The BRG will automatically begin counting on a write to the I2CxTRN register.
    Equation 19-1 and Equation 19-2 provide the BRG reload formula and FSCL frequency, respectively.

    EQUATION 19-1: BRG FORMULA
    \[
    I 2 C x B R G=\left(\left(\frac{1}{F S C L}-\text { Delay }\right) \times \frac{F C Y}{2}\right)-2
    \]

    Where:
    Delay varies from 110 ns to 130 ns .

    \section*{EQUATION 19-2: Fscl FREQUENCY}
    \[
    F S C L=F C Y /((I 2 C x B R G+2) * 2)
    \]

    FIGURE 19-1: I2Cx BLOCK DIAGRAM (x=1)
    

    \section*{19.2 \(\quad I^{2} C\) Control Registers}

    \section*{REGISTER 19-1: I2CxCON1: I2Cx CONTROL REGISTER 1}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline \multicolumn{8}{|c|}{ R/W-0 } \\
    \hline I2CEN & - & R-0 & R/S-1 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline I2CSIDL & SCLREL \({ }^{(1)}\) & STRICT & A10M & DISSLW & SMEN \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0, HC & R/W-0, HC & R/W-0, HC & R/W-0, HC & R/W-0, HC \\
    \hline GCEN & STREN & ACKDT & ACKEN & RCEN & PEN & RSEN & SEN \\
    \hline bit 7 & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & \(S=\) Settable bit & HC = Hardware Clearable bit \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared \(\quad \mathrm{x}=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15 I2CEN: I2Cx Enable bit (writable from SW only)
    1 = Enables the \(I^{2} C^{\top M}\) module and configures the SDAx and SCLx pins as serial port pins
    \(0=\) Disables the \(\mathrm{I}^{2} \mathrm{C}\) module and all \(\mathrm{I}^{2} \mathrm{C}\) pins are controlled by port functions
    bit \(14 \quad\) Unimplemented: Read as ' 0 '
    bit 13 I2CSIDL: I2Cx Stop in Idle Mode bit
    1 = Discontinues module operation when the device enters Idle mode
    \(0=\) Continues module operation in Idle mode
    SCLREL: SCLx Release Control bit ( \(\mathrm{I}^{2} \mathrm{C}\) Slave mode only) \({ }^{(1)}\)
    Module resets and (I2CEN = 0) sets SCLREL = 1 .
    If STREN = 0: \({ }^{(2)}\)
    1 = Releases clock
    \(0=\) Forces clock low (clock stretch)
    If STREN = 1:
    1 = Releases clock
    0 = Holds clock low (clock stretch); user may program this bit to '0', clock stretch at the next SCLx low
    STRICT: Strict \({ }^{2}\) C Reserved Address Rule Enable bit
    1 = Strict reserved addressing is enforced
    In Slave mode, the device does not respond to reserved address space and addresses falling in that category are NACKed.
    \(0=\) Reserved addressing would be Acknowledged
    In Slave mode, the device will respond to an address falling in the reserved address space. When there is a match with any of the reserved addresses, the device will generate an ACK.
    bit 10
    A10M: 10-Bit Slave Address Flag bit
    \(1=I 2 C x A D D\) is a 10 -bit slave address
    \(0=12 C x A D D\) is a 7 -bit slave address
    bit 9 DISSLW: Slew Rate Control Disable bit
    1 = Slew rate control is disabled for Standard Speed mode ( 100 kHz , also disabled for 1 MHz mode)
    \(0=\) Slew rate control is enabled for High-Speed mode ( 400 kHz )
    bit 8 SMEN: SMBus Input Levels Enable bit
    1 = Enables the input logic so thresholds are compliant with the SMBus specification
    \(0=\) Disables the SMBus-specific inputs
    Note 1: Automatically cleared to ' 0 ' at the beginning of slave transmission; automatically cleared to ' 0 ' at the end of slave reception.
    2: Automatically cleared to ' 0 ' at the beginning of slave transmission.

    \section*{REGISTER 19-1: I2CxCON1: I2Cx CONTROL REGISTER 1}
    bit \(7 \quad\) GCEN: General Call Enable bit ( \(I^{2} \mathrm{C}\) Slave mode only)
    1 = Enables interrupt when a general call address is received in I2CxRSR; module is enabled for reception
    \(0=\) General call address is disabled.
    bit 6 STREN: SCLx Clock Stretch Enable bit
    In \(I^{2} C\) Slave mode only, used in conjunction with the SCLREL bit.
    1 = Enables clock stretching
    0 = Disables clock stretching
    bit 5 ACKDT: Acknowledge Data bit
    In \(I^{2} C\) Master mode, during Master Receive mode. The value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
    In \(I^{2} \mathrm{C}\) Slave mode when AHEN \(=1\) or DHEN = 1 . The value that the slave will transmit when it initiates an Acknowledge sequence at the end of an address or data reception.
    1 = NACK is sent
    \(0=A C K\) is sent
    bit 4 ACKEN: Acknowledge Sequence Enable bit
    In I \({ }^{2} \mathrm{C}\) Master mode only; applicable during Master Receive mode.
    1 = Initiates Acknowledge sequence on SDAx and SCLx pins, and transmits ACKDT data bit
    \(0=\) Acknowledge sequence is Idle
    bit 3 RCEN: Receive Enable bit ( \(I^{2} \mathrm{C}\) Master mode only)
    1 = Enables Receive mode for \(I^{2} \mathrm{C}\), automatically cleared by hardware at the end of 8-bit receive data byte
    \(0=\) Receive sequence is not in progress
    bit 2 PEN: Stop Condition Enable bit ( \({ }^{2}\) C Master mode only)
    1 = Initiates Stop condition on SDAx and SCLx pins
    0 = Stop condition is Idle
    bit 1 RSEN: Restart Condition Enable bit ( \({ }^{2}\) C Master mode only)
    1 = Initiates Restart condition on SDAx and SCLx pins
    \(0=\) Restart condition is Idle
    bit \(0 \quad\) SEN: Start Condition Enable bit ( \(I^{2} \mathrm{C}\) Master mode only)
    1 = Initiates Start condition on SDAx and SCLx pins
    \(0=\) Start condition is Idle
    Note 1: Automatically cleared to ' 0 ' at the beginning of slave transmission; automatically cleared to ' 0 ' at the end of slave reception.
    2: Automatically cleared to ' 0 ' at the beginning of slave transmission.

    \section*{REGISTER 19-2: I2CxCON2: I2Cx CONTROL REGISTER 2}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline- & - & - & - & - & - & - & - \\
    \hline bit 15 & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & PCIE & SCIE & BOEN & SDAHT & SBCDE & AHEN & DHEN \\
    \hline bit 7
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' \(=\) Bit is set & \(\prime 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-7 Unimplemented: Read as ' 0 '
    bit \(6 \quad\) PCIE: Stop Condition Interrupt Enable bit ( \(I^{2} \mathrm{C}^{\text {TM }}\) Slave mode only).
    1 = Enables interrupt on detection of Stop condition
    \(0=\) Stop detection interrupts are disabled
    bit \(5 \quad\) SCIE: Start Condition Interrupt Enable bit ( \({ }^{2} \mathrm{C}\) Slave mode only)
    1 = Enables interrupt on detection of Start or Restart conditions
    \(0=\) Start detection interrupts are disabled
    BOEN: Buffer Overwrite Enable bit ( \(I^{2} \mathrm{C}\) Slave mode only)
    1 = The I2CxRCV register bit is updated and an ACK is generated for a received address/data byte, ignoring the state of the I2COV bit only if the RBF bit \(=0\)
    \(0=\) The I2CxRCV register bit is only updated when I2COV is clear
    bit 3 SDAHT: SDAx Hold Time Selection bit
    1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx
    \(0=\) Minimum of 100 ns hold time on SDAx after the falling edge of SCLx
    bit \(2 \quad\) SBCDE: Slave Mode Bus Collision Detect Enable bit ( \({ }^{2}\) C Slave mode only)
    If, on the rising edge of SCLx, SDAx is sampled low when the module is outputting a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.
    1 = Slave bus collision interrupts are enabled
    0 = Slave bus collision interrupts are disabled
    bit 1 AHEN: Address Hold Enable bit ( \({ }^{2}\) C Slave mode only)
    \(1=\) Following the \(8^{\text {th }}\) falling edge of SCLx for a matching received address byte; the SCLREL bit (I2CxCON1<12>) will be cleared and the SCLx will be held low
    \(0=\) Address holding is disabled
    bit \(0 \quad\) DHEN: Data Hold Enable bit ( \(I^{2} \mathrm{C}\) Slave mode only)
    \(1=\) Following the \(8^{\text {th }}\) falling edge of SCLx for a received data byte; slave hardware clears the SCLREL bit (I2CxCON1<12>) and the SCLx is held low
    \(0=\) Data holding is disabled

    \section*{REGISTER 19-3: I2CxSTAT: I2Cx STATUS REGISTER}
    \begin{tabular}{|c|cc|c|c|c|c|c|c|}
    \hline R-0, HSC & R-0, HSC & R-0, HSC & U-0 & U-0 & R/C-0, HSC & R-0, HSC & R-0, HSC \\
    \hline ACKSTAT & TRSTAT & ACKTIM & - & - & BCL & GCSTAT & ADD10 \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|c|}
    \hline R/C-0, HS & R/C-0, HS & R-0, HSC & R/C-0, HSC & R/C-0, HSC & R-0, HSC & R-0, HSC & R-0, HSC \\
    \hline IWCOL & I2COV & D_A & P & S & R_W & RBF & TBF \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & C = Clearable bit & HS = Hardware Settable bit \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & ' 0 ' = Bit is cleared \(\quad \mathrm{x}=\) Bit is unknown \\
    HSC = Hardware Settable/Clearable bit & & \\
    \hline
    \end{tabular}
    bit 15 ACKSTAT: Acknowledge Status bit (updated in all Master and Slave modes)
    1 = Acknowledge was not received from slave
    0 = Acknowledge was received from slave
    bit 14 TRSTAT: Transmit Status bit (when operating as \(\mathrm{I}^{2} \mathrm{C}^{\mathrm{TM}}\) master; applicable to master transmit operation)
    \(1=\) Master transmit is in progress (8 bits \(+\overline{\mathrm{ACK}}\) )
    \(0=\) Master transmit is not in progress
    bit 13 ACKTIM: Acknowledge Time Status bit (valid in \(I^{2} \mathrm{C}\) Slave mode only)
    \(1=\) Indicates \(I^{2} \mathrm{C}\) bus is in an Acknowledge sequence, set on \(8^{\text {th }}\) falling edge of SCLx clock
    \(0=\) Not an Acknowledge sequence, cleared on \(9^{\text {th }}\) rising edge of SCLx clock
    bit 12-11 Unimplemented: Read as ' 0 '
    bit 10 BCL: Bus Collision Detect bit (Master/Slave mode; cleared when \(I^{2} \mathrm{C}\) module is disabled, I2CEN = 0)
    1 = A bus collision has been detected during a master or slave transmit operation
    \(0=\) Bus collision has not been detected
    bit 9 GCSTAT: General Call Status bit (cleared after Stop detection)
    1 = General call address was received
    \(0=\) General call address was not received
    bit 8 ADD10: 10-Bit Address Status bit (cleared after Stop detection)
    1 = 10-bit address was matched
    \(0=10\)-bit address was not matched
    bit \(7 \quad\) IWCOL: Write Collision Detect bit
    1 = An attempt to write to the I2CxTRN register failed because the \(I^{2} \mathrm{C}\) module is busy; must be cleared in software
    \(0=\) Collision has not occurred
    bit \(6 \quad\) I2COV: I2Cx Receive Overflow Flag bit
    1 = A byte was received while the I2CxRCV register is still holding the previous byte; I2COV is a "don't care" in Transmit mode, must be cleared in software
    \(0=\) Overflow has not occurred
    bit \(5 \quad\) D_A: Data/Address bit (when operating as \(I^{2} \mathrm{C}\) slave)
    1 = Indicates that the last byte received was data
    \(0=\) Indicates that the last byte received or transmitted was an address
    bit 4
    P: I2Cx Stop bit
    Updated when Start, Reset or Stop is detected; cleared when the \(I^{2} \mathrm{C}\) module is disabled, I2CEN \(=0\).
    1 = Indicates that a Stop bit has been detected last
    \(0=\) Indicates that a Stop bit was not detected last

    \section*{REGISTER 19-3: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)}
    bit \(3 \quad\) S: I2Cx Start bit
    Updated when Start, Reset or Stop is detected; cleared when the \(\mathrm{I}^{2} \mathrm{C}\) module is disabled, I2CEN \(=0\).
    1 = Indicates that a Start (or Repeated Start) bit has been detected last
    \(0=\) Indicates that a Start bit was not detected last
    bit 2 R_W: Read/Write Information bit (when operating as \(\mathrm{I}^{2} \mathrm{C}\) slave)
    1 = Read: Indicates that the data transfer is output from the slave
    \(0=\) Write: Indicates that the data transfer is input to the slave
    bit 1 RBF: Receive Buffer Full Status bit
    1 = Receive is complete, the I2CxRCV bit is full
    \(0=\) Receive is not complete, the I2CxRCV bit is empty
    bit 0
    TBF: Transmit Buffer Full Status bit
    1 = Transmit is in progress, I2CxTRN is full (8 bits of data)
    \(0=\) Transmit is complete, I2CxTRN is empty

    REGISTER 19-4: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & \(\mathrm{U}-0\) & \(\mathrm{U}-0\) & \(\mathrm{U}-0\) & \(\mathrm{U}-0\) & \(\mathrm{U}-0\) & \(\mathrm{R} / \mathrm{W}-0\) & R/W-0 \\
    \hline- & - & - & - & - & - & MSK<9:8> \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|llllllll|}
    \hline\(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) \\
    \hline & & \(M S K<7: 0>\) & & & \\
    \hline bit 7 & & & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & & \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared \(\quad \mathrm{x}=\) Bit is unknown \\
    \hline
    \end{tabular}
    \begin{tabular}{ll} 
    bit 15-10 & Unimplemented: Read as ' 0 ' \\
    bit 9-0 & MSK<9:0>: I2Cx Mask for Address Bit \(x\) Select bits \\
    & \(1=\) Enables masking for bit \(x\) of the incoming message address; bit match is not required in this position \\
    & \(0=\) Disables masking for bit \(x\); bit match is required in this position
    \end{tabular}

    \section*{dsPIC33EVXXXGM00X/10X FAMILY}

    NOTES:

    \subsection*{20.0 SINGLE-EDGE NIBBLE TRANSMISSION (SENT)}

    Note 1: This data sheet summarizes the features of this group of dsPIC33EVXXXGM00X/ 10X family devices. It is not intended to be a comprehensive reference source. For more information on Single-Edge Nibble Transmission, refer to "SingleEdge Nibble Transmission (SENT) Module" (DS70005145) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
    2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

    \subsection*{20.1 Module Introduction}

    The Single-Edge Nibble Transmission (SENT) module is based on the SAE J2716, "SENT - Single-Edge Nibble Transmission for Automotive Applications". The SENT protocol is a one-way, single wire time modulated serial communication, based on successive falling edges. It is intended for use in applications where high-resolution sensor data needs to be communicated from a sensor to an Engine Control Unit (ECU).
    The SENTx module has the following major features:
    - Selectable Transmit or Receive mode
    - Synchronous or Asynchronous Transmit modes
    - Automatic Data Rate Synchronization
    - Optional Automatic Detection of CRC Errors in Receive mode
    - Optional Hardware Calculation of CRC in Transmit mode
    - Support for Optional Pause Pulse Period
    - Data Buffering for One Message Frame
    - Selectable Data Length for Transmit/Receive from 3 to 6 Nibbles
    - Automatic Detection of Framing Errors

    SENT protocol timing is based on a predetermined time unit, TTICK. Both the transmitter and receiver must be preconfigured for TTICK, which can vary from 3 to \(90 \mu \mathrm{~s}\). A SENT message frame starts with a Sync pulse. The purpose of the Sync pulse is to allow the receiver to calculate the data rate of the message encoded by the transmitter. The SENT specification allows messages to be validated with up to a \(20 \%\) variation in Tтіск. This allows for the transmitter and receiver to run from different clocks that may be inaccurate, and drift with time and temperature. The data nibbles are 4 bits in length and are encoded as the data value +12 ticks. This yields a 0 value of 12 ticks and the maximum value, \(0 x F\), of 27 ticks.

    \section*{A SENT message consists of the following:}
    - A synchronization/calibration period of 56 tick times
    - A status nibble of 12-27 tick times
    - Up to six data nibbles of 12-27 tick times
    - A CRC nibble of 12-27 tick times
    - An optional pause pulse period of 12-768 tick times
    Figure 20-1 shows a block diagram of the SENTx module.

    Figure 20-2 shows the construction of a typical 6-nibble data frame, with the numbers representing the minimum or maximum number of tick times for each section.

    FIGURE 20-1: SENTx MODULE BLOCK DIAGRAM
    

    FIGURE 20-2: SENTx PROTOCOL DATA FRAMES
    

    \subsection*{20.2 Transmit Mode}

    By default, the SENTx module is configured for transmit operation. The module can be configured for continuous asynchronous message frame transmission, or alternatively, for Synchronous mode triggered by software. When enabled, the transmitter will send a Sync followed by the appropriate number of data nibbles, an optional CRC and optional pause pulse. The tick period used by the SENTx transmitter is set by writing a value to the TICKTIME<15:0> (SENTxCON2<15:0>) bits. The tick period calculations are shown in Equation 20-1.

    \section*{EQUATION 20-1: TICK PERIOD CALCULATION}
    TICKTIME \(<15: 0>=\frac{\text { TTICK }}{\text { TCLK }}-1\)

    An optional pause pulse can be used in Asynchronous mode to provide a fixed message frame time period. The frame period used by the SENTx transmitter is set by writing \(a\) value to the FRAMETIME<15:0> (SENTxCON3<15:0>) bits. The formulas used to calculate the value of frame time are shown in Equation 20-2.

    \section*{EQUATION 20-2: FRAME TIME} CALCULATIONS
    \[
    \begin{aligned}
    \text { FRAMETIME }<15: 0> & =\text { TTICK/TFRAME } \\
    \text { FRAMETIME }<15: 0> & \geq 122+27 \mathrm{~N} \\
    \text { FRAMETIME }<15: 0> & \geq 848+12 \mathrm{~N}
    \end{aligned}
    \]

    Where:
    TFRAME \(=\) Total time of the message from ms \(N=\) The number of data nibbles in message, 1-6

    Note: The module will not produce a pause period with less than 12 ticks, regardless of the FRAMETIME<15:0> value. FRAMETIME<15:0> values beyond 2047 will have no effect on the length of a data frame.

    \subsection*{20.2.1 TRANSMIT MODE CONFIGURATION}

    \subsection*{20.2.1.1 Initializing the SENTx Module:}

    Perform the following steps to initialize the module:
    1. Write RCVEN (SENTxCON1<11>) = for Transmit mode.
    2. Write TXM (SENTxCON1<10>) \(=0\) for Asynchronous Transmit mode or TXM = 1 for Synchronous mode.
    3. Write NIBCNT<2:0> (SENTxCON1<2:0>) for the desired data frame length.
    4. Write CRCEN (SENTxCON1<8>) for hardware or software CRC calculation.
    5. Write PPP (SENTxCON1<7>) for optional pause pulse.
    6. If PPP \(=1\), write TfRAme to SENTxCON3.
    7. Write SENTxCON2 with the appropriate value for desired tick period.
    8. Enable interrupts and set interrupt priority.
    9. Write initial status and data values to SENTxDATH/L.
    10. If \(C R C E N=0\), calculate \(C R C\) and write the value to \(\mathrm{CRC}<3: 0>\) (SENTxDATL<3:0>).
    11. Set the SNTEN (SENTxCON1<15>) bit to enable the module.
    User software updates to SENTxDATH/L must be performed after the completion of the CRC and before the next message frame's status nibble. The recommended method is to use the message frame completion interrupt to trigger data writes.

    \subsection*{20.3 Receive Mode}

    The module can be configured for receive operation by setting the RCVEN (SENTxCON1<11>) bit. The time between each falling edge is compared to SYNCMIN<15:0> (SENTxCON3<15:0>) and SYNCMAX<15:0> (SENTxCON2<15:0>), and if the measured time lies between the minimum and maximum limits, the module begins to receive data. The validated Sync time is captured in the SENTxSYNC register and the tick time is calculated. Subsequent falling edges are verified to be within the valid data width and the data is stored in the SENTxDATH/L register. An interrupt event is generated at the completion of the message and the user software should read the SENTx Data register before the reception of the next nibble. The equation for SYNCMIN<15:0> and SYNCMAX<15:0> is shown in Equation 20-3.

    \section*{EQUATION 20-3: SYNCMIN<15:0> AND SYNCMAX<15:0> CALCULATIONS}
    \[
    \begin{gathered}
    \text { TTICK }=\text { TCLK } \bullet(\text { TICKTIME }<15: 0>+1) \\
    \text { FRAMETIME }<15: 0>=\text { TTICK } / \text { TFRAME } \\
    \text { SyncCount }=8 \times \text { FRCV } \times \text { TTICK } \\
    \text { SYNCMIN }<15: 0>=0.8 \times \text { SyncCount } \\
    \text { SYNCMAX }<15: 0>=1.2 \times \text { SyncCount } \\
    \text { FRAMETIME }<15: 0>\geq 122+27 N \\
    \text { FRAMETIME }<15: 0>\geq 848+12 N
    \end{gathered}
    \]

    Where:
    TFRAME \(=\) Total time of the message from ms
    \(N=\) The number of data nibbles in message, 1-6
    \(F_{R C V}=\) FCY x prescaler
    TCLK \(=\) FCY/Prescaler

    For Ttick \(=3.0 \mu \mathrm{~s}\) and Fclk \(=4 \mathrm{MHz}\), SYNCMIN<15:0> \(=76\).

    Note: To ensure a Sync period can be identified, the value written to SYNCMIN<15:0> must be less than the value written to SYNCMAX<15:0>.

    \subsection*{20.3.1 RECEIVE MODE CONFIGURATION}

    \subsection*{20.3.1.1 Initializing the SENTx Module:}

    Perform the following steps to initialize the module:
    1. Write RCVEN (SENTxCON1<11>) = 1 for Receive mode.
    2. Write NIBCNT<2:0> (SENTxCON1<2:0>) for the desired data frame length.
    3. Write CRCEN (SENTxCON1<8>) for hardware or software CRC validation.
    4. Write PPP (SENTxCON1<7>) = 1 if pause pulse is present.
    5. Write SENTxCON2 with the value of SYNCMAXx (Nominal Sync Period + 20\%).
    6. Write SENTxCON3 with the value of SYNCMINx (Nominal Sync Period - 20\%).
    7. Enable interrupts and set interrupt priority.
    8. Set the SNTEN (SENTxCON1<15>) bit to enable the module.
    The data should be read from the SENTxDATH/L register after the completion of the CRC and before the next message frame's status nibble. The recommended method is to use the message frame completion interrupt trigger.

    \section*{REGISTER 20-1: SENTxCON1: SENTx CONTROL REGISTER 1}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & U-0 & R/W-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline SNTEN & - & SNTSIDL & - & RCVEN & TXM \({ }^{(1)}\) & TXPOL \({ }^{(1)}\) & CRCEN \\
    \hline \multicolumn{7}{|l|}{bit 15} & bit 8 \\
    \hline R/W-0 & R/W-0 & U-0 & R/W-0 & U-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline PPP & SPCEN \({ }^{(2)}\) & - & PS & - & NIBCNT2 & NIBCNT1 & NIBCNT0 \\
    \hline \multicolumn{2}{|l|}{bit 7} & & & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|}
    \hline \multicolumn{4}{|l|}{Legend:} \\
    \hline \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemente & as ' 0 ' \\
    \hline -n = Value at POR & ' 1 ' = Bit is set & ' 0 ' = Bit is cleared & \(x=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15 SNTEN: SENTx Enable bit
    1 = SENTx is enabled
    \(0=\) SENTx is disabled
    bit 14 Unimplemented: Read as ' 0 '
    bit 13 SNTSIDL: SENTx Stop in Idle Mode bit
    1 = Discontinues module operation when the device enters Idle mode
    \(0=\) Continues module operation in Idle mode
    bit 12 Unimplemented: Read as ' 0 '
    bit 11 RCVEN: SENTX Receive Enable bit
    \(1=\) SENTx operates as a receiver
    \(0=\) SENTx operates as a transmitter (sensor)
    bit 10 TXM: SENTx Transmit Mode bit \({ }^{(1)}\)
    1 = SENTx transmits data frame only when triggered using the SYNCTXEN status bit
    \(0=\) SENTx transmits data frames continuously while SNTEN \(=1\)
    bit \(9 \quad\) TXPOL: SENTx Transmit Polarity bit \({ }^{(1)}\)
    1 = SENTx data output pin is low in the Idle state
    \(0=\) SENTx data output pin is high in the Idle state
    bit 8 CRCEN: CRC Enable bit
    Module in Receive Mode (RCVEN = 1):
    1 = SENTx performs CRC verification on received data using the preferred J2716 method
    \(0=\) SENTx does not perform CRC verification on received data
    Module in Transmit Mode (RCVEN = 1):
    1 = SENTx automatically calculates CRC using the preferred J 2716 method
    \(0=\) SENTx does not calculate CRC
    bit \(7 \quad\) PPP: Pause Pulse Present bit
    1 = SENTx is configured to transmit/receive SENT messages with pause pulse
    \(0=\) SENTx is configured to transmit/receive SENT messages without pause pulse
    bit 6 SPCEN: Short PWM Code Enable bit \({ }^{(2)}\)
    1 = SPC control from external source is enabled
    \(0=\) SPC control from external source is disabled
    bit 5 Unimplemented: Read as ' 0 '
    bit 4 PS: SENTx Module Clock Prescaler (divider) bits
    1 = Divide-by-4
    \(0=\) Divide-by-1
    Note 1: This bit has no function in Receive mode (RCVEN =1).
    2: This bit has no function in Transmit mode (RCVEN \(=0\) ).

    \section*{REGISTER 20-1: SENTxCON1: SENTx CONTROL REGISTER 1 (CONTINUED)}
    bit \(3 \quad\) Unimplemented: Read as ' 0 '
    bit 2-0 NIBCNT<2:0>: Nibble Count Control bits
    111 = Reserved; do not use
    \(110=\) Module transmits/receives 6 data nibbles in a SENT data pocket
    101 = Module transmits/receives 5 data nibbles in a SENT data pocket
    \(100=\) Module transmits/receives 4 data nibbles in a SENT data pocket
    011 = Module transmits/receives 3 data nibbles in a SENT data pocket
    \(010=\) Module transmits/receives 2 data nibbles in a SENT data pocket
    \(001=\) Module transmits/receives 1 data nibbles in a SENT data pocket
    \(000=\) Reserved; do not use
    Note 1: This bit has no function in Receive mode (RCVEN =1).
    2: \(\quad\) This bit has no function in Transmit mode (RCVEN \(=0\) ).

    \section*{REGISTER 20-2: SENTxSTAT: SENTx STATUS REGISTER}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline - & - & - & - & - & - & - & - \\
    \hline \multicolumn{8}{|l|}{bit 15 bit 8} \\
    \hline R-0 & R-0 & R-0 & R-0 & R-0 & R/C-0 & R-0 & R/W/HC-0 \\
    \hline PAUSE & NIB2 & NIB1 & NIB0 & CRCERR & FRMERR & RXIDLE & SYNCTXEN \({ }^{(1)}\) \\
    \hline \multicolumn{8}{|l|}{bit 7 bit 0} \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & \(C=\) Clearable bit & HC = Hardware Clearable bit \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' = Bit is set & ' 0 ' = Bit is cleared \(\quad x=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-8 Unimplemented: Read as ' 0 '
    bit \(7 \quad\) PAUSE: Pause Period Status bit
    1 = The module is transmitting/receiving a pause period
    \(0=\) The module is not transmitting/receiving a pause period
    bit 6-4 NIB<2:0>: Nibble Status bit
    Module in Transmit Mode (RCVEN = 0):
    111 = Module is transmitting a CRC nibble
    \(110=\) Module is transmitting Data Nibble 6
    \(101=\) Module is transmitting Data Nibble 5
    \(100=\) Module is transmitting Data Nibble 4
    011 = Module is transmitting Data Nibble 3
    \(010=\) Module is transmitting Data Nibble 2
    001 = Module is transmitting Data Nibble 1
    \(000=\) Module is transmitting a status nibble or pause period, or is not transmitting
    Module in Receive Mode (RCVEN = 1):
    111 = Module is receiving a CRC nibble or was receiving this nibble when an error occurred
    \(110=\) Module is receiving Data Nibble 6 or was receiving this nibble when an error occurred
    101 = Module is receiving Data Nibble 5 or was receiving this nibble when an error occurred
    \(100=\) Module is receiving Data Nibble 4 or was receiving this nibble when an error occurred
    011 = Module is receiving Data Nibble 3 or was receiving this nibble when an error occurred
    \(010=\) Module is receiving Data Nibble 2 or was receiving this nibble when an error occurred
    \(001=\) Module is receiving Data Nibble 1 or was receiving this nibble when an error occurred
    \(000=\) Module is receiving a status nibble or waiting for Sync
    bit 3 CRCERR: CRC Status bit (Receive mode only)
    1 = A CRC error occurred for the 1-6 data nibbles in SENTxDATH/L
    \(0=\mathrm{A}\) CRC error has not occurred
    bit 2 FRMERR: Framing Error Status bit (Receive mode only)
    1 = A data nibble was received with less than 12 tick periods or greater than 27 tick periods
    0 = Framing error has not occurred
    bit 1 RXIDLE: SENTx Receiver Idle Status bit (Receive mode only)
    \(1=\) The SENTx data bus has been Idle (high) for a period of SYNCMAX<15:0> or greater
    \(0=\) The SENTx data bus is not Idle
    Note 1: In Receive mode (RCVEN = 1), the SYNCTXEN bit is read-only.

    \section*{REGISTER 20-2: SENTxSTAT: SENTx STATUS REGISTER (CONTINUED)}
    bit 0 SYNCTXEN: SENTx Synchronization Period Status/Transmit Enable bit \({ }^{(1)}\)
    Module in Receive Mode (RCVEN = 1):
    1 = A valid synchronization period was detected; the module is receiving nibble data
    \(0=\) No synchronization period has been detected; the module is not receiving nibble data
    Module in Asynchronous Transmit Mode (RCVEN = 0, TXM = 0):
    The bit always reads as ' 1 ' when the module is enabled, indicating the module transmits SENTx data frames continuously. The bit reads ' 0 ' when the module is disabled.
    Module in Synchronous Transmit Mode (RCVEN = 0, TXM = 1):
    1 = The module is transmitting a SENTx data frame
    \(0=\) The module is not transmitting a data frame, user software may set SYNCTXEN to start another data frame transmission

    Note 1: In Receive mode (RCVEN = 1), the SYNCTXEN bit is read-only.

    REGISTER 20-3: SENTxDATL: SENTX RECEIVE DATA REGISTER LOW \({ }^{(1)}\)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline & \multicolumn{2}{|l|}{DATA4<3:0>} & & \multicolumn{4}{|c|}{DATA5<3:0>} \\
    \hline \multicolumn{7}{|l|}{bit 15} & bit 8 \\
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{4}{|c|}{DATA6<3:0>} & \multicolumn{4}{|c|}{CRC<3:0>} \\
    \hline \multicolumn{7}{|l|}{bit 7} & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' \(=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-12 DATA4<3:0>: Data Nibble 4 Data bits
    bit 11-8 DATA5<3:0>: Data Nibble 5 Data bits
    bit 7-4 DATA6<3:0>: Data Nibble 6 Data bits
    bit 3-0 \(\quad\) CRC \(<3: 0>\) : CRC Nibble Data bits
    Note 1: Register bits are read-only in Receive mode ( \(R C V E N=1\) ). In Transmit mode, the \(C R C<3: 0>\) bits are read-only when automatic CRC calculation is enabled (RCVEN \(=0\), CRCEN \(=1\) ).

    \section*{REGISTER 20-4: SENTxDATH: SENTX RECEIVE DATA REGISTER HIGH \({ }^{(1)}\)}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{4}{|c|}{STAT<3:0>} & \multicolumn{4}{|c|}{DATA1<3:0>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lccccccc|}
    \hline\(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) & \(R / W-0\) \\
    \hline & DATA2 \(<3: 0>\) & & DATA3<3:0> & \\
    \hline bit 7 & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' \(=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-12 STAT<3:0>: Status Nibble Data bits
    bit 11-8 DATA1<3:0>: Data Nibble 1 Data bits
    bit 7-4 DATA2<3:0>: Data Nibble 2 Data bits
    bit 3-0 DATA3<3:0>: Data Nibble 3 Data bits
    Note 1: Register bits are read-only in Receive mode ( \(R C V E N=1\) ). In Transmit mode, the \(C R C<3: 0>\) bits are read-only when automatic CRC calculation is enabled (RCVEN \(=0, \operatorname{CRCEN}=1\) ).

    \section*{dsPIC33EVXXXGM00X/10X FAMILY}

    NOTES:

    \subsection*{21.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)}

    Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Universal Asynchronous Receiver Transmitter (UART)" (DS70000582) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
    2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

    The dsPIC33EVXXXGM00X/10X family of devices contains two UART modules.
    The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EVXXXGM00X/10X device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a
    hardware flow control option with the \(\overline{U x C T S}\) and UxRTS pins, and also includes an IrDA \({ }^{\circledR}\) encoder and decoder.

    Note: Hardware flow control using \(\overline{U x R T S}\) and \(\overline{\text { UxCTS }}\) is not available on all pin count devices. See the "Pin Diagrams" section for availability.

    The primary features of the UARTx module are:
    - Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
    - Even, Odd or No Parity Options (for 8-bit data)
    - One or Two Stop Bits
    - Hardware Flow Control Option with \(\overline{U x C T S}\) and UxRTS Pins
    - Fully Integrated Baud Rate Generator with 16-Bit Prescaler
    - Baud Rates Ranging from 4.375 Mbps to 67 bps at \(16 x\) mode at 70 MIPS
    - Baud Rates Ranging from 17.5 Mbps to 267 bps at \(4 x\) mode at 70 MIPS
    - 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
    - 4-Deep FIFO Receive Data Buffer
    - Parity, Framing and Buffer Overrun Error Detection
    - Support for 9-Bit mode with Address Detect ( \(9^{\text {th }}\) bit \(=1\) )
    - Transmit and Receive Interrupts
    - A Separate Interrupt for All UART Error Conditions

    FIGURE 21-1: UARTx SIMPLIFIED BLOCK DIAGRAM
    

    \subsection*{21.1 UART Helpful Tips}
    1. In multi-node direct connect UART networks, UART receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the \(R X\) line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pullup or pull-down resistor on the RX pin, depending on the value of the URXINV bit.
    a) If \(\mathrm{URXINV}=0\), use a pull-up resistor on the RX pin.
    b) If \(\operatorname{URXINV}=1\), use a pull-down resistor on the \(R X\) pin.
    2. The first character received on wake-up from Sleep mode, caused by activity on the UxRX pin of the UART module, will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid. This is to be expected.

    \subsection*{21.2 UART Control Registers}

    \section*{REGISTER 21-1: UxMODE: UARTx MODE REGISTER}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & U-0 & R/W-0 & R/W-0 \\
    \hline UARTEN \(^{(1)}\) & - & USIDL & IREN \(^{(2)}\) & RTSMD & - & UEN1 & UEN0 \\
    \hline bit 15 &
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline R/W-0, HC & R/W-0 & R/W-0, HC & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline WAKE & LPBACK & ABAUD & URXINV & BRGH & PDSEL1 & PDSEL0 & STSEL \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & \(\mathrm{HC}=\) Hardware Clearable bit & \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared \(\quad x=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15 UARTEN: UARTx Enable bit \({ }^{(1)}\)
    \(1=\) UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>
    \(0=\) UARTx is disabled; all UARTx pins are controlled by PORT latches; UARTx power consumption is minimal
    bit 14 Unimplemented: Read as ' 0 '
    bit 13 USIDL: UARTx Stop in Idle Mode bit
    1 = Discontinues module operation when the device enters Idle mode
    \(0=\) Continues module operation in Idle mode
    bit 12 IREN: IrDA \({ }^{\circledR}\) Encoder and Decoder Enable bit \({ }^{(2)}\)
    \(1=\operatorname{IrDA}\) encoder and decoder are enabled
    \(0=\operatorname{IrDA}\) encoder and decoder are disabled
    bit \(11 \quad\) RTSMD: Mode Selection for \(\overline{\text { UxRTS }}\) Pin bit
    \(1=\overline{\text { UxRTS }}\) pin is in Simplex mode
    \(0=\overline{\text { UxRTS }}\) pin is in Flow Control mode
    bit \(10 \quad\) Unimplemented: Read as ' 0 '
    bit 9-8 UEN<1:0>: UARTx Pin Enable bits
    \(11=U x T X, U x R X\) and BCLKx pins are enabled and used; \(\overline{U x C T S}\) pin is controlled by PORT latches \({ }^{(3)}\)
    \(10=U x T X, U x R X, \overline{U x C T S}\) and \(\overline{U x R T S}\) pins are enabled and used \({ }^{(4)}\)
    \(01=U x T X, U x R X\) and \(\overline{U x R T S}\) pins are enabled and used; \(\overline{U x C T S}\) pin is controlled by PORT latches \({ }^{(4)}\)
    \(00=\) UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/BCLKx pins are controlled by PORT latches
    bit 7 WAKE: UARTx Wake-up on Start bit Detect During Sleep Mode Enable bit
    \(1=\) UARTx continues to sample the UxRX pin; interrupt is generated on the falling edge, bit is cleared in hardware on the following rising edge
    \(0=\) Wake-up is not enabled
    bit 6 LPBACK: UARTx Loopback Mode Select bit
    1 = Loopback mode is enabled
    \(0=\) Loopback mode is disabled
    Note 1: Refer to "Universal Asynchronous Receiver Transmitter (UART)" (DS70000582) in the "dsPIC33/PIC24 Family Reference Manual" for information on enabling the UART module for receive or transmit operation.
    2: This feature is only available for the \(16 x\) BRG mode ( \(\mathrm{BRGH}=0\) ).
    3: This feature is only available on 44-pin and 64-pin devices.
    4: This feature is only available on 64-pin devices.

    \section*{REGISTER 21-1: UxMODE: UARTx MODE REGISTER (CONTINUED)}
    bit 5 ABAUD: Auto-Baud Enable bit
    \(1=\) Baud rate measurement on the next character is enabled - requires reception of a Sync field (55h)
    before other data; cleared in hardware upon completion
    \(0=\) Baud rate measurement is disabled or has completed
    bit 4 URXINV: UARTx Receive Polarity Inversion bit
    \(1=U \times R X\) Idle state is ' 0 '
    \(0=U \times R X\) Idle state is ' 1 '
    bit 3 BRGH: High Baud Rate Enable bit
    \(1=\) BRG generates 4 clocks per bit period ( \(4 x\) baud clock, High-Speed mode)
    \(0=\) BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
    bit 2-1 PDSEL<1:0>: Parity and Data Selection bits
    11 = 9-bit data, no parity
    \(10=8\)-bit data, odd parity
    \(01=8\)-bit data, even parity
    \(00=8\)-bit data, no parity
    bit \(0 \quad\) STSEL: Stop Bit Selection bit
    1 = Two Stop bits
    \(0=\) One Stop bit
    Note 1: Refer to "Universal Asynchronous Receiver Transmitter (UART)" (DS70000582) in the "dsPIC33/PIC24 Family Reference Manual" for information on enabling the UART module for receive or transmit operation.
    2: This feature is only available for the \(16 x \operatorname{BRG}\) mode ( \(\mathrm{BRGH}=0\) ).
    3: This feature is only available on 44-pin and 64-pin devices.
    4: This feature is only available on 64-pin devices.

    \section*{REGISTER 21-2: UxSTA: UARTx STATUS AND CONTROL REGISTER}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & U-0 & R/W-0, HC & R/W-0 & R-0 & R-1 \\
    \hline UTXISEL1 & UTXINV & UTXISEL0 & - & UTXBRK & UTXEN \({ }^{(1)}\) & UTXBF & TRMT \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R-1 & R-0 & R-0 & R/C-0 & R-0 \\
    \hline URXISEL1 & URXISEL0 & ADDEN & RIDLE & PERR & FERR & OERR & URXDA \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & \(C=\) Clearable bit & HC = Hardware Clearable bit \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared \(\quad x=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15,13 UTXISEL<1:0>: UARTx Transmission Interrupt Mode Selection bits
    11 = Reserved; do not use
    \(10=\) Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
    01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
    \(00=\) Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
    bit 14 UTXINV: UARTx Transmit Polarity Inversion bit
    If IREN \(=0\) :
    1 = UxTX Idle state is ' 0 '
    \(0=U x T X\) Idle state is ' 1 '
    If IREN = 1:
    \(1=\operatorname{IrDA}{ }^{\circledR}\) encoded UxTX Idle state is ' 1 '
    \(0=\) IrDA encoded UxTX Idle state is ' 0 '
    bit 12 Unimplemented: Read as ' 0 '
    bit 11 UTXBRK: UARTx Transmit Break bit
    1 = Sends Sync Break on next transmission - Start bit, followed by twelve ' 0 ' bits, followed by Stop bit; cleared by hardware upon completion
    \(0=\) Sync Break transmission is disabled or has completed
    bit 10 UTXEN: UARTx Transmit Enable bit \({ }^{(1)}\)
    1 = Transmit is enabled, UxTX pin is controlled by UARTx
    \(0=\) Transmit is disabled, any pending transmission is aborted and the buffer is reset; UxTX pin is controlled by the PORT
    bit 9 UTXBF: UARTx Transmit Buffer Full Status bit (read-only)
    1 = Transmit buffer is full
    \(0=\) Transmit buffer is not full, at least one more character can be written
    bit 8 TRMT: Transmit Shift Register Empty bit (read-only)
    1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
    \(0=\) Transmit Shift Register is not empty, a transmission is in progress or queued
    bit 7-6 URXISEL<1:0>: UARTx Receive Interrupt Mode Selection bits
    11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
    \(10=\) Interrupt is set on UxRSR transfer, making the receive buffer \(3 / 4\) full (i.e., has 3 data characters)
    \(0 \mathrm{x}=\) Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters

    Note 1: Refer to "Universal Asynchronous Receiver Transmitter (UART)" (DS70000582) in the "dsPIC33/ PIC24 Family Reference Manual" for information on enabling the UART module for transmit operation.

    \section*{REGISTER 21-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)}
    bit 5 ADDEN: Address Character Detect bit (bit 8 of received data \(=1\) )
    1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
    \(0=\) Address Detect mode is disabled
    bit 4 RIDLE: Receiver Idle bit (read-only)
    1 = Receiver is Idle
    \(0=\) Receiver is active
    bit 3 PERR: Parity Error Status bit (read-only)
    1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
    \(0=\) Parity error has not been detected
    bit 2 FERR: Framing Error Status bit (read-only)
    \(1=\) Framing error has been detected for the current character (character at the top of the receive FIFO)
    \(0=\) Framing error has not been detected
    bit 1 OERR: Receive Buffer Overrun Error Status bit (clear/read-only)
    1 = Receive buffer has overflowed
    \(0=\) Receive buffer has not overflowed; clearing a previously set OERR bit ( \(1 \rightarrow 0\) transition) resets the receive buffer and the UxRSR to the empty state
    bit \(0 \quad\) URXDA: UARTx Receive Buffer Data Available bit (read-only)
    \(1=\) Receive buffer has data, at least one more character can be read
    \(0=\) Receive buffer is empty
    Note 1: Refer to "Universal Asynchronous Receiver Transmitter (UART)" (DS70000582) in the "dsPIC33/ PIC24 Family Reference Manual" for information on enabling the UART module for transmit operation.

    \subsection*{22.0 CONTROLLER AREA NETWORK (CAN) MODULE (dsPIC33EVXXXGM10X DEVICES ONLY)}

    Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Enhanced Controller Area Network (ECAN \({ }^{\text {TM }}\) )" (DS70353) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
    2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

    \subsection*{22.1 Overview}

    The Controller Area Network (CAN) module is a serial interface, useful for communicating with other CAN modules or microcontroller devices. This interface/ protocol was designed to allow communications within noisy environments. The dsPIC33EVXXXGM10X devices contain one CAN module.

    The CAN module is a communication controller implementing the CAN 2.0 A/B protocol, as defined in the BOSCH CAN specification. The module supports CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system. The CAN specification is not covered within this data sheet. The reader can refer to the BOSCH CAN specification for further details.

    The CAN module features are as follows:
    - Implementation of the CAN Protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
    - Standard and Extended Data Frames
    - 0 to 8-Byte Data Length
    - Programmable Bit Rate, up to \(1 \mathrm{Mbit} / \mathrm{sec}\)
    - Automatic Response to Remote Transmission Requests
    - Up to Eight Transmit Buffers with Application Specified Prioritization and Abort Capability (each buffer can contain up to 8 bytes of data)
    - Up to 32 Receive Buffers (each buffer can contain up to 8 bytes of data)
    - Up to 16 Full (Standard/Extended Identifier) Acceptance Filters
    - Three Full Acceptance Filter Masks
    - DeviceNet \({ }^{\text {TM }}\) Addressing Support
    - Programmable Wake-up Functionality with Integrated Low-Pass Filter
    - Programmable Loopback Mode Supports Self-Test Operation
    - Signaling through Interrupt Capabilities for All CAN Receiver and Transmitter Error States
    - Programmable Clock Source
    - Programmable Link to Input Capture 2 (IC2) module for Timestamping and Network Synchronization
    - Low-Power Sleep and Idle Modes

    The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors, and then matched against filters to see if it should be received and stored in one of the Receive registers.

    Figure 22-1 shows a block diagram of the CANx module.

    FIGURE 22-1: CANx MODULE BLOCK DIAGRAM
    

    \subsection*{22.2 Modes of Operation}

    The CANx module can operate in one of several operation modes selected by the user. These modes include:
    - Initialization mode
    - Disable mode
    - Normal Operation mode
    - Listen Only mode
    - Listen All Messages mode
    - Loopback mode

    Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

    \subsection*{22.3 CAN Control Registers}

    \section*{REGISTER 22-1: CxCTRL1: CANx CONTROL REGISTER 1}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-1 & R/W-0 & R/W-0 \\
    \hline- & - & CSIDL & ABAT & CANCKS & REQOP2 & REQOP1 & REQOP0 \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R-1 & R-0 & R-0 & U-0 & R/W-0 & U-0 & U-0 & R/W-0 \\
    \hline OPMODE2 & OPMODE1 & OPMODE0 & - & CANCAP & - & - & WIN \\
    \hline bit 7
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & & \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & 0 ' = Bit is cleared \\
    \hline
    \end{tabular}
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13 CSIDL: CANx Stop in Idle Mode bit
    1 = Discontinues module operation when the device enters Idle mode
    \(0=\) Continues module operation in Idle mode
    bit 12
    ABAT: Abort All Pending Transmissions bit
    1 = Signals all transmit buffers to abort transmission
    \(0=\) Module will clear this bit when all transmissions are aborted
    bit 11 CANCKS: CANx Module Clock (FCAN) Source Select bit
    1 = FCAN is equal to 2 * FP
    \(0=\) FCAN is equal to Fp
    bit 10-8 REQOP<2:0>: Request Operation Mode bits
    111 = Sets Listen All Messages mode
    \(110=\) Reserved
    101 = Reserved
    \(100=\) Sets Configuration mode
    011 = Sets Listen Only mode
    010 = Sets Loopback mode
    001 = Sets Disable mode
    \(000=\) Sets Normal Operation mode
    bit 7-5 OPMODE<2:0>: Operation Mode bits
    111 = Module is in Listen All Messages mode
    \(110=\) Reserved
    101 = Reserved
    \(100=\) Module is in Configuration mode
    \(011=\) Module is in Listen Only mode
    \(010=\) Module is in Loopback mode
    001 = Module is in Disable mode
    \(000=\) Module is in Normal Operation mode
    bit 4 Unimplemented: Read as ' 0 '
    bit 3 CANCAP: CANx Message Receive Timer Capture Event Enable bit
    1 = Enables input capture based on CAN message receive
    0 = Disables CAN capture
    bit 2-1 Unimplemented: Read as ' 0 '
    bit \(0 \quad\) WIN: SFR Map Window Select bit
    1 = Uses filter window
    \(0=\) Uses buffer window

    \section*{REGISTER 22-2: CxCTRL2: CANx CONTROL REGISTER 2}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline- & - & - & - & - & - & - & - \\
    \hline bit 15 & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|l|c|c|ccccc|}
    \hline U-0 & U-0 & U-0 & R-0 & R-0 & R-0 & R-0 & R-0 \\
    \hline- & - & - & & & DNCNT<4:0> & & \\
    \hline bit 7 & & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & & \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared \(\quad x=\) Bit is unknown \\
    \hline
    \end{tabular}
    \begin{tabular}{ll} 
    bit 15-5 & Unimplemented: Read as '0' \\
    bit 4-0 & DNCNT<4:0>: DeviceNet \({ }^{\text {TM }}\) Filter Bit Number bits \\
    & \(10010-11111=\) Invalid selection \\
    & \(10001=\) Compare up to Data Byte 3, bit 6 with EID<17> \\
    & - \\
    & \(00001=\) Compare up to Data Byte 1, bit 7 with EID<0> \\
    & \(00000=\) Do not compare data bytes
    \end{tabular}

    \section*{REGISTER 22-3: CxVEC: CANx INTERRUPT CODE REGISTER}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & R-0 & R-0 & R-0 & R-0 & R-0 \\
    \hline- & - & - & FILHIT4 & FILHIT3 & FILHIT2 & FILHIT1 & FILHIT0 \\
    \hline bit 15 & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & R-1 & R-0 & R-0 & R-0 & R-0 & R-0 & R-0 \\
    \hline- & ICODE6 & ICODE5 & ICODE4 & ICODE3 & ICODE2 & ICODE1 & ICODE0 \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}
    bit 15-13 Unimplemented: Read as ' 0 '
    bit 12-8 FILHIT<4:0>: Filter Hit Number bits
    10000-11111 = Reserved
    01111 = Filter 15
    -
    -

    00001 = Filter 1
    \(00000=\) Filter 0
    bit \(7 \quad\) Unimplemented: Read as ' 0 '
    bit 6-0 ICODE<6:0>: Interrupt Flag Code bits
    1000101-1111111 = Reserved
    \(1000100=\) FIFO almost full interrupt
    1000011 = Receiver overflow interrupt
    \(1000010=\) Wake-up interrupt
    1000001 = Error interrupt
    \(1000000=\) No interrupt
    -
    -
    -
    0010000-0111111 = Reserved
    \(0001111=\) RB15 buffer interrupt
    -
    -
    0001001 = RB9 buffer interrupt
    \(0001000=\) RB8 buffer interrupt
    \(0000111=\) TRB7 buffer interrupt
    \(0000110=\) TRB6 buffer interrupt
    0000101 = TRB5 buffer interrupt
    \(0000100=\) TRB4 buffer interrupt
    0000011 = TRB3 buffer interrupt
    \(0000010=\) TRB2 buffer interrupt
    \(0000001=\) TRB1 buffer interrupt
    \(0000000=\) TRBO Buffer interrupt

    REGISTER 22-4: CxFCTRL: CANx FIFO CONTROL REGISTER
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline DMABS2 & DMABS1 & DMABS0 & - & - & - & - & - \\
    \hline bit 15 & & \\
    bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & FSA5 & FSA4 & FSA3 & FSA2 & FSA1 & FSA0 \\
    \hline bit 7 &
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-13 DMABS<2:0>: DMA Buffer Size bits
    111 = Reserved
    \(110=32\) buffers in RAM
    \(101=24\) buffers in RAM
    \(100=16\) buffers in RAM
    \(011=12\) buffers in RAM
    \(010=8\) buffers in RAM
    \(001=6\) buffers in RAM
    \(000=4\) buffers in RAM
    bit 12-6 Unimplemented: Read as ' 0 '
    bit 5-0 FSA<5:0>: FIFO Area Starts with Buffer bits
    11111 = Receive Buffer RB31
    11110 = Receive Buffer RB30
    -
    -
    -
    00001 = TX/RX Buffer TRB1
    \(00000=\) TX/RX Buffer TRB0

    \section*{REGISTER 22-5: CxFIFO: CANx FIFO STATUS REGISTER}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R-0 & R-0 & R-0 & R-0 & R-0 & R-0 \\
    \hline- & - & FBP5 & FBP4 & FBP3 & FBP2 & FBP1 & FBP0 \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R-0 & R-0 & R-0 & R-0 & R-0 & R-0 \\
    \hline- & - & FNRB5 & FNRB4 & FNRB3 & FNRB2 & FNRB1 & FNRB0 \\
    \hline bit 7 & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13-8 FBP<5:0>: FIFO Buffer Pointer bits
    ```

    011111 = RB31 buffer
    011110 = RB30 buffer
    •
    -
    000001 = TRB1 buffer
    000000 = TRB0 buffer

    ```
    bit 7-6 Unimplemented: Read as ' 0 '
    bit 5-0 FNRB<5:0>: FIFO Next Read Buffer Pointer bits
    011111 = RB31 buffer
    011110 = RB30 buffer
    -
    -

    000001 = TRB1 buffer
    \(000000=\) TRBO buffer

    \section*{REGISTER 22-6: CxINTF: CANx INTERRUPT FLAG REGISTER}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & R-0 & R-0 & R-0 & R-0 & R-0 & R-0 \\
    \hline- & - & TXBO & TXBP & RXBP & TXWAR & RXWAR & EWARN \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline R/C-0 & R/C-0 & R/C-0 & U-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 \\
    \hline IVRIF & WAKIF & ERRIF & - & FIFOIF & RBOVIF & RBIF & TBIF \\
    \hline bit 7 & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & \(C=\) Writable bit, but only ' 0 ' can be written to clear the bit \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' = Bit is set & ' 0 ' = Bit is cleared \(\quad x=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-14 Unimplemented: Read as ' 0 '
    bit 13 TXBO: Transmitter in Error State Bus Off bit
    1 = Transmitter is in Bus Off state
    \(0=\) Transmitter is not in Bus Off state
    bit 12 TXBP: Transmitter in Error State Bus Passive bit
    1 = Transmitter is in Bus Passive state
    \(0=\) Transmitter is not in Bus Passive state
    bit 11 RXBP: Receiver in Error State Bus Passive bit
    1 = Receiver is in Bus Passive state
    \(0=\) Receiver is not in Bus Passive state
    bit 10 TXWAR: Transmitter in Error State Warning bit
    1 = Transmitter is in Error Warning state
    \(0=\) Transmitter is not in Error Warning state
    bit 9 RXWAR: Receiver in Error State Warning bit
    1 = Receiver is in Error Warning state
    \(0=\) Receiver is not in Error Warning state
    bit 8 EWARN: Transmitter or Receiver in Error State Warning bit
    1 = Transmitter or receiver is in Error Warning state
    \(0=\) Transmitter or receiver is not in Error Warning state
    bit \(7 \quad\) IVRIF: Invalid Message Interrupt Flag bit
    1 = Interrupt request has occurred
    0 = Interrupt request has not occurred
    bit \(6 \quad\) WAKIF: Bus Wake-up Activity Interrupt Flag bit
    1 = Interrupt request has occurred
    \(0=\) Interrupt request has not occurred
    bit 5 ERRIF: Error Interrupt Flag bit (multiple sources in CxINTF<13:8> register)
    1 = Interrupt request has occurred
    \(0=\) Interrupt request has not occurred
    bit \(4 \quad\) Unimplemented: Read as ' 0 '
    bit \(3 \quad\) FIFOIF: FIFO Almost Full Interrupt Flag bit
    1 = Interrupt request has occurred
    \(0=\) Interrupt request has not occurred
    bit \(2 \quad\) RBOVIF: RX Buffer Overflow Interrupt Flag bit
    1 = Interrupt request has occurred
    \(0=\) Interrupt request has not occurred

    \section*{REGISTER 22-6: CxINTF: CANx INTERRUPT FLAG REGISTER (CONTINUED)}
    bit \(1 \quad\) RBIF: RX Buffer Interrupt Flag bit
    \(1=\) Interrupt request has occurred
    \(0=\) Interrupt request has not occurred
    bit 0
    TBIF: TX Buffer Interrupt Flag bit
    \(1=\) Interrupt request has occurred
    \(0=\) Interrupt request has not occurred

    REGISTER 22-7: CxINTE: CANx INTERRUPT ENABLE REGISTER
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline- & - & - & - & - & - & - & - \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline IVRIE & WAKIE & ERRIE & - & FIFOIE & RBOVIE & RBIE & TBIE \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & & \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared \(\quad x=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-8 Unimplemented: Read as ' 0 '
    bit \(7 \quad\) IVRIE: Invalid Message Interrupt Enable bit
    \(1=\) Interrupt request is enabled
    \(0=\) Interrupt request is not enabled
    bit 6 WAKIE: Bus Wake-up Activity Interrupt Enable bit
    \(1=\) Interrupt request is enabled
    \(0=\) Interrupt request is not enabled
    bit 5 ERRIE: Error Interrupt Enable bit
    1 = Interrupt request is enabled
    \(0=\) Interrupt request is not enabled
    bit \(4 \quad\) Unimplemented: Read as ' 0 '
    bit \(3 \quad\) FIFOIE: FIFO Almost Full Interrupt Enable bit
    1 = Interrupt request is enabled
    0 = Interrupt request is not enabled
    bit 2 RBOVIE: RX Buffer Overflow Interrupt Enable bit
    1 = Interrupt request is enabled
    \(0=\) Interrupt request is not enabled
    bit 1 RBIE: RX Buffer Interrupt Enable bit
    1 = Interrupt request is enabled
    \(0=\) Interrupt request is not enabled
    bit \(0 \quad\) TBIE: TX Buffer Interrupt Enable bit
    1 = Interrupt request is enabled
    \(0=\) Interrupt request is not enabled

    REGISTER 22-8: CxEC: CANx TRANSMIT/RECEIVE ERROR COUNT REGISTER
    \begin{tabular}{|lllllll|}
    \hline R-0 & R-0 & R-0 & R-0 & R-0 & R-0 & R-0
    \end{tabular}\(\quad\) R-0 \begin{tabular}{llll|}
    \hline & & TERRCNT<7:0> & \\
    \hline bit 15 & & & \\
    \hline
    \end{tabular}
    \begin{tabular}{|lllllll|}
    \hline R-0 & R-0 & R-0 & R-0 & R-0 & R-0 & R-0
    \end{tabular}\(\quad\) R-0 10

    \section*{Legend:}
    \begin{tabular}{|c|c|c|c|}
    \hline \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplement & as ' 0 ' \\
    \hline -n = Value at POR & ' 1 ' = Bit is set & ' 0 ' = Bit is cleared & \(\mathrm{x}=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-8 TERRCNT<7:0>: Transmit Error Count bits
    bit 7-0 RERRCNT<7:0>: Receive Error Count bits

    REGISTER 22-9: CxCFG1: CANx BAUD RATE CONFIGURATION REGISTER 1
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline- & - & - & - & - & - & - & - \\
    \hline bit 15 &
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline SJW1 & SJW0 & BRP5 & BRP4 & BRP3 & BRP2 & BRP1 & BRP0 \\
    \hline \multicolumn{8}{|l|}{bit \(7 \times\) bit 0} \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & & \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' \(=\) Bit is set & \(' 0\) ' = Bit is cleared \(\quad x=\) Bit is unknown \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|}
    \hline bit 15-8 & Unimplemented: Read as ' 0 ' \\
    \hline \multirow[t]{5}{*}{bit 7-6} & SJW<1:0>: Synchronization Jump Width bits \\
    \hline & \(11=\) Length is \(4 \times \mathrm{TQ}\) \\
    \hline & \(10=\) Length is \(3 \times \mathrm{TQ}\) \\
    \hline & \(01=\) Length is \(2 \times \mathrm{TQ}\) \\
    \hline & \(00=\) Length is \(1 \times\) TQ \\
    \hline \multirow[t]{8}{*}{bit 5-0} & BRP<5:0>: Baud Rate Prescaler bits \\
    \hline & \(111111=\) TQ \(=2 \times 64 \times 1 / \mathrm{FCAN}\) \\
    \hline & - \\
    \hline & - \\
    \hline & - \\
    \hline & \(000010=\) TQ \(=2 \times 3 \times 1 /\) FCAN \\
    \hline & \(000001=\) TQ \(=2 \times 2 \times 1 /\) CCAN \\
    \hline & \(000000=\) TQ \(=2 \times 1 \times 1 / \mathrm{FCAN}\) \\
    \hline
    \end{tabular}

    REGISTER 22-10: CxCFG2: CANx BAUD RATE CONFIGURATION REGISTER 2
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & R/W-x & U-0 & U-0 & U-0 & R/W-x & R/W-x & R/W-x \\
    \hline- & WAKFIL & - & - & - & SEG2PH2 & SEG2PH1 & SEG2PH0 \\
    \hline bit 15 \\
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x \\
    \hline SEG2PHTS & SAM & SEG1PH2 & SEG1PH1 & SEG1PH0 & PRSEG2 & PRSEG1 & PRSEG0 \\
    \hline bit 7 &
    \end{tabular}
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}
    bit 15 Unimplemented: Read as ' 0 '
    bit 14 WAKFIL: Select CAN Bus Line Filter for Wake-up bit
    1 = Uses CAN bus line filter for wake-up
    \(0=\) CAN bus line filter is not used for wake-up
    bit 13-11 Unimplemented: Read as ' 0 '
    bit 10-8 SEG2PH<2:0>: Phase Segment 2 bits
    \(111=\) Length is \(8 \times\) TQ
    -
    -
    -
    \(000=\) Length is \(1 \times\) TQ
    bit 7 SEG2PHTS: Phase Segment 2 Time Select bit
    1 = Freely programmable
    \(0=\) Maximum of SEG1PH<2;0> bits or Information Processing Time (IPT), whichever is greater
    bit 6
    SAM: Sample of the CAN Bus Line bit
    1 = Bus line is sampled three times at the sample point
    \(0=\) Bus line is sampled once at the sample point
    bit 5-3 SEG1PH<2:0>: Phase Segment 1 bits
    \(111=\) Length is \(8 \times\) TQ
    -
    -
    -
    \(000=\) Length is \(1 \times\) TQ
    bit 2-0 PRSEG<2:0>: Propagation Time Segment bits
    \(111=\) Length is \(8 \times\) TQ
    -
    -
    -
    \(000=\) Length is \(1 \times\) TQ

    REGISTER 22-11: CxFEN1: CANx ACCEPTANCE FILTER ENABLE REGISTER 1
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-1 \\
    \hline \multicolumn{8}{|c|}{FLTEN<15:8>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-1 & R/W-1 \\
    \hline \multicolumn{8}{|c|}{FLTEN<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{|c|c|c|c|}
    \hline \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \multicolumn{2}{|l|}{\(\mathrm{U}=\) Unimplemented bit, read as ' 0 '} \\
    \hline -n = Value at POR & ' 1 ' = Bit is set & ' 0 ' = Bit is cleared & \(x=B\) \\
    \hline
    \end{tabular}
    bit 15-0 FLTEN<15:0>: Enable Filter n to Accept Messages bits
    1 = Enables Filter n
    0 = Disables Filter n

    \section*{REGISTER 22-12: CxBUFPNT1: CANx FILTERS 0-3 BUFFER POINTER REGISTER 1}
    \begin{tabular}{|l|l|l|l|l|l|l|l|l|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline F3BP3 & F3BP2 & F3BP1 & F3BP0 & F2BP3 & F2BP2 & F2BP1 & F2BP0 \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|l|l|l|l|l|l|l|l|l|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline F1BP3 & F1BP2 & F1BP1 & F1BP0 & F0BP3 & F0BP2 & F0BP1 & F0BP0 \\
    \hline bit 7
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-12 F3BP<3:0>: RX Buffer Mask for Filter 3 bits
    1111 = Filter hits received in RX FIFO buffer
    \(1110=\) Filter hits received in RX Buffer 14
    -
    -
    -
    0001 = Filter hits received in RX Buffer 1
    \(0000=\) Filter hits received in RX Buffer 0
    bit 11-8 F2BP<3:0>: RX Buffer Mask for Filter 2 bits (same values as bits 15-12)
    bit 7-4 \(\quad\) F1BP \(<3: 0>\) : RX Buffer Mask for Filter 1 bits (same values as bits 15-12)
    bit 3-0 \(\quad\) FOBP<3:0>: RX Buffer Mask for Filter 0 bits (same values as bits 15-12)

    REGISTER 22-13: CxBUFPNT2: CANx FILTER 4-7 BUFFER POINTER REGISTER 2
    \begin{tabular}{|l|l|l|l|l|l|l|l|l|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline F7BP3 & F7BP2 & F7BP1 & F7BP0 & F6BP3 & F6BP2 & F6BP1 & F6BP0 \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|l|l|l|l|l|l|l|l|l|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline F5BP3 & F5BP2 & F5BP1 & F5BP0 & F4BP3 & F4BP2 & F4BP1 & F4BP0 \\
    \hline bit 7
    \end{tabular}

    Legend:
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-12 F7BP<3:0>: RX Buffer Mask for Filter 7 bits
    1111 = Filter hits received in RX FIFO buffer
    \(1110=\) Filter hits received in RX Buffer 14
    -
    -
    -
    0001 = Filter hits received in RX Buffer 1 \(0000=\) Filter hits received in RX Buffer 0
    bit 11-8 \(\quad\) F6BP<3:0>: RX Buffer Mask for Filter 6 bits (same values as bits 15-12)
    bit 7-4 F5BP<3:0>: RX Buffer Mask for Filter 5 bits (same values as bits 15-12)
    bit 3-0 F4BP<3:0>: RX Buffer Mask for Filter 4 bits (same values as bits 15-12)

    REGISTER 22-14: CxBUFPNT3: CANx FILTERS 8-11 BUFFER POINTER REGISTER 3
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline F11BP3 & F11BP2 & F11BP1 & F11BP0 & F10BP3 & F10BP2 & F10BP1 & F10BP0 \\
    \hline bit 15 & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|l|l|l|l|l|l|l|l|l|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline F9BP3 & F9BP2 & F9BP1 & F9BP0 & F8BP3 & F8BP2 & F8BP1 & F8BP0 \\
    \hline bit 7
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & & \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0\) ' = Bit is cleared \\
    \hline
    \end{tabular}
    bit 15-12 F11BP<3:0>: RX Buffer Mask for Filter 11 bits
    1111 = Filter hits received in RX FIFO buffer
    \(1110=\) Filter hits received in RX Buffer 14
    -
    -
    -
    0001 = Filter hits received in RX Buffer 1
    0000 = Filter hits received in RX Buffer 0
    bit 11-8 \(\quad\) F10BP<3:0>: RX Buffer Mask for Filter 10 bits (same values as bits 15-12)
    bit 7-4 F9BP<3:0>: RX Buffer Mask for Filter 9 bits (same values as bits 15-12)
    bit 3-0 F8BP<3:0>: RX Buffer Mask for Filter 8 bits (same values as bits 15-12)

    REGISTER 22-15: CxBUFPNT4: CANx FILTERS 12-15 BUFFER POINTER REGISTER 4
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline F15BP3 & F15BP2 & F15BP1 & F15BP0 & F14BP3 & F14BP2 & F14BP1 & F14BP0 \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline F13BP3 & F13BP2 & F13BP1 & F13BP0 & F12BP3 & F12BP2 & F12BP1 & F12BP0 \\
    \hline bit 7
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}
    bit 15-12 F15BP<3:0>: RX Buffer Mask for Filter 15 bits
    1111 = Filter hits received in RX FIFO buffer
    \(1110=\) Filter hits received in RX Buffer 14
    -
    -
    -
    0001 = Filter hits received in RX Buffer 1
    \(0000=\) Filter hits received in RX Buffer 0
    bit 11-8 F14BP<3:0>: RX Buffer Mask for Filter 14 bits (same values as bits 15-12)
    bit 7-4 \(\quad\) F13BP<3:0>: RX Buffer Mask for Filter 13 bits (same values as bits 15-12)
    bit 3-0 \(\quad\) F12BP<3:0>: RX Buffer Mask for Filter 12 bits (same values as bits 15-12)

    \section*{REGISTER 22-16: CxRXFnSID: CANx ACCEPTANCE FILTER n STANDARD IDENTIFIER REGISTER ( \(\mathbf{n}=\mathbf{0 - 1 5}\) )}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x \\
    \hline SID10 & SID9 & SID8 & SID7 & SID6 & SID5 & SID4 & SID3 \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-x & R/W-x & R/W-x & U-0 & R/W-x & U-0 & R/W-x & R/W-x \\
    \hline SID2 & SID1 & SID0 & - & EXIDE & - & EID17 & EID16 \\
    \hline \multicolumn{8}{|l|}{bit 7 bit 0} \\
    \hline
    \end{tabular}
    \[
    \begin{array}{|lll}
    \hline \text { Legend: } & & \\
    R=\text { Readable bit } & W=\text { Writable bit } & U=\text { Unimplemented bit, read as ' } 0 \text { ' } \\
    -n=\text { Value at POR } & ' 1 '=\text { Bit is set } & ' 0 '=\text { Bit is cleared }
    \end{array}
    \]
    bit 15-5
    SID<10:0>: Standard Identifier bits
    1 = Message address bit, SIDx, must be ' 1 ' to match filter
    \(0=\) Message address bit, SIDx, must be ' 0 ' to match filter
    bit 4 Unimplemented: Read as ' 0 '
    bit 3 EXIDE: Extended Identifier Enable bit
    If MIDE = 1 :
    1 = Matches only messages with Extended Identifier addresses
    \(0=\) Matches only messages with Standard Identifier addresses
    If MIDE \(=0\) :
    Ignore EXIDE bit.
    bit 2 Unimplemented: Read as ' 0 '
    bit 1-0 EID<17:16>: Extended Identifier bits
    1 = Message address bit, EIDx, must be ' 1 ' to match filter
    \(0=\) Message address bit, EIDx, must be ' 0 ' to match filter

    \section*{REGISTER 22-17: CxRXFnEID: CANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER ( \(\mathrm{n}=0-15\) )}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x \\
    \hline \multicolumn{8}{|c|}{EID<15:8>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x \\
    \hline \multicolumn{8}{|c|}{EID<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(0 '=B i t\) is cleared
    \end{tabular}
    bit 15-0
    EID<15:0>: Extended Identifier bits
    1 = Message address bit, EIDx, must be ' 1 ' to match filter
    \(0=\) Message address bit, EIDx, must be ' 0 ' to match filter

    REGISTER 22-18: CxFMSKSEL1: CANx FILTERS 7-0 MASK SELECTION REGISTER 1
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline F7MSK1 & F7MSK0 & F6MSK1 & F6MSK0 & F5MSK1 & F5MSK0 & F4MSK1 & F4MSK0 \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{1}{|c}{ R/W-0 } & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline F3MSK1 & F3MSK0 & F2MSK1 & F2MSK0 & F1MSK1 & F1MSK0 & FOMSK1 & F0MSK0 \\
    \hline bit 7
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-14 F7MSK<1:0>: Mask Source for Filter 7 bit
    11 = Reserved
    10 = Acceptance Mask 2 registers contain the mask
    01 = Acceptance Mask 1 registers contain the mask
    \(00=\) Acceptance Mask 0 registers contain the mask
    bit 13-12 F6MSK<1:0>: Mask Source for Filter 6 bit (same values as bits 15-14)
    bit 11-10 F5MSK<1:0>: Mask Source for Filter 5 bit (same values as bits 15-14)
    bit 9-8 F4MSK<1:0>: Mask Source for Filter 4 bit (same values as bits 15-14)
    bit 7-6 F3MSK<1:0>: Mask Source for Filter 3 bit (same values as bits 15-14)
    bit 5-4 F2MSK<1:0>: Mask Source for Filter 2 bit (same values as bits 15-14)
    bit 3-2 F1MSK<1:0>: Mask Source for Filter 1 bit (same values as bits 15-14)
    bit 1-0 FOMSK<1:0>: Mask Source for Filter 0 bit (same values as bits 15-14)

    REGISTER 22-19: CxFMSKSEL2: CANx FILTERS 15-8 MASK SELECTION REGISTER 2
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{9}{|c|}{ R/W-0 } & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline F15MSK1 & F15MSK0 & F14MSK1 & F14MSK0 & F13MSK & F13MSK0 & F12MSK1 & F12MSK0 \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline \multicolumn{1}{|c}{ R/W-0 } & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline F11MSK1 & F11MSK0 & F10MSK1 & F10MSK0 & F9MSK1 & F9MSK0 & F8MSK1 & F8MSK0 \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-14 F15MSK<1:0>: Mask Source for Filter 15 bit
    11 = Reserved
    \(10=\) Acceptance Mask 2 registers contain the mask
    01 = Acceptance Mask 1 registers contain the mask
    \(00=\) Acceptance Mask 0 registers contain the mask
    bit 13-12 F14MSK<1:0>: Mask Source for Filter 14 bit (same values as bits 15-14)
    bit 11-10 F13MSK<1:0>: Mask Source for Filter 13 bit (same values as bits 15-14)
    bit 9-8 F12MSK<1:0>: Mask Source for Filter 12 bit (same values as bits 15-14)
    bit 7-6 F11MSK<1:0>: Mask Source for Filter 11 bit (same values as bits 15-14)
    bit 5-4 F10MSK<1:0>: Mask Source for Filter 10 bit (same values as bits 15-14)
    bit 3-2 F9MSK<1:0>: Mask Source for Filter 9 bit (same values as bits 15-14)
    bit 1-0 F8MSK<1:0>: Mask Source for Filter 8 bit (same values as bits 15-14)

    \section*{REGISTER 22-20: CxRXMnSID: CANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER REGISTER ( \(\mathrm{n}=0-2\) )}
    \begin{tabular}{|l|c|c|c|c|c|c|c|c|}
    \hline R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x \\
    \hline SID10 & SID9 & SID8 & SID7 & SID6 & SID5 & SID4 & SID3 \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{9}{|c|}{ R/W-x } \\
    \hline SID2 & R/W-x & R/W-x & U-0 & R/W-x & R/W-x \\
    \hline SID1 & SID0 & - & MIDE & - & EID17 & EID16 \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & & \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared \(\quad x=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-5 SID<10:0>: Standard Identifier bits
    1 = Includes bit, SIDx, in filter comparison
    \(0=\) Bit, SIDx, is a don't care in filter comparison
    bit 4 Unimplemented: Read as ' 0 '
    bit 3 MIDE: Identifier Receive Mode bit
    1 = Matches only message types (standard or extended address) that correspond to the EXIDE bit in the filter
    \(0=\) Matches either standard or extended address message if filters match, i.e., if: (Filter SID) \(=(\) Message SID \()\) or if (Filter SID/EID) \(=(\) Message SID/EID \()\)
    bit 2 Unimplemented: Read as ' 0 '
    bit 1-0 EID<17:16>: Extended Identifier bits
    1 = Includes bit, EIDx, in filter comparison
    \(0=\) Bit, EIDx, is a don't care in filter comparison

    \section*{REGISTER 22-21: CxRXMnEID: CANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER ( \(\mathrm{n}=0-2\) )}
    \begin{tabular}{|llllllll|}
    \hline R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x \\
    \hline & & EID<15:8> & & & \\
    \hline bit 15 & & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lllllll|}
    \hline\(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\)
    \end{tabular}\(\quad\) R/W-x \begin{tabular}{llll|}
    \hline & EID \(<7: 0>\) & & \\
    \hline & & & \\
    \hline bit 7 & & & \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{|c|c|c|c|}
    \hline \(R=\) Readable bit & W = Writable bit & \(\mathrm{U}=\) Unimplemen & as '0' \\
    \hline -n = Value at POR & ' 1 ' = Bit is set & ' 0 ' = Bit is cleared & \(\mathrm{x}=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-0 EID<15:0>: Extended Identifier bits
    1 = Includes bit, EIDx, in filter comparison
    \(0=\) Bit, EIDx, is a don't care in filter comparison

    REGISTER 22-22: CxRXFUL1: CANx RECEIVE BUFFER FULL REGISTER 1
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 \\
    \hline \multicolumn{8}{|c|}{RXFUL<15:8>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 \\
    \hline \multicolumn{8}{|c|}{RXFUL<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & \(C=\) Writable bit, but only ' 0 ' can be written to clear the bit \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' \(=\) Bit is set & ' 0 ' = Bit is cleared \(\quad \mathrm{x}=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-0 RXFUL<15:0>: Receive Buffer \(n\) Full bits
    1 = Buffer is full (set by module)
    \(0=\) Buffer is empty (cleared by user software)

    REGISTER 22-23: CxRXFUL2: CANx RECEIVE BUFFER FULL REGISTER 2
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 \\
    \hline \multicolumn{8}{|c|}{RXFUL<31:24>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 \\
    \hline \multicolumn{8}{|c|}{RXFUL<23:16>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & \(C=\) Writable bit, but only ' 0 ' can be written to clear the bit \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' \(=\) Bit is set & ' 0 ' = Bit is cleared \(\quad \mathrm{x}=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-0 RXFUL<31:16>: Receive Buffer \(n\) Full bits
    1 = Buffer is full (set by module)
    \(0=\) Buffer is empty (cleared by user software)

    \section*{REGISTER 22-24: CxRXOVF1: CANx RECEIVE BUFFER OVERFLOW REGISTER 1}
    \begin{tabular}{|llllllll|}
    \hline R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 \\
    \hline & & \(R X O V F<15: 8>\) & & & \\
    \hline bit 15 & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|llllllll|}
    \hline\(R / C-0\) & \(R / C-0\) & \(R / C-0\) & \(R / C-0\) & \(R / C-0\) & \(R / C-0\) & \(R / C-0\) & \(R / C-0\) \\
    \hline & & \(R X O V F<7: 0>\) & & & \\
    \hline bit 7 & & & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & \(\mathrm{C}=\) Writable bit, but only ' 0 ' can be written to clear the bit \\
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & ' 0 ' = Bit is cleared \(\quad \mathrm{x}=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-0 RXOVF<15:0>: Receive Buffer \(n\) Overflow bits
    1 = Module attempted to write to a full buffer (set by module)
    \(0=\) No overflow condition (cleared by user software)

    REGISTER 22-25: CxRXOVF2: CANx RECEIVE BUFFER OVERFLOW REGISTER 2
    \begin{tabular}{|llllllll|}
    \hline R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 \\
    \hline & & \(R X O V F<31: 24>\) & & & \\
    \hline bit 15 & & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|llllllll|}
    \hline R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 & R/C-0 \\
    \hline & & \(R X O V F<23: 16>\) & & & \\
    \hline bit 7 & & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & \(C=\) Writable bit, but only ' 0 ' can be written to clear the bit \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' \(=\) Bit is set & ' 0 ' = Bit is cleared \(\quad \mathrm{x}=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-0 RXOVF<31:16>: Receive Buffer \(n\) Overflow bits
    1 = Module attempted to write to a full buffer (set by module)
    \(0=\) No overflow condition (cleared by user software)

    REGISTER 22-26: CxTRmnCON: CANx TX/RX BUFFER mn CONTROL REGISTER ( \(m=0,2,4,6 ; n=1,3,5,7\) )
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R-0 & R-0 & R-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline TXENn & TXABTn & TXLARBn & TXERRn & TXREQn & RTRENn & TXnPRI1 & TXnPRI0 \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline R/W-0 & R-0 & R-0 & R-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline TXENm & TXABTm \({ }^{(1)}\) & TXLARBm \({ }^{(1)}\) & TXERRm \({ }^{(1)}\) & TXREQm & RTRENm & TXmPRI1 & TXmPRI0 \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & & \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared \(\quad x=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-8 See Definition for bits 7-0, controls Buffer \(n\)
    bit 7 TXENm: TX/RX Buffer Selection bit
    1 = Buffer, TRBn, is a transmit buffer
    \(0=\) Buffer, TRBn, is a receive buffer
    bit \(6 \quad\) TXABTm: Message Aborted bit \({ }^{(1)}\)
    1 = Message was aborted
    \(0=\) Message completed transmission successfully
    bit 5 TXLARBm: Message Lost Arbitration bit \({ }^{(1)}\)
    1 = Message lost arbitration while being sent
    \(0=\) Message did not lose arbitration while being sent
    bit 4 TXERRm: Error Detected During Transmission bit \({ }^{(1)}\)
    1 = A bus error occurred while the message was being sent
    \(0=A\) bus error did not occur while the message was being sent
    bit 3 TXREQm: Message Send Request bit
    \(1=\) Requests that a message be sent; the bit automatically clears when the message is successfully sent
    \(0=\) Clearing the bit to ' 0 ' while set requests a message abort
    bit 2 RTRENm: Auto-Remote Transmit Enable bit
    \(1=\) When a remote transmit is received, TXREQ will be set
    \(0=\) When a remote transmit is received, TXREQ will be unaffected
    bit 1-0 TXmPRI<1:0>: Message Transmission Priority bits
    11 = Highest message priority
    \(10=\) High intermediate message priority
    01 = Low intermediate message priority
    \(00=\) Lowest message priority
    Note 1: This bit is cleared when TXREQm is set.

    Note: \(\quad\) The buffers, SID, EID, DLC, Data Field and Receive Status registers, are located in DMA RAM.

    \subsection*{22.4 CAN Message Buffers}

    CAN Message Buffers are part of RAM memory. They are not CAN Special Function Registers. The user application must directly write into the RAM area that is configured for CAN Message Buffers. The location and size of the buffer area is defined by the user application.

    \section*{BUFFER 21-1: CANx MESSAGE BUFFER WORD 0}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x \\
    \hline- & - & - & SID10 & SID9 & SID8 & SID7 & SID6 \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|c|}
    \hline R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x \\
    \hline SID5 & SID4 & SID3 & SID2 & SID1 & SID0 & SRR & IDE \\
    \hline bit 7
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-13 Unimplemented: Read as ' 0 '
    bit 12-2 SID<10:0>: Standard Identifier bits
    bit 1 SRR: Substitute Remote Request bit
    When IDE = 0:
    1 = Message will request remote transmission
    \(0=\) Normal message
    When IDE = 1:
    The SRR bit must be set to ' 1 '.
    bit 0
    IDE: Extended Identifier bit
    1 = Message will transmit an Extended Identifier
    \(0=\) Message will transmit a Standard Identifier

    \section*{BUFFER 21-2: CANx MESSAGE BUFFER WORD 1}
    \begin{tabular}{|c|c|c|c|cccc|}
    \hline U-0 & \(\mathrm{U}-0\) & \(\mathrm{U}-0\) & \(\mathrm{U}-0\) & \(\mathrm{R} / \mathrm{W}-\mathrm{x}\) & \(\mathrm{R} / \mathrm{W}-\mathrm{x}\) & \(\mathrm{R} / \mathrm{W}-\mathrm{x}\) & \(\mathrm{R} / \mathrm{W}-\mathrm{x}\) \\
    \hline- & - & - & - & & EID<17:14> & \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|llllllll|}
    \hline\(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) \\
    \hline & & EID<13:6> & & & & \\
    \hline bit 7 & & & & & & \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' \(=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-12 Unimplemented: Read as ' 0 '
    bit 11-0 EID<17:6>: Extended Identifier bits

    \section*{BUFFER 21-3: CANx MESSAGE BUFFER WORD 2}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x \\
    \hline EID5 & EID4 & EID3 & EID2 & EID1 & EIDO & RTR & RB1 \\
    \hline \multicolumn{8}{|l|}{bit 15 bit 8} \\
    \hline
    \end{tabular}
    \begin{tabular}{|l|l|l|l|l|l|l|l|l|}
    \hline \multicolumn{8}{|c|}{ U-x } & U-x \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}
    bit 15-10 EID<5:0>: Extended Identifier bits
    bit \(9 \quad\) RTR: Remote Transmission Request bit
    When IDE = 1:
    1 = Message will request remote transmission
    0 = Normal message
    When IDE = 0:
    The RTR bit is ignored.
    bit 8 RB1: Reserved Bit 1
    User must set this bit to ' 0 ' per CAN protocol.
    bit 7-5 Unimplemented: Read as ' 0 '
    bit \(4 \quad\) RB0: Reserved Bit 0
    User must set this bit to '0' per CAN protocol.
    bit 3-0 \(\quad\) DLC<3:0>: Data Length Code bits

    BUFFER 21-4: CANx MESSAGE BUFFER WORD 3
    
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x \\
    \hline \multicolumn{8}{|c|}{Byte 0<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' \(=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-8 Byte \(1<15: 8>\) : CANx Message Byte 1 bits
    bit 7-0 Byte 0<7:0>: CANx Message Byte 0 bits

    \section*{BUFFER 21-5: CANx MESSAGE BUFFER WORD 4}
    \begin{tabular}{|llllllll|}
    \hline \multicolumn{1}{|c|}{\(R / W-x\)} & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) \\
    \hline & & Byte \(3<15: 8>\) & & & \\
    \hline bit 15 & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|llllllll|}
    \hline\(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) & \(R / W-x\) \\
    \hline & & Byte \(2<7: 0>\) & & & \\
    \hline bit 7 & & & & & & & \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-8 Byte \(3<15: 8>\) : CANx Message Byte 3 bits
    bit 7-0 Byte 2<7:0>: CANx Message Byte 2 bits

    BUFFER 21-6: CANx MESSAGE BUFFER WORD 5
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x \\
    \hline \multicolumn{8}{|c|}{Byte 5<15:8>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x \\
    \hline \multicolumn{8}{|c|}{Byte 4<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}
    bit 15-8 Byte 5<15:8>: CANx Message Byte 5 bits
    bit 7-0 Byte 4<7:0>: CANx Message Byte 4 bits

    \section*{BUFFER 21-7: CANx MESSAGE BUFFER WORD 6}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x \\
    \hline \multicolumn{8}{|c|}{Byte 7<15:8>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x & R/W-x \\
    \hline \multicolumn{8}{|c|}{Byte 6<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \(R=\) Readable bit
    W = Writable bit
    \(\mathrm{U}=\) Unimplemented bit, read as ' 0 '
    \(-n=\) Value at POR
    ' 1 ' = Bit is set
    ' 0 ' = Bit is cleared
    \(x=\) Bit is unknown
    bit 15-8 Byte \(\mathbf{7 < 1 5 : 8}\) : CANx Message Byte 7 bits
    bit 7-0 Byte 6<7:0>: CANx Message Byte 6 bits

    BUFFER 21-8: CANx MESSAGE BUFFER WORD 7
    \begin{tabular}{|c|c|c|ccccc|}
    \hline U-0 & U-0 & U-0 & R/W-x & R/W-x & R/W-x & \(R / W-x\) & R/W-x \\
    \hline- & - & - & & & FILHIT<4:0>(1) & & \\
    \hline bit 15 & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline - & - & - & - & - & - & - & - \\
    \hline \multicolumn{8}{|l|}{bit \(7 \times 1\)} \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown \begin{tabular}{l} 
    \\
    \hline
    \end{tabular}
    \begin{tabular}{ll} 
    bit 15-13 & Unimplemented: Read as ' 0 ' \\
    bit 12-8 & FILHIT<4:0>: Filter Hit Code bits \({ }^{(1)}\) \\
    & Encodes number of filter that resulted in writing this buffer. \\
    bit 7-0 & Unimplemented: Read as ' 0 '
    \end{tabular}

    Note 1: Only written by module for receive buffers, unused for transmit buffers.

    \subsection*{23.0 CHARGE TIME MEASUREMENT UNIT (CTMU)}

    Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Charge Time Measurement Unit (CTMU)" (DS70661) in the "dsPIC33/PIC24 Family Reference Manual", which is available on the Microchip web site (www.microchip.com).

    2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

    The Charge Time Measurement Unit (CTMU) is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. Its key features include:
    - Nine Edge Input Trigger Sources
    - Polarity Control for Each Edge Source
    - Control of Edge Sequence
    - Control of Response to Edges
    - Time Measurement Resolution Down to 200 ps
    - Accurate Current Source Suitable for Capacitive Measurement
    - On-Chip Temperature Measurement using a Built-in Diode
    - Pulse Generation Generates a Pulse using the C1INB Comparator Input and Outputs the Pulse onto the CTPLS Remappable Output

    Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock.
    The CTMU module is ideal for interfacing with capacitive-based sensors. The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 and CTMUCON2 enable the module and control edge source selection, edge source polarity selection and edge sequencing. The CTMUICON register controls the selection and trim of the current source.

    FIGURE 23-1: CTMU BLOCK DIAGRAM
    

    Note 1: Current source to particular ANx pins is provided only when 10-Bit ADC mode is chosen.

    \subsection*{23.1 CTMU Control Registers}

    \section*{REGISTER 23-1: CTMUCON1: CTMU CONTROL REGISTER 1}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline CTMUEN & - & CTMUSIDL & TGEN \(^{(2)}\) & EDGEN & EDGSEQEN & IDISSEN \({ }^{(1)}\) & CTTRIG \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|l|l|l|l|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline- & - & - & - & - & - & - & - \\
    \hline bit 7
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & ' 0 ' = Bit is cleared
    \end{tabular}
    \(\left.\begin{array}{ll}\text { bit } 15 & \text { CTMUEN: CTMU Enable bit } \\
    & 1=\text { Module is enabled } \\
    0=\text { Module is disabled }\end{array}\right]\)\begin{tabular}{l} 
    Unit 14 \\
    bit 13
    \end{tabular}\(\quad\)\begin{tabular}{l} 
    CTMUSIemented: Read as ' 0 ' \\
    1
    \end{tabular}
    bit 12 TGEN: Time Generation Enable bit \({ }^{(2)}\)
    1 = Edge delay generation is enabled
    \(0=\) Edge delay generation is disabled
    bit 11 EDGEN: Edge Enable bit
    1 = Hardware modules are used to trigger edges (TMRx, CTEDx, etc.)
    \(0=\) Software is used to trigger edges (manual set of EDGxSTAT)
    bit 10 EDGSEQEN: Edge Sequence Enable bit
    1 = Edge 1 event must occur before Edge 2 event can occur
    \(0=\) No edge sequence is needed
    bit 9 IDISSEN: Analog Current Source Control bit \({ }^{(1)}\)
    1 = Analog current source output is grounded
    \(0=\) Analog current source output is not grounded
    bit 8 CTTRIG: ADC Trigger Control bit
    1 = CTMU triggers the ADC start of conversion
    \(0=\) CTMU does not trigger the ADC start of conversion
    bit 7-0 Unimplemented: Read as ' 0 '
    Note 1: The ADC module Sample-and-Hold (S\&H) capacitor is not automatically discharged between sample/ conversion cycles. Any software using the ADC as part of a capacitance measurement must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to ' 1 ', performs this function. The ADC must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.
    2: If the TGEN bit is set to ' 1 ', then the CMP1 module should be selected as the Edge 2 source in the EDG2SELx bits field; otherwise, the module will not function.

    REGISTER 23-2: CTMUCON2: CTMU CONTROL REGISTER 2
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline EDG1MOD & EDG1POL & EDG1SEL3 & EDG1SEL2 & EDG1SEL1 & EDG1SEL0 & EDG2STAT & EDG1STAT \\
    \hline bit 15 \\
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & U-0 & U-0 \\
    \hline EDG2MOD & EDG2POL & EDG2SEL3 & EDG2SEL2 & EDG2SEL1 & EDG2SEL0 & - & - \\
    \hline bit 7 &
    \end{tabular}
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}
    bit 15 EDG1MOD: Edge 1 Edge Sampling Mode Selection bit
    1 = Edge 1 is edge-sensitive
    0 = Edge 1 is level-sensitive
    bit 14 EDG1POL: Edge 1 Polarity Select bit
    1 = Edge 1 is programmed for a positive edge response
    \(0=\) Edge 1 is programmed for a negative edge response
    bit 13-10 EDG1SEL<3:0>: Edge 1 Source Select bits
    1111 = Fosc
    \(1110=\) OSCI pin
    1101 = FRC Oscillator
    \(1100=\) BFRC Oscillator
    1011 = Internal LPRC Oscillator
    1010 = Reserved
    1001 = Reserved
    \(1000=\) Reserved
    0111 = Reserved
    0110 = Reserved
    0101 = Reserved
    0100 = Reserved
    0011 = CTED1 pin
    \(0010=\) CTED2 pin
    \(0001=\) OC1 module
    0000 = TMR1 module
    bit 9 EDG2STAT: Edge 2 Status bit
    Indicates the status of Edge 2 and can be written to control the edge source.
    1 = Edge 2 has occurred
    \(0=\) Edge 2 has not occurred
    bit 8 EDG1STAT: Edge 1 Status bit
    Indicates the status of Edge 1 and can be written to control the edge source.
    1 = Edge 1 has occurred
    \(0=\) Edge 1 has not occurred
    bit 7 EDG2MOD: Edge 2 Edge Sampling Mode Selection bit
    \(1=\) Edge 2 is edge-sensitive
    \(0=\) Edge 2 is level-sensitive
    bit 6 EDG2POL: Edge 2 Polarity Select bit
    \(1=\) Edge 2 is programmed for a positive edge response
    \(0=\) Edge 2 is programmed for a negative edge response

    \section*{REGISTER 23-2: CTMUCON2: CTMU CONTROL REGISTER 2 (CONTINUED)}
    bit 5-2 EDG2SEL<3:0>: Edge 2 Source Select bits
    1111 = Fosc
    \(1110=\) OSCI pin
    1101 = FRC Oscillator
    1100 = BFRC Oscillator
    1011 = Internal LPRC Oscillator
    1010 = Reserved
    1001 = Reserved
    \(1000=\) Reserved
    0111 = Reserved
    0110 = Reserved
    0101 = Reserved
    0100 = CMP1 module
    0011 = CTED2 pin
    \(0010=\) CTED1 pin
    0001 = OCMP1 module
    0000 = IC1 module
    bit 1-0 Unimplemented: Read as ' 0 '

    \section*{REGISTER 23-3: CTMUICON: CTMU CURRENT CONTROL REGISTER \({ }^{(3)}\)}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline ITRIM5 & ITRIM4 & ITRIM3 & ITRIM2 & ITRIM1 & ITRIM0 & IRNG1 \({ }^{(2)}\) & IRNG0 \({ }^{(2)}\) \\
    \hline \multicolumn{7}{|l|}{bit 15} & bit 8 \\
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline - & - & - & - & - & - & - & - \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared \(\quad x=\) Bit is unknown
    \end{tabular}
    bit 15-10 ITRIM<5:0>: Current Source Trim bits
    011111 = Maximum positive change from nominal current \(+62 \%\)
    \(011110=\) Maximum positive change from nominal current \(+60 \%\)
    -
    -
    \(000010=\) Minimum positive change from nominal current \(+4 \%\)
    \(000001=\) Minimum positive change from nominal current \(+2 \%\)
    \(000000=\) Nominal current output specified by IRNG<1:0>
    111111 = Minimum negative change from nominal current \(-2 \%\)
    \(111110=\) Minimum negative change from nominal current \(-4 \%\)
    -
    -
    \(100010=\) Maximum negative change from nominal current \(-60 \%\)
    100001 = Maximum negative change from nominal current - \(62 \%\)
    bit 9-8 IRNG<1:0>: Current Source Range Select bits \({ }^{(2)}\)
    \(11=100 \times\) Base Current
    \(10=10 \times\) Base Current
    01 = Base Current Level
    \(00=1000 \times\) Base Current \({ }^{(1)}\)
    bit 7-0 Unimplemented: Read as ' 0 '
    Note 1: This current range is not available for use with the internal temperature measurement diode.
    2: Refer to the CTMU Current Source Specifications (Table 30-52) in Section 30.0 "Electrical Characteristics" for the current range selection values.
    3: Current sources are not generated when 12-Bit ADC mode is chosen. Current sources are active only when 10-Bit ADC mode is chosen.

    \subsection*{24.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)}

    Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Analog-to-Digital Converter (ADC)" (DS70621) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
    2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

    The Analog-to-Digital (ADC) module in the dsPIC33EVXXXGM00X/10X family devices supports up to 36 analog input channels.
    The ADC module can be configured by the user as either a 10-bit, 4 Sample-and-Hold (S\&H) ADC (default configuration) or a 12-bit, 1 S\&H ADC.
    Note: The ADC module needs to be disabled before modifying the AD12B bit.

    \subsection*{24.1 Key Features}

    \subsection*{24.1.1 10-BIT ADC CONFIGURATION}

    The 10-bit ADC configuration has the following key features:
    - Successive Approximation (SAR) Conversion
    - Conversion Speeds of up to 1.1 Msps
    - Up to 36 Analog Input Pins
    - Connections to Four Internal Op Amps
    - Connections to the Charge Time Measurement Unit (CTMU) and Temperature Measurement Diode
    - Simultaneous Sampling of:
    - Up to four analog input pins
    - Four op amp outputs
    - Combinations of Analog Inputs and Op Amp Outputs
    - Automatic Channel Scan mode
    - Selectable Conversion Trigger Source
    - Selectable Buffer Fill modes
    - Four Result Alignment Options (signed/unsigned, fractional/integer)
    - Operation during CPU Sleep and Idle Modes

    \subsection*{24.1.2 12-BIT ADC CONFIGURATION}

    The 12-bit ADC configuration supports all the features listed previously, with the exception of the following:
    - In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
    - There is only one S\&H amplifier in the 12-bit configuration. Therefore, simultaneous sampling of multiple channels is not supported.

    The ADC has up to 36 analog inputs. The analog inputs, AN32 through AN63, are multiplexed, thus providing flexibility in using any of these analog inputs in addition to the analog inputs, ANO through AN31. Since AN32 through AN63 are multiplexed, do not use two channels simultaneously, since it may result in erroneous output from the module. These analog inputs are shared with op amp inputs and outputs, comparator inputs and external voltage references. When op amp/comparator functionality is enabled, the analog input that shares that pin is no longer available. The actual number of analog input pins and op amps depends on the specific device.
    A block diagram of the ADC module with connection options is shown in Figure 24-1. Figure 24-2 shows a block diagram of the ADC conversion clock period.
    FIGURE 24-1:
    

    FIGURE 24-2: ADCx CONVERSION CLOCK PERIOD BLOCK DIAGRAM
    

    Note 1: \(T P=1 / \mathrm{FP}\).
    2: Refer to the ADC electrical specifications in Section 30.0 "Electrical Characteristics" for the exact RC clock value.

    \subsection*{24.2 ADC Helpful Tips}
    1. The SMPIx control bits in the ADxCON2 registers:
    a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
    b) When the CSCNA bit in the ADxCON2 register is set to ' 1 ', this determines when the ADC analog scan channel list, defined in the ADxCSSL/ADxCSSH registers, starts over from the beginning.
    c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
    d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using the DMA peripheral.
    2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMPIx bits and the condition described in 1.c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
    3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer (i.e., ADCxBUFO) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA Controller, before the next ADC conversion is complete to avoid overwriting the previous value.
    4. The DONE bit (ADxCON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (ADxCON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.
    5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for ANO, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUX A selections use AN0-AN2. Carefully study the ADC block diagram to determine the configuration that will best suit your application. For configuration examples, refer to "Analog-to-Digital Converter (ADC)" (DS70621) in the "dsPIC33/PIC24 Family Reference Manual".

    \subsection*{24.3 ADC Control Registers}

    \section*{REGISTER 24-1: ADxCON1: ADCx CONTROL REGISTER 1}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline R/W-0 & U-0 & R/W-0 & R/W-0 & U-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline ADON & - & ADSIDL & ADDMABM & - & AD12B & FORM1 & FORM0 \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & \multicolumn{2}{c|}{ R/W-0, HC, HS R/C-0, HC, HS } \\
    \hline SSRC2 & SSRC1 & SSRC0 & SSRCG & SIMSAM & ASAM & SAMP & DONE \(^{(1)}\) \\
    \hline bit 7
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & \(C=\) Clearable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(H S=\) Hardware Settable bit \(\quad H C=\) Hardware Clearable bit \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|}
    \hline \multirow[t]{3}{*}{bit 15} & ADON: ADCx Operating Mode bit \\
    \hline & 1 = ADCx module is operating \\
    \hline & \(0=\) ADCx is off \\
    \hline bit 14 & Unimplemented: Read as ' 0 ' \\
    \hline bit 13 & ADSIDL: ADCx Stop in Idle Mode bit \\
    \hline & \begin{tabular}{l}
    1 = Discontinues module operation when the device enters Idle mode \\
    \(0=\) Continues module operation in Idle mode
    \end{tabular} \\
    \hline
    \end{tabular}
    bit 12 ADDMABM: ADCx DMA Buffer Build Mode bit
    \(1=\) DMA buffers are written in the order of conversion; the module provides an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer
    \(0=\) DMA buffers are written in Scatter/Gather mode; the module provides a Scatter/Gather mode address to the DMA channel based on the index of the analog input and the size of the DMA buffer
    bit 11 Unimplemented: Read as ' 0 '
    bit 10 AD12B: ADCx 10-Bit or 12-Bit Operation Mode bit
    1 = 12-bit, 1-channel ADC operation
    \(0=10\)-bit, 4-channel ADC operation
    bit 9-8 FORM<1:0>: Data Output Format bits
    For 10-Bit Operation:
    11 = Signed fractional (Dout \(=\) sddd dddd dd00 0000, where \(s=. N O T . d<9>\) )
    \(10=\) Fractional (Dout = dddd dddd dd00 0000)
    01 = Signed integer (Dout = ssss sssd dddd dddd, where s=.NOT.d<9>)
    \(00=\) Integer (Dout \(=0000\) 00dd dddd dddd)
    For 12-Bit Operation:
    \(11=\) Signed fractional (Dout \(=\) sddd dddd dddd 0000 , where \(s=. N O T . d<11>\) )
    \(10=\) Fractional (Dout = dddd dddd dddd 0000)
    \(01=\) Signed integer (Dout = ssss sddd dddd dddd, where s=.NOT.d<11>)
    \(00=\) Integer \((\) Dout \(=0000\) dddd dddd dddd)
    Note 1: Do not clear the DONE bit in software if auto-sample is enabled (ASAM = 1).

    \section*{REGISTER 24-1: ADxCON1: ADCx CONTROL REGISTER 1 (CONTINUED)}
    ```

    bit 7-5 SSRC<2:0>: Sample Clock Source Select bits
    If SSRCG = 1:
    111 = Reserved
    110 = Reserved
    1 0 1 ~ = ~ R e s e r v e d ~
    100 = Reserved
    011 = Reserved
    010 = PWM Generator 3 primary trigger compare ends sampling and starts conversion
    001 = PWM Generator 2 primary trigger compare ends sampling and starts conversion
    000 = PWM Generator 1 primary trigger compare ends sampling and starts conversion
    If SSRCG = 0:
    111 = Internal counter ends sampling and starts conversion (auto-convert)
    110 = CTMU ends sampling and starts conversion
    101 = Reserved
    100 = Timer5 compare ends sampling and starts conversion
    011 = PWM primary Special Event Trigger ends sampling and starts conversion
    010 = Timer3 compare ends sampling and starts conversion
    001 = Active transition on the INT0 pin ends sampling and starts conversion
    000 = Clearing the Sample bit (SAMP) ends sampling and starts conversion (Manual mode)
    bit 4 SSRCG: Sample Trigger Source Group bit
    See SSRC<2:0> for details.
    bit 3 SIMSAM: Simultaneous Sample Select bit (only applicable when CHPS<1:0> = 01 or 1x)
    In 12-Bit Mode (AD12B = 1), SIMSAM is Unimplemented and is Read as ' 0':
    1 = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS<1:0> = 1x}\mathrm{ ) or samples CH0 and CH1
    simultaneously (when CHPS<1:0> = 01)
    0 = Samples multiple channels individually in sequence
    bit 2 ASAM: ADCx Sample Auto-Start bit
    1 = Sampling begins immediately after last conversion; SAMP bit is auto-set
    0 = Sampling begins when SAMP bit is set
    bit 1 SAMP: ADCx Sample Enable bit
    1 = ADCx Sample-and-Hold amplifiers are sampling
    0 = ADCx Sample-and-Hold amplifiers are holding
    If ASAM = 0, software can write ' }1\mathrm{ ' to begin sampling. Automatically set by hardware if ASAM = 1. If
    SSRC<2:0> = 000, software can write ' 0' to end sampling and start conversion. If SSRC<2:0> \not=000,
    automatically cleared by hardware to end sampling and start conversion.
    bit 0 DONE: ADCx Conversion Status bit }\mp@subsup{}{}{(1)
    1 = ADCx conversion cycle is completed.
    0 = ADCx conversion has not started or is in progress

    ```
    Automatically set by hardware when conversion is complete. Software can write ' 0 ' to clear DONE bit
    status (software not allowed to write ' 1 '). Clearing this bit does NOT affect any operation in progress.
    Automatically cleared by hardware at the start of a new conversion.

    Note 1: Do not clear the DONE bit in software if auto-sample is enabled (ASAM = 1).

    \section*{REGISTER 24-2: ADxCON2: ADCx CONTROL REGISTER 2}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline VCFG2 \({ }^{(1)}\) & VCFG1 \({ }^{(1)}\) & VCFG0 \({ }^{(1)}\) & - & - & CSCNA & CHPS1 & CHPS0 \\
    \hline \multicolumn{8}{|l|}{bit 15 bit 8} \\
    \hline
    \end{tabular}
    \begin{tabular}{|l|l|l|l|l|l|l|l|}
    \hline \multicolumn{1}{|c}{ R-0 } & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline BUFS & SMPI4 & SMPI3 & SMPI2 & SMPI1 & SMPI0 & BUFM & ALTS \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared \(\quad x=\) Bit is unknown \\
    \hline
    \end{tabular}
    bit 15-13 VCFG<2:0>: Converter Voltage Reference Configuration bits \({ }^{(1)}\)
    \begin{tabular}{|c|c|c|}
    \hline Value & Vrefh & Vrefl \\
    \hline \hline\(x x x\) & AVDD & AVsS \\
    \hline
    \end{tabular}
    bit 12-11 Unimplemented: Read as '0'
    bit 10
    CSCNA: Input Scan Select bit
    1 = Scans inputs for \(\mathrm{CH} 0+\) during Sample MUX A
    \(0=\) Does not scan inputs
    bit 9-8
    CHPS<1:0>: Channel Select bits
    In 12-Bit Mode (AD21B = 1), CHPS<1:0> bits are Unimplemented and are Read as ' 0 ':
    \(1 \mathrm{x}=\) Converts \(\mathrm{CH} 0, \mathrm{CH} 1, \mathrm{CH} 2\) and CH 3
    \(01=\) Converts CH 0 and CH 1
    00 = Converts CH0
    bit 7 BUFS: Buffer Fill Status bit (only valid when BUFM = 1)
    \(1=\) ADCx is currently filling the second half of the buffer; the user application should access data in the first half of the buffer
    \(0=A D C x\) is currently filling the first half of the buffer; the user application should access data in the second half of the buffer
    bit 6-2 SMPI<4:0>: Increment Rate bits
    When ADDMAEN = 0:
    x1111 = Generates interrupt after completion of every 16th sample/conversion operation
    x1110 \(=\) Generates interrupt after completion of every 15 th sample/conversion operation
    -
    -
    -
    x0001 \(=\) Generates interrupt after completion of every 2nd sample/conversion operation \(\times 0000=\) Generates interrupt after completion of every sample/conversion operation When ADDMAEN = 1:
    11111 = Increments the DMA address after completion of every 32nd sample/conversion operation \(11110=\) Increments the DMA address after completion of every 31st sample/conversion operation -
    -
    -
    00001 = Increments the DMA address after completion of every 2nd sample/conversion operation \(00000=\) Increments the DMA address after completion of every sample/conversion operation

    Note 1: The ADCx Vreft is connected to AVDD and the Vrefl input is connected to AVss.

    \section*{REGISTER 24-2: ADxCON2: ADCx CONTROL REGISTER 2 (CONTINUED)}
    bit \(1 \quad\) BUFM: Buffer Fill Mode Select bit
    \(1=\) Starts buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on the next interrupt
    \(0=\) Always starts filling the buffer from the Start address
    bit \(0 \quad\) ALTS: Alternate Input Sample Mode Select bit
    1 = Uses channel input selects for Sample MUX A on the first sample and Sample MUX B on the next sample 0 = Always uses channel input selects for Sample MUX A

    Note 1: The ADCx VREFH is connected to AVDD and the Vrefl input is connected to AVss.

    \section*{REGISTER 24-3: ADxCON3: ADCx CONTROL REGISTER 3}
    \begin{tabular}{|l|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & U-0 & U-0 & R/W-0 & R/W & R/W-0 & R/W-0 & R/W-0 \\
    \hline ADRC & - & - & SAMC4 \(^{(1)}\) & SAMC3 \(^{(1)}\) & SAMC2 \(^{(1)}\) & SAMC1 \(^{(1)}\) & SAMC0 \(^{(1)}\) \\
    \hline bit 15 & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline ADCS7 \({ }^{(2)}\) & ADCS6 \({ }^{(2)}\) & ADCS5 \({ }^{(2)}\) & ADCS4 \({ }^{(2)}\) & ADCS3 \({ }^{(2)}\) & ADCS2 \({ }^{(2)}\) & ADCS1 \({ }^{(2)}\) & ADCS0 \({ }^{(2)}\) \\
    \hline \multicolumn{8}{|l|}{bit \(7 \times\) bit} \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}
    bit 15 ADRC: ADCx Conversion Clock Source bit
    1 = ADCx internal RC clock
    \(0=\) Clock derived from system clock
    bit 14-13 Unimplemented: Read as ' 0 '
    bit 12-8 SAMC<4:0>: Auto-Sample Time bits \({ }^{(1)}\)
    11111 = 31 TAD
    -
    -
    \(00001=1\) TAD
    \(00000=0\) TAD
    bit 7-0 ADCS<7:0>: ADCx Conversion Clock Select bits \({ }^{(2)}\)
    \(11111111=\operatorname{TP} \cdot(A D C S<7: 0>+1)=T P \cdot 256=T A D\)
    -
    -
    \(00000010=\) TP \(\cdot(A D C S<7: 0>+1)=T P \cdot 3=\) TAD
    \(00000001=\mathrm{TP} \cdot(\operatorname{ADCS}<7: 0>+1)=T P \cdot 2=\) TAD
    \(00000000=\mathrm{TP} \cdot(\operatorname{ADCS}<7: 0>+1)=\) TP \(\cdot 1=\) TAD
    Note 1: These bits are only used if SSRC<2:0> (ADxCON1<7:5>) = 111 and SSRCG (ADxCON1<4>) \(=0\).
    2: These bits are not used if ADRC (ADxCON3<15>) \(=1\).

    \section*{REGISTER 24-4: ADxCON4: ADCx CONTROL REGISTER 4}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-O & U-0 & U-0 & R/W-0 \\
    \hline- & - & - & - & - & - & - & ADDMAEN \\
    \hline bit 15 &
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline \multicolumn{9}{|c|}{\(\mathrm{U}-0\)} & \(\mathrm{U}-0\) & \(\mathrm{U}-0\) & \(\mathrm{U}-0\) & \(\mathrm{U}-0\) & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & - & - & - & DMABL2 & DMABL1 & DMABL0 \\
    \hline bit 7 & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' \(=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15-9
    Unimplemented: Read as ' 0 '
    bit 8
    ADDMAEN: ADCx DMA Enable bit
    1 = Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA
    \(0=\) Conversion results are stored in the ADC1BUF0 through ADC1BUFF registers; DMA will not be used
    bit 7-3
    Unimplemented: Read as '0'
    bit 2-0 DMABL<2:0>: Selects Number of DMA Buffer Locations per Analog Input bits
    111 = Allocates 128 words of buffer to each analog input
    \(110=\) Allocates 64 words of buffer to each analog input
    101 = Allocates 32 words of buffer to each analog input
    \(100=\) Allocates 16 words of buffer to each analog input
    011 = Allocates 8 words of buffer to each analog input
    \(010=\) Allocates 4 words of buffer to each analog input
    \(001=\) Allocates 2 words of buffer to each analog input
    \(000=\) Allocates 1 word of buffer to each analog input

    \section*{REGISTER 24-5: ADxCHS123: ADCx INPUT CHANNELS 1, 2, 3 SELECT REGISTER}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & - & CH123SB2 & CH123SB1 & CH123NB1 & CH123NB0 & CH123SB0 \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & - & - & CH123SA2 & CH123SA1 & CH123NA1 & CH123NA0 & CH123SA0 \\
    \hline bit 7 & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-13 Unimplemented: Read as ' 0 '
    bit 12-11 CH123SB<2:1>: Channels 1, 2, 3 Positive Input Select for Sample B bits
    \(1 \mathrm{xx}=\mathrm{CH} 1\) positive input is AN0 (Op Amp 2), CH 2 positive input is AN25 (Op Amp 5), CH3 positive input is AN6 (Op Amp 3)
    \(011=\mathrm{CH} 1\) positive input is AN3 (Op Amp 1), CH 2 positive input is ANO ( Op Amp 2 ), CH 3 positive input is AN25 (Op Amp 5)
    \(010=\mathrm{CH} 1\) positive input is \(\mathrm{AN} 3(\mathrm{Op} \mathrm{Amp} 1), \mathrm{CH} 2\) positive input is ANO (Op Amp 2), CH 3 positive input is AN6 (Op Amp 3)
    \(001=\mathrm{CH} 1\) positive input is \(\mathrm{AN} 3, \mathrm{CH} 2\) positive input is \(\mathrm{AN} 4, \mathrm{CH} 3\) positive input is AN5
    \(000=\mathrm{CH} 1\) positive input is \(\mathrm{AN} 0, \mathrm{CH} 2\) positive input is \(\mathrm{AN} 1, \mathrm{CH} 3\) positive input is AN2
    bit 10-9
    bit 8 CH123SB0: Channels 1, 2, 3 Positive Input Select for Sample B bit See bits<12:11> for bit selections.
    bit 7-5 Unimplemented: Read as ' 0 '
    bit 4-3 CH123SA<2:1>: Channels 1, 2, 3 Positive Input Select for Sample A bits
    \(1 \mathrm{xx}=\mathrm{CH} 1\) positive input is AN0 (Op Amp 2), CH 2 positive input is AN25 (Op Amp 5), CH3 positive input is AN6 (Op Amp 3)
    011 = CH 1 positive input is AN 3 (Op Amp 1), CH 2 positive input is AN0 (Op Amp 2), CH 3 positive input is AN25 (Op Amp 5)
    \(010=\mathrm{CH} 1\) positive input is \(\mathrm{AN} 3(\mathrm{Op} \mathrm{Amp} 1), \mathrm{CH} 2\) positive input is AN 0 (Op Amp 2), CH 3 positive input is AN6 (Op Amp 3)
    \(001=\mathrm{CH} 1\) positive input is \(\mathrm{AN} 3, \mathrm{CH} 2\) positive input is \(\mathrm{AN} 4, \mathrm{CH} 3\) positive input is AN5
    \(000=\mathrm{CH} 1\) positive input is AN0, CH 2 positive input is AN1, CH3 positive input is AN2
    bit 2-1 CH123NA<1:0>: Channels 1, 2, 3 Negative Input Select for Sample A bits
    \(11=\mathrm{CH} 1\) negative input is AN9, CH 2 negative input is AN10, CH3 negative input is AN11
    \(10=\mathrm{CH} 1\) negative input is AN6, CH 2 negative input is AN7, CH 3 negative input is AN8
    \(0 \mathrm{x}=\mathrm{CH} 1, \mathrm{CH} 2, \mathrm{CH} 3\) negative inputs are Vrefl
    bit \(0 \quad\) CH123SA0: Channels 1, 2, 3 Positive Input Select for Sample A bit
    See bits<4:3> for bit selections.

    REGISTER 24-6: ADxCHS0: ADCx INPUT CHANNEL 0 SELECT REGISTER
    \begin{tabular}{|l|c|c|c|c|c|c|r|}
    \hline \multicolumn{1}{|c}{ R/W-0 } & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline CHONB & - & CHOSB5 \(^{(1,3)}\) & CHOSB4 \(^{(1,3)}\) & CHOSB3 \(^{(1,3)}\) & CHOSB2 \({ }^{(1,3)}\) & CH0SB1 \({ }^{(1,3)}\) & CHOSB0 \(^{(1,3)}\) \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline CHONA & - & CHOSA5 \({ }^{(1,3)}\) & CHOSA4 \({ }^{(1,3)}\) & CHOSA3 \({ }^{(1,3)}\) & CHOSA2 \({ }^{(1,3)}\) & CHOSA1 \({ }^{(1,3)}\) & CHOSA0 \({ }^{(1,3)}\) \\
    \hline \multicolumn{8}{|l|}{bit \(7 \quad\) bit 0} \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}
    bit 15 CHONB: Channel 0 Negative Input Select for Sample MUX B bit
    \(1=\) Channel 0 negative input is \(\mathrm{AN} 1^{(1)}\)
    \(0=\) Channel 0 negative input is VREFL
    bit 14 Unimplemented: Read as ' 0 '
    bit 13-8 CHOSB<5:0>: Channel 0 Positive Input Select for Sample MUX B bits \({ }^{(1,3)}\)
    111111 = Channel 0 positive input is AN63
    \(111110=\) Channel 0 positive input is AN62
    111101 = Channel 0 positive input is AN61 (internal band gap voltage)
    -
    -
    -
    011111 = Channel 0 positive input is AN31
    \(011110=\) Channel 0 positive input is AN30
    -
    -
    000001 = Channel 0 positive input is AN1
    \(000000=\) Channel 0 positive input is ANO (Op Amp 2) \()^{(2)}\)
    bit 7 CHONA: Channel 0 Negative Input Select for Sample MUX A bit
    \(1=\) Channel 0 negative input is \(\mathrm{AN} 1^{(1)}\)
    \(0=\) Channel 0 negative input is VREFL
    bit 6
    Unimplemented: Read as '0'
    Note 1: AN0 to AN7 are repurposed when comparator and op amp functionality are enabled. See Figure 24-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.
    2: If the op amp is selected (OPAEN bit \((C M x C O N<10>)=1)\), the OAx input is used; otherwise, the ANx input is used.
    3: See the "Pin Diagrams" section for the available analog channels for each device.

    \section*{REGISTER 24-6: ADxCHSO: ADCx INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)}
    bit 5-0 CHOSA<5:0>: Channel 0 Positive Input Select for Sample MUX A bits \({ }^{(1,3)}\)
    111111 = Channel 0 positive input is AN63
    \(111110=\) Channel 0 positive input is AN62
    111101 = Channel 0 positive input is AN61 (internal band gap voltage)
    -
    -
    011111 = Channel 0 positive input is AN31
    \(011110=\) Channel 0 positive input is AN30
    -
    \(\cdot\)
    -
    000001 = Channel 0 positive input is AN1
    \(000000=\) Channel 0 positive input is ANO (Op Amp 2) \()^{(2)}\)
    Note 1: AN0 to AN7 are repurposed when comparator and op amp functionality are enabled. See Figure 24-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.
    2: If the op amp is selected (OPAEN bit \((C M x C O N<10>)=1)\), the OAx input is used; otherwise, the ANx input is used.
    3: See the "Pin Diagrams" section for the available analog channels for each device.

    \section*{REGISTER 24-7: ADxCSSH: ADCx INPUT SCAN SELECT REGISTER HIGH \({ }^{(2)}\)}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline CSS31 & CSS30 & CSS29 & CSS28 & CSS27 & CSS26 \({ }^{(1)}\) & CSS25 \(^{(1)}\) & CSS24 \({ }^{(1)}\) \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline - & - & - & - & CSS19 & CSS18 & CSS17 & CSS16 \\
    \hline \multicolumn{8}{|l|}{bit 7 bit 0} \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|}
    \hline bit 15 & CSS31: ADCx Input Scan Selection bit \\
    \hline & \[
    \begin{aligned}
    & 1=\text { Selects ANx for input scan } \\
    & 0=\text { Skips ANx for input scan }
    \end{aligned}
    \] \\
    \hline bit 14 & \begin{tabular}{l}
    CSS30: ADCx Input Scan Selection bit \\
    1 = Selects ANx for input scan \\
    0 = Skips ANx for input scan
    \end{tabular} \\
    \hline bit 13 & \begin{tabular}{l}
    CSS29: ADCx Input Scan Selection bits \\
    1 = Selects ANx for input scan \\
    \(0=\) Skips ANx for input scan
    \end{tabular} \\
    \hline bit 12 & \begin{tabular}{l}
    CSS28: ADCx Input Scan Selection bit \\
    1 = Selects ANx for input scan \\
    0 = Skips ANx for input scan
    \end{tabular} \\
    \hline bit 11 & \begin{tabular}{l}
    CSS27: ADCx Input Scan Selection bit \\
    1 = Selects ANx for input scan \\
    0 = Skips ANx for input scan
    \end{tabular} \\
    \hline bit 10 & \begin{tabular}{l}
    CSS26: ADCx Input Scan Selection bit \({ }^{(1)}\) \\
    1 = Selects OA3/AN6 for input scan \\
    0 = Skips OA3/AN6 for input scan
    \end{tabular} \\
    \hline bit 9 & \begin{tabular}{l}
    CSS25: ADCx Input Scan Selection bit \({ }^{(1)}\) \\
    1 = Selects OA2/AN0 for input scan \\
    \(0=\) Skips OA2/AN0 for input scan
    \end{tabular} \\
    \hline bit 8 & \begin{tabular}{l}
    CSS24: ADCx Input Scan Selection bit \({ }^{(1)}\) \\
    1 = Selects OA1/AN3 for input scan \\
    \(0=\) Skips OA1/AN3 for input scan
    \end{tabular} \\
    \hline bit 7-4 & Unimplemented: Read as ' 0 ' \\
    \hline bit 3 & \begin{tabular}{l}
    CSS19: ADCx Input Scan Selection bit \\
    1 = Selects ANx for input scan \\
    \(0=\) Skips ANx for input scan
    \end{tabular} \\
    \hline bit 2 & \begin{tabular}{l}
    CSS18: ADCx Input Scan Selection bit \\
    1 = Selects ANx for input scan \\
    \(0=\) Skips ANx for input scan
    \end{tabular} \\
    \hline
    \end{tabular}

    Note 1: If the op amp is selected (OPAEN bit \((C M x C O N<10>)=1\) ), the OAx input is used; otherwise, the ANx input is used.
    2: All bits in this register can be selected by the user application. However, inputs selected for scan without a corresponding input on the device convert VREFL.

    \section*{REGISTER 24-7: ADxCSSH: ADCx INPUT SCAN SELECT REGISTER HIGH \({ }^{(2)}\) (CONTINUED)}
    bit \(1 \quad\) CSS17: ADCx Input Scan Selection bit
    1 = Selects ANx for input scan
    \(0=\) Skips ANx for input scan
    bit \(0 \quad\) CSS16: ADCx Input Scan Selection bit
    1 = Selects ANx for input scan
    \(0=\) Skips ANx for input scan
    Note 1: If the op amp is selected (OPAEN bit \((C M x C O N<10>)=1\) ), the OAx input is used; otherwise, the ANx input is used.
    2: All bits in this register can be selected by the user application. However, inputs selected for scan without a corresponding input on the device convert VREFL.

    REGISTER 24-8: ADxCSSL: ADCx INPUT SCAN SELECT REGISTER LOW \({ }^{(1,2)}\)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{CSS<15:8>} \\
    \hline bit 15 & & & & & & & bit 8 \\
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline \multicolumn{8}{|c|}{CSS<7:0>} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & ' 1 ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared \\
    \hline
    \end{tabular}
    bit 15-0
    CSS<15:0>: ADCx Input Scan Selection bits
    1 = Selects ANx for input scan
    \(0=\) Skips ANx for input scan
    Note 1: On devices with less than 16 analog inputs, all bits in this register can be selected by the user application. However, inputs selected for scan without a corresponding input on the device convert Vrefl.
    2: \(\operatorname{CSS} x=A N x\), where ' \(x\) ' \(=0-5\).

    \subsection*{25.0 OP AMP/COMPARATOR MODULE}

    Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Op Amp/Comparator" (DS70000357) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
    2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

    The dsPIC33EVXXXGM00X/10X family devices contain up to five comparators that can be configured in various ways. CMP1, CMP2, CMP3 and CMP5 also have the option to be configured as op amps, with the output being brought to an external pin for gain/filtering connections. As shown in Figure 25-1, individual comparator options are specified by the comparator module's Special Function Register (SFR) control bits.
    The following options allow users to:
    - Select the Edge for Trigger and Interrupt Generation
    - Configure the Comparator Voltage Reference
    - Configure Output Blanking and Masking
    - Configure as a Comparator or Op Amp (CMP1, CMP2, CMP3 and CMP5 only)

    Note: Not all op amp/comparator input/output connections are available on all devices. See the "Pin Diagrams" section for available connections.

    \section*{FIGURE 25-1: OP AMP/COMPARATOR x MODULE BLOCK DIAGRAM}
    

    Note 1: The CxOUT pin is not a dedicated output pin on the device. This must be mapped to a physical pin using Peripheral Pin Select (PPS). Refer to Section 11.0 "I/O Ports" for more information.

    Figure \(25-2\), shows the user-programmable blanking function block diagram.

    FIGURE 25-2: USER-PROGRAMMABLE BLANKING FUNCTION BLOCK DIAGRAM
    

    Figure 25-3, shows digital filter interconnect block diagram.

    FIGURE 25-3: DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM
    

    Note 1: See the Type C Timer Block Diagram (Figure 13-2).
    2: See the Type B Timer Block Diagram (Figure 13-1).
    3: \(\quad\) See the PWMx Module Register Interconnect Diagram (Figure 17-2).
    4: See the Oscillator System Diagram (Figure 9-1).

    \subsection*{25.1 Op Amp/Comparator Control Registers}

    \section*{REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline \multicolumn{1}{|c|}{ R/W-0 } & U-0 & U-0 & R-0 & R-0 & R-0 & R-0 & R-0 \\
    \hline PSIDL & - & - & C5EVT \({ }^{(1)}\) & C4EVT \({ }^{(1)}\) & C3EVT \(^{(1)}\) & C2EVT \({ }^{(1)}\) & C1EVT \(^{(1)}\) \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & R-0 & R-0 & R-0 & R-0 \\
    \hline- & - & - & C5OUT \(^{(\mathbf{2})}\) & C4OUT \(^{(\mathbf{2})}\) & C3OUT \(^{(\mathbf{2})}\) & C2OUT \(^{(\mathbf{2})}\) & C1OUT \(^{(\mathbf{2})}\) \\
    \hline bit 7 & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(\prime 0 '=\) Bit is cleared \(\quad x=\) Bit is unknown
    \end{tabular}
    bit 15 PSIDL: Op Amp/Comparator Stop in Idle Mode bit
    1 = Discontinues operation of all op amps/comparators when device enters Idle mode
    \(0=\) Continues operation of all op amps/comparators in Idle mode
    bit 14-13 Unimplemented: Read as ' 0 '
    bit 12-8 C5EVT:C1EVT: Op Amp/Comparator 1-5 Event Status bits \({ }^{(1)}\)
    1 = Op amp/comparator event occurred
    0 = Op amp/comparator event did not occur
    bit 7-5 Unimplemented: Read as ' 0 '
    bit 4-0 C5OUT:C10UT: Op Amp/Comparator 1-5 Output Status bits \({ }^{(2)}\)
    When CPOL = 0 :
    \(1=\) VIN \(+>\) VIN-
    \(0=\mathrm{VIN}+<\mathrm{VIN}-\)
    When CPOL = 1 :
    \(1=\) VIN \(+<\) VIN-
    \(0=\mathrm{VIN}+>\) VIN -
    Note 1: Reflects the value of the of the CEVT bit in the respective Op Amp/Comparator Control register, CMxCON<9>.
    2: Reflects the value of the COUT bit in the respective Op Amp/Comparator Control register, \(\mathrm{CMxCON}<8>\).

    REGISTER 25-2: CMxCON: COMPARATOR \(x\) CONTROL REGISTER ( \(x=1,2,3\) OR 5)
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & U-0 & U-0 & R/W-0 & R/W-0 & R-0 \\
    \hline CON & COE & CPOL & - & - & OPAEN & CEVT & COUT \\
    \hline \multicolumn{7}{|l|}{bit 15} & bit 8 \\
    \hline R/W-0 & R/W-0 & U-0 & R/W-0 & U-0 & U-0 & R/W-0 & R/W-0 \\
    \hline EVPOL1 & EVPOLO & - & CREF \({ }^{(1)}\) & - & - & \(\mathrm{CCH} 1^{(1)}\) & \(\mathrm{CCH0}{ }^{(1)}\) \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0 '=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15 CON: Op Amp/Comparator \(x\) Enable bit
    1 = Op Amp/Comparator \(x\) is enabled
    \(0=\) Op Amp/Comparator \(x\) is disabled
    bit 14 COE: Comparator \(x\) Output Enable bit
    1 = Comparator output is present on the CxOUT pin
    0 = Comparator output is internal only
    bit 13 CPOL: Comparator \(x\) Output Polarity Select bit
    1 = Comparator output is inverted \(0=\) Comparator output is not inverted
    bit 12-11 Unimplemented: Read as ' 0 '
    bit 10
    OPAEN: Op Amp x Enable bit
    1 = Op amp is enabled
    \(0=\) Op amp is disabled
    bit 9
    CEVT: Comparator x Event bit
    \(1=\) Comparator event, according to EVPOL<1:0> settings, occurred; disables future triggers and interrupts until the bit is cleared
    \(0=\) Comparator event did not occur
    bit 8
    COUT: Comparator x Output bit
    When CPOL \(=0\) (non-inverted polarity):
    \(1=\) VIN \(+>\) VIN-
    \(0=\) VIN \(+<\) VIN-
    When CPOL = 1 (inverted polarity):
    1 = VIN+ < VIN-
    \(0=\mathrm{VIN}+>\) VIN -
    Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.

    \section*{REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2, 3 OR 5) (CONTINUED)}
    ```

    bit 7-6 EVPOL<1:0>: Trigger/Event/Interrupt Polarity Select bits
    11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)
    10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator
    output (while CEVT = 0)
    If CPOL = 1 (inverted polarity):
    Low-to-high transition of the comparator output.
    If CPOL = 0 (non-inverted polarity):
    High-to-low transition of the comparator output.
    01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator
    output (while CEVT = 0)
    If CPOL = 1 (inverted polarity):
    High-to-low transition of the comparator output.
    If CPOL = 0 (non-inverted polarity):
    Low-to-high transition of the comparator output.
    00 = Trigger/event/interrupt generation is disabled
    bit 5 Unimplemented: Read as '0'
    bit 4 CREF: Comparator x Reference Select bit (VIN+ input)(1)
    1 = VIN+ input connects to the internal CVREFIN voltage
    0 = VIN+ input connects to the CxIN1+ pin
    bit 3-2 Unimplemented: Read as ' }0\mathrm{ '
    bit 1-0 $\quad \mathbf{C C H}<1: 0>$ : Op Amp/Comparator $x$ Channel Select bits ${ }^{(1)}$
    11 = Inverting input of op amp/comparator connects to the OA3/AN6/C4IN4- pin
    $10=$ Inverting input of op amp/comparator connects to the OA2/ANO/C4IN3- pin
    01 = Inverting input of op amp/comparator connects to the OA1/AN3/CxIN2- pin
    $00=$ Inverting input of op amp/comparator connects to the CxIN1- pin

    ```

    Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.

    \section*{REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & U-0 & U-0 & U-0 & R/W-0 & R-0 \\
    \hline CON & COE & CPOL & - & - & - & CEVT & COUT \\
    \hline bit 15 & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & U-0 & R/W-0 & U-0 & U-0 & R/W-0 & R/W-0 \\
    \hline EVPOL1 & EVPOLO & - & CREF \({ }^{(1)}\) & - & - & \(\mathrm{CCH} 1^{(1)}\) & \(\mathrm{CCH0}{ }^{(1)}\) \\
    \hline \multicolumn{8}{|l|}{bit 7 bit 0} \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1\) ' \(=\) Bit is set & 0 ' \(=\) Bit is cleared
    \end{tabular}\(\quad x=\) Bit is unknown
    bit 15 CON: Op Amp/Comparator 4 Enable bit
    1 = Comparator is enabled
    \(0=\) Comparator is disabled
    bit 14 COE: Comparator 4 Output Enable bit
    1 = Comparator output is present on the C4OUT pin
    \(0=\) Comparator output is internal only
    bit 13 CPOL: Comparator 4 Output Polarity Select bit
    1 = Comparator output is inverted
    \(0=\) Comparator output is not inverted
    bit 12-10 Unimplemented: Read as ' 0 '
    bit 9
    CEVT: Comparator 4 Event bit
    1 = Comparator event, according to EVPOL<1:0> settings, occurred; disables future triggers and interrupts until the bit is cleared
    \(0=\) Comparator event did not occur
    bit 8
    COUT: Comparator 4 Output bit
    When CPOL \(=0\) (non-inverted polarity):
    \(1=\) VIN \(+>\) VIN-
    \(0=\mathrm{VIN}+<\mathrm{VIN}-\)
    When CPOL \(=1\) (inverted polarity):
    \(1=\mathrm{VIN}+<\mathrm{VIN}-\)
    \(0=\) VIN \(+>\) VIN-
    bit 7-6 EVPOL<1:0>: Trigger/Event/Interrupt Polarity Select bits
    \(11=\) Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)
    \(10=\) Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
    If \(\mathrm{CPOL}=1\) (inverted polarity):
    Low-to-high transition of the comparator output.
    If CPOL \(=0\) (non-inverted polarity):
    High-to-low transition of the comparator output.
    01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)
    If CPOL \(=1\) (inverted polarity):
    High-to-low transition of the comparator output.
    If CPOL \(=0\) (non-inverted polarity):
    Low-to-high transition of the comparator output.
    \(00=\) Trigger/event/interrupt generation is disabled
    Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.

    \section*{REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER (CONTINUED)}
    bit \(5 \quad\) Unimplemented: Read as ' 0 '
    bit 4 CREF: Comparator 4 Reference Select bit (VIN+ input) \({ }^{(1)}\)
    \(1=\) VIN + input connects to the internal CVREFIN voltage
    \(0=\mathrm{VIN}+\) input connects to the C4IN1+ pin
    bit 3-2 Unimplemented: Read as ' 0 '
    bit 1-0 \(\quad \mathbf{C C H}<1: 0>\) : Comparator 4 Channel Select bits \({ }^{(1)}\)
    \(11=\) VIN- input of comparator connects to the C4IN4- pin
    \(10=\) VIN- input of comparator connects to the C4IN3- pin
    \(01=\) VIN- input of comparator connects to the C4IN2- pin
    \(00=\) VIN- input of comparator connects to the C4IN1- pin
    Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.

    \section*{REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT} CONTROL REGISTER
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & RW-0 \\
    \hline- & - & - & - & SELSRCC3 & SELSRCC2 & SELSRCC1 & SELSRCC0 \\
    \hline bit 15 & & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|}
    \hline \multicolumn{1}{|c}{ R/W-0 } & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline SELSRCB3 & SELSRCB2 & SELSRCB1 & SELSRCB0 & SELSRCA3 & SELSRCA2 & SELSRCA1 & SELSRCA0 \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & ' 1 ' = Bit is set & \(' 0\) ' = Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-12 Unimplemented: Read as ' 0 '
    bit 11-8 SELSRCC<3:0>: Mask C Input Select bits
    \[
    \begin{aligned}
    & 1111=\text { FLT4 } \\
    & 1110=\text { FLT2 } \\
    & 1101=\text { Reserved } \\
    & 1100=\text { Reserved } \\
    & 1011=\text { Reserved } \\
    & 1010=\text { Reserved } \\
    & 1001=\text { Reserved } \\
    & 1000=\text { Reserved } \\
    & 0111=\text { Reserved } \\
    & 0110=\text { Reserved } \\
    & 0101=\text { PWM3H } \\
    & 0100=\text { PWM3L } \\
    & 0011=\text { PWM2H } \\
    & 0010=\text { PWM2L } \\
    & 0001=\text { PWM1H } \\
    & 0000=\text { PWM1L }
    \end{aligned}
    \]
    bit 7-4 SELSRCB<3:0>: Mask B Input Select bits
    ```

    1111 = FLT4
    1110 = FLT2
    1101 = Reserved
    1100 = Reserved
    1011 = Reserved
    1010 = Reserved
    1001 = Reserved
    1000 = Reserved
    0 1 1 1 ~ = ~ R e s e r v e d ~
    0 1 1 0 ~ = ~ R e s e r v e d ~
    0101 = PWM3H
    0100 = PWM3L
    011 = PWM2H
    0010 = PWM2L
    0001 = PWM1H
    0000 = PWM1L

    ```

    REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER (CONTINUED)
    bit 3-0 SELSRCA<3:0>: Mask A Input Select bits
    \[
    \begin{aligned}
    & 1111=\text { FLT4 } \\
    & 1110=\text { FLT2 } \\
    & 1101=\text { Reserved } \\
    & 1100=\text { Reserved } \\
    & 1011=\text { Reserved } \\
    & 1010=\text { Reserved } \\
    & 1001=\text { Reserved } \\
    & 1000=\text { Reserved } \\
    & 0111=\text { Reserved } \\
    & 0110=\text { Reserved } \\
    & 0101=\text { PWM3H } \\
    & 0100=\text { PWM3L } \\
    & 0011=\text { PWM2H } \\
    & 0010=\text { PWM2L } \\
    & 0001=\text { PWM1H } \\
    & 0000=\text { PWM1L }
    \end{aligned}
    \]

    \section*{REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline HLMS & - & OCEN & OCNEN & OBEN & OBNEN & OAEN & OANEN \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|l|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline NAGS & PAGS & ACEN & ACNEN & ABEN & ABNEN & AAEN & AANEN \\
    \hline bit 7 & & & & bit 0 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lll}
    \hline Legend: & & \\
    \(R=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' = Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15 HLMS: High or Low-Level Masking Select bit
    1 = The masking (blanking) function will prevent any asserted ('0') comparator signal from propagating
    \(0=\) The masking (blanking) function will prevent any asserted (' 1 ') comparator signal from propagating
    bit 14 Unimplemented: Read as ' 0 '
    bit 13 OCEN: OR Gate \(C\) Input Enable bit
    \(1=\mathrm{MCl}\) is connected to OR gate
    \(0=\mathrm{MCl}\) is not connected to OR gate
    bit 12 OCNEN: OR Gate C Input Inverted Enable bit
    1 = Inverted MCI is connected to OR gate
    \(0=\) Inverted MCI is not connected to OR gate
    bit 11 OBEN: OR Gate B Input Enable bit
    \(1=\mathrm{MBI}\) is connected to OR gate
    \(0=\mathrm{MBI}\) is not connected to OR gate
    bit 10
    bit 9 OAEN: OR Gate A Input Enable bit
    \(1=\) MAI is connected to OR gate
    \(0=\) MAI is not connected to OR gate
    bit 8 OANEN: OR Gate A Input Inverted Enable bit
    1 = Inverted MAI is connected to OR gate
    \(0=\) Inverted MAI is not connected to OR gate
    bit 7 NAGS: AND Gate Output Inverted Enable bit 1 = Inverted ANDI is connected to OR gate \(0=\) Inverted ANDI is not connected to OR gate
    bit 6 PAGS: AND Gate Output Enable bit
    \(1=\) ANDI is connected to OR gate
    \(0=\) ANDI is not connected to OR gate
    bit 5 ACEN: AND Gate C Input Enable bit \(1=\mathrm{MCl}\) is connected to AND gate \(0=\mathrm{MCl}\) is not connected to AND gate
    bit \(4 \quad\) ACNEN: AND Gate C Input Inverted Enable bit
    \(1=\) Inverted MCl is connected to AND gate
    \(0=\) Inverted MCI is not connected to AND gate

    \section*{REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER (CONTINUED)}
    bit 3 ABEN: AND Gate B Input Enable bit
    \(1=\mathrm{MBI}\) is connected to AND gate \(0=\mathrm{MBI}\) is not connected to AND gate
    bit 2 ABNEN: AND Gate B Input Inverted Enable bit
    1 = Inverted MBI is connected to AND gate
    \(0=\) Inverted MBI is not connected to AND gate
    bit 1
    AAEN: AND Gate A Input Enable bit
    \(1=\) MAI is connected to AND gate
    \(0=\) MAI is not connected to AND gate
    bit \(0 \quad\) AANEN: AND Gate A Input Inverted Enable bit
    1 = Inverted MAI is connected to AND gate
    \(0=\) Inverted MAI is not connected to AND gate

    REGISTER 25-6: CMxFLTR: COMPARATOR x FILTER CONTROL REGISTER
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 & U-0 \\
    \hline- & - & - & - & - & - & - & - \\
    \hline bit 15 \\
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline - & CFSEL2 & CFSEL1 & CFSEL0 & CFLTREN & CFDIV2 & CFDIV1 & CFDIV0 \\
    \hline bit 7 &
    \end{tabular}
    \end{tabular}\(.\)\begin{tabular}{l} 
    bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & \(' 1\) ' = Bit is set & \(' 0\) ' \(=\) Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15-7 Unimplemented: Read as ' 0 '
    bit 6-4 CFSEL<2:0>: Comparator x Filter Input Clock Select bits
    \[
    \begin{aligned}
    & 111=\operatorname{T5CLK}^{(1)} \\
    & 110=\operatorname{T4CLK}^{(2)} \\
    & 101=\operatorname{T3CLK}^{(1)} \\
    & 100=\operatorname{T2CLK}^{(2)} \\
    & 011=\operatorname{Reserved}^{2} \\
    & 010=\operatorname{SYNCO}^{(3)} \\
    & 001=\operatorname{Fosc}^{(4)} \\
    & 000=\operatorname{FP}^{(4)}
    \end{aligned}
    \]
    bit 3 CFLTREN: Comparator x Filter Enable bit
    1 = Digital filter is enabled
    \(0=\) Digital filter is disabled
    bit 2-0 CFDIV<2:0>: Comparator x Filter Clock Divide Select bits
    111 = Clock divide 1:128
    \(110=\) Clock divide 1:64
    101 = Clock divide 1:32
    \(100=\) Clock divide 1:16
    011 = Clock divide 1:8
    \(010=\) Clock divide 1:4
    001 = Clock divide 1:2
    \(000=\) Clock divide 1:1
    Note 1: See the Type C Timer Block Diagram (Figure 13-2).
    2: See the Type B Timer Block Diagram (Figure 13-1).
    3: See the High-Speed PWMx Module Register Interconnection Diagram (Figure 17-2).
    4: See the Oscillator System Diagram (Figure 9-1).

    \subsection*{26.0 COMPARATOR VOLTAGE REFERENCE}

    Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Op Amp/Comparator" (DS70000357) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
    2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

    \subsection*{26.1 Configuring the Comparator Voltage Reference}

    The comparator voltage reference module is controlled through the CVRxCON registers (Register 26-1 and Register 26-2). The comparator voltage reference provides a range of output voltages with 128 distinct levels. The comparator reference supply voltage can come from either VDD and Vss, or the external CVRef+ and AVss pins. The voltage source is selected by the CVRSS bit (CVRxCON<11>). The settling time of the comparator voltage reference must be considered when changing the CVREF output.

    FIGURE 26-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM
    

    \subsection*{26.2 Comparator Voltage Reference Registers}

    \section*{REGISTER 26-1: CVR1CON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER 1}
    \begin{tabular}{|l|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & U-0 & U-0 & R/W-0 & R/W-0 & U-0 & U-0 \\
    \hline CVREN & CVROE & - & - & CVRSS & VREFSEL & - & - \\
    \hline bit 15 & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|}
    \hline U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline- & CVR6 & CVR5 & CVR4 & CVR3 & CVR2 & CVR1 & CVR0 \\
    \hline bit 7
    \end{tabular}
    \begin{tabular}{|lll|}
    \hline Legend: & \\
    \(R=\) Readable bit & \(W=\) Writable bit & \(U=\) Unimplemented bit, read as ' 0 ' \\
    \(-n=\) Value at POR & \(' 1 '=\) Bit is set & \(' 0\) ' \(=\) Bit is cleared \\
    \hline
    \end{tabular}
    \begin{tabular}{|c|c|}
    \hline bit 15 & CVREN: Comparator Voltage Reference Enable bit \\
    \hline & \begin{tabular}{l}
    1 = Comparator voltage reference circuit is powered on \\
    0 = Comparator voltage reference circuit is powered down
    \end{tabular} \\
    \hline bit 14 & \begin{tabular}{l}
    CVROE: Comparator Voltage Reference Output Enable (CVREF10 Pin) bit \\
    1 = Voltage level is output on the CVREF10 pin \\
    \(0=\) Voltage level is disconnected from the CVREF10 pin
    \end{tabular} \\
    \hline bit 13-12 & Unimplemented: Read as '0' \\
    \hline bit 11 & \begin{tabular}{l}
    CVRSS: Comparator Voltage Reference Source Selection bit \\
    1 = Comparator reference source, CVRSRC = CVREF+ - AVSS \\
    0 = Comparator reference source, CVRSRC = AVDD - AVss
    \end{tabular} \\
    \hline bit 10 & VREFSEL: Voltage Reference Select bit
    \[
    \begin{aligned}
    & 1=\text { CVREFIN }=\text { CVREF }+ \\
    & 0=\text { CVREFIN is generated by the resistor network }
    \end{aligned}
    \] \\
    \hline bit 9-7 & Unimplemented: Read as '0' \\
    \hline bit 6-0 & CVR<6:0>: Comparator Voltage Reference Value Selection bits 1111111 = 127/128 x VREF input voltage
    \[
    0000000=0.0 \text { volts }
    \] \\
    \hline
    \end{tabular}

    REGISTER 26-2: CVR2CON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER 2
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R/W-0 & R/W-0 & U-0 & U-0 & R/W-0 & R/W-0 & U-0 & U-0 \\
    \hline CVREN & CVROE & - & - & CVRSS & VREFSEL & - & - \\
    \hline \multicolumn{7}{|l|}{bit 15} & bit 8 \\
    \hline U-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 & R/W-0 \\
    \hline - & CVR6 & CVR5 & CVR4 & CVR3 & CVR2 & CVR1 & CVR0 \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}

    \section*{Legend:}
    \begin{tabular}{lll}
    \(\mathrm{R}=\) Readable bit & \(\mathrm{W}=\) Writable bit & \(\mathrm{U}=\) Unimplemented bit, read as ' 0 ' \\
    \(-\mathrm{n}=\) Value at POR & ' 1 ' \(=\) Bit is set & ' 0 ' = Bit is cleared
    \end{tabular}\(\quad \mathrm{x}=\) Bit is unknown
    bit 15 CVREN: Comparator Voltage Reference Enable bit
    1 = Comparator voltage reference circuit is powered on
    0 = Comparator voltage reference circuit is powered down
    bit 14 CVROE: Comparator Voltage Reference Output Enable (CVREF2O Pin) bit
    1 = Voltage level is output on the CVREF2O pin
    \(0=\) Voltage level is disconnected from the CVREF2O pin
    bit 13-12 Unimplemented: Read as ' 0 '
    bit 11
    CVRSS: Comparator Voltage Reference Source Selection bit
    1 = Comparator reference source, CVRSRC = CVREF+ - AVss
    \(0=\) Comparator reference source, CVRSRC = AVDD - AVss
    bit 10
    bit 9-7 Unimplemented: Read as ' 0 '
    bit 6-0 CVR<6:0>: Comparator Voltage Reference Value Selection bits
    \(1111111=127 / 128 \times\) VREF input voltage
    -
    -
    -
    \(0000000=0.0\) volts

    \subsection*{27.0 SPECIAL FEATURES}

    Note: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

    The dsPIC33EVXXXGM00X/10X family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:
    - Flexible Configuration
    - Watchdog Timer (WDT)
    - Code Protection and CodeGuard \({ }^{\text {TM }}\) Security
    - In-Circuit Serial Programming \({ }^{\text {TM }}\) (ICSP \({ }^{\text {TM }}\) )
    - In-Circuit Emulation

    \subsection*{27.1 Configuration Bits}

    In dsPIC33EVXXXGM00X/10X family devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored at the top of the on-chip program memory space, known as the Flash Configuration bytes. Their specific locations are shown in Table 27-1. The configuration data is automatically loaded from the Flash Configuration bytes to the proper Configuration Shadow registers during device Resets.

    Note: Configuration data is reloaded on all types of device Resets.

    When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration bytes for configuration data in their code for the compiler. This is to ensure that program code is not stored in this address when the code is compiled.
    The upper 2 bytes of all Flash Configuration Words in program memory should always be '1111 11111111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing ' 1 's to these locations has no effect on device operation.
    Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

    The Configuration Flash bytes map is shown in Table 27-1.
    TABLE 27-1: CONFIGURATION BYTE REGISTER MAP
    \begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
    \hline File Name & Address & Device
    Memory
    Size
    (Kbytes) & \[
    \begin{array}{|c|}
    \text { Bits } \\
    23-16
    \end{array}
    \] & Bit 15 & Bit 14 & Bit 13 & Bit 12 & Bit 11 & Bit 10 & Bit 9 & Bit 8 & Bit 7 & Bit 6 & Bit 5 & Bit 4 & Bit 3 & Bit 2 & Bit 1 & Bit 0 \\
    \hline \multirow[t]{3}{*}{FSEC} & 00AB80 & 64 & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{AIVTDIS} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{CSS2} & \multirow[t]{3}{*}{CSS1} & \multirow[t]{3}{*}{csso} & \multirow[t]{3}{*}{CWRP} & \multirow[t]{3}{*}{GSS1} & \multirow[t]{3}{*}{GSSO} & \multirow[t]{3}{*}{GWRP} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{BSEN} & \multirow[t]{3}{*}{BSS1} & \multirow[t]{3}{*}{BSSO} & \multirow[t]{3}{*}{BWRP} \\
    \hline & 015780 & 128 & & & & & & & & & & & & & & & & & \\
    \hline & 02AB80 & 256 & & & & & & & & & & & & & & & & & \\
    \hline \multirow[t]{3}{*}{FBSLIM} & 00Ab90 & 64 & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multicolumn{13}{|l|}{\multirow[t]{3}{*}{- BSLIM<12:0>}} \\
    \hline & 015790 & 128 & & & & & & & & & & & & & & & & & \\
    \hline & 02AB90 & 256 & & & & & & & & & & & & & & & & & \\
    \hline \multirow[t]{3}{*}{Reserved} & 00AB94 & 64 & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{Reserved \({ }^{(1)}\)} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} \\
    \hline & 015794 & 128 & & & & & & & & & & & & & & & & & \\
    \hline & 02AB94 & 256 & & & & & & & & & & & & & & & & & \\
    \hline \multirow[t]{3}{*}{FOSCSEL} & 00AB98 & 64 & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{\(\overline{\text { ESO }}\)} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{FNOSC2} & \multirow[t]{3}{*}{FNOSC1} & \multirow[t]{3}{*}{FNOSCO} \\
    \hline & 015798 & 128 & & & & & & & & & & & & & & & & & \\
    \hline & 02AB98 & 256 & & & & & & & & & & & & & & & & & \\
    \hline \multirow[t]{3}{*}{FOSC} & 00AB9C & 64 & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{PLLKEN} & \multirow[t]{3}{*}{FCKSM1} & \multirow[t]{3}{*}{FCKSMO} & \multirow[t]{3}{*}{IOL1WAY} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{OSCIOFNC} & \multirow[t]{3}{*}{POSCMD1} & \multirow[t]{3}{*}{POSCMDO} \\
    \hline & 01579C & 128 & & & & & & & & & & & & & & & & & \\
    \hline & 02AB9C & 256 & & & & & & & & & & & & & & & & & \\
    \hline \multirow[t]{3}{*}{FWDT} & 00ABAO & 64 & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{WDTWIN1} & \multirow[t]{3}{*}{WDTWINO} & \multirow[t]{3}{*}{WINDIS} & \multirow[t]{3}{*}{FWDTEN1} & \multirow[t]{3}{*}{FWDTENO} & \multirow[t]{3}{*}{WDTPRE} & \multirow[t]{3}{*}{WDTPS3} & \multirow[t]{3}{*}{WDTPS2} & \multirow[t]{3}{*}{WDTPS1} & \multirow[t]{3}{*}{WDTPSO} \\
    \hline & 0157A0 & 128 & & & & & & & & & & & & & & & & & \\
    \hline & 02ABA0 & 256 & & & & & & & & & & & & & & & & & \\
    \hline \multirow[t]{3}{*}{FPOR} & 00ABA4 & 64 & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{BOREN} \\
    \hline & 0157A4 & 128 & & & & & & & & & & & & & & & & & \\
    \hline & 02ABA4 & 256 & & & & & & & & & & & & & & & & & \\
    \hline \multirow[t]{3}{*}{FICD} & O0ABAB & 64 & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{Reserved \({ }^{(2)}\)} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{-} & \multirow[t]{3}{*}{ICS1} & \multirow[t]{3}{*}{ICSO} \\
    \hline & 0157A8 & 128 & & & & & & & & & & & & & & & & & \\
    \hline & 02ABA8 & 256 & & & & & & & & & & & & & & & & & \\
    \hline \multirow[t]{3}{*}{FDMTINTVL} & 00ABAC & 64 & \multirow[t]{3}{*}{-} & \multicolumn{16}{|l|}{\multirow[t]{3}{*}{DMTIVT<15:0>}} \\
    \hline & 0157AC & 128 & & & & & & & & & & & & & & & & & \\
    \hline & 02ABAC & 256 & & & & & & & & & & & & & & & & & \\
    \hline \multirow[t]{3}{*}{FDMTINTVH} & 00AbB0 & 64 & \multirow[t]{3}{*}{-} & \multicolumn{16}{|l|}{\multirow[t]{3}{*}{DMTIVT<31:16>}} \\
    \hline & 0157B0 & 128 & & & & & & & & & & & & & & & & & \\
    \hline & 02ABB0 & 256 & & & & & & & & & & & & & & & & & \\
    \hline
    \end{tabular}
    Legend: - = unimplemented, read as ' 1 ',
    Note 1: This bit is reserved and must be programmed as ' 0 ',
    TABLE 27-1: CONFIGURATION BYTE REGISTER MAP (CONTINUED)
    
    Legend: \(-=\) unimplemented, read as ' 1 ',
    \(\begin{array}{ll}\text { Note 1: } & \text { This bit is reserved and must be programmed as ' } 0 \text { '. } \\ \text { 2: } & \text { This bit is reserved and must be programmed as ' } 1 \text { '. }\end{array}\)

    TABLE 27-2: dsPIC33EVXXXGM00X/10X CONFIGURATION BITS DESCRIPTION
    \begin{tabular}{|c|c|c|}
    \hline Bit Field & Register & Description \\
    \hline BWRP & FSEC & \begin{tabular}{l}
    Boot Segment Write-Protect bit \\
    1 = User program memory is not write-protected \\
    \(0=\) User program memory is write-protected
    \end{tabular} \\
    \hline BSS<1:0> & FSEC & \begin{tabular}{l}
    Boot Segment Code Flash Protection Level bits \\
    11 = No protection (other than BWRP write protection) \\
    \(10=\) Standard security \\
    \(0 \mathrm{x}=\) High security
    \end{tabular} \\
    \hline BSEN & FSEC & \[
    \begin{aligned}
    & \hline \text { Boot Segment Control bit } \\
    & 1=\text { No Boot Segment } \\
    & 0=\text { Boot Segment size is determined by BSLIM<12:0> }
    \end{aligned}
    \] \\
    \hline GWRP & FSEC & \[
    \begin{array}{|l|}
    \hline \text { General Segment Write-Protect bit } \\
    1=\text { User program memory is not write-protected } \\
    0=\text { User program memory is write-protected } \\
    \hline
    \end{array}
    \] \\
    \hline GSS<1:0> & FSEC & \begin{tabular}{l}
    General Segment Code Flash Protection Level bits \(11=\) No protection (other than GWRP write protection) \\
    \(10=\) Standard security \\
    \(0 \mathrm{x}=\) High security
    \end{tabular} \\
    \hline CWRP & FSEC & \[
    \begin{aligned}
    & \hline \text { Configuration Segment Write-Protect bit } \\
    & 1=\text { Configuration Segment is not write-protected } \\
    & 0=\text { Configuration Segment is write-protected } \\
    & \hline
    \end{aligned}
    \] \\
    \hline CSS<2:0> & FSEC & \begin{tabular}{l}
    Configuration Segment Code Flash Protection Level bits 111 = No protection (other than CWRP write protection) \\
    \(110=\) Standard security \\
    10x = Enhanced security \\
    \(0 \mathrm{xx}=\) High security
    \end{tabular} \\
    \hline AIVTDIS & FSEC & Alternate Interrupt Vector Table Disable bit
    \[
    \begin{aligned}
    & 1=\text { Disables AIVT } \\
    & 0=\text { Enables AIVT }
    \end{aligned}
    \] \\
    \hline BSLIM<12:0> & FBSLIM & Boot Segment Code Flash Page Address Limit bits Contains the page address of the first active General Segment page. The value to be programmed is the inverted page address, such that programming additional ' 0 's can only increase the Boot Segment size. For example, \(0 \times 1 \mathrm{FFD}=2\) pages or 1024 instruction words. \\
    \hline FNOSC<2:0> & FOSCSEL & ```
    Initial Oscillator Source Selection bits
    111 = Internal Fast RC (FRC) Oscillator with Postscaler
    \(110=\) Internal Fast RC (FRC) Oscillator with Divide-by-16
    101 = LPRC Oscillator
    100 = Reserved
    011 = Primary (XT, HS, EC) Oscillator with PLL
    010 = Primary (XT, HS, EC) Oscillator
    001 = Internal Fast RC (FRC) Oscillator with PLL
    \(000=\) FRC Oscillator
    ``` \\
    \hline \(\overline{\text { IESO }}\) & FOSCSEL & ```
    Two-Speed Oscillator Start-up Enable bit
    1 = Starts up device with FRC, then automatically switches to the
    user-selected oscillator source when ready
    \(0=\) Starts up device with user-selected oscillator source
    ``` \\
    \hline POSCMD<1:0> & FOSC & \begin{tabular}{l}
    Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled \\
    \(10=\) HS Crystal Oscillator mode \\
    01 = XT Crystal Oscillator mode \\
    00 = EC (External Clock) mode
    \end{tabular} \\
    \hline
    \end{tabular}

    TABLE 27-2: dsPIC33EVXXXGM00X/10X CONFIGURATION BITS DESCRIPTION (CONTINUED)
    \begin{tabular}{|c|c|c|}
    \hline Bit Field & Register & Description \\
    \hline OSCIOFNC & FOSC & \[
    \begin{aligned}
    & \text { OSC2 Pin Function bit (except in XT and HS modes) } \\
    & 1=\text { OSC2 is the clock output } \\
    & 0=\text { OSC2 is the general purpose digital I/O pin }
    \end{aligned}
    \] \\
    \hline IOL1WAY & FOSC & \begin{tabular}{l}
    Peripheral Pin Select Configuration bit \\
    1 = Allows only one reconfiguration \\
    \(0=\) Allows multiple reconfigurations
    \end{tabular} \\
    \hline FCKSM<1:0> & FOSC & \begin{tabular}{l}
    Clock Switching Mode bits \\
    \(1 \mathrm{x}=\) Clock switching is disabled, Fail-Safe Clock Monitor is disabled \\
    \(01=\) Clock switching is enabled, Fail-Safe Clock Monitor is disabled \\
    \(00=\) Clock switching is enabled, Fail-Safe Clock Monitor is enabled
    \end{tabular} \\
    \hline PLLKEN & FOSC & ```
    PLL Lock Wait Enable bit
    1 = Clock switches to the PLL source; will wait until the PLL lock signal is
    valid
    \(0=\) Clock switch will not wait for PLL lock
    ``` \\
    \hline WDTPS<3:0> & FWDT & Watchdog Timer Postscaler bits
    \[
    \begin{aligned}
    & 1111=1: 32,768 \\
    & 1110=1: 16,384
    \end{aligned}
    \]
    \[
    \begin{aligned}
    & 0001=1: 2 \\
    & 0000=1: 1
    \end{aligned}
    \] \\
    \hline WDTPRE & FWDT & Watchdog Timer Prescaler bit
    \[
    \begin{aligned}
    & 1=1: 128 \\
    & 0=1: 32
    \end{aligned}
    \] \\
    \hline FWDTEN<1:0> & FWDT & ```
    Watchdog Timer Enable bits
    11 = WDT is enabled in hardware
    \(10=\) WDT is controlled through the SWDTEN bit
    01 = WDT is enabled only while device is active and disabled in Sleep; the
    SWDTEN bit is disabled
    \(00=\) WDT and the SWDTEN bit are disabled
    ``` \\
    \hline WINDIS & FWDT & \[
    \begin{aligned}
    & \text { Watchdog Timer Window Enable bit } \\
    & 1=\text { Watchdog Timer is in Non-Window mode } \\
    & 0=\text { Watchdog Timer is in Window mode } \\
    & \hline
    \end{aligned}
    \] \\
    \hline WDTWIN<1:0> & FWDT & \begin{tabular}{l}
    Watchdog Timer Window Select bits \\
    11 = WDT window is \(25 \%\) of WDT period \\
    \(10=\) WDT window is \(37.5 \%\) of WDT period \\
    \(01=\) WDT window is \(50 \%\) of WDT period \\
    \(00=\) WDT window is \(75 \%\) of WDT period
    \end{tabular} \\
    \hline BOREN & FPOR & \begin{tabular}{l}
    Brown-out Reset (BOR) Detection Enable bit \(1=B O R\) is enabled \\
    \(0=B O R\) is disabled
    \end{tabular} \\
    \hline ICS<1:0> & FICD & \begin{tabular}{l}
    ICD Communication Channel Select bits \\
    \(11=\) Communicates on PGEC1 and PGED1 \\
    \(10=\) Communicates on PGEC2 and PGED2 \\
    01 = Communicates on PGEC3 and PGED3 \\
    \(00=\) Reserved, do not use
    \end{tabular} \\
    \hline DMTIVT<15:0> & FDMTINTVL & Lower 16 Bits of 32-Bit Field that Configures the DMT Window Interval bits \\
    \hline DMTIVT<31:16> & FDMTINTVH & Upper 16 Bits of 32-Bit Field that Configures the DMT Window Interval bits \\
    \hline DMTCNT<15:0> & FDMTCNTL & Lower 16 Bits of 32-Bit Field that Configures the DMT Instruction Count Time-out Value bits \\
    \hline
    \end{tabular}

    TABLE 27-2: dsPIC33EVXXXGM00X/10X CONFIGURATION BITS DESCRIPTION (CONTINUED)
    \begin{tabular}{|c|c|c|}
    \hline Bit Field & Register & Description \\
    \hline DMTCNT<31:16> & FDMCNTH & Upper 16 Bits of 32-Bit Field that Configures the DMT Instruction Count Time-out Value bits \\
    \hline DMTEN & FDMT & \begin{tabular}{l}
    Deadman Timer Enable bit \\
    1 = Deadman Timer is enabled and cannot be disabled by software \\
    \(0=\) Deadman Timer is disabled and can be enabled by software
    \end{tabular} \\
    \hline PWMLOCK & FDEVOPT & \begin{tabular}{l}
    PWM Lock Enable bit \\
    1 = Certain PWM registers may only be written after a key sequence \\
    \(0=\) PWM registers may be written without a key sequence
    \end{tabular} \\
    \hline ALTI2C1 & FDEVOPT & \[
    \begin{aligned}
    & \text { Alternate } \mathrm{I}^{2} \mathrm{C}^{\mathrm{TM}} \text { Pins for I2C1 bit } \\
    & 1=\mathrm{I} 2 \mathrm{C} 1 \text { is mapped to the SDA1/SCL1 pins } \\
    & 0=\mathrm{I} 2 \mathrm{C} 1 \text { is mapped to the ASDA1/ASCL1 pins }
    \end{aligned}
    \] \\
    \hline CTXT1<2:0> & FALTREG & \begin{tabular}{l}
    Specifies the Alternate Working Register Set 1 Association with Interrupt Priority Level (IPL) bits \\
    111 = Not assigned \\
    110 = Alternate Register Set 1 is assigned to IPL Level 6 \\
    101 = Alternate Register Set 1 is assigned to IPL Level 5 \\
    100 = Alternate Register Set 1 is assigned to IPL Level 4 \\
    011 = Alternate Register Set 1 is assigned to IPL Level 3 \\
    010 = Alternate Register Set 1 is assigned to IPL Level 2 \\
    001 = Alternate Register Set 1 is assigned to IPL Level 1 \\
    \(000=\) Not assigned
    \end{tabular} \\
    \hline CTXT2<2:0> & FALTREG & \begin{tabular}{l}
    Specifies the Alternate Working Register Set 2 Association with Interrupt Priority Level (IPL) bits \\
    111 = Not assigned \\
    110 = Alternate Register Set 2 is assigned to IPL Level 6 \\
    101 = Alternate Register Set 2 is assigned to IPL Level 5 \\
    \(100=\) Alternate Register Set 2 is assigned to IPL Level 4 \\
    011 = Alternate Register Set 2 is assigned to IPL Level 3 \\
    010 = Alternate Register Set 2 is assigned to IPL Level 2 \\
    001 = Alternate Register Set 2 is assigned to IPL Level 1 \\
    \(000=\) Not assigned
    \end{tabular} \\
    \hline
    \end{tabular}

    \section*{REGISTER 27-1: DEVID: DEVICE ID REGISTER}
    \(\left.\begin{array}{|lllllll|}\hline R & R & R & R & R & R & R\end{array}\right]\)\begin{tabular}{l}
    \(R\) \\
    \hline \\
    \hline bit 23
    \end{tabular}
    \begin{tabular}{|rlllllll|}
    \hline\(R\) & \(R\) & \(R\) & \(R\) & \(R\) & \(R\) & \(R\) & \(R\) \\
    \hline & & \(D E V I D<15: 8>(1)\) & & & \\
    \hline bit 15 & & & & bit 8 \\
    \hline
    \end{tabular}
    \begin{tabular}{|lllllll|}
    \hline R & R & R & R & R & R & R \\
    \hline & & \(\mathrm{DEVID}<7: 0>(1)\) & R \\
    \hline bit 7 & & & & & \\
    \hline
    \end{tabular}
    Legend: \(\mathrm{R}=\) Read-Only bit \(\mathrm{U}=\) Unimplemented bit
    bit 23-0 DEVID<23:0>: Device Identifier bits \({ }^{(1)}\)
    Note 1: Refer to "dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits" (DS70663) for the list of Device ID values.

    \section*{REGISTER 27-2: DEVREV: DEVICE REVISION REGISTER}
    \begin{tabular}{|ccccccc|}
    \hline R & R & R & R & R & R & R \\
    \hline & & DEVREV<23:16>(1) & & R \\
    \hline bit 23 & & & & & bit 16 \\
    \hline
    \end{tabular}
    \(\left.\begin{array}{|ccccccc|}\hline R & R & R & R & R & R & R\end{array}\right]\)\begin{tabular}{l} 
    R \\
    \hline \\
    \hline bit 15
    \end{tabular}
    \begin{tabular}{|c|c|c|c|c|c|c|c|}
    \hline R & R & R & R & R & R & R & R \\
    \hline \multicolumn{8}{|c|}{DEVREV<7:0> \({ }^{(1)}\)} \\
    \hline bit 7 & & & & & & & bit 0 \\
    \hline
    \end{tabular}
    Legend: \(\mathrm{R}=\) Read-only bit \(\mathrm{U}=\) Unimplemented bit
    bit 23-0 DEVREV<23:0>: Device Revision bits \({ }^{(1)}\)
    Note 1: Refer to "dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits" (DS70663) for the list of device revision values.

    \subsection*{27.2 User OTP Memory}

    Locations, 800F80h-800FFEh, are a One-TimeProgrammable (OTP) memory area. The user OTP words can be used for storing product information, such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

    \subsection*{27.3 On-Chip Voltage Regulator}

    All of the dsPIC33EVXXXGM00X/10X family devices power their core digital logic at a nominal 1.8 V . This can create a conflict for designs that are required to operate at a higher typical voltage, such as 5.0 V . To simplify system design, all devices in the dsPIC33EVXXXGM00X/10X family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

    The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (see Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5, located in Section 30.0 "Electrical Characteristics".
    \begin{tabular}{ll} 
    Note: & \begin{tabular}{l} 
    It is important for the low-ESR capacitor to \\
    be placed as close as possible to the VCAP \\
    pin.
    \end{tabular} \\
    \hline
    \end{tabular}

    FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR \({ }^{(1,2,3)}\)
    

    Note 1: These are typical operating voltages. Refer to Table 30-4 located in Section 30.1 "DC Characteristics" for the full operating ranges of VDD and VCAP.
    2: It is important for the low-ESR capacitor to be placed as close as possible to the Vcap pin.
    3: Typical VcAP pin voltage \(=1.8 \mathrm{~V}\) when VDD \(\geq\) VDDMIN.

    \subsection*{27.4 Brown-out Reset (BOR)}

    The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).
    A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).
    If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit ( \(O S C C O N<5>\) ) is ' 1 '.
    Concurrently, the Power-up Timer (PWRT) Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT \(=0\) and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is Tfscm. Refer to Parameter SY35 in Table 30-21 of Section 30.0 "Electrical Characteristics" for specific TFSCM values.

    The BOR status bit ( \(\mathrm{RCON}<1>\) ) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle mode and resets the device should VDD fall below the BOR threshold voltage.

    \subsection*{27.5 Watchdog Timer (WDT)}

    For dsPIC33EVXXXGM00X/10X family devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

    \subsection*{27.5.1 PRESCALER/POSTSCALER}

    The nominal WDT clock source from LPRC is 32 kHz . This feeds a prescaler that can be configured for either 5 -bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a WDT Time-out Period (TWDT), as shown in Parameter SY12 in Table 30-21.
    A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from \(1: 1\) to \(1: 32,768\). Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.
    The WDT, prescaler and postscaler are reset:
    - On any device Reset
    - On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
    - When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
    - When the device exits Sleep or Idle mode to resume normal operation
    - By a CLRWDT instruction during normal execution

    Note: The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

    \subsection*{27.5.2 SLEEP AND IDLE MODES}

    If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes the device and code execution continues from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON<3:2>) needs to be cleared in software after the device wakes up.

    \subsection*{27.5.3 ENABLING WDT}

    The WDT is enabled or disabled by the FWDTEN<1:0> Configuration bits in the FWDT Configuration register. When the FWDTEN<1:0> Configuration bits are set, the WDT is always enabled.
    The WDT can be optionally controlled in software when the FWDTENx Configuration bits have been programmed to ' 00 '. The WDT is enabled in software by setting the SWDTEN control bit ( \(\mathrm{RCON}<5>\) ). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.
    The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

    \subsection*{27.5.4 WDT WINDOW}

    The Watchdog Timer has an optional Windowed mode enabled by programming the WINDIS bit in the WDT Configuration register (FWDT<7>). In the Windowed mode (WINDIS = 0), the WDT should be cleared based on the settings in the programmable Watchdog Timer Window (WDTWIN<1:0>) select bits.

    \section*{FIGURE 27-2: WDT BLOCK DIAGRAM}
    

    \subsection*{27.6 In-Circuit Serial Programming}

    The dsPIC33EVXXXGM00X/10X family devices can be serially programmed while in the end application circuit. This is done with two lines for clock and data, and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to "dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits" (DS70663) for details about In-Circuit Serial Programming \({ }^{\text {TM }}\) (ICSP \({ }^{\text {TM }}\) ).

    Any of the following three pairs of programming clock/ data pins can be used:
    - PGEC1 and PGED1
    - PGEC2 and PGED2
    - PGEC3 and PGED3

    \subsection*{27.7 In-Circuit Debugger}

    When MPLAB \({ }^{\circledR}\) ICD 3 or REAL ICE \({ }^{\text {TM }}\) is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB X IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

    Any of the following three pairs of debugging clock/data pins can be used:
    - PGEC1 and PGED1
    - PGEC2 and PGED2
    - PGEC3 and PGED3

    To use the in-circuit debugger function of the device, the design must implement ICSP connections to \(\overline{M C L R}\), VDd, Vss and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins (PGECx and PGEDx).

    \subsection*{27.8 Code Protection and CodeGuard \({ }^{\text {TM }}\) Security}

    The dsPIC33EVXXXGM00X/10X family devices offer Intermediate CodeGuard Security that supports General Segment (GS) security, Boot Segment (BS) security and Configuration Segment (CS) security. This feature helps protect individual Intellectual Properties.

    Note: Refer to "CodeGuard \({ }^{\text {TM }}\) Intermediate Security" (DS70005182) in the "dsPIC33/ PIC24 Family Reference Manual" for further information on usage, configuration and operation of CodeGuard Security.

    \subsection*{28.0 INSTRUCTION SET SUMMARY}

    Note: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

    The dsPIC33EV instruction set is almost identical to that of the dsPIC30F and dsPIC33F.
    Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.
    Each single-word instruction is a 24 -bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.
    The instruction set is highly orthogonal and is grouped into following five basic categories:
    - Word or byte-oriented operations
    - Bit-oriented operations
    - Literal operations
    - DSP operations
    - Control operations

    Table 28-1 lists the general symbols used in describing the instructions.
    The dsPIC33E instruction set summary in Table 28-2 lists all the instructions, along with the Status Flags affected by each instruction.
    Most word or byte-oriented W register instructions (including barrel shift instructions) have the following three operands:
    - The first source operand, which is typically a register 'Wb' without any address modifier
    - The second source operand, which is typically a register 'Ws' with or without an address modifier
    - The destination of the result, which is typically a register 'Wd' with or without an address modifier
    However, word or byte-oriented file register instructions have two operands:
    - The file register specified by the value ' \(f\) '
    - The destination, which could be either the file register ' \(f\) ' or the W0 register, which is denoted as 'WREG'

    Most bit-oriented instructions (including simple rotate/ shift instructions) have two operands:
    - The W register (with or without an address modifier) or file register (specified by the value of 'Ws' or ' \(f\) ')
    - The bit in the W register or file register (specified by a literal value or indirectly by the contents of register ' Wb ')

    The literal instructions that involve data movement can use some of the following operands:
    - A literal value to be loaded into a W register or file register (specified by ' \(k\) ')
    - The W register or file register where the literal value is to be loaded (specified by 'Wb' or ' \(f\) ')
    However, literal instructions that involve arithmetic or logical operations use some of the following operands:
    - The first source operand, which is a register 'Wb' without any address modifier
    - The second source operand, which is a literal value
    - The destination of the result (only if not the same as the first source operand), which is typically a register 'Wd' with or without an address modifier
    The MAC class of DSP instructions can use some of the following operands:
    - The accumulator (A or B) to be used (required operand)
    - The W registers to be used as the two operands
    - The \(X\) and \(Y\) address space prefetch operations
    - The \(X\) and \(Y\) address space prefetch destinations
    - The accumulator write-back destination

    The other DSP instructions do not involve any multiplication and can include:
    - The accumulator to be used (required)
    - The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
    - The amount of shift specified by a W register 'Wn' or a literal value
    The control instructions can use some of the following operands:
    - A program memory address
    - The mode of the Table Read and Table Write instructions

    Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are ' 0 's. If this second word is executed as an instruction (by itself), it executes as a NOP.
    The double-word instructions execute in two instruction cycles.

    Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed. In these cases, the execution takes multiple instruction
    cycles with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or twoword instruction. Moreover, double-word moves require two cycles.

    Note: For more details on the instruction set, refer to the "16-bit MCU and DSC Programmer's Reference Manual" (DS70157).

    TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS
    \begin{tabular}{|c|c|}
    \hline Field & Description \\
    \hline \#text & Means literal defined by "text" \\
    \hline (text) & Means "content of text" \\
    \hline [text] & Means "the location addressed by text" \\
    \hline \{ \} & Optional field or operation \\
    \hline \(a \in\{b, c, d\}\) & \(a\) is selected from the set of values b, c, d \\
    \hline <n:m> & Register bit field \\
    \hline .b & Byte mode selection \\
    \hline .d & Double-Word mode selection \\
    \hline . S & Shadow register select \\
    \hline .w & Word mode selection (default) \\
    \hline Acc & One of two accumulators \(\{\mathrm{A}, \mathrm{B}\}\) \\
    \hline AWB & Accumulator Write-Back Destination Address register \(\in\{W\) 13, [W13]+ = 2 \(\}\) \\
    \hline bit4 & 4-bit bit selection field (used in word-addressed instructions) \(\in\{0 . . .15\}\) \\
    \hline C, DC, N, OV, Z & MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero \\
    \hline Expr & Absolute address, label or expression (resolved by the linker) \\
    \hline f & File register address \(\in\{0 \times 0000 \ldots 0 \times 1 \mathrm{FFF}\}\) \\
    \hline lit1 & 1-bit unsigned literal \(\in\{0,1\}\) \\
    \hline lit4 & 4-bit unsigned literal \(\in\{0 \ldots 15\}\) \\
    \hline lit5 & 5 -bit unsigned literal \(\in\{0 \ldots 31\}\) \\
    \hline lit8 & 8-bit unsigned literal \(\in\{0 . . .255\}\) \\
    \hline lit10 & 10-bit unsigned literal \(\in\{0 . . .255\}\) for Byte mode, \(\{0: 1023\}\) for Word mode \\
    \hline lit14 & 14 -bit unsigned literal \(\in\{0 . . .16384\}\) \\
    \hline lit16 & 16 -bit unsigned literal \(\in\{0 . . .65535\}\) \\
    \hline lit23 & 23-bit unsigned literal \(\in\{0 \ldots .8388608\}\); LSb must be '0' \\
    \hline None & Field does not require an entry, can be blank \\
    \hline OA, OB, SA, SB & DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate \\
    \hline PC & Program Counter \\
    \hline Slit10 & 10-bit signed literal \(\in\{-512 . .511\}\) \\
    \hline Slit16 & 16-bit signed literal \(\in\{-32768 \ldots 32767\}\) \\
    \hline Slit6 & 6 -bit signed literal \(\in\{-16 \ldots 16\}\) \\
    \hline Wb & Base W register \(\in\{\) W0...W15\} \\
    \hline Wd & Destination W register \(\in\{\mathrm{Wd}\), [Wd], [Wd++], [Wd--], [++Wd], [--Wd] \(\}\) \\
    \hline Wdo & \begin{tabular}{l}
    Destination W register \(\in\) \\
    \{ Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] \}
    \end{tabular} \\
    \hline Wm, Wn & Dividend, Divisor Working register pair (Direct Addressing) \\
    \hline
    \end{tabular}

    TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)
    \begin{tabular}{|c|c|}
    \hline Field & Description \\
    \hline Wm*Wm & Multiplicand and Multiplier Working register pair for Square instructions \(\in\) \{W4 * W4,W5 * W5,W6 * W6, W7 * W7 \} \\
    \hline Wm*Wn & Multiplicand and Multiplier Working register pair for DSP instructions \(\in\) \{W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7\} \\
    \hline Wn & One of 16 Working registers \(\in\{\) W0...W15\} \\
    \hline Wnd & One of 16 Destination Working registers \(\in\{\) W0...W15\} \\
    \hline Wns & One of 16 Source Working registers \(\in\{\) W0...W15\} \\
    \hline WREG & W0 (Working register used in file register instructions) \\
    \hline Ws & Source W register \(\in\{\) Ws, [Ws], [Ws++], [Ws--], [++Ws], [-Ws] \} \\
    \hline Wso & ```
    l}\begin{array}{l}{\mathrm{ Source W register є }}\\{{Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb]}```

