

STW48N60DM2

N-channel 600 V, 0.065 Ω typ., 40 A MDmesh™ DM2 Power MOSFET in a TO-247 package

Datasheet - production data

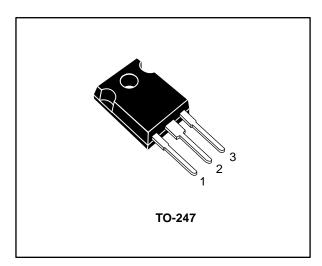
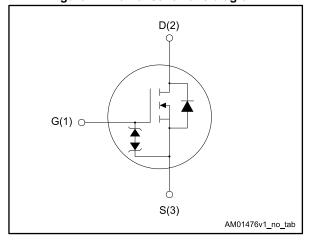


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	Ι _D
STW48N60DM2	600 V	0.079 Ω	40 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

• Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh $^{\text{TM}}$ DM2 fast recovery diode series. It offers very low recovery charge (Qrr) and time (tr) combined with low $R_{\text{DS(on)}}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STW48N60DM2	48N60DM2	TO-247	Tube

Contents STW48N60DM2

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STW48N60DM2 Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit		
V _{GS}	Gate-source voltage	±25	V		
,	Drain current (continuous) at T _{case} = 25 °C	40	۸		
I _D	Drain current (continuous) at T _{case} = 100 °C	25	Α		
I _{DM} ⁽¹⁾	Drain current (pulsed)	160	Α		
P _{TOT}	Total dissipation at T _{case} = 25 °C	300 W			
dv/dt ⁽²⁾	Peak diode recovery voltage slope	50 144			
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50 V/ns			
T _{stg}	Storage temperature	FF to 1F0	°C		
T _j	Operating junction temperature	-55 to 150 °C			

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	0.42	900
R _{thj-amb}	Thermal resistance junction-ambient	50	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (Pulse width limited by T_{jmax})	7	Α
E _{AR}	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	950	mJ

 $^{^{\}left(1\right)}$ Pulse width is limited by safe operating area.

 $^{^{(2)}}$ $I_{SD} \leq$ 40 A, di/dt=900 A/µs; V_{DS} peak < $V_{(BR)DSS},~V_{DD}$ = 400 V.

 $^{^{(3)}}$ V_{DS} \leq 480 V.

Electrical characteristics STW48N60DM2

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			٧
	Zero gate voltage drain	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}$			1	
I _{DSS}	current	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V},$ $T_{case} = 125 \text{ °C}$			100	μΑ
I _{GSS}	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			±5	μΑ
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3	4	5	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 20 A		0.065	0.079	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	3250	•	
C _{oss}	Output capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz}, I_D = 0 \text{ A}$	-	142	ı	pF
C _{rss}	Reverse transfer capacitance			4.5	-	
Coss (1) eq.	Equivalent output capacitance	$V_{DS} = 0$ to 480 V, $V_{GS} = 0$ V	-	258	-	pF
R _G	Intrinsic gate resistance	$f = 1 \text{ MHz}, I_D = 0 \text{ A}$	-	4	ı	Ω
Q_g	Total gate charge		-	70	-	
Q_{gs}	Gate-source charge	V _{DD} = 480 V, I _D = 40 A, V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	18	-	nC
Q_{gd}	Gate-drain charge	,	-	28	-	

Notes:

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time		-	27	-	
t _r	Rise time	$V_{DD} = 300 \text{ V}, I_D = 20 \text{ A R}_G = 4.7 \Omega,$	-	27	ı	
t _{d(off)}	Turn-off delay time	V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times" and)	-	131	1	ns
t _f	Fall time		-	9.8	1	

 $^{^{(1)}}$ $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD} ⁽¹⁾	Source-drain current		-		40	Α
I _{SDM} ⁽²⁾	Source-drain current (pulsed)		ı		160	А
V _{SD} ⁽³⁾	Forward on voltage	V _{GS} = 0 V, I _{SD} = 40 A	ı		1.6	V
t _{rr}	Reverse recovery time		ı	140		ns
Q _{rr}	Reverse recovery charge	I _{SD} = 40 A, di/dt = 100 A/μs, V _{DD} = 60 V (see <i>Figure 15</i> : "Test circuit for inductive	-	0.7		μC
I _{RRM}	Reverse recovery current	load switching and diode recovery times")		10		Α
t _{rr}	Reverse recovery time		1	256		ns
Qrr	Reverse recovery charge	I_{SD} = 40 A, di/dt = 100 A/ μ s, V_{DD} = 60 V, T_{j} = 150 °C (see <i>Figure 15: "Test circuit for inductive load switching and diode</i>	ı	2.5		μC
I _{RRM}	Reverse recovery current	recovery times")	-	20		А

Notes:

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)GSO}	Gate-source breakdown voltage	$I_{GS} = \pm 250 \ \mu A, \ I_{D} = 0 \ A$	±30	-	-	V

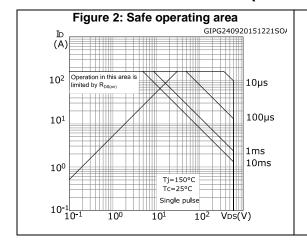
The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

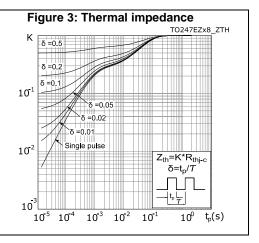
⁽¹⁾Limited by maximum junction temperature

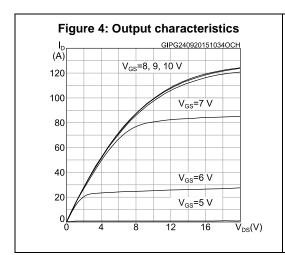
 $^{^{\}left(2\right) }$ Pulse width is limited by safe operating area.

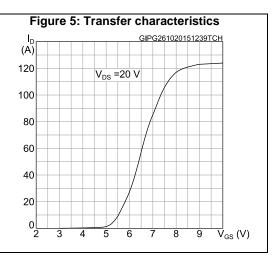
 $^{^{(3)}}$ Pulse test: pulse duration = 300 $\mu s,$ duty cycle 1.5%.

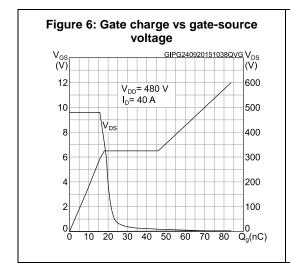
2.2 Electrical characteristics (curves)

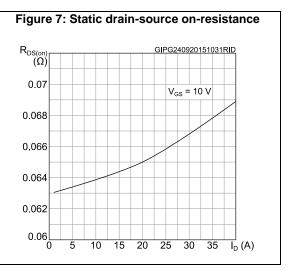












STW48N60DM2 Electrical characteristics

Figure 8: Capacitance variations C (pF) GIPG240920151034CVR 10⁴ C_{ISS} 10³ $\mathsf{C}_{\mathsf{oss}}$ 10² f=1MHz $\mathsf{C}_{\mathsf{RSS}}$ 10¹ 10⁰ V_{DS}(V) 10⁻¹ 10⁰ 10¹ 10²

Figure 9: Normalized gate threshold voltage vs temperature V_{GS(th)} (norm.) GIPG240920151209VTH $I_D = 250 \mu A$ 1.1 1.0 0.9 8.0 0.7 0.6 -75 -25 25 75 125 T_i (°C)

Figure 10: Normalized on-resistance vs temperature

R_{DS(on)} GIPG240920151029RON
(norm.)

2.2

1.8

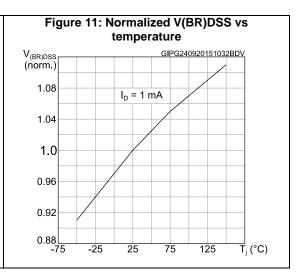
1.4

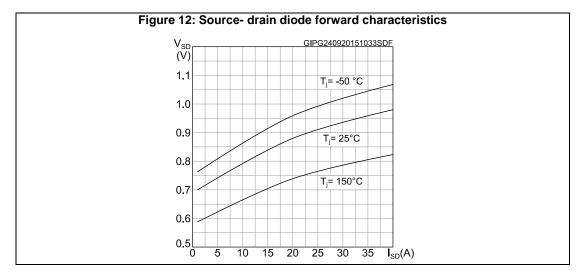
1.0

0.6

0.2

-75
-25
25
75
125
T_j (°C)

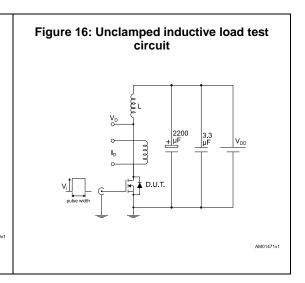


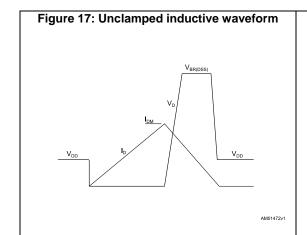


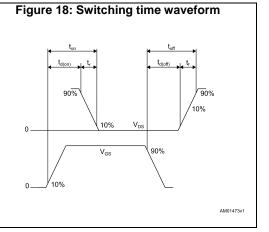
Test circuits STW48N60DM2

3 Test circuits

Figure 13: Test circuit for resistive load switching times







4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 TO-247 package information

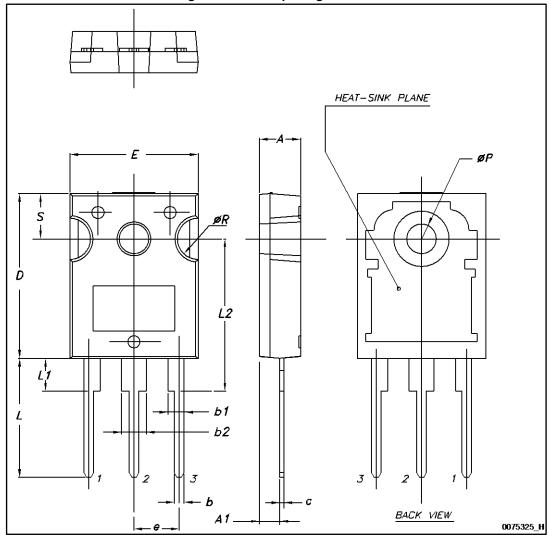


Figure 19: TO-247 package outline

Table 10: TO-247 package mechanical data

Dim	mm.				
Dim.	Min.	Тур.	Max.		
А	4.85		5.15		
A1	2.20		2.60		
b	1.0		1.40		
b1	2.0		2.40		
b2	3.0		3.40		
С	0.40		0.80		
D	19.85		20.15		
Е	15.45		15.75		
е	5.30	5.45	5.60		
L	14.20		14.80		
L1	3.70		4.30		
L2		18.50			
ØP	3.55		3.65		
ØR	4.50		5.50		
S	5.30	5.50	5.70		

STW48N60DM2 Revision history

5 Revision history

Table 11: Document revision history

Date	Revisi on	Changes
21-Oct-2014	1	First release.
29-Oct-2015	2	Document status promoted from preliminary to production data. Modified: title Modified: V _{DS} in cover page Modified: Peak diode recovery voltage slope parameter value and <i>note 2</i> Modified: R _{thj-case} value in <i>Table 3: "Thermal data"</i> Modified: the entire values in <i>Table 4: "Avalanche characteristics"</i> Modified: I _{DSS} , I _{GSS} max values and R _{DS(on)} typical value in <i>Table 5: "Static"</i> Modified: the entire values in <i>Table 6: "Dynamic"</i> , <i>Table 7: "Switching times"</i> and <i>Table 8: "Source-drain diode"</i> Added: <i>Table 9: "Gate-source Zener diode"</i> Added: <i>Section 2.1: "Electrical characteristics (curves)"</i> Minor text changes

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