

# FND43060T2

## Motion SPM<sup>®</sup> 45 Series

### General Description

FND43060T2 is an advanced Motion SPM<sup>®</sup> 45 module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, over-current shutdown, thermal monitoring, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's robust short-circuit-rated IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

### Features

- UL Certified No. E209204 (UL1557)
- 600 V – 30 A 3-Phase IGBT Inverter with Integral Gate Drivers and Protection
- Low Thermal Resistance Using Ceramic Substrate
- Low-Loss, Short-Circuit Rated IGBTs
- Built-In Bootstrap Diodes and Dedicated Vs Pins Simplify PCB Layout
- Built-In NTC Thermistor for Temperature Monitoring
- Separate Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- Single-Grounded Power Supply
- Isolation Rating: 4000 V<sub>rms</sub>/min.
- Remove Dummy Pin

### Applications

- Motion Control – Home Appliance/Industrial Motor

### Related Resources

- [AN-9084](#) – Smart Power Module, Motion SPM<sup>®</sup> 45 H V3 Series User's Guide
- [AN-9072](#) – Smart Power Module, Motion SPM<sup>®</sup> in SPM45H Thermal Performance Information
- [AN-9071](#) – Smart Power Module Motion SPM<sup>®</sup> in SPM45H Mounting Guidance
- [AN-9760](#) – PCB Design Guidance for SPM<sup>®</sup>

### Integrated Power Functions

- 600 V–30 A IGBT inverter for three-phase DC/AC power conversion (Refer to Figure 3)



ON Semiconductor<sup>®</sup>

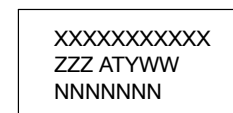
[www.onsemi.com](http://www.onsemi.com)



SPMAA-C26  
CASE MODFC

Figure 1. Package Overview  
(Click to Activate 3D Content)

### MARKING DIAGRAM



XXXX = Specific Device Code  
ZZZ = Lot ID  
AT = Assembly and Test Location  
Y = Year  
WW = Work Week  
NNN = Serial Number

### ORDERING INFORMATION

Device	Package	Shipping
FND43060T2	SPMAA-J26	12 Units/Rail

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## Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: gate drive circuit, high-voltage isolated high-speed level shifting control circuit Under-Voltage Lock-Out (UVLO) protection
- For inverter low-side IGBTs: gate drive circuit, Short-Circuit Protection (SCP) control supply circuit, Under-Voltage Lock-Out (UVLO) protection
- Fault signaling: corresponding to UVLO (low-side supply) and SC faults
- Input interface: active-HIGH interface, works with 3.3/5 V logic, Schmitt-trigger input

## PIN CONFIGURATION

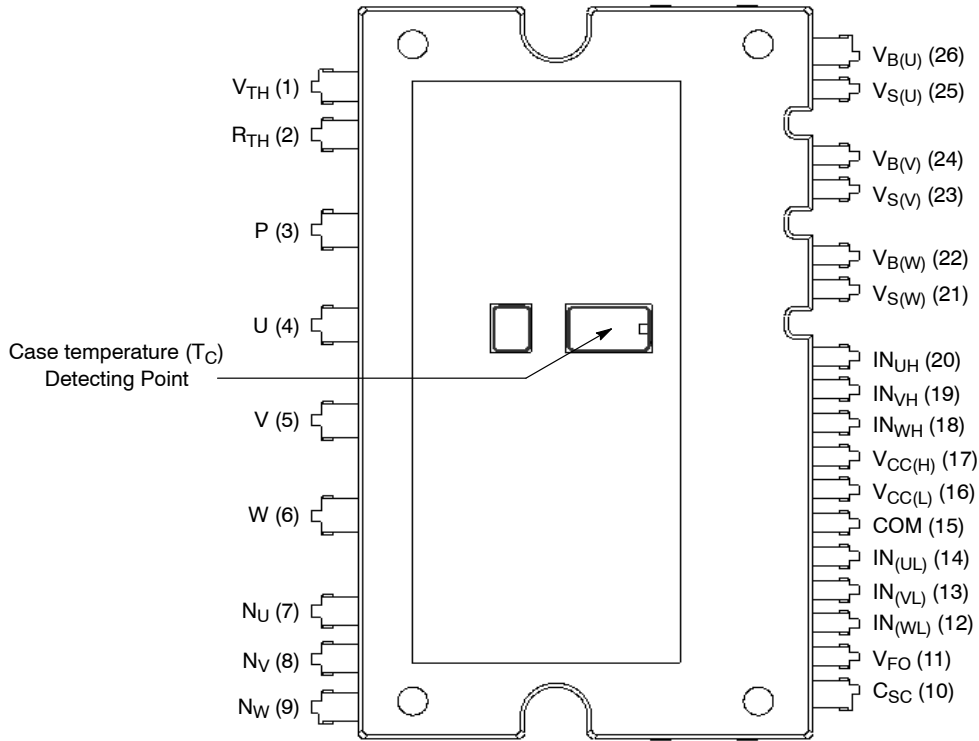


Figure 2. Top View

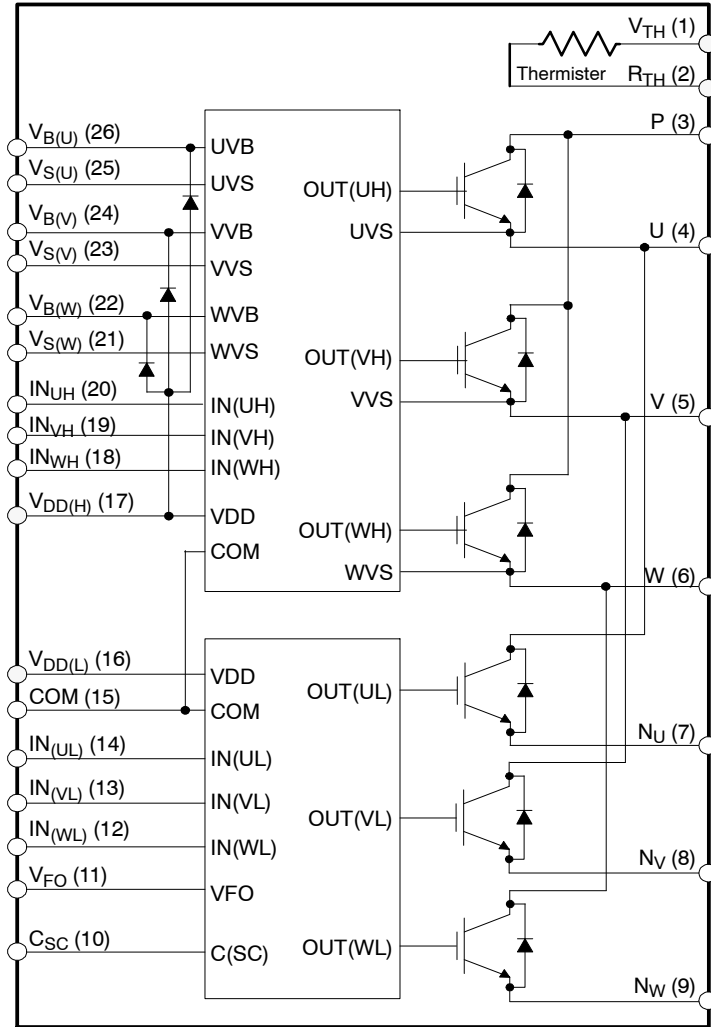
## FND43060T2

### PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Description
1	$V_{TH}$	Thermistor Bias Voltage
2	$R_{TH}$	Series Resistor for the Use of Thermistor (Temperature Detection)
3	P	Positive DC-Link Input
4	U	Output for U-Phase
5	V	Output for V-Phase
6	W	Output for W-Phase
7	$N_U$	Negative DC-Link Input for U-Phase
8	$N_V$	Negative DC-Link Input for V-Phase
9	$N_W$	Negative DC-Link Input for W-Phase
10	$C_{SC}$	Capacitor (Low-Pass Filter) for Short-circuit Current Detection Input
11	$V_{FO}$	Fault Output
12	$IN_{(WL)}$	Signal Input for Low-Side W-Phase
13	$IN_{(VL)}$	Signal Input for Low-Side V-Phase
14	$IN_{(UL)}$	Signal Input for Low-Side U-Phase
15	COM	Common Supply Ground
16	$V_{DD(L)}$	Low-Side Common Bias Voltage for IC and IGBTs Driving
17	$V_{DD(H)}$	High-Side Common Bias Voltage for IC and IGBTs Driving
18	$IN_{(WH)}$	Signal Input for High-Side W-Phase
19	$IN_{(VH)}$	Signal Input for High-Side V-Phase
20	$IN_{(UH)}$	Signal Input for High-Side U-Phase
21	$V_{S(W)}$	High-Side Bias Voltage Ground for W-Phase IGBT Driving
22	$V_{B(W)}$	High-Side Bias Voltage for W-Phase IGBT Driving
23	$V_{S(V)}$	High-Side Bias Voltage Ground for V-Phase IGBT Driving
24	$V_{B(V)}$	High-Side Bias Voltage for V-Phase IGBT Driving
25	$V_{S(U)}$	High-Side Bias Voltage Ground for U-Phase IGBT Driving
26	$V_{B(U)}$	High-Side Bias Voltage for U-Phase IGBT Driving

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## INTERNAL EQUIVALENT CIRCUIT AND INPUT/OUTPUT PINS



### NOTES:

1. Inverter high-side is composed of three IGBTs, freewheeling diodes, and one control IC for each IGBT.
2. Inverter low-side is composed of three IGBTs, freewheeling diodes, and one control IC for each IGBT. It has gate drive and protection functions.
3. Inverter power side is composed of four inverter DC-link input terminals and three inverter output terminals.

**Figure 3. Internal Block Diagram**

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## ABSOLUTE MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Rating	Unit
<b>INVERTER PART</b>				
$V_{PN}$	Supply Voltage	Applied between P-N <sub>U</sub> , N <sub>V</sub> , N <sub>W</sub>	450	V
$V_{PN(\text{Surge})}$	Supply Voltage (Surge)	Applied between P-N <sub>U</sub> , N <sub>V</sub> , N <sub>W</sub>	500	V
$V_{CES}$	Collector-Emitter Voltage		600	V
$\pm I_C$	Each IGBT Collector Current	$T_C = 25^\circ\text{C}$ , $T_J < 150^\circ\text{C}$	30	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	$T_C = 25^\circ\text{C}$ , $T_J < 150^\circ\text{C}$ , Under 1 ms Pulse Width (Note 1)	60	A
$P_C$	Collector Dissipation	$T_C = 25^\circ\text{C}$ per One Chip (Note 1)	59	W
$T_J$	Operating Junction Temperature		-40 ~ 150	$^\circ\text{C}$

## CONTROL PART

$V_{DD}$	Control Supply Voltage	Applied between $V_{DD(H)}$ , $V_{DD(L)}$ - COM	20	V
$V_{BS}$	High-Side Control Bias Voltage	Applied between $V_{B(U)} - V_{S(U)}$ , $V_{B(V)} - V_{S(V)}$ , $V_{B(W)} - V_{S(W)}$	20	V
$V_{IN}$	Input Signal Voltage	Applied between $IN_{(UH)}$ , $IN_{(VH)}$ , $IN_{(WH)}$ , $IN_{(UL)}$ , $IN_{(VL)}$ , $IN_{(WL)}$ - COM	-0.3 ~ $V_{DD}+0.3$	V
$V_{FO}$	Fault Output Supply Voltage	Applied between $V_{FO}$ - COM	-0.3 ~ $V_{DD}+0.3$	V
$I_{FO}$	Fault Output Current	Sink Current at $V_{FO}$ pin	1	mA
$V_{SC}$	Current Sensing Input Voltage	Applied between $C_{SC}$ - COM	-0.3 ~ $V_{DD}+0.3$	V

## BOOTSTRAP DIODE PART

$V_{RRM}$	Maximum Repetitive Reverse Voltage		600	V
$I_F$	Forward Current	$T_C = 25^\circ\text{C}$ , $T_J < 150^\circ\text{C}$	0.50	A
$I_{FP}$	Forward Current (Peak)	$T_C = 25^\circ\text{C}$ , $T_J < 150^\circ\text{C}$ , Under 1 ms Pulse Width (Note 1)	2.0	A
$T_J$	Operating Junction Temperature		-40 ~ 150	$^\circ\text{C}$

## TOTAL SYSTEM

$V_{PN(\text{PROT})}$	Self-Protection Supply Voltage Limit (Short-Circuit Protection Capability)	$V_{DD} = V_{BS} = 13.5\text{ V} \sim 16.5\text{ V}$ $T_J = 150^\circ\text{C}$ , Non-repetitive, $< 2\ \mu\text{s}$	400	V
$T_C$	Module Case Operation Temperature	See Figure 2	-40 ~ 125	$^\circ\text{C}$
$T_{STG}$	Storage Temperature		-40 ~ 125	$^\circ\text{C}$
$V_{ISO}$	Isolation Voltage	60 Hz, Sinusoidal, AC 1 minute, Connect Pins to Heat Sink Plate (Note 3)	2000	$V_{rms}$

## THERMAL RESISTANCE

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance (Note 2)	Inverter IGBT Part (per 1/6 module)	-	-	2.1	$^\circ\text{C}/\text{W}$
$R_{th(j-c)F}$		Inverter FWDi Part (per 1/6 module)	-	-	2.8	$^\circ\text{C}/\text{W}$

1. These values had been made an acquisition by the calculation considered to design factor.
2. For the measurement point of case temperature ( $T_C$ ), please refer to Figure 2.
3. For Recommended Heat-Sink Design, please see Figure 11. If do not follow Recommended, Viso is 2000 Vrms.

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## ELECTRICAL CHARACTERISTICS – INVERTER PART ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{CE(SAT)}$	Collector – Emitter Saturation Voltage	$V_{DD} = V_{BS} = 15\text{ V}$ , $V_{IN} = 5\text{ V}$	-	1.65	2.25	V
$V_F$	FWDi Forward Voltage	$V_{IN} = 0\text{ V}$	-	2.00	2.60	V
HS	$t_{ON}$	Switching Times $V_{PN} = 300\text{ V}$ , $V_{DD} = V_{BS} = 15\text{ V}$ , $I_C = 30\text{ A}$ , $T_J = 25^\circ\text{C}$ $V_{IN} = 0\text{ V} \leftrightarrow 5\text{ V}$ , Inductive Load (Note 4)	0.45	0.85	1.35	$\mu\text{s}$
			-	0.20	0.50	$\mu\text{s}$
			-	0.70	1.20	$\mu\text{s}$
			-	0.15	0.45	$\mu\text{s}$
			-	0.10	-	$\mu\text{s}$
LS	$t_{ON}$	$V_{PN} = 300\text{ V}$ , $V_{DD} = V_{BS} = 15\text{ V}$ , $I_C = 30\text{ A}$ , $T_J = 25^\circ\text{C}$ $V_{IN} = 0\text{ V} \leftrightarrow 5\text{ V}$ , Inductive Load (Note 4)	0.5	0.90	1.40	$\mu\text{s}$
			-	0.30	0.60	$\mu\text{s}$
			-	0.80	1.30	$\mu\text{s}$
			-	0.15	0.45	$\mu\text{s}$
			-	0.15	-	$\mu\text{s}$
$I_{CES}$	Collector-Emitter Leakage Current	$V_{CE} = V_{CES}$	-	-	1	mA

4.  $t_{ON}$  and  $t_{OFF}$  include the propagation delay of the internal drive IC.  $t_{C(ON)}$  and  $t_{C(OFF)}$  are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 4.

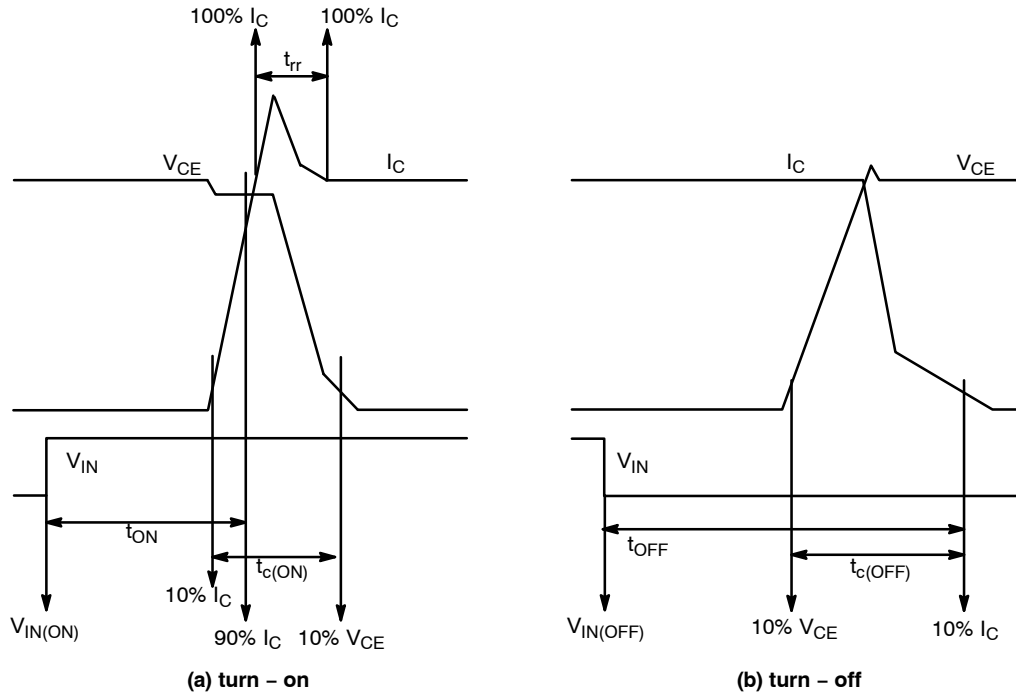


Figure 4. Switching Time Definition

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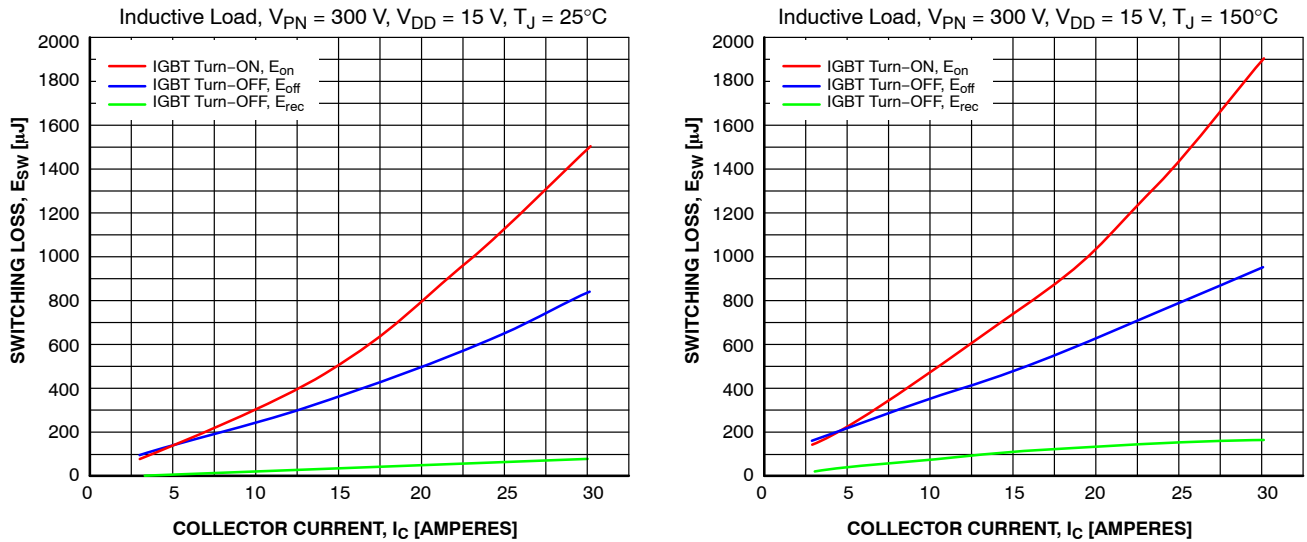


Figure 5. Switching Loss Characteristics (Typical)

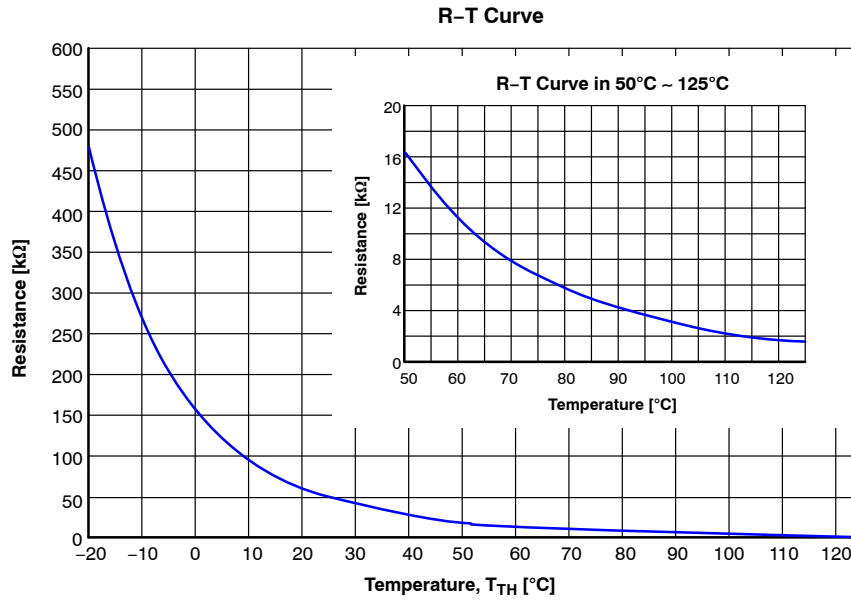
## CONTROL PART

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
I <sub>QDDH</sub>	Quiescent V <sub>DD</sub> Supply Current	V <sub>DD(H)</sub> = 15 V, I <sub>N(UH,VH,WH)</sub> = 0 V	V <sub>DD(H)</sub> - COM	-	-	0.10	mA
I <sub>QDDL</sub>		V <sub>DD(L)</sub> = 15 V, I <sub>N(UL,VL,WL)</sub> = 0 V	V <sub>DD(L)</sub> - COM	-	-	2.65	mA
I <sub>PDDH</sub>	Operating V <sub>DD</sub> Supply Current	V <sub>DD(H)</sub> = 15 V, f <sub>PWM</sub> = 20 kHz, duty = 50%, Applied to one PWM Signal Input for High-Side	V <sub>DD(H)</sub> - COM	-	-	0.15	mA
I <sub>PDDL</sub>		V <sub>DD(L)</sub> = 15 V, f <sub>PWM</sub> = 20 kHz, duty = 50%, Applied to one PWM Signal Input for Low-Side	V <sub>DD(L)</sub> - COM	-	-	4.00	mA
I <sub>QBS</sub>	Quiescent V <sub>BS</sub> Supply Current	V <sub>BS</sub> = 15 V, I <sub>N(UH,VH,WH)</sub> = 0 V	V <sub>B(U)</sub> - V <sub>S(U)</sub> , V <sub>B(V)</sub> - V <sub>S(V)</sub> , V <sub>B(W)</sub> - V <sub>S(W)</sub>	-	-	0.30	mA
I <sub>PBS</sub>	Operating V <sub>BS</sub> Supply Current	V <sub>DD</sub> = V <sub>BS</sub> = 15 V, f <sub>PWM</sub> = 20 kHz, duty = 50%, Applied to one PWM Signal Input for High-Side	V <sub>B(U)</sub> - V <sub>S(U)</sub> , V <sub>B(V)</sub> - V <sub>S(V)</sub> , V <sub>B(W)</sub> - V <sub>S(W)</sub>	-	-	2.00	mA
V <sub>FOH</sub>	Fault Output Voltage	V <sub>SC</sub> = 0 V, V <sub>FO</sub> Circuit: 4.7 kΩ to 5 V Pull-up		4.5	-	-	V
V <sub>FOL</sub>		V <sub>SC</sub> = 1 V, V <sub>FO</sub> Circuit: 4.7 kΩ to 5 V Pull-up		-	-	0.5	V
V <sub>SC(ref)</sub>	Short Circuit Trip Level	V <sub>DD</sub> = 15 V (Note 5)	C <sub>SC</sub> -COM	0.45	0.50	0.55	V
UV <sub>DDD</sub>	Supply Circuit Under-Voltage Protection	Detection Level		10.5	-	13.0	V
UV <sub>DDR</sub>		Reset Level		11.0	-	13.5	V
UV <sub>BSD</sub>		Detection Level		10.0	-	12.5	V
UV <sub>BSR</sub>		Reset Level		10.5	-	13.0	V
t <sub>FOD</sub>	Fault-Out Pulse Width			30	-	-	μs
V <sub>IN(ON)</sub>	ON Threshold Voltage	Applied between I <sub>N(UH)</sub> , I <sub>N(VH)</sub> , I <sub>N(WH)</sub> , I <sub>N(UL)</sub> , I <sub>N(VL)</sub> , I <sub>N(WL)</sub> - COM		-	-	2.6	V
V <sub>IN(OFF)</sub>	OFF Threshold Voltage			0.8	-	-	V
R <sub>TH</sub>	Resistance of Thermistor	@ T <sub>TH</sub> = 25°C (Note 6)		-	47	-	kΩ
		@ T <sub>TH</sub> = 100°C		-	2.9	-	kΩ

5. Short-circuit current protection os functioning only at the low-sides.

6. T<sub>TH</sub> is the temperature of thermister itself. To know case temperature (T<sub>C</sub>), please make the experiment considering your application.

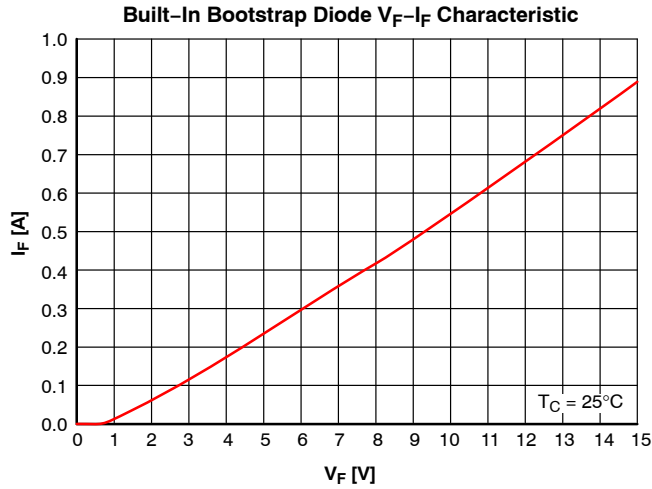
# FND43060T2



**Figure 6. R-T Curve of the Built-In Thermistor**

## BOOTSTRAP DIODE PART

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_F$	Forward Voltage	$I_F = 0.1 \text{ A}$ , $T_C = 25^\circ\text{C}$	-	2.5	-	V
$t_{rr}$	Reverse-Recovery Time	$I_F = 0.1 \text{ A}$ , $dI_F/dt = 50 \text{ A}/\mu\text{s}$ , $T_J = 25^\circ\text{C}$	-	80	-	ns



NOTE: Built-in bootstrap diode includes around 15  $\Omega$  resistance characteristic.

**Figure 7. Built-In Bootstrap Diode Characteristics**

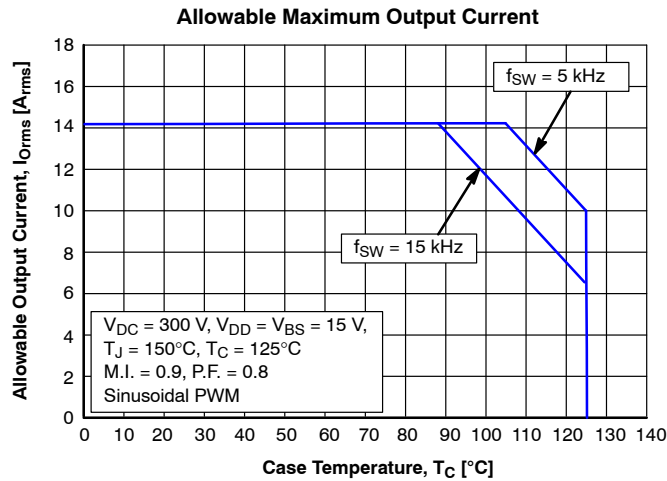


# FND43060T2

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{PN}$	Supply Voltage	Applied between P – $N_U$ , $N_V$ , $N_W$	–	300	400	V
$V_{DD}$	Control Supply Voltage	Applied between $V_{DD(H)}$ – COM, $V_{DD(L)}$ – COM	13.5	15.0	16.5	V
$V_{BS}$	High-Side Bias Voltage	Applied between $V_{B(U)}$ – $V_{S(U)}$ , $V_{B(V)}$ – $V_{S(V)}$ , $V_{B(W)}$ – $V_{S(W)}$	13.0	15.0	18.5	V
$dV_{DD}/dt$ , $dV_{BS}/dt$	Control Supply Variation		–1	–	1	V/ $\mu$ s
$t_{dead}$	Blanking Time for Preventing Arm-Short	For Each Input Signal	1.0	–	–	$\mu$ s
$f_{PWM}$	PWM Input Signal	$-40^{\circ}\text{C} \leq T_C \leq 150^{\circ}\text{C}$ , $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$	–	–	20	kHz
$V_{SEN}$	Voltage for Current Sensing	Applied between $N_U$ , $N_V$ , $N_W$ – COM (Including Surge Voltage)	–4	–	4	V
$PW_{IN(ON)}$	Minimum Input Pulse Width	$V_{DD} = V_{BS} = 15\text{ V}$ , $I_C \leq 60\text{ A}$ , Wiring Inductance between $N_U$ , $N_V$ , $N_W$ and DC Link N < 10 nH (Note 7)	1.2	–	–	$\mu$ s
$PW_{IN(OFF)}$			1.2	–	–	
$T_J$	Junction Temperature		–40	–	150	$^{\circ}\text{C}$

7. This product might not make response if input pulse width is less than the recommended value.



NOTE: This allowable output current value is the reference data for the safe operation of this product. This may be different from the actual application and operating condition

**Figure 8. Allowable Maximum Output Current**

## MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Conditions	Value			Unit	
		Min.	Typ.	Max.		
Device Flatness	See Figure 9	0	–	+120	$\mu\text{m}$	
Mounting Torque	Mounting Screw: M3 See Figure 10	Recommended 0.7 N•m	0.6	0.7	0.8	N•m
		Recommended 7.1 kg•cm	6.2	7.1	8.1	kg•cm
Weight		–	11.00	–	g	

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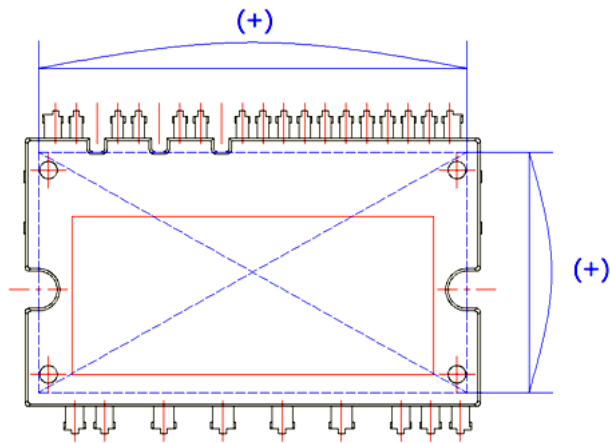


Figure 9. Flatness Measurement Position

Pre-Screwing: 1 à 2  
Final Screwing: 2 à 1

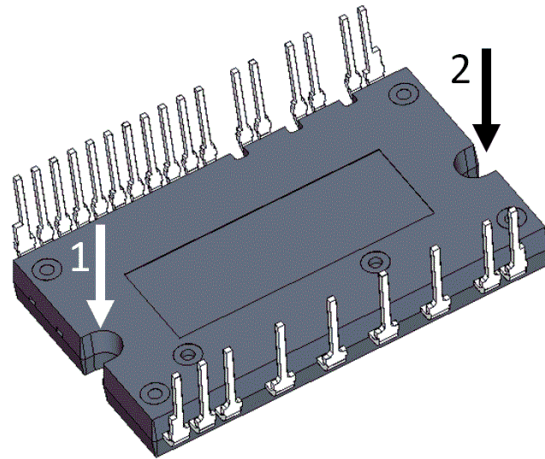


Figure 10. Mounting Screws Torque Order

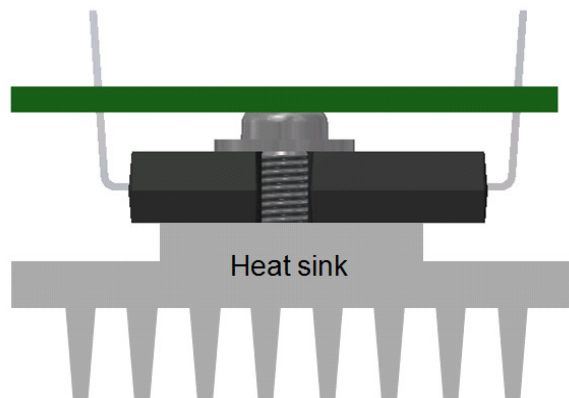
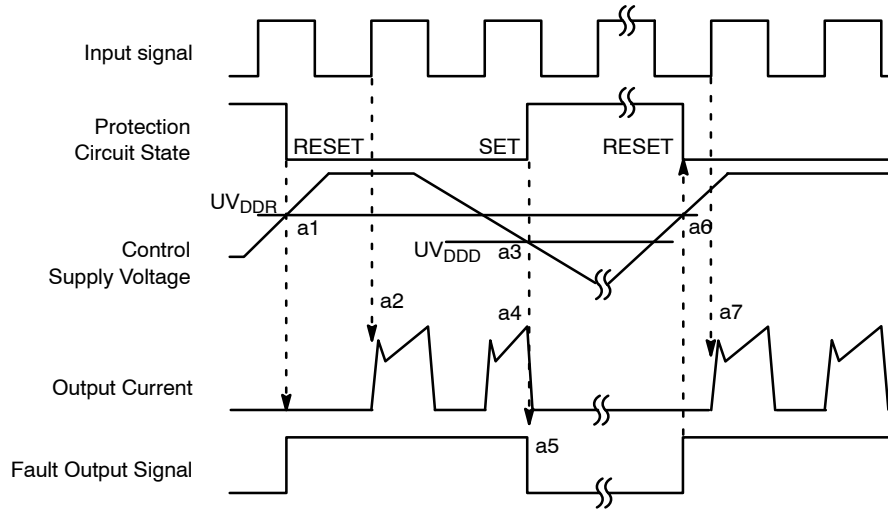


Figure 11. Recommended Heat-Sink Design

## NOTES:

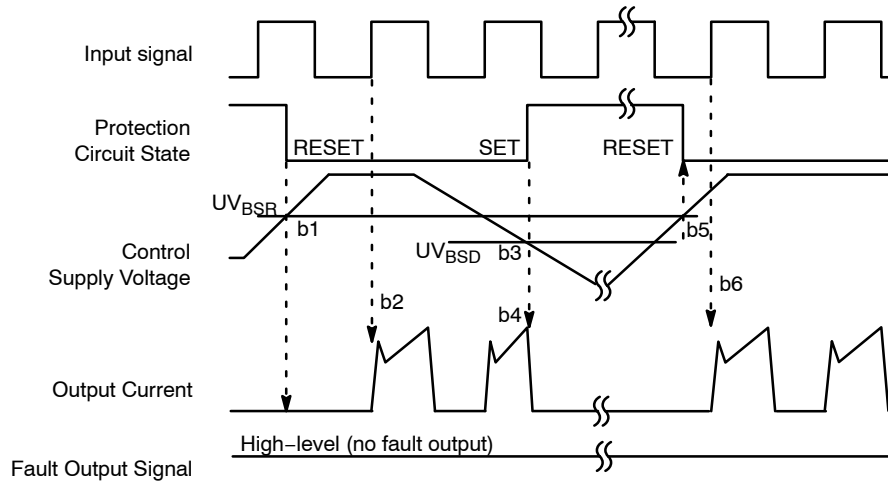
8. Do not make over torque when mounting screws. Much mounting torque may cause ceramic cracks, as well as bolts and Al heat-sink destruction.
9. Avoid one side tightening stress. Figure 10 shows the recommended torque order for mounting screws. Uneven mounting can cause the ceramic substrate of the SPM<sup>®</sup> 45 package to be damaged. The pre-screwing torque is set to 20 ~ 30% of maximum torque rating.

TIME CHARTS OF PROTECTIVE FUNCTION



- a1: Control supply voltage rises: after the voltage rises  $UV_{DDR}$ , the circuits start to operate when next input is applied.
- a2: Normal operation: IGBT ON and carrying current.
- a3: Under voltage detection ( $UV_{DDD}$ ).
- a4: IGBT OFF in spite of control input condition.
- a5: Fault output operation starts.
- a6: Under voltage reset ( $UV_{DDR}$ ).
- a7: Normal operation: IGBT ON and carrying current.

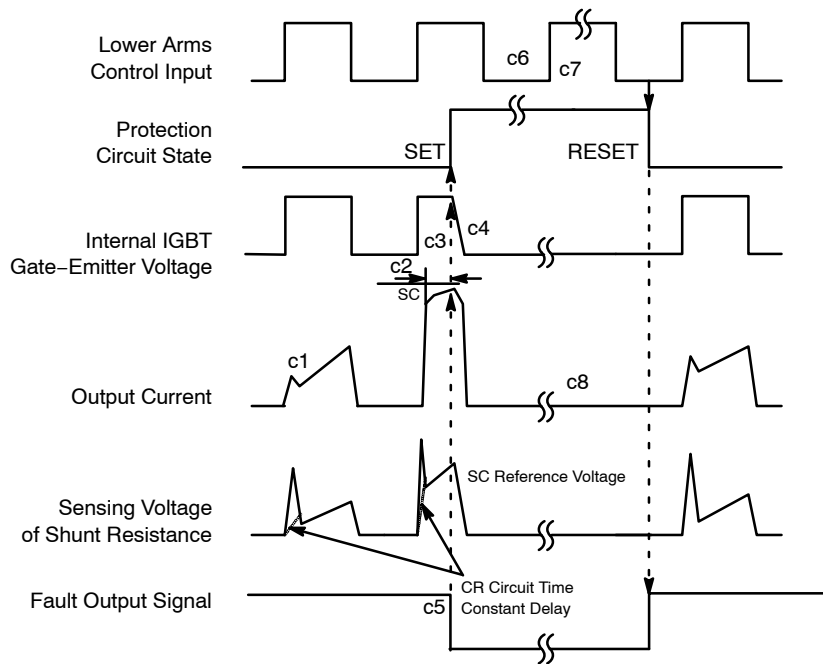
Figure 12. Under-Voltage Protection (Low-Side)



- b1: Control supply voltage rises: after the voltage reaches  $UV_{BSR}$ , the circuits start to operate when next input is applied.
- b2: Normal operation: IGBT ON and carrying current.
- b3: Under voltage detection ( $UV_{BSD}$ ).
- b4: IGBT OFF in spite of control input condition, but there is no fault output signal.
- b5: Under voltage reset ( $UV_{BSR}$ ).
- b6: Normal operation: IGBT ON and carrying current..

Figure 13. Under-Voltage Protection (High-Side)

## FND43060T2

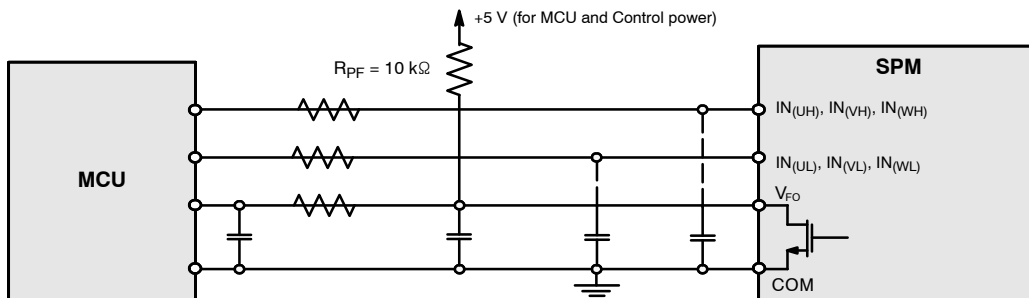


(with the external sense resistance and CR connection)

- c1: Normal operation: IGBT ON and carrying current.
- c2: Short-circuit current detection (SC trigger).
- c3: Hard IGBT gate interrupt.
- c4: IGBT turns OFF.
- c5: Input "LOW": IGBT OFF state.
- c6: Input "HIGH": IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.
- c7: IGBT OFF state.
- c8: Normal operation: IGBT ON and carrying current.

**Figure 14. Short-Circuit Protection (Low-Side Operation Only)**

### INPUT/OUTPUT INTERFACE CIRCUIT

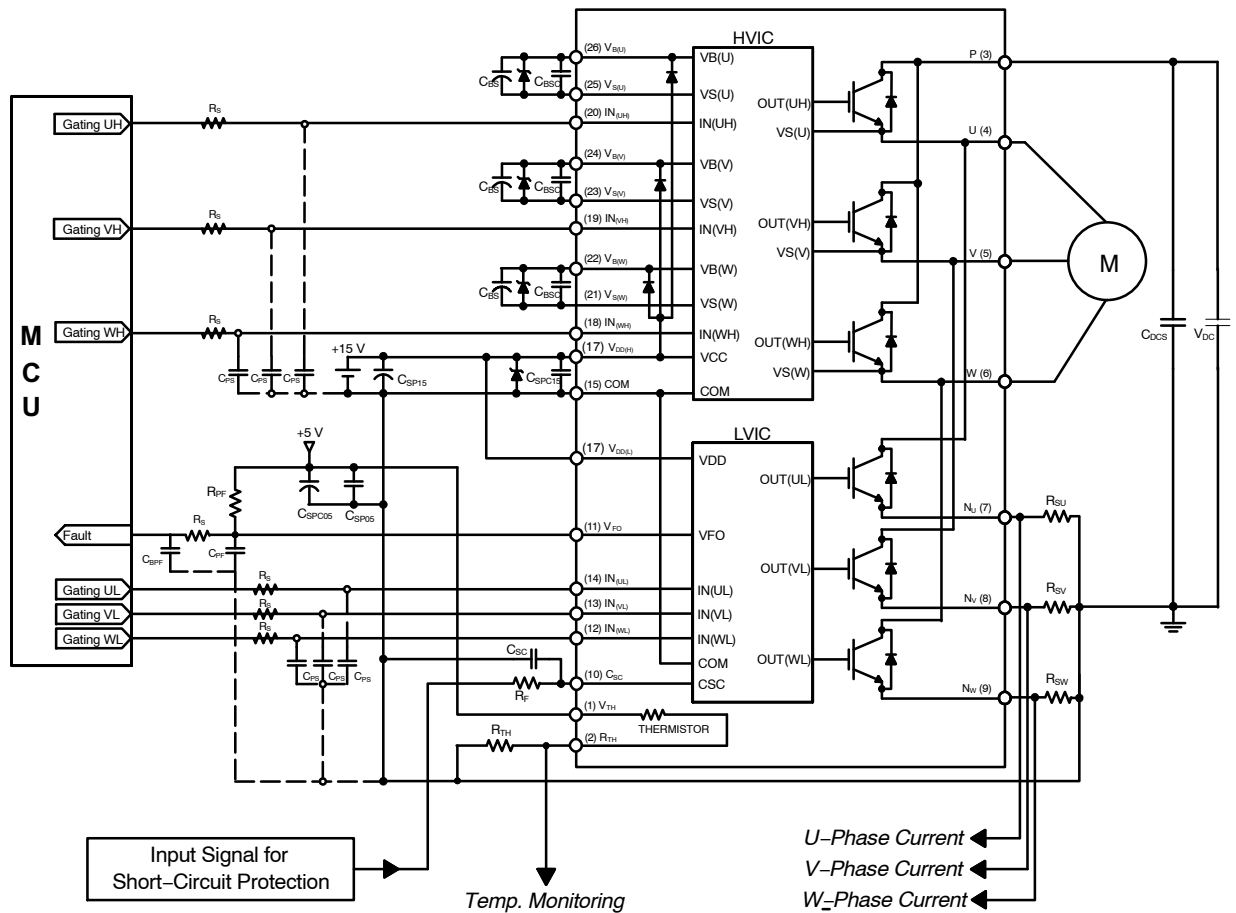


NOTE:

10. RC coupling at each input (parts shown dotted) might change depending on the PWM control scheme in the application and the wiring impedance of the application's printed circuit board. The input signal section of the Motion SPM<sup>®</sup> 45 product integrates a 5 kΩ (typ.) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the signal voltage drop at input terminal.

**Figure 15. Recommended MCU I/O Interface Circuit**

# FND4306T2



## NOTES:

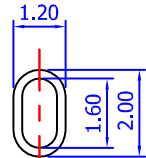
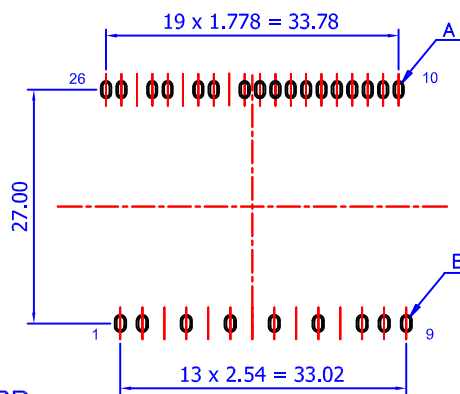
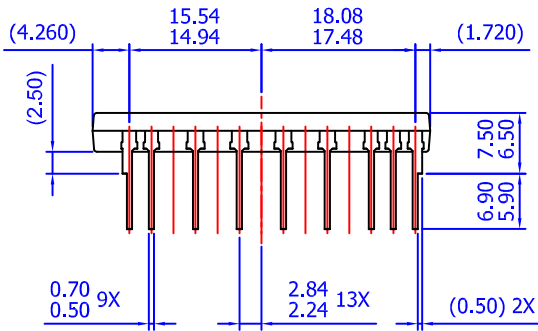
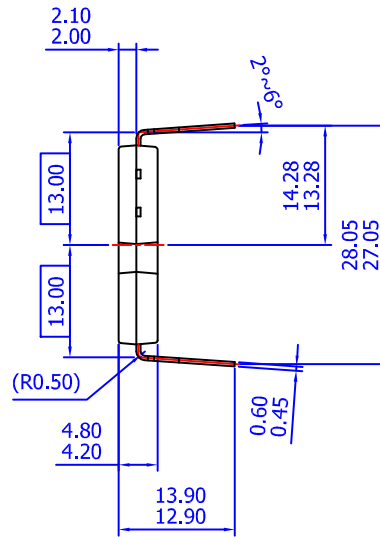
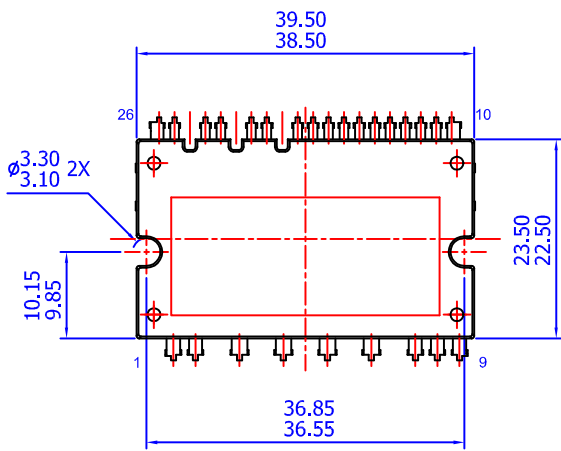
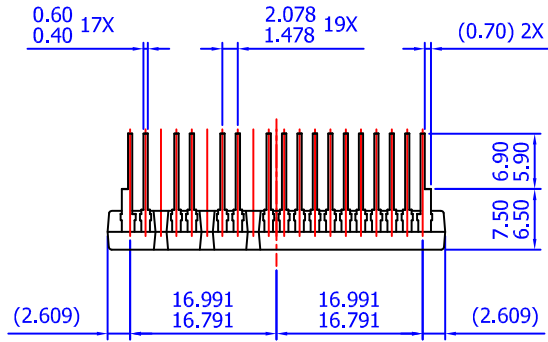
11. To avoid malfunction, the wiring of each input should be as short as possible. (less than 2–3 cm).
12.  $V_{FO}$  output is open–drain type. The signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes  $I_{FO}$  up to 1 mA.
13.  $C_{SP15}$  of around seven times larger than bootstrap capacitor  $C_{BS}$  is recommended.
14. Input signal is active–HIGH type. There is a 5 k $\Omega$  resistor inside the IC to pull–down each input signal line to GND. RC coupling circuits is recommended for the prevention of input signal oscillation.  $R_S C_{PS}$  time constant should be selected in the range 50 ~ 150 ns (recommended  $R_S = 100 \Omega$ ,  $C_{PS} = 1 \text{ nF}$ ).
15. To prevent errors of the protection function, the wiring around  $R_F$  and  $C_{SC}$  should be as short as possible
16. In the short–circuit protection circuit, please select the  $R_F C_{SC}$  time constant in the range 1.5 ~ 2  $\mu\text{s}$ . Do enough evaluation on the real system because short–circuit protection time may vary wiring pattern layout and value of the  $R_F C_{SC}$  time constant.
17. The connection between control GND line and power GND line which includes the  $N_U$ ,  $N_V$ ,  $N_W$  must be connected to only one point. Please do not connect the control GND to the power GND by the broad pattern. Also, the wiring distance between control GND and power GND should be as short as possible.
18. Each capacitor should be mounted as close to the pins of the Motion SPM 45 product as possible.
19. To prevent surge destruction, the wiring between the smoothing capacitor and the P & GND pins should be as short as possible. The use of a high–frequency non–inductive capacitor of around 0.1 ~ 0.22  $\mu\text{s}$  between the P and GND pins is recommended.
20. Relays are used in almost every systems of electrical equipment in home appliances. In these cases, there should be sufficient distance between the MCU and the relays.
21. The zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (recommended zener diode is 22 V/1 W. which has the lower zener impedance characteristic than about 15  $\Omega$ ).
22. Please choose the electrolytic capacitor with good temperature characteristic in  $C_{BS}$ . Also choose 0.1 ~ 0.2  $\mu\text{F}$  R–category ceramic capacitors with good temperature and frequency characteristics in  $C_{BSC}$ .

**Figure 16. Typical Application Circuit**

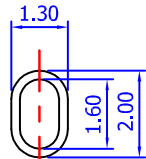
# FND43060T2

## PACKAGE DIMENSIONS

SPMAA-C26 / 26LD, PDD STD CERAMIC TYPE, LONG LEAD DUAL FORM TYPE  
CASE MODFC  
ISSUE O



DETAIL A  
(SCALE N/A)




DETAIL B  
(SCALE N/A)

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