Product introduction

SN74LVC1G00 is a 2-input NAND integrated circuit, which can realize the mathematical logic operation of $Y=\overline{A}+\overline{B}$ and $Y=\overline{A*B}$. Advanced CMOS process design is adopted, which has the working characteristics of low power consumption and high output driving capability. The chip can work normally when the power supply voltage VCC is between 1.65V and 5.5V V. And 74LVC1G00 has a variety of small package shapes,It can be widely used in high-end precision instruments, miniaturized low-power handheld devices, artificial intelligence and other fields.

Product features

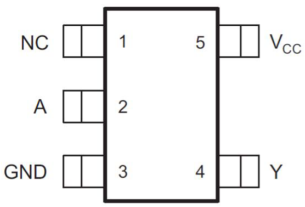
- Low input current: 0.1uA typical
- Low static power consumption: 0.1uA typical
- High output drive: VCC=4.5V, more than 32MA
- Wide working voltage range: 1.65V to 5.5V
- Package form: DBV/DCK/DRL/YZP/ DRY/DSF/ DPW

product usage

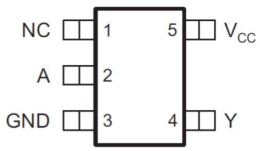
- Portable audio interface
- digital television
- Wireless headphones, smart watches, etc.
- Blu-ray player and home theater
- Solid state drive
- Smart wearable devices

Package form and pin function definition

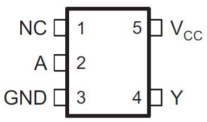
SOT23-5
DBV PACKAGE
(TOP VIEW)



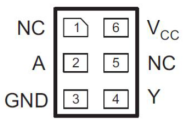
SC70-5
DCK PACKAGE
(TOP VIEW)



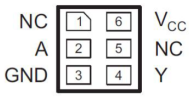
SOT-553
DRL PACKAGE
(TOP VIEW)



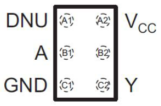
SOT-886
DRY PACKAGE
(TOP VIEW)



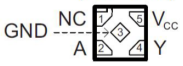
SON-6
DSF PACKAGE
(TOP VIEW)



DSBGA-5
YZP PACKAGE
(TOP VIEW)



X2SON-5
DPW PACKAGE
(TOP VIEW)



	Pin				
Name	DBV/ DCK/ DRL	DRY/DSF	YZP	DPW	Description
NC	1	1,5	A1, B2	1	Empty foot
A	2	2	B1	2	Input
GND	3	3	C1	3	Power supply ground
Y	4	4	C2	4	Output
VCC	5	6	A2	5	Power supply positive

Note: NC null pin, no connecting wire inside.

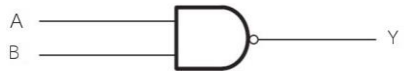
Limit parameter

parameter	symbol	limit value	unit
operating voltage	V_{CC}	6.5	V
input	V_{IN}	-0.5~6.5	V
Output voltage (1)	V_{OUT}	-0.5~6.5	V
Single pin output current	I_{OUT}	25	mA
Or Vcc current.	I_{CC}	50	mA
Storage temperature	T_S	-65-150	℃
Pin welding temperature	T_W	260,10s	℃

Note: 1. In the power-off state of VCC=0V, the limit voltage that the output can bear,

2. Limit parameter refers to the limit value that can't be exceeded under any conditions. If it exceeds this limit value, it may cause physical damage such as product deterioration; At the same time, the chip can't work normally when it is close to the limit parameters.

Principle logic diagram



truth table

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

working conditions

project	symbol	test condition	minimum value	typical value	maximum	unit
operating voltage	VC	-	1.65	-	5.5	V
Input high level voltage	VHI	VC =1.65V~1.95V	0.65* VC	-	-	V
		VC =2.3V~2.7V	1.7V	-	-	
		VC =3V~5.5V	0.7* VC	-	-	
Input high level voltage	VHI	VC =1.65V~1.95V	-	-	0.35* VC	V
		VC =2.3V~2.7V	-	-	0.7	
		VC =3V~5.5V	-	-	0.3* VC	
input voltage	VI	-	0	-	5.5	V
Output voltage	VO	-	0	-	VC	V
High level output current	IOH	VC =1.65V	-	-	-4	mA
		VC =2.3V	-	-	-8	
		VC =3V	-	-	-16	
		VC =4.5V	-	-	-32	
Low level output current	IOL	VC =1.65V	-	-	4	mA
		VC =2.3V	-	-	8	
		VC =3V	-	-	16	
		VC =4.5V	-	-	32	

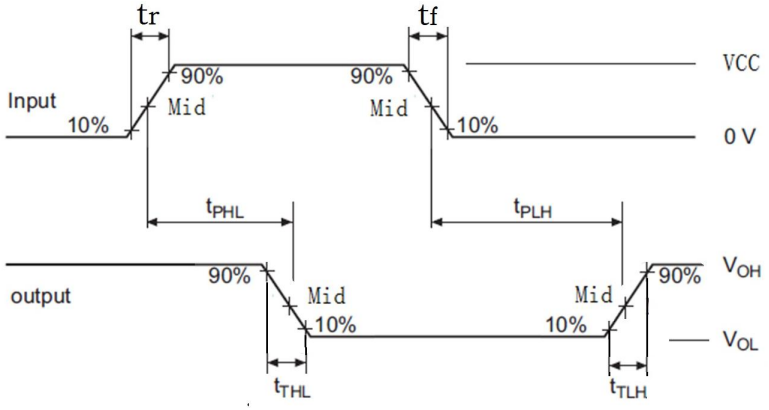
■ Electrical characteristics

Electrical characteristics of DC: T_a=25℃

project	symbol		test condition	V	typical value	maximum	unit
High level load voltage	V_{OH}		I_{OH} =-100uA	1.65V~5.5V	1.64	-	V
			I_{OH} =-4 mA	1.65V	1.47	-	
			I_{OH} =-8 mA	2.3V	2.15	-	
			I_{OH} =-16 mA	3V	2.73	-	
			I_{OH} =-32 mA	4.5V	4.0		
Low level load voltage	V_{OL}		I_{OH} =100uA	1.65V~5.5V	0.01	-	V
			I_{OH} =4 mA	1.65V	0.11	-	
			I_{OH} =8 mA	2.3V	0.11	-	
			I_{OH} =16 mA	3V	0.2	-	
			I_{OH} =32 mA	4.5V	0.35	-	
incoming current	I_I	A	V_I =5.5V 或 GND	0~5.5V	0.01	±5	uA
		B			0.01	±5	
Turn-off current	I_{OFF}	V_I	V_I =5.5V	0	0.01	±10	uA
		V_O	V_O =5.5V	0	0.01	±10	
operational current	I_{CC}		V_I =5.5V, I_O =0	1.65V~5.5V	0.01	10	uA
			V_I =GND , I_O =0		0.01	10	
Working current variation value	ΔI_{CC}		A=V_{CC} -0.6V B=V_{CC} 或 GND	3V~5.5V	25	-	uA
			B=V_{CC} -0.6V A= V_{CC} 或 GND		25	-	uA

Ac electrical characteristics: Ta=25℃ V(298)=5.0V, tr =≤20ns. See test method.

project	symbol	test condition	minimum value	typical value	maximum	unit
Maximum transmission delay time a, B to Y		C =15pF	-	10	-	ns
		C =15pF	-	10	-	ns



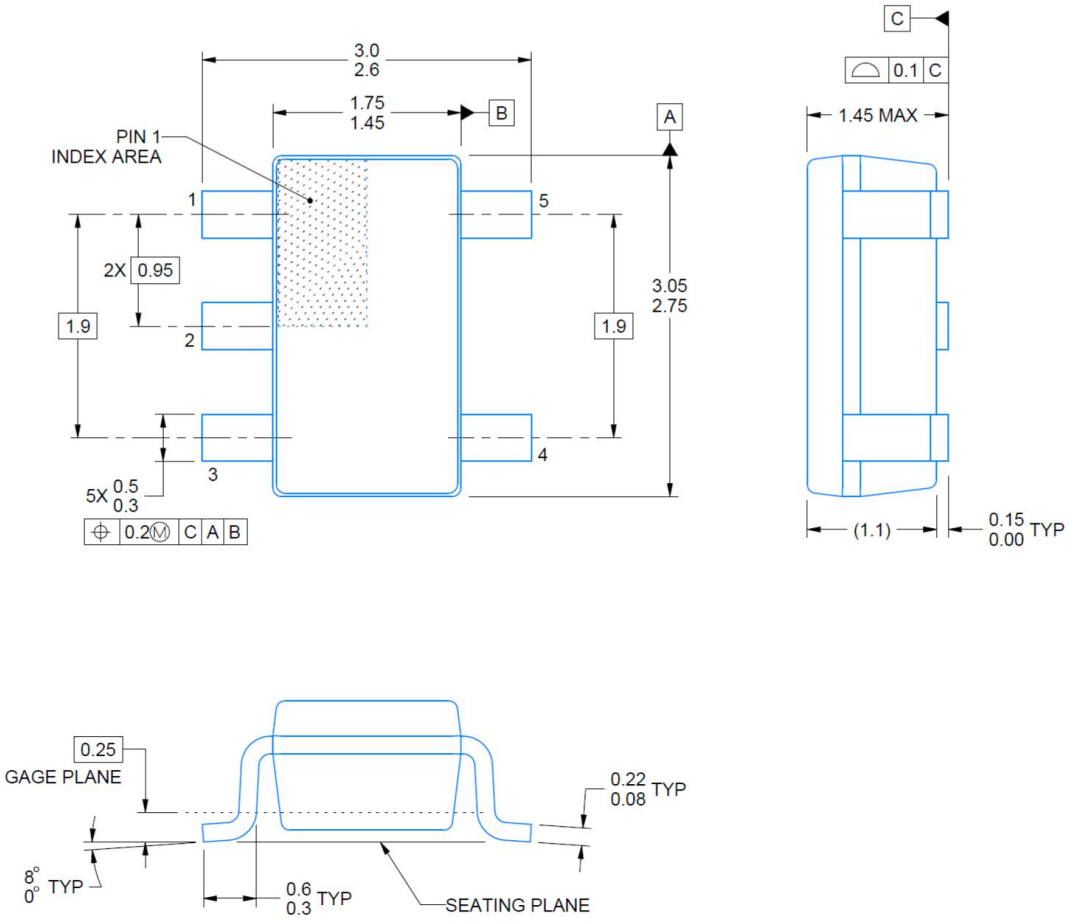
Note: 1. CL capacitor is external chip capacitor (0603), which is connected close to the output pin, and the capacitor ground is close to the chip GND;

2. Input: port input level, f=500kHz, D=50%; tr=tf≤20ns;

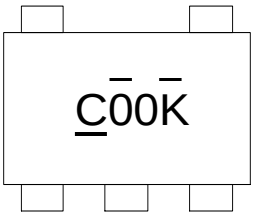
3. Output: Y-terminal output test.

■ Encapsulated information

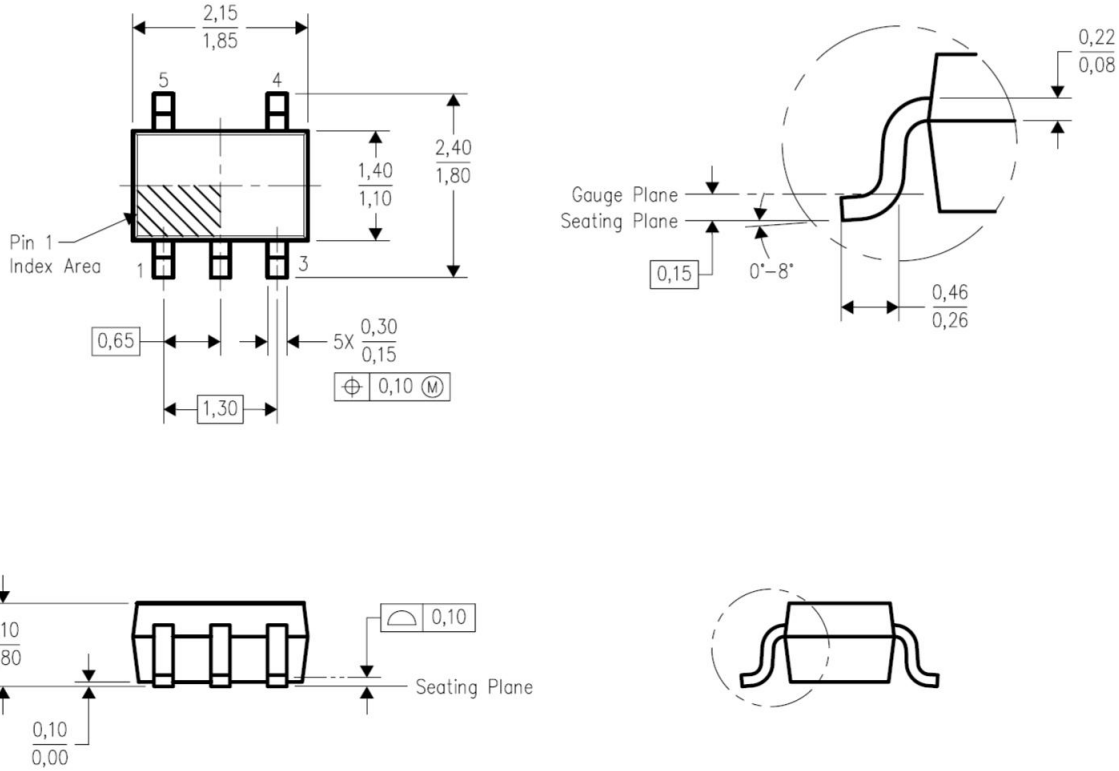
DBV(SOT23-5)



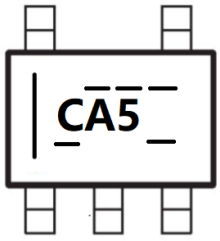
■ Marking



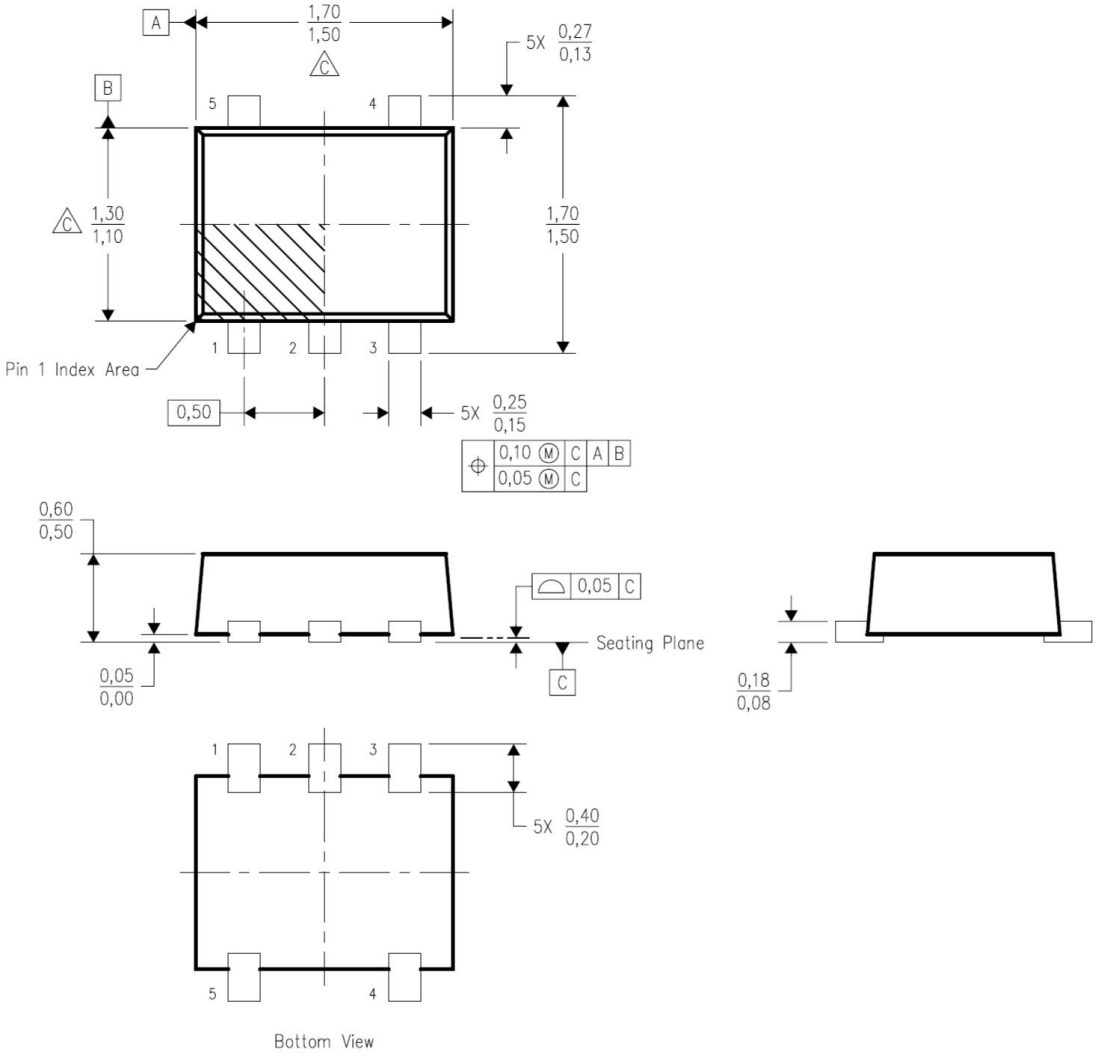
DCK(SC70-5)



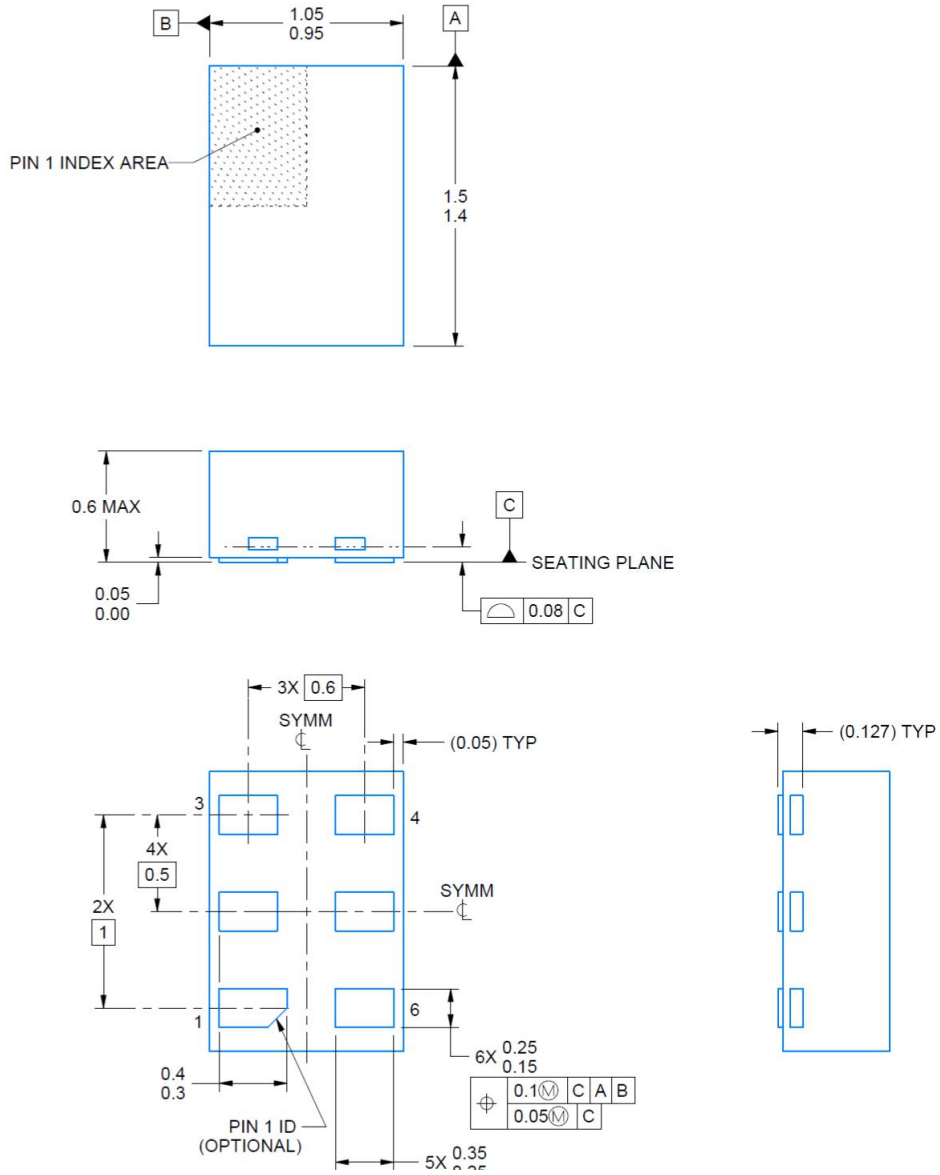
■ Marking



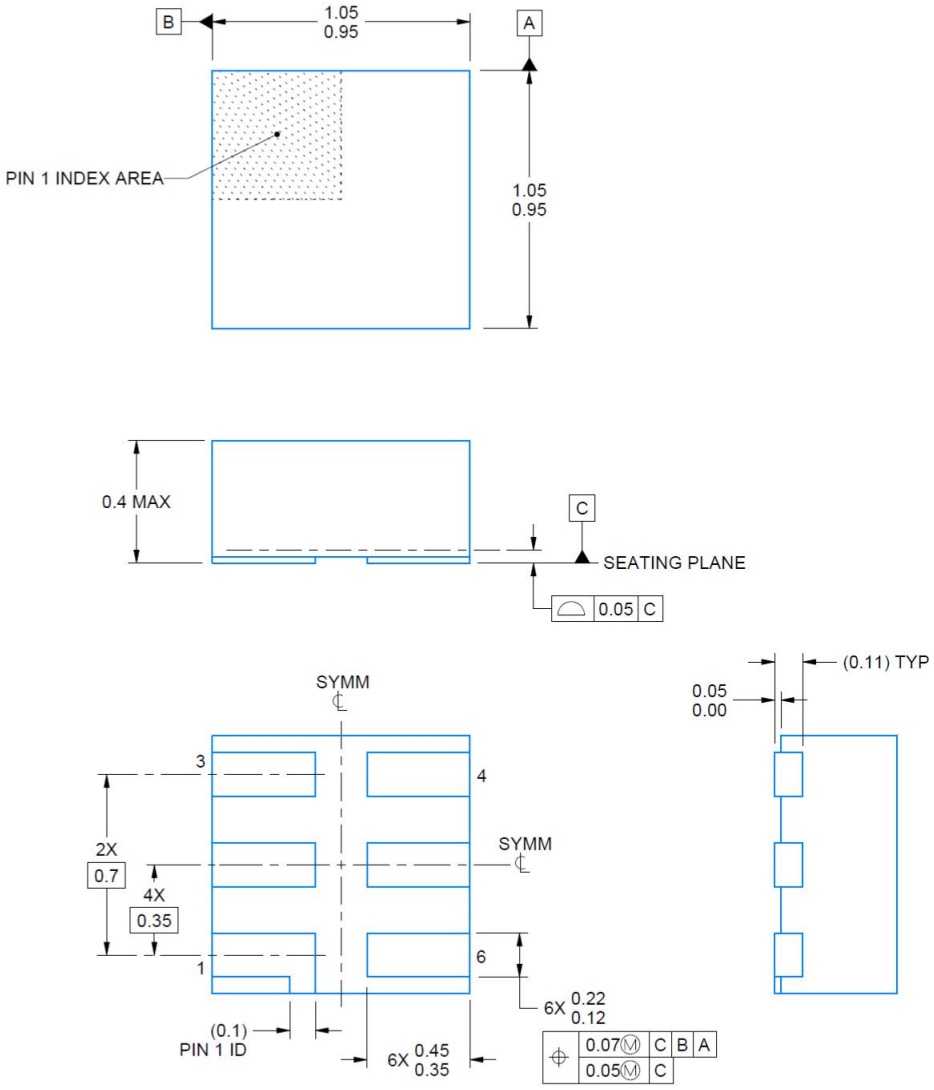
DRL (SOT-553)


A
1,70
1,50
C
5X 0,27
0,13
B
5
4
1,30
1,10
1,70
1,50
1
2
3
Pin 1 Index Area
0,50
5X 0,25
0,15
0,10 M C A B
0,05 M C
0,60
0,50
0,05 C
Seating Plane
C
0,05
0,00
0,18
0,08
1
2
3
5X 0,40
0,20
5
4
Bottom View

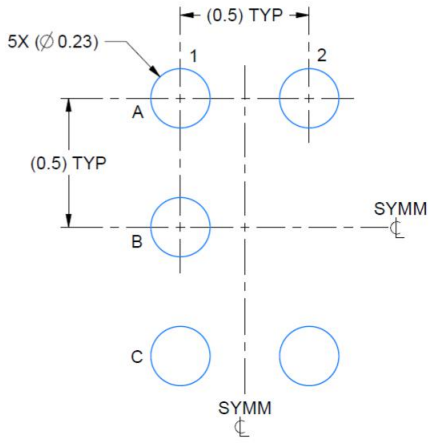
DRY(SOT-886)


B
1.05
0.95
A
PIN 1 INDEX AREA
1.5
1.4
0.6 MAX
C
SEATING PLANE
0.05
0.00
0.08 C
3X 0.6
SYMM
(0.05) TYP
(0.127) TYP
3
4
4X
0.5
SYMM
2X
1
1
6
6X 0.25
0.15
0.1 M C A B
0.05 M C
0.4
0.3
PIN 1 ID
(OPTIONAL)
5X 0.35

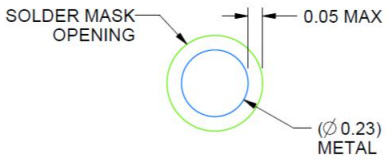
DSF(SON-6)


B
1.05
0.95
A
PIN 1 INDEX AREA
1.05
0.95
0.4 MAX
C
SEATING PLANE
0.05 C
SYMM
(0.11) TYP
0.05
0.00
3
4
2X
0.7
4X
0.35
SYMM
1
6
6X 0.22
0.12
(0.1)
PIN 1 ID
6X 0.45
0.35
0.07 M C B A
0.05 M C

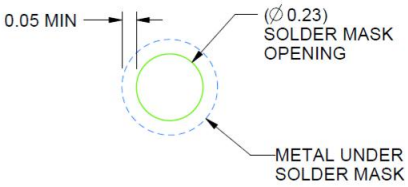
YZP(DSBGA-5)



LAND PATTERN EXAMPLE
SCALE:40X

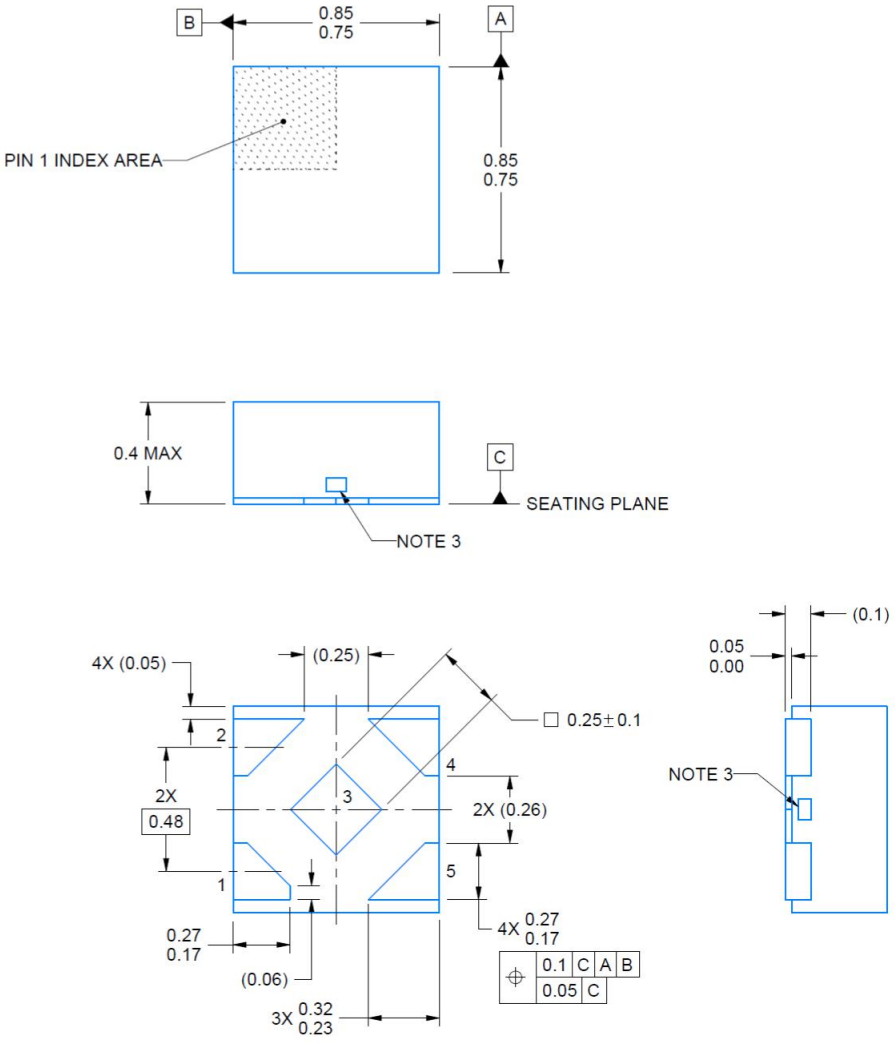


NON-SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

DPW(X2SON-4)


B
0.85
0.75
A
PIN 1 INDEX AREA
0.85
0.75
0.4 MAX
C
SEATING PLANE
NOTE 3
4X (0.05)
(0.25)
0.25±0.1
2
4
2X
0.48
3
2X (0.26)
1
5
4X 0.27
0.17
0.27
0.17
(0.06)
3X 0.32
0.23
0.1 C A B
0.05 C
(0.1)
0.05
0.00
NOTE 3