User's Manual

32

RX65N Group

Renesas Starter Kit+ for RX65N-2MB User's Manual

RENESAS 32-Bit MCU
RX Family / RX600 Series

Renesas Electronics
www.renesas.com

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Disclaimer

By using this Renesas Starter Kit+ (RSK+), the user accepts the following terms:

The RSK+ is not guaranteed to be error free, and the entire risk as to the results and performance of the RSK+ is assumed by the User. The RSK+ is provided by Renesas on an “as is” basis without warranty of any kind whether express or implied, including but not limited to the implied warranties of satisfactory quality, fitness for a particular purpose, title and non-infringement of intellectual property rights with regard to the RSK+. Renesas expressly disclaims all such warranties. Renesas or its affiliates shall in no event be liable for any loss of profit, loss of data, loss of contract, loss of business, damage to reputation or goodwill, any economic loss, any reprogramming or recall costs (whether the foregoing losses are direct or indirect) nor shall Renesas or its affiliates be liable for any other direct or indirect special, incidental or consequential damages arising out of or in relation to the use of this RSK+, even if Renesas or its affiliates have been advised of the possibility of such damages.

Precautions

The following precautions should be observed when operating any RSK+ product:

This Renesas Starter Kit+ is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the CPU Board hardware functionality, and electrical characteristics. It is intended for users designing sample code on the CPU Board platform, using the many different incorporated peripheral devices.

The manual comprises of an overview of the capabilities of the RSK+ product, but does not intend to be a guide to embedded programming or hardware design.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RX65N Group, RX651 Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the CPU Board hardware.	RSK+RX65N-2MB User's Manual	R20UT3888EG
Tutorial Manual	Provides a guide to setting up RSK+ environment, running sample code and debugging programs.	RSK+RX65N-2MB Tutorial Manual	CS+: R20UT3889EG e^2 studio: R20UT3892EG
Quick Start Guide	Provides simple instructions to setup the RSK+ and run the first sample, on a single A4 sheet.	RSK+RX65N-2MB Quick Start Guide	CS+: R20UT3890EG e^2 studio: R20UT3893EG
Smart Configurator Tutorial	Provides a guide to code generation and importing into the e^{2}studio/CS+ IDE.	RSK+RX65N-2MB Smart Configurator Tutorial Manual	CS+: R20UT3891EG e^2 studio: R20UT3894EG
Schematics	Full detail circuit schematics of the CPU Board.	RSK+RX65N-2MB CPU Board Schematics	R20UT3887EG
User's Manual: Hardware	Provides technical details of the RX65N microcontroller.	RX65N Group, RX651 Group User's Manual: Hardware	R01UH0590EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
BC	Battery Charging
bps	bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DIP	Dual In-line Package
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DNF	Do Not Fit
E1/E2 Lite	Renesas On-chip Debugging Emulator
EEPROM	Electronically Erasable Programmable Read Only Memory
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
GLCDC	Graphic LCD Controller
GPT	General PWM Timer
I^2C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LIN	Local Interconnect Network
MCU	Micro-controller Unit
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not Applicable
n/c (NC)	Not Connected
NMI	Non-maskable Interrupt
OTG	On The Go™
PC	Personal Computer
PDC	Parallel Data Capture Unit
PLL	Phase Locked Loop
Pmod™	This is a Digilent Pmod™ Compatible connector. Pmod™ is registered to Digilent Inc. Digilent-Pmod_Interface_Specification
POE	Port Output Enable
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read Only Memory
RSK+	Renesas Starter Kit+
RTC	Real Time Clock
SAU	Serial Array Unit
SCI	Serial Communications Interface
SFR	Special Function Registers
SPI	Serial Peripheral Interface
SSI	Serial Sound Interface
TAU	Timer Array Unit
TFT	Thin Film Transistor
TPU	Timer Pulse Unit
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WDT	Watchdog Timer

Table of Contents

1. Overview

1.1 Purpose

This CPU Board is an evaluation tool for Renesas microcontrollers. This manual describes the technical details of the CPU Board hardware.

1.2 Board specification

Board specification was shown in **Table 1-1** below.

Item	Specification
Microcontroller	Part No : R5F565NEDDFC
	Package : 176-pin LFQFP
	On-Chip Memory : ROM 2MB, RAM 640KB+8KB
On-Board Memory	SDRAM: 128Mbit
	I^2C EEPROM: 2Kbit
	SPI Serial Flash: 32Mbit x 2
Input Clock	RX65N Main : 24MHz
	RX65N Sub : 32.768kHz
	RL78/G1C Main: 12MHz
	Ethernet PHY (for MII) : 25MHz
Power Supply	DC Power Jack : 5 V Input
	Power Supply IC : 5V Input, 3.3V Output
	Power Supply IC : 5V Input, Max.38V Output(For TFT Backlight)
	Power Supply IC : 3.3V Input, 3.3V Output(For SDHI)
	Power Supply IC : 5V Input, 5V Output(For USB Host)
Debug Interface	E1/E2 Lite 14-pin box header
DIP Switch	Mode Configuration : 4-pole x 1
Push Switch	Reset Switch x 1
	User Switch x 3
Potentiometer(for ADC)	Single-turn, 10kΩ
LED	5V Power indicator: green x 1
	3.3V Power Indicator : green x 1
	User : green x 1, orange x 1, red x 2
	Ethernet Status: green x 2, yellow x 1
Ethernet	Connector : RJ45 x 1
	PHY : Single Channel PHY
SDHI *1	SD Card Slot (4-bit) x 1
SDSI *2, *3	2.54mm pitch, 16-pin x 1
CAN	Connector : 2.54mm pitch, 3-pin x 1
	CAN Driver x 1
USB	USB0-Functiont : USB-MiniB
	USB0-Host : USB-TypeA
USB to Serial Converter Interface	Connector : USB-MiniB
	Driver : RL78/G1C Microcontroller (Part No R5F10JBCANA)
Pmod™	PMOD1 : Angle type, 12-pin Connector
	PMOD2*3 : Straight type, 12-pin Connector
GLCDC Interface (Mounts On-Board TFT Panel)	FPC Connector : 40-pin x 1 (ONTFT1)
	FPC Connector : 6-pin x 1 (ONTFT2)
PDC Interface *3	2.54 mm pitch, 20-pin x 1 (J15)
TFT Header *3	2.54 mm pitch, 50-pin x 1 (TFT)
Application Board Interface *3	2.54 mm pitch, 26-pin x 2 (JA1, JA2), 50-pin x 1 (JA3), 24-pin x 2 (JA5, JA6)

Table 1-1: Board Specification

*1: The RX65N Group and RX651 Group incorporate an SD Host Interface (SDHI) which is compliant with the SD Specifications. When developing host devices that are compliant with the SD Specifications, the user must enter into the SD Host/Ancillary Product License Agreement (SD HALA).

*2: The RX65N Group and RX651 Group incorporates an SD slave interface which is compliant with the SDIO Card Specification Version 2.00. Developing a slave device compliant with the SD specification requires execution of an SD Host/Ancillary Product License Agreement (SD HALA) or Card License Agreement (CLA).

*3: The connector is not included in the product.

2. Power Supply

2.1 Requirements

This board have an optional centre positive supply connector using a 2.0mm barrel power jack (PWR). The main power supply connected to PWR should supply a minimum of 10W to ensure full functionality. When the board is connected to another system then that system should supply power to the board.

This CPU board supports one external voltage input. Details of the external power supply connection are shown in **Table 2-1 and Table 2-2** below. The default power configuration is shown in **bold, blue text.**

Connector	Supply voltage
PWR	Input 5VDC

Table 2-1: PWR connector Requirements

There are RSK products which supports the 12V voltage input. Since this board is supporting the 5V voltage input, be careful not to connect the power supply of a high-voltage output accidentally.
Moreover, the main power supply connected to PWR should supply a minimum of 10W to ensure full functionality.

J14[*1] Setting	Supply Source	Board_5V	UC_VCC
Open	**PWR connector**/JA1-5V/Unregulated_VCC	**5V**	**3.3V**
	JA1-3V3	NA	3.3V
Shorted	VBUS0	5V	3.3V

[*1]: The connector is not included to a product.

Table 2-2: Main Power Supply Requirements

2.2 Power-Up Behaviour

When the RSK+ is purchased, the RSK+ board has the ‘Release’ build of the example Tutorial_withTFT software pre-programmed into the Renesas microcontroller.

3. Board Layout

3.1 Component Layout

Figure 3-1 below shows the top component layout of the board.

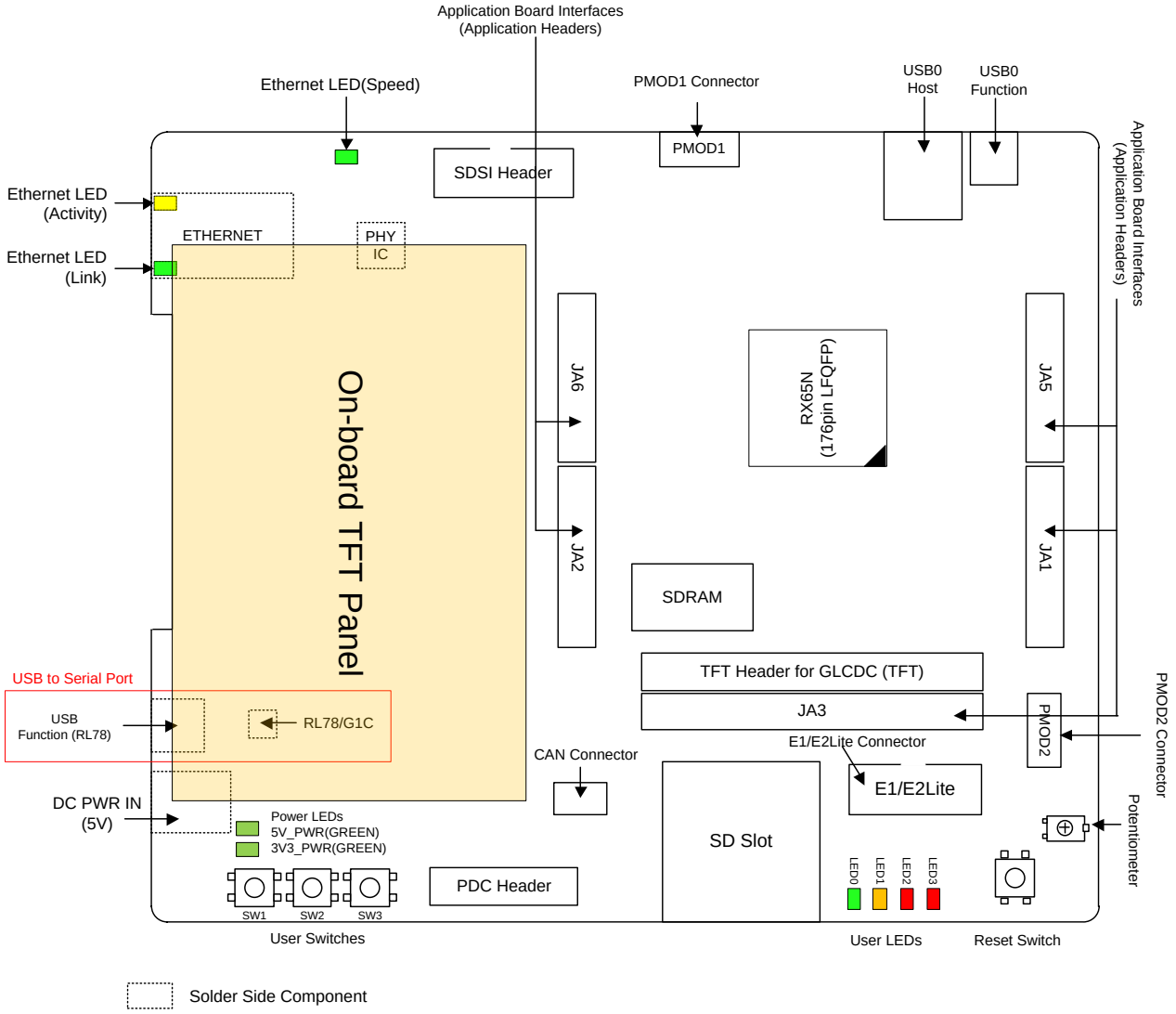

Figure 3-1: Board Layout

3.2 Board Dimensions

Figure 3-2 below gives the board dimensions and connector positions. All the through-hole connectors are on a common 2.54mm pitch grid for easy interfacing.

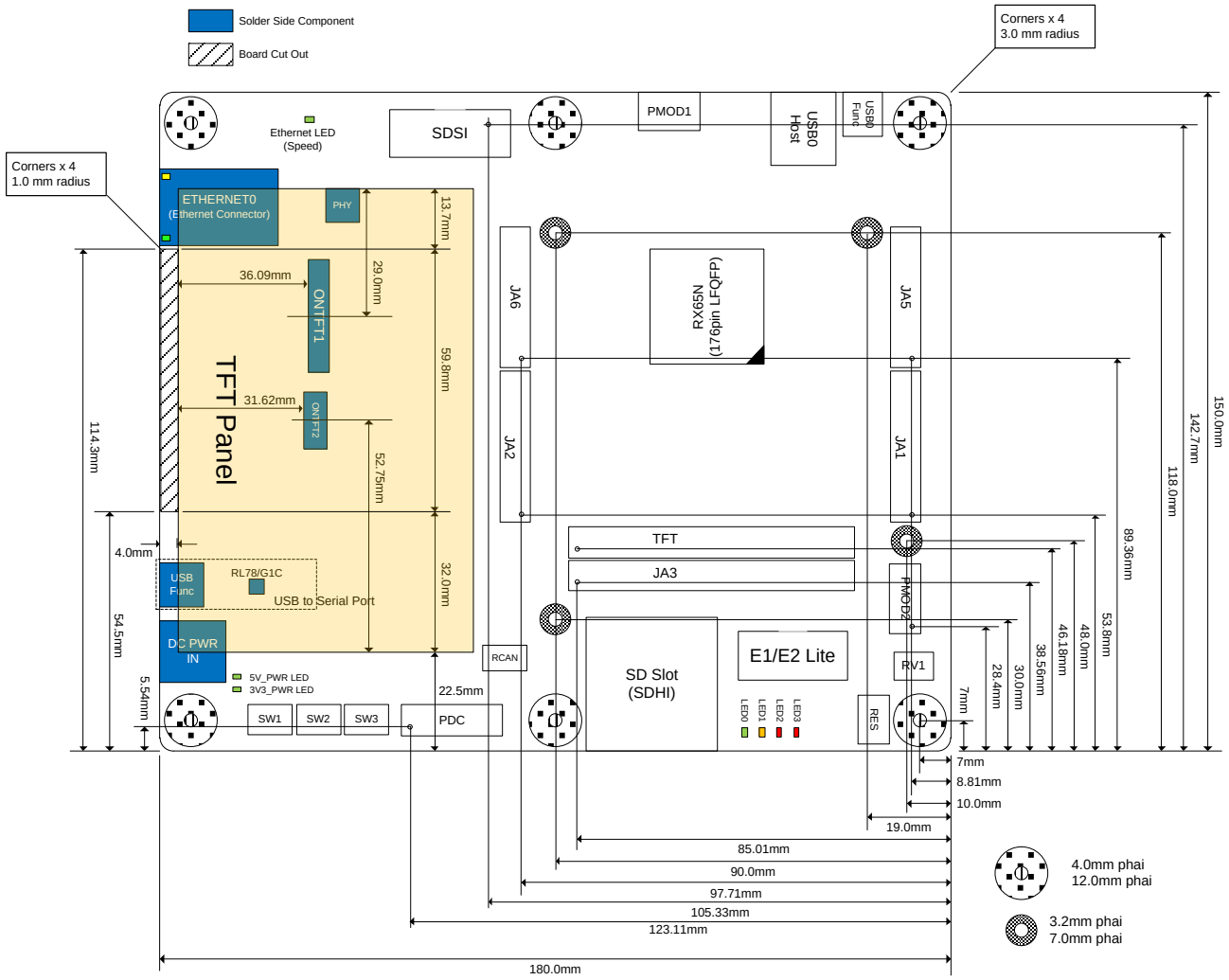

Figure 3-2: Board Dimensions

3.3 Component Placement

Figure 3-3 below shows placement of individual components on the top-side PCB – bottom-side component placement can be seen in **Figure 3-4**. Component types and values are shown on the board schematics.

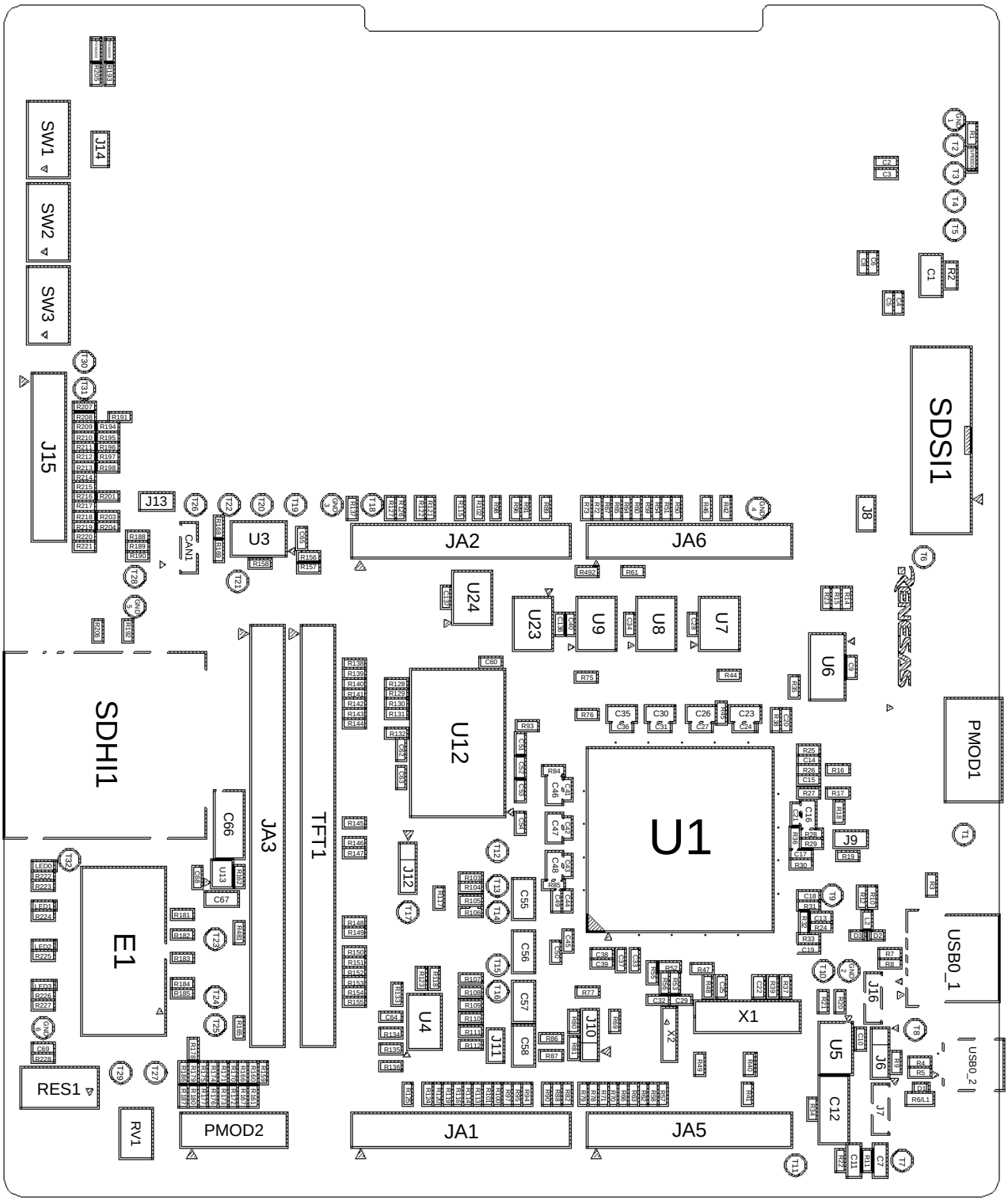

Figure 3-3: Top-Side Component Placement

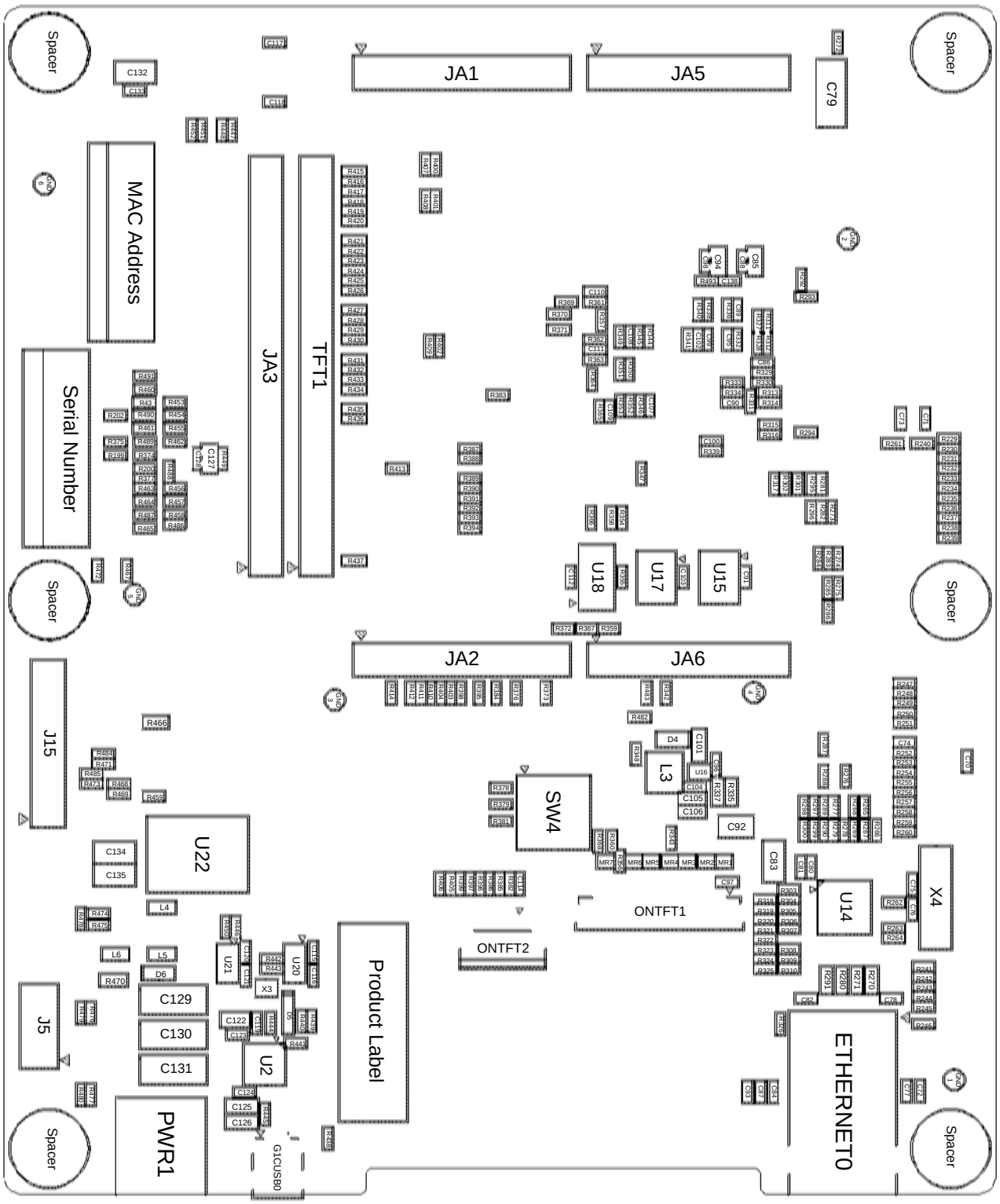

Figure 3-4: Bottom-Side Component Placement

4. Connectivity

4.1 Internal Board Connections

The diagram below shows the CPU board components and their connectivity to the MCU.

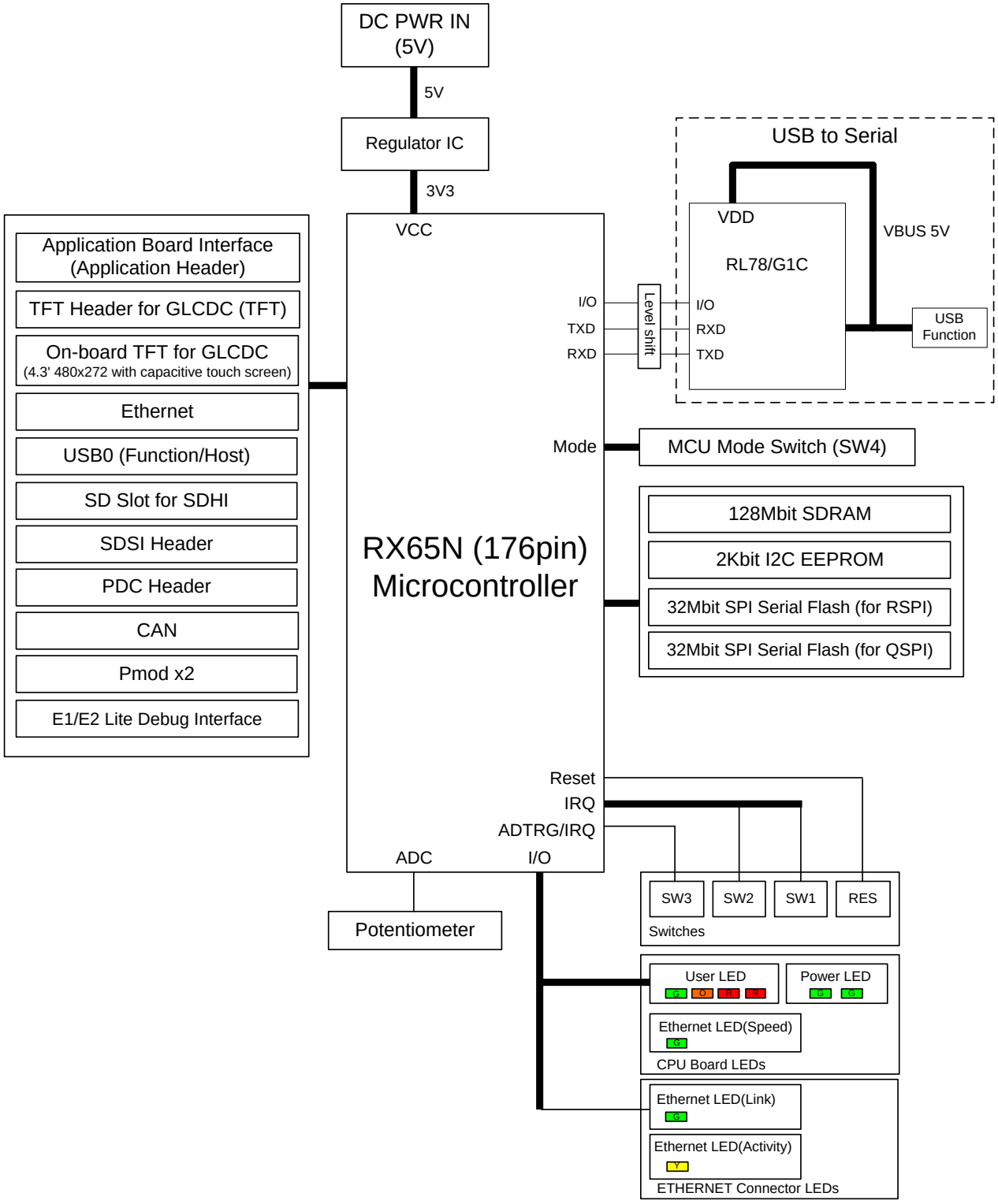

Figure 4-1: Internal Board Block Diagram

4.2 Debugger Connections

Figure 4-2 below shows the connections between the CPU board, E1/E2 Lite debugger and the host PC.

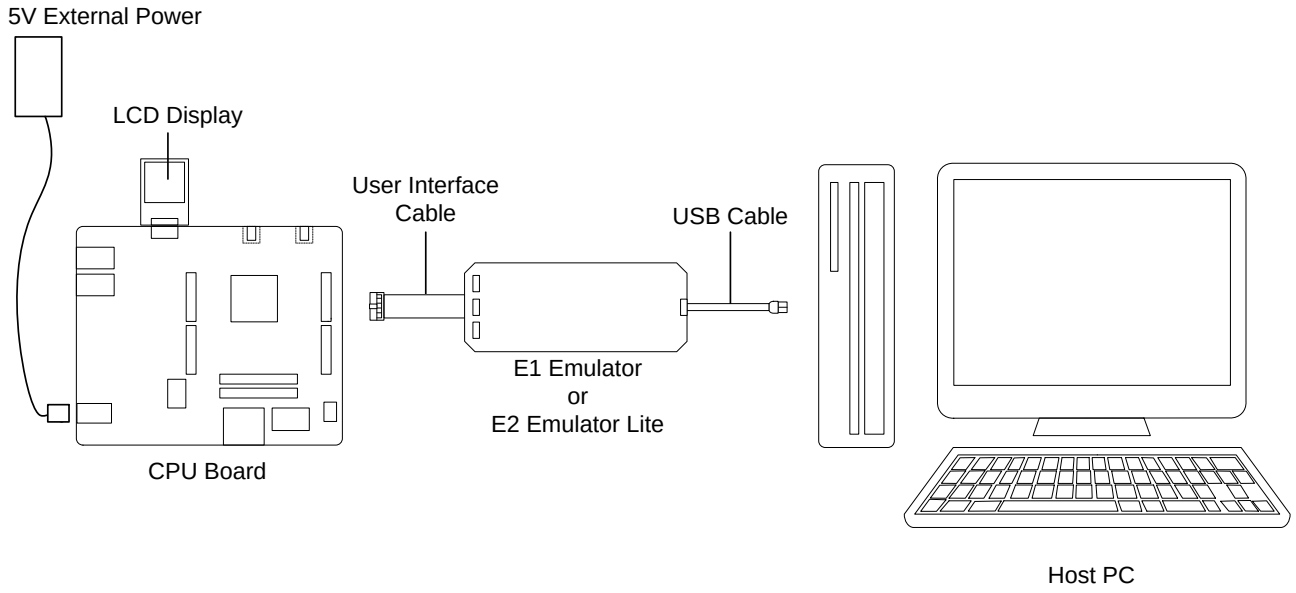

Figure 4-2: Debugger Connection Diagram

5. User Circuitry

5.1 Reset Circuit

A reset control circuit is fitted to the CPU board to generate the required reset signal, and is triggered from the RES switch. Refer to the RX65N Group, RX651 Group User's Manual: Hardware for details regarding the reset signal timing requirements, and the CPU board schematics for information regarding the reset circuitry in use on the board.

5.2 Clock Circuit

A clock circuit is fitted to the CPU board to generate the required clock signal to drive the MCU, and associated peripherals. Refer to the RX65N Group, RX651 Group Hardware Manual and the RL78/G1C hardware manual for details regarding the clock signal requirements, and the CPU board schematics for information regarding the clock circuitry in use on the CPU board. Details of the oscillators fitted to the board are listed in **Table 5-1**: Crystal below.

Crystal	Function	Default Placement	Frequency	Device Package
X1	Main MCU crystal for RX65N	Fitted	24MHz	Encapsulated, SMT
X2	Real time Clock for RX65N	Fitted	32.768kHz	Encapsulated, SMT
X3	Main MCU crystal for RL78/G1C	Fitted	12MHz	Encapsulated, SMT
X4	Crystal for Ethernet (MII)	Fitted	25MHz	Encapsulated, SMT

Table 5-1: Crystal

5.3 Switches

There are four switches located on the CPU board. The function of each switch and its connection is shown in **Table 5-2**. For further information regarding switch connectivity, refer to the CPU board schematics.

Switch	Function	MCU	
		Signal (Port)	Pin
RES	When pressed, the microcontroller is reset.	RES#	21
SW1	Connects to an IRQ11 input for user controls.	P03	4
SW2	Connects to an IRQ13 input for user controls.	P05	2
SW3	Connects to an IRQ15 input for user controls. Connects to an ADTRG0 input for ADC controls.	P07	176

Table 5-2: Switch Connections

5.4 LEDs

There are 9 LEDs on the RSK+ board. The function of each LED, its colour, and its connections are shown in **Table 5-3**.

LED	Colour	Function	MCU	
			Port	Pin
POWLED3	Green	Indicates the status of the Board_3V3 power rail.	NC	NC
POWLED5	Green	Indicates the status of the Board_5V power rail.	NC	NC
LED0	Green	User operated LED.	P73	93
LED1	Orange	User operated LED.	PG7	111
LED2	Red	User operated LED.	PG6	113
LED3	Red	User operated LED.	PG5	116
SPEED0	Green	Ethernet LED (Speed)	NC	NC
ETHERNET Connector	Green	Ethernet LED (Link)	P34	27
ETHERNET Connector	Yellow	Ethernet LED (Activity)	NC	NC

Table 5-3: LED Connections

5.5 Potentiometer

A single-turn potentiometer is connected as a potential divider to analog input AN000, pin 173. The potentiometer can be used to create a voltage between Board_3V3 and AVSS0.
Refer to the maker site for specification of the potentiometer (VISHAY with part number TS53 series).

The potentiometer offers an easy method of supplying a variable analog input to the microcontroller. It does not necessarily reflect the accuracy of the controller's ADC. Refer to the RX65N Group, RX651 Group User's Manual: Hardware for further details.

5.6 Pmod™

The RSK+ board is equipped with connectors for Digilent Pmod™ interface. Please connect the PMOD1 connector that is compatible with LCD module.

Care should be taken when installing the LCD module to ensure pins are not bent or damaged. The LCD module is vulnerable to electrostatic discharge (ESD); therefore appropriate ESD protection should be used.

The Digilent Pmod™ Compatible headers use an SPI interface. **Figure 5-1** below shows Digilent Pmod™ Compatible Header Pin Numbering. Connection information for the Digilent Pmod™ Compatible header is provided in **Table 5-4 and Table 5-5** below.

Please note that the connector numbering adheres to the Digilent Pmod™ standard and is different from all other connectors on the RSK designs. Details can be found in the Digilent Pmod™ Interface Specification Revision: November 20, 2011.

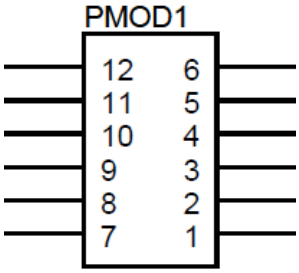

Figure 5-1: Digilent Pmod™ Compatible Header Pin Numbering

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	PMOD1-CS	PJ3	13	7	PMOD1-IO0	P15	50
2	PMOD1-MOSI	P00	8	8	PMOD1-IO1	PF5	9
3	PMOD1-MISO	P01	7	9	PMOD1-IO2	PG4	119
4	PMOD1-SCK	P02	6	10	PMOD1-IO3	PG3	121
5	GROUND	-	-	11	GROUND	-	-
6	Board_3V3	-	-	12	Board_3V3	-	-

Table 5-4: Pmod™1 Header Connections

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	PMOD2-CS	P31	32	7	PMOD2-IO0	P21	44
2	PMOD2-MOSI	PF0	35	8	PMOD2-IO1	P20	45
3	PMOD2-MISO	PF2	31	9	PMOD2-IO2	P17	46
4	PMOD2-SCK	PF1	34	10	PMOD2-IO3	P86	49
5	GROUND	-	-	11	GROUND	-	-
6	Board_3V3	-	-	12	Board_3V3	-	-

Table 5-5: Pmod™2 Header Connections

5.7 USB Serial Port

A USB serial port is implemented in a Renesas low power microcontroller (RL78/G1C) and is connected to the RX65N Serial Communications Interface (SCI) module. Multiple options are provided to allow the selection of the connected SCI8 port. Connections between the USB to Serial converter and the microcontroller are listed in **Table 5-6** below.

Signal Name	Function	MCU	
		Port	Pin
SERIAL-TXD	SCI1 Transmit Signal. *1	PF0	35
	SCI2 Transmit Signal. *1	P50	72
	SCI8 Transmit Signal.	PJ2	58
	External RS232 Transmit Signal. *1	-	-
SERIAL-RXD	SCI1 Receive Signal. *1	PF2	31
	SCI2 Receive Signal. *1	P52	70
	SCI8 Receive Signal.	PJ1	59
	External RS232 Receive Signal. *1	-	-
SERIAL-CTS	Clear To Send.	P10	68
SERIAL-RTS	Request To Send.	PG2	123

Table 5-6: Serial Port Connections

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

When the CPU board is first connected to a PC running Windows™ with the USB/Serial connection, the PC will look for a driver. This driver is installed during the installation process, so the PC should be able to find it. The PC will report that it is installing for a driver and then report that a driver has been installed successfully, as shown in **Figure 5-2**. The exact messages may vary depending upon operating system.

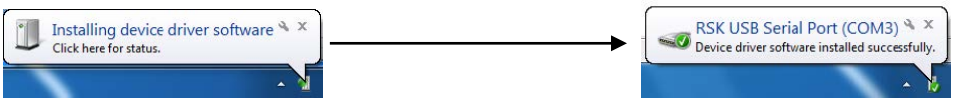

Figure 5-2: USB-Serial Windows™ Installation message

If you do not have the driver, please download the driver installer from the following URL.
https://www.renesas.com/en-eu/software/D6000699.html

5.8 Controller Area Network (CAN)

A CAN transceiver IC is fitted to the RSK+ board, and connected to the CAN MCU peripheral. For further details regarding the CAN protocol and supported modes of operation, please refer to the RX65N Group, RX651 Group User's Manual: Hardware. The connections for the CAN microcontroller signals are listed in **Table 5-7** below.

CAN Signal	Function	MCU	
		Port	Pin
CAN1TX JA5-CAN1TX *1	CAN Data Transmission.	P32	29
CAN1RX JA5-CAN1RX *1	CAN Data Reception.	P33	28

Table 5-7: CAN Connections

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

5.9 Ethernet

When running any Ethernet software, a unique MAC address should be used. A unique Renesas allocated MAC address is attached to the PCB as a sticker, and should be always be used with this device ensured to ensure full compatibility when using other Renesas hardware on a common Ethernet connection.

An Ethernet controller IC is fitted to the CPU board, and is connected to the Ethernet MCU peripheral. The RX65N MCU supports full duplex 10Mb/s and 100Mb/s transmission and reception. Refer to §5.4 Ethernet LEDs. The connections for the Ethernet controller are listed in **Table 5-8** below.

Ethernet signal	Function	MCU	
		Port	Pin
ET-ET0MDIO	MII/RMII: Management data I/O	P71	102
ET-ET0MDC	MII/RMII: Management data clock	P72	101
ET-ET0TXCLK	MII: Transmit clock	PC4	82
ET-ET0TXEN_RMII0TXDEN	MII/RMII: Transmit data valid	P80	81
ET-ET0ETXD0_RMII0TXD0	MII: 4-bit transmit data RMII: 2-bit transmit data	P81	80
ET-ET0ETXD1_RMII0TXD1	MII: 4-bit transmit data RMII: 2-bit transmit data	P82	79
ET-ET0ETXD2	MII: 4-bit transmit data	PC5	78
ET-ET0ETXD3	MII: 4-bit transmit data	PC6	77
ET-ET0RXCLK_REF50CK0	MII: Receive clock RMII: Reference clock	P76	85
ET-ET0RXDV	MII: Receive data valid	PC2	86
ET-ET0RXER_RMII0RXER	MII/RMII: Receive error	P77	84
ET-ET0ERXD0_RMII0RXD0	MII: 4-bit receive data RMII: 2-bit receive data	P75	87
ET-ET0ERXD1_RMII0RXD1	MII: 4-bit receive data RMII: 2-bit receive data	P74	88
ET-ET0ERXD2	MII: 4-bit receive data	PC1	89
ET-ET0ERXD3	MII: 4-bit receive data	PC0	91
ET-ET0COL	MII: Collision detect signal	PC7	76
ET-ET0LINKSTA	MII: Link status input from the PHY-LSI	P34	27
ET-ET0CRS_RMII0CRSDV	MII: Carrier sense RMII: Carrier sense/receive data valid	P83	74
ET-RESn	PHY Reset	RESn	21

Table 5-8: Ethernet Connections (ET0)

5.10 Universal Serial Bus (USB)

This CPU board is fitted with a USB Host socket (type A) and a Function socket (type Mini B). USB module USB0 is connected to the Host and Function socket, and can operate as either a Host or Function device. The connection for the USB0 module is shown in **Table 5-9** below.

USB Signal	Function	MCU	
		Port	Pin
USB0-DP	D+ I/O pin of the USB on-chip transceiver	USB0_DP	56
USB0-DM	D– I/O pin of the USB on-chip transceiver	USB0_DM	55
USB0-VBUS	USB cable connection monitor pin	P16	48
USB0-VBUSEN *1	VBUS (5V) supply enable signal for external power supply chip		
USB0-OVRCURA	External overcurrent detection signals	P14	51

Table 5-9: USB0 Module Connections

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

5.11 TFT Header

This CPU board is fitted with a TFT interface thru-hole pattern. Further details of TFT Header, refer to §7.

5.12 External Bus

The RX65N features an external data bus, which is connected to various devices on the CPU board. Details of the devices connected to the external data bus are listed in **Table 5-10** below. Further details of the devices connected to the external bus can be found in the board schematics.

Chip Select	Device Name	Device Description	Address Space
CS0(JA3-CSa)	JA3	Application Header	FF000000h – FFFFFFFFh (16Mbyte)
SDCS(SDRAM-SDCSn)	U12	128Mbit SDRAM	08000000h – 0FFFFFFFh (128Mbyte)
SDCS(JA3-CSb)	JA3	Application Header	08000000h – 0FFFFFFFh (128Mbyte)
CS1 - CS5	-	Unused	03000000h – 07FFFFFFh (5 x 16Mbyte)
CS6(JA3-CSc)	JA3	Application Header	02000000h – 02FFFFFFh (16Mbyte)
CS7	-	Unused	01000000h – 01FFFFFFh (16Mbyte)

Table 5-10: External Bus Address Space

5.13 Renesas Serial Peripheral Interface (RSPI)

The RX65N features three Renesas Serial Peripheral Interface modules (Renesas SPI or RSPI). **Table 5-11** below details the connected devices, and their connections to the MCU.

Slave Select	Device Name	Device Description
SSLB0-A(RSPI-CS)	U6,	Serial Flash, 32Mbits
SSLB0-A(TFT-SS)	TFT	TFT Header
SSLB0-A(PMOD2-CS)	PMOD2	PMOD2 Connector

Table 5-11: RSPI Connections

5.14 Quad Serial Peripheral Interface (QSPI)

The RX65N features one Quad Serial Peripheral Interface modules (QSPI). **Table 5-12** below details the connected devices, and their connections to the MCU.

Slave Select	Device Name	Device Description
QSSL-B (QSPI-CS)	U18	Serial Flash, 32Mbits

Table 5-12: QSPI Connections

5.15 I^2C Bus (Inter-IC Bus)

The RX65N features two I^2C (Inter-IC Bus) interface modules. RIIC0 is connected to a 2Kbit EEPROM. Specific details of the EEPROM device and the connections can be found in the board schematics.

5.16 SD Host Interface (SDHI)

A SD Card Slot is fitted to the CPU board, and connected to the SD Host Interface (SDHI) MCU peripheral. For further details regarding the SDHI operation, please refer to the RX65N Group, RX651 Group User's Manual: Hardware. The connections for the SDHI signals are listed in **Table 5-13** below.

SD Card Slot (SD1)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	SDHI-D3	P17	46	2	SDHI-CMD	P20	45
3	GROUND	-	-	4	SDHI-PE(SDHI-VCC)	P86	49
5	SDHI-CLK	P21	44	6	GROUND	-	-
7	SDHI-D0	P22	43	8	SDHI-D1	P23	42
9	SDHI-D2	P87	47	10	SDHI-CD	P25	38
11	GROUND	-	-	12	SDHI-WP	P24	40

Table 5-13: SDHI Connections

5.17 SD Slave Interface (SDSI)

This CPU board is fitted with a SD Slave Interface (SDSI) thru-hole pattern. The connections for the SDSI signals are listed in **Table 5-14** below.

SDSI (2x8 thru-hole)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	SDSI-D2	PB2	99	2	GROUND	-	-
3	SDSI-D3	PB3	98	4	GROUND	-	-
5	SDSI-CMD	PB4	97	6	GROUND	-	-
7	GROUND	-	-	8	GROUND	-	-
9	Board_3V3	-	-	10	GROUND	-	-
11	SDSI-CLK	PB5	96	12	GROUND	-	-
13	SDSI-D0	PB6	95	14	GROUND	-	-
15	SDSI-D1	PB7	94	16	GROUND	-	-

Table 5-14: SDSI Connections

5.18 Parallel Data Capture Unit (PDC)

This CPU board is fitted with a Parallel Data Capture Unit (PDC) thru-hole pattern. The connections for the PDC signals are listed in **Table 5-15** below.

PDC Header (J15)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	Board_5V	-	-	2	Board_3V3	-	-
3	GROUND	-	-	4	GROUND	-	-
5	PDC-PCKO	P33	28	6	PDC-RESn	RESn	21
7	GROUND	-	-	8	PDC-PIXCLK	P24	40
9	PDC-VSYNC	P32	29	10	PDC-HSYNC	P25	38
11	PDC-PIXD7	P23	42	12	PDC-PIXD6	P22	43
13	PDC-PIXD5	P21	44	14	PDC-PIXD4	P20	45
15	PDC-PIXD3	P17	46	16	PDC-PIXD2	P87	47
17	PDC-PIXD1	P86	49	18	PDC-PIXD0	P15	50
19	PDC-SSDA	P00	8	20	PDC-SSCL	P01	7

Table 5-15: PDC Connections

5.19 Graphic LCD Controller (GLCDC)

The RX65N features a graphic LCD controller (GLCDC) built in and is connected to via the FPC connector to NHD - 4.3 - 480272EF - ATXL - CTP manufactured by Newhaven Display International, Inc.
Table 5-16 and Table 5-17 show the connection relationship of the GLCDC interface.

GLCDC (ONTFT1) *1							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	OnTFT-LEDK	-	-	2	OnTFT-LEDA	-	-
3	GROUND	-	-	4	Board_3V3	-	-
5	OnTFT-R5(R0) *2	PA6	107	6	OnTFT-R6(R1) *2	PA5	108
7	OnTFT-R7(R2) *2	PA4	109	8	OnTFT-R3	PB0	104
9	OnTFT-R4	PA7	106	10	OnTFT-R5	PA6	107
11	OnTFT-R6	PA5	108	12	OnTFT-R7	PA4	109
13	OnTFT-G6(G0) *2	PE7	125	14	OnTFT-G7(G1) *2	PE6	126
15	OnTFT-G2	PA3	110	16	OnTFT-G3	PA2	112
17	OnTFT-G4	PA1	114	18	OnTFT-G5	PA0	118
19	OnTFT-G6	PE7	125	20	OnTFT-G7	PE6	126
21	OnTFT-B5(B0) *2	PE3	132	22	OnTFT-B6(B1) *2	PE2	133
23	OnTFT-B7(B2) *2	PE1	134	24	OnTFT-B3	PE5	130
25	OnTFT-B4	PE4	131	26	OnTFT-B5	PE3	132
27	OnTFT-B6	PE2	133	28	OnTFT-B7	PE1	134
29	GROUND	-	-	30	OnTFT-CLK	PB5	96
31	OnTFT-DISP	P97	149	32	OnTFT-HSYNC	PB2	99
33	OnTFT-VSYNC	PB4	97	34	OnTFT-DEN	PB1	100
35	NC	-	-	36	GROUND	-	-
37	NC	-	-	38	NC	-	-
39	NC	-	-	40	NC	-	-

Table 5-16: GLCDC Connections(1)

*1: Connection driver: HK8257-A manufactured by SK HYNIX INC.
*2: Normalization from RGB 565 to RGB 888.

GLCDC (ONTFT2)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	Board_3V3	-	-	2	GROUND	-	-
3	OnTFT-SCL*3	P92	160	4	OnTFT-SDA*3	P90	163
5	OnTFT-INT	P42	170	6	OnTFT-RESn	RESn	21

Table 5-17: GLCDC Connections(2)

*3: Simple I2C bus is used for TFT touch interface.
Connection touch controller: FT5306 manufactured by Focal Tech, Inc.
Slave address (A6-0): 0111000.

6. Configuration

6.1 Modifying the RSK+

This section lists the option links that are used to modify the way CPU board operates in order to access different configurations. Configurations are made by modifying link resistors or headers with movable jumpers or by configuration DIP switches

A link resistor is a 0Ω surface mount resistor, which is used to short or isolate parts of a circuit. Option links are listed in the following sections, detailing their function when fitted or removed. **Bold, blue text** indicates the default configuration that the CPU board is supplied with. Refer to the component placement diagram (§3) to locate the option links, jumpers and DIP switches.

When removing soldered components, always ensure that the CPU board is not exposed to a soldering iron for intervals greater than 5 seconds. This is to avoid damage to nearby components mounted on the board.

When modifying a link resistor, always check the related option links to ensure there is no possible signal contention or short circuits. Because many of the MCU's pins are multiplexed, some of the peripherals must be used exclusively. Refer to the RX65N Group, RX651 Group User's Manual: Hardware and CPU board schematics for further information.

6.2 MCU Operating Modes

Table 6-1 below details the option links associated with configuring the MCU Operating Modes.

SW4 Pin1	SW4 Pin2	J9 *1	Explanation	Related Ref.
OFF	**OFF(don't care)**	**OFF(don't care)**	**Single Chip Mode**	**R409**, R402, J12*1, *2
ON	OFF	don't care	SCI Boot Mode	R409, R402, J12*1, *2
ON	ON	Open	USB Boot Mode (Bus-powered)	R409, R402, J12*1, *2
		Shorted	USB Boot Mode (Self-powered)	R409, R402, J12*1, *2

Table 6-1: MCU Operating Modes Switch Settings

*1: Jumpers J12, J9 are not mounted on the board at the time of product shipment.

*2: The COL terminal of the PHY IC (U14) is connected to the PC7 (UB terminal) of the MCU.

6.3 E1/E2 Lite Debugger Configuration

Table 6-2 below details the function of the option links associated with E1/E2 Lite Debugger Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
E1-TRSTn	17	PF4	E1-TRSTn	-	-	E1.3	-	-
E1-TMS	30	PF3	E1-TMS	-	-	E1.9	-	-
PF2	31	PF2	E1-TDI_RXD	R447	R448, R170	E1.11	-	-
			SERIAL-RXD	R448	R447, R170	U20.3	-	R60, R121, R483
			PMOD2-MISO	R170	R447, R448	PMOD2.3	R172	-
PF1	34	PF1	E1-TCK	R160, R338	R159	E1.1	-	-
			PMOD2-SCK	R159, R338	R160	PMOD2.4	R161	-
PF0	35	PF0	E1-TDO_TXD	R451	R452, R175	E1.5	-	-
			SERIAL-TXD	R452	R451, R175	U21.3	-	R64, R126, R482
			PMOD2-MOSI	R175	R451, R452	PMOD2.2	R177	-
PC7	76	PC7	ET-ET0COL	R409 or J12 (1-2pin short)	R402	U14.42	-	-
			E1-UB	J12 (2-3pin short)	R409, R402	E1.10	-	-
			DSW-UB			SW4.2	-	-
			TFT-G4	R402	R409, J12 open	TFT.16	-	-
RESn	21	-	E1-RESn	-	-	E1.13	-	-
			SW-RESn	-	-	RES1(Switch)	-	-
			JA2-RESn	-	-	JA2.1	-	-
			PDC-RESn	-	-	J15.6	R207	-
			TFT-RESn	-	-	TFT.33	R149	-
			ET-RESn	-	-	U14.29	R264	-
			OnTFT-RESn	-	-	ONTFT2.6	R137	-
EMLE	10	-	E1-EMLE	-	-	E1.4	-	-
			JP-EMLE	-	-	J10.2	R69	-
MD_FINED	18	-	E1-MD_FINED	-	-	E1.7	-	-
			DSW-MD_FINED	-	-	SW4.1	-	-

Table 6-2: E1/E2 Lite Debugger Configuration Option Links

Table 6-3 below details the function of the jumpers associated with the E1/E2 Lite Debugger.

Reference	Jumper Position	Explanation	Related Ref.
J10(DNF) *1	Shorted Pin1-2	Enable E1/E2 Lite debugging with Hot plug-in function.	-
	Shorted Pin2-3	Enable E1/E2 Lite normal debugging and MCU single operation (without E1/E2 Lite).	R69
	All open	DO NOT SET.	-

Table 6-3: E1/E2 Lite Debugger Configuration Jumper Settings

*1: Jumper J10 is not fitted on the default CPU board. Same as Jumper Position “shorted pin2-3” setting by resistor R69.

6.4 Power Supply Configuration

Table 6-4 below details the function of the option links associated with Power Supply Configuration.

Reference	Explanation	Fit	DNF	Related Ref.
VBUS0	Connect 5V Power rail to VBUS0.	J14.shorted, J7.Pin2-3	-	U22
Board_5V	Connect 5V power rail to Board_5V.	R470	-	Simple IIC pull-up resistor, POWLED5, U4.8, U3.3, J15.1, TFT.1, TFT.2, U16.6
SD_3V3	Connect 3.3V power rail to SD_3V3.	R466	-	U13.1
JA1-3V3	Connect 3.3V power rail to JA1-3V3.	R459	-	JA1.3
UC_VCC	Connect 3.3V power rail to UC_VCC.	J13.Short or (R45, R40, R35, R18, R84, R77, R85, R76, R117, R49, R31)	-	U1, R86, R293, R108, R105
	Enable current probe for measurement MCU current consumption.	-	J13.open or (R45, R40, R35, R18, R84, R77, R85, R76, R117, R49, R31)	U1, R86, R293, R108, R105
VBATT	Connect UC_VCC power rail to VBATT.	R86	R87	U1
	J11 connected to VBATT of MCU	R87	R86	U1

Table 6-4: Power Supply Configuration Option Links

Table 6-5 below details the function of the jumpers associated with the Power Supply Configuration.

Reference	Jumper Position	Explanation	Related Ref.
J13(DNF) *1	Shorted	Connect 3.3V power rail to UC_VCC.	R45, R40, R35, R18, R84, R77, R85, R76, R117, R49, R31
	All open	Enable current probe for measurement MCU current consumption.	-
J14(DNF) *2	Shorted	Enable VBUS0.	J7
	All open	Disable VBUS0	J7

Table 6-5: Power Supply Configuration Jumper Settings

*1: Jumper J13 is not fitted on the default CPU board. Same as Jumper Position “shorted” setting by resistor R45, R40, R35, R18, R84, R77, R85, R76, R117, R49, and R31

*2: Jumper J14 is not fitted on the default CPU board.

6.5 Clock Configuration

Table 6-6 below details the function of the option links associated with Clock Configuration.

Reference	Explanation	Fit	DNF	Related Ref.
XTAL, EXTAL	Connect 24MHz crystal (X1) to RX65N.	R48, R39	R37	U1.22, U1.24
	Connect JA2-EXTAL to RX65N.	R37	R48, R39	U1.24
XCIN, XCOUT	Connect 32.768kHz crystal (X2) to RX65N.	R56, R53	R55	U1.19, U1.20
	Disconnect X2 from RX65N.	R55	R56, R53	-

Table 6-6: Clock Configuration Option Links

6.6 Analog Power & ADC & DAC Configuration

Table 6-7 below details the function of the option links associated with Analog Power & ADC & DAC Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P07	176	P07	SW3	R478	-	SW3	-	-
			JA1-ADTRG	R125	-	JA1.8	-	-
P05	2	P05	SW2	R479	R119	SW2	-	-
			JA1-DAC1	R119	R479	JA1.14	-	-
P03	4	P03	SW1	R480	R120	SW1	-	-
			JA1-DAC0	R120	R480	JA1.13	-	-
P47	165	P47	TFT-YINPUT2	R154	R70	TFT.46	-	-
			JA5-ADC7	R70	R154	JA5.4	-	-
P46	166	P46	TFT-XINPUT2	R155	R71	TFT.45	-	-
			JA5-ADC6	R71	R155	JA5.3	-	-
P45	167	P45	TFT-YINPUT1	R152	R78	TFT.44	-	-
			JA5-ADC5	R78	R152	JA5.2	-	-
P44	168	P44	TFT-XINPUT1	R153	R79	TFT.43	-	-
			JA5-ADC4	R79	R153	JA5.1	-	-
JA1-ADC3	169	P43	JA1-ADC3	-	-	JA1.12	-	-
P42	170	P42	OnTFT-INT	R405	R124, R370	ONTFT2.5	-	-
			JA1-ADC2	R124	R405, R370	JA1.11	-	-
			JA2-RCAP_IRQ	R370	R405, R124	JA2.9	R410	R404
JA1-ADC1	171	P41	JA1-ADC1	-	-	JA1.10	-	-
P40	173	P40	RV1-ADC	R361	R369	RV1	-	-
			JA1-ADC0	R369	R361	JA1.9	-	-
VREFH0	174	-	UC_VCC	R105	R106	-	-	-
			JA1-VREFH	R106	R105	JA1.7	-	-
VREFL0	172	-	GROUND	R104	R103	-	-	-
			JA1-AVSS	R103	R104	JA1.6	-	-
AVCC0-1	175, 3	-	UC_VCC	R108	R109 or R110, R107	-	-	-
			JA1-AVCC	R107	R109 or R110, R108	JA1.5		
			Board_3V3	R110, R109	R108, R107	-	-	-
AVSS0-1	1, 5	-	GROUND	R112	R111	-	-	-
			JA1-AVSS	R111	R112	JA1.6	-	-

Table 6-7: Analog Power & ADC & DAC Configuration Option Links

6.7 BUS & SDRAM Configuration

Table 6-8 to Table 6-10 below details the function of the option links associated with BUS & SDRAM Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P10	68	P10	SERIAL-CTS	R29	R36	U20.2	-	-
			JA3-ALE	R36	R29	JA3.46	R421	R422
P26	37	P26	RSPI-MOSI	R301	R302, R317	U6.5	-	-
			JA3-CSc	R302	R301, R317	JA3.45	R148	R424
			TFT-MOSI	R317	R301, R302	TFT.31	-	-
JA3-BCLK	69	P53	JA3-BCLK	R329	-	JA3.44	R426	R425
P52	70	P52	SERIAL-RXD	R121	R436, R122	U20.3	-	R60, R448, R483
			JA2-RXDa	R122	R121, R436	JA2.8	-	-
			JA3-RDn	R436	R121, R122	JA3.25	-	-
P51	71	P51	JA3-WRHn	R334, R330	R331, R333	JA3.47	R419	R420
			JA3-WAIT	R333, R330	R331, R334	JA3.45	R424	R148
			JA2-SCKa	R331, R330	R334, R333	JA2.10	-	-
P50	72	P50	SERIAL-TXD	R126	R127, R313, R314	U21.3	-	R64, R452, R482
			JA2-TXDa	R127	R126, R313, R314	JA2.6	-	-
			JA3-WRn	R313	R314, R126, R127	JA3.26	R433	R434
			JA3-WRLn	R314	R313, R126, R127	JA3.48	R417	R416
P67	120	P67	SDRAM-DQMH	R132	R413	U12.39	-	-
			JA3-DQMH	R413	R132	JA3.47	R420	R419
P66	122	P66	SDRAM-DQML	R388	R387	U12.15	-	-
			JA3-DQML	R387	R388	JA3.48	R416	R417
P65	124	P65	SDRAM-CKE	R130	R131	U12.37	-	-
			JA3-CKE	R131	R130	JA3.46	R422	R421
P64	136	P64	SDRAM-WEn	R390	R389	U12.16	-	-
			JA3-WEn	R389	R390	JA3.26	R434	R433
P63	137	P63	SDRAM-CASn	-	-	U12.17	-	-
			JA3-CAS	-	-	JA3.49	-	-
P62	138	P62	SDRAM-RASn	-	-	U12.18	-	-
			JA3-RAS	-	-	JA3.50	-	-
P61	139	P61	SDRAM-SDCSn	R393	R394	U12.19	-	-
			JA3-CSb	R394	R393	JA3.28	-	-
JA3-CSa	141	P60	JA3-CSa	-	-	JA3.27	-	-
P70	128	P70	SDRAM-SDCLK	R352, R353	R346	U12.38	-	-
			JA3-SDCLK	R346, R353	R352	JA3.44	R425	R426
JA3-A22	152	P96	JA3-A22	-	-	JA3.43	-	-
JA3-A21	155	P95	JA3-A21	-	-	JA3.42	-	-
JA3-A20	157	P94	JA3-A20	-	-	JA3.41	-	-
P93	159	P93	JA3-A19	R427, R363	R89	JA3.40	-	-
			JA2-M1POE	R89, R363	R427	JA2.24	-	-
P92	160	P92	JA3-A18	R428, R362	R385	JA3.39	-	-
			OnTFT-SCL	R385, R362	R428	OnTFT2.3	-	-
			TFT-SCL			JA1.26	R386	R82
JA3-A17	161	P91	JA3-A17	-	-	JA3.38	-	-
P90	163	P90	JA3-A16	R429, R371	R397	JA3.37	-	-
			OnTFT-SDA	R397, R371	R429	OnTFT2.4	-	-
			TFT-SDA			JA1.25	R396	R88
PB0	104	PB0	JA6-M1WIN	R44, SW4.3:ON	-	JA6.16	-	-
			OnTFT-R3	SW4.4:ON	R44, SW4.3:OFF	ONTFT1.8	MR1	-
			SDRAM-A8	-	R44, SW4.3:OFF	U12.32	-	-
			JA3-A8		SW4.4:OFF	JA3.9	-	-

Table 6-8: BUS & SDRAM Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PA7	106	PA7	OnTFT-R4	SW4.4:ON	SW4.3:OFF	ONTFT1.9	MR2	-
			SDRAM-A7	-	SW4.4:OFF, SW4.3:OFF	U12.31	-	-
			JA3-A7			JA3.8	-	-
PA6	107	PA6	OnTFT-R5	SW4.4:ON	SW4.3:OFF	ONTFT1.10	MR2	-
						ONTFT1.5	MR1	-
			SDRAM-A6	-	SW4.4:OFF, SW4.3:OFF	U12.30	-	-
			JA3-A6			JA3.7	-	-
PA5	108	PA5	OnTFT-R6	SW4.4:ON	SW4.3:OFF	ONTFT1.11	MR2	-
						ONTFT1.6	MR1	-
			SDRAM-A5	-	SW4.4:OFF, SW4.3:OFF	U12.29	-	-
			JA3-A5			JA3.6	-	-
PA4	109	PA4	OnTFT-R7	SW4.4:ON	-	ONTFT1.12	MR2	-
						ONTFT1.7	MR1	-
			SDRAM-A4	-	SW4.4:OFF	U12.26	-	-
			JA3-A4			JA3.5	-	-
PA3	110	PA3	OnTFT-G2	SW4.4:ON	-	ONTFT1.15	MR3	-
			SDRAM-A3	-	SW4.4:OFF	U12.25	-	-
			JA3-A3			JA3.4	-	-
PA2	112	PA2	OnTFT-G3	SW4.4:ON	-	ONTFT1.16	MR3	-
			SDRAM-A2	-	SW4.4:OFF	U12.24	-	-
			JA3-A2			JA3.3	-	-
PA1	114	PA1	OnTFT-G4	SW4.4:ON	-	ONTFT1.17	MR4	-
			SDRAM-A1	-	SW4.4:OFF	U12.23	-	-
			JA3-A1			JA3.2	-	-
PA0	118	PA0	JA3-A0	R437	R343, R395, R96	JA3.1	-	-
			OnTFT-G5	R343	R437, R395, R96	ONTFT1.18	MR4	-
			JA2-M1VP	R395	R343, R437, R96	JA2.15	-	-
			JA2-TIMOUT1	R96	R343, R437, R395	JA2.20	-	-
PB7	94	PB7	JA3-A15	R260	R258, R259, R257	JA3.16	-	-
			OnTFT-BACKLIGHT	R258	R260, R259, R257	U16.5	-	-
			TFT-BACKLIGHT	R259	R258, R260, R257	TFT.35	-	-
			SDSI-D1	R257	R258, R260, R259	SDSI1.15	R256	-
PB6	95	PB6	SDRAM-A14	R253	R254	U12.21	-	-
			JA3-A14			JA3.15	-	-
			SDSI-D0	R254	R253	SDSI1.13	R255	
PB5	96	PB5	SDSI-CLK	R75, R339, SW4.3:ON	-	SDSI1.11	R252	-
			OnTFT-CLK	SW4.4:ON, R339	R75, SW4.3:OFF	ONTFT1.30	R356	-
			SDRAM-A13	R339	R75, SW4.4:OFF, SW4.3:OFF	U12.20	-	-
			JA3-A13			JA3.14	-	-
PB4	97	PB4	SDSI-CMD	R355, SW4.3:ON	-	SDSI1.5	R251	-
			OnTFT-VSYNC	SW4.4:ON	R355, SW4.3:OFF	ONTFT1.33	MR7	-
			SDRAM-A12	-	R355, SW4.4:OFF, SW4.3:OFF	U12.35	-	-
			JA3-A12			JA3.13	-	-
PB2	99	PB2	SDSI-D2	R61, SW4.3:ON	-	SDSI1.1	R247	-
			OnTFT-HSYNC	SW4.4:ON	R61, SW4.3:OFF	ONTFT1.32	MR7	-
			SDRAM-A10	-	R61, SW4.4:OFF, SW4.3:OFF	U12.34	-	-
			JA3-A10			JA3.11	-	-
PB1	100	PB1	OnTFT-DEN	SW4.4:ON	SW4.3:OFF	ONTFT1.34	MR7	-
			SDRAM-A9	-	SW4.4:OFF, SW4.3:OFF	U12.33	-	-
			JA3-A9			JA3.10	-	-
PB3	98	PB3	SDRAM-A11	R248	R249	U12.22	-	-
			JA3-A11			JA3.12	-	-
			SDSI-D3	R249	R248	SDSI1.3	R250	-

Table 6-9: BUS & SDRAM Configuration Option Links (2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PD7	143	PD7	QSPI-IO1	SW4.4:ON	-	U18.2	-	-
			SDRAM-D7	-	SW4.4:OFF	U12.13	-	-
			JA3-D7			JA3.24	-	-
PD6	145	PD6	QSPI-IO0	SW4.4:ON	-	U18.5	-	-
			SDRAM-D6	-	SW4.4:OFF	U12.11	-	-
			JA3-D6			JA3.23	-	-
PD5	147	PD5	QSPI-CLK	SW4.4:ON, R365	-	U18.6	-	-
			SDRAM-D5	R365	SW4.4:OFF	U12.10	-	-
			JA3-D5			JA3.22	-	-
PD4	148	PD4	QSPI-CS	SW4.4:ON	-	U18.1	-	-
			SDRAM-D4	-	SW4.4:OFF	U12.8	-	-
			JA3-D4			JA3.21	-	-
PD3	150	PD3	QSPI-IO3	SW4.4:ON	-	U18.7	-	-
			SDRAM-D3	-	SW4.4:OFF	U12.7	-	-
			JA3-D3			JA3.20	-	-
PD2	154	PD2	QSPI-IO2	SW4.4:ON	-	U18.3	-	-
			SDRAM-D2	-	SW4.4:OFF	U12.5	-	-
			JA3-D2			JA3.19	-	-
PD1	156	PD1	SDRAM-D1	-	-	U12.4	-	-
			JA3-D1	-	-	JA3.18	-	-
PD0	158	PD0	SDRAM-D0	R383	-	U12.2	-	-
			JA3-D0			JA3.17	-	-
PE7	125	PE7	OnTFT-G6	SW4.4:ON	-	ONTFT1.19	MR4	-
						ONTFT1.13	MR3	-
			SDRAM-D15	-	SW4.4:OFF	U12.53	-	-
			JA3-D15			JA3.36	-	-
PE6	126	PE6	OnTFT-G7	SW4.4:ON	-	ONTFT1.20	MR4	-
						ONTFT1.14	MR3	-
			SDRAM-D14	-	SW4.4:OFF	U12.51	-	-
			JA3-D14			JA3.35	-	-
PE5	130	PE5	OnTFT-B3	SW4.4:ON	-	ONTFT1.24	MR5	-
			SDRAM-D13	-	SW4.4:OFF	U12.50	-	-
			JA3-D13			JA3.34	-	-
PE4	131	PE4	OnTFT-B4	SW4.4:ON	-	ONTFT1.25	MR6	-
			SDRAM-D12	-	SW4.4:OFF	U12.48	-	-
			JA3-D12			JA3.33	-	-
PE3	132	PE3	OnTFT-B5	SW4.4:ON	-	ONTFT1.26	MR6	-
						ONTFT1.21	MR5	-
			SDRAM-D11	-	SW4.4:OFF	U12.47	-	-
			JA3-D11			JA3.32	-	-
PE2	133	PE2	OnTFT-B6	SW4.4:ON	-	ONTFT1.27	MR6	-
						ONTFT1.22	MR5	-
			SDRAM-D10	-	SW4.4:OFF	U12.45	-	-
			JA3-D10			JA3.31	-	-
PE1	134	PE1	OnTFT-B7	SW4.4:ON	-	ONTFT1.28	MR6	-
						ONTFT1.23	MR5	-
			SDRAM-D9	-	SW4.4:OFF	U12.44	-	-
			JA3-D9			JA3.30	-	-
PE0	135	PE0	SDRAM-D8	-	-	U12.42	-	-
			JA3-D8	-	-	JA3.29	-	-

Table 6-10: BUS & SDRAM Configuration Option Links (3)

6.8 CAN Configuration

Table 6-11 below details the function of the option links associated with CAN Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P33	28	P33	PDC-PCKO	R208, R340	R473, R468, R62	J15.5	-	-
			CAN1RX	R473, R340	R208, R468, R62	U3.4	-	-
			JA2-IRQc_M1HSIN2	R468, R340	R473, R208, R62	JA2.23	R469	R373
			JA5-CAN1RX	R62, R340	R473, R208, R468	JA5.6	-	-
P32	29	P32	PDC-VSYNC	R196	R156, R157, R66	J15.9	R211	-
			CAN1TX	R156	R196, R157, R66	U3.1	-	-
			JA2-IRQb_M1HSIN1	R157	R156, R196, R66	JA2.9	R404	R410
			JA5-CAN1TX	R66	R156, R196, R157	JA5.5	-	-

Table 6-11: CAN Configuration Option Links

6.9 Ethernet Configuration

Table 6-12 below details the function of the option links associated with Ethernet Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P83	74	P83	ET-ET0CRS_RMII0CRSDV	R269	R268	U14.40	-	-
			TFT-G3	R268	R269	TFT.15	-	-
P82	79	P82	ET-ET0ETXD1_RMII0TXD1	R321	R320	U14.4	R307	-
			TFT-R2	R320	R321	TFT.19	-	-
P81	80	P81	ET-ET0ETXD0_RMII0TXD0	R305	R319	U14.3	R306	-
			TFT-R3	R319	R305	TFT.20	-	-
P80	81	P80	ET-ET0TXEN_RMII0TXDEN	R304	R318	U14.2	-	-
			TFT-R4	R318	R304	TFT.21	-	-
PC7	76	PC7	ET-ET0COL	R409 or J12 (1-2pin short)	R402	U14.42	-	-
			E1-UB	J12 (2-3pin short)	R409, R402	E1.10	-	-
			DSW-UB			SW4.2	-	-
			TFT-G4	R402	R409, J12 open	TFT.16	-	-
PC6	77	PC6	ET-ET0ETXD3	R324	R325	U14.6	R308	-
			TFT-G5	R325	R324	TFT.17	-	-
PC5	78	PC5	ET-ET0ETXD2	R17	R27	U14.5	R322	-
			TFT-R1	R27	R17	TFT.18	-	-
PC4	82	PC4	ET-ET0TXCLK	R16, R26	R294	U14.1	R303	-
			TFT-R5	R294, R26	R16	TFT.22	-	-
PC2	86	PC2	ET-ET0RXDV	R267	R265	U14.39	-	-
			JA6-RXDc	R265	R267	JA6.12	-	-
PC1	89	PC1	ET-ET0ERXD2	R288, R38	R287	U14.44	R290	-
			JA6-SCKc	R287, R38	R288	JA6.11	-	-
PC0	91	PC0	ET-ET0ERXD3	R315	R316	U14.43	R279	-
			JA1-IRQd	R316	R315	JA1.23	-	-
ET-ET0LINKSTA	27	P34	ET-ET0LINKSTA	-	-	ETHERNET1.11	-	-
						U14.28	-	-
ET-ET0RXER_RMII0RXER	84	P77	ET-ET0RXER_RMII0RXER	-	-	U14.41	-	-
ET-ET0RXCLK_REF50CK0	85	P76	ET-ET0RXCLK_REF50CK0	R25	-	U14.38	R266	-
ET-ET0ERXD0_RMII0RXD0	87	P75	ET-ET0ERXD0_RMII0RXD0	-	-	U14.46	R300	-
ET-ET0ERXD1_RMII0RXD1	88	P74	ET-ET0ERXD1_RMII0RXD1	-	-	U14.45	R299	-
ET-ET0MDC	101	P72	ET-ET0MDC	-	-	U14.31	-	-
ET-ET0MDIO	102	P71	ET-ET0MDIO	-	-	U14.30	-	-
RESn	21	-	E1-RESn	-	-	E1.13	-	-
			SW-RESn	-	-	RES1(Switch)	-	-
			JA2-RESn	-	-	JA2.1	-	-
			PDC-RESn	-	-	J15.6	R207	-
			TFT-RESn	-	-	TFT.33	R149	-
			ET-RESn	-	-	U14.29	R264	-
			OnTFT-RESn	-	-	ONTFT2.6	R137	-

Table 6-12: Ethernet Configuration Option Links

Table 6-13 below details the function of the jumpers associated with the Ethernet Configuration.

Reference	Jumper Position	Explanation	Related Ref.
J8(DNF) *1	Shorted Pin1-2	RMII Master Mode	-
	All open	MII Mode	-

Table 6-13: Ethernet Configuration Jumper Option Links

*1: Jumper J8 is not fitted on the default CPU board. Same as Jumper Position “All open”.

6.10 General IO & LED Configuration

Table 6-14 below details the function of the option links associated with General IO & LED Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P57	63	P57	TFT-B4	R140	R95	TFT.10	-	-
			JA1-IO6	R95	R140	JA1.21	-	-
P56	64	P56	TFT-B5	R141	R94	TFT.11	-	-
			JA1-IO7	R94	R141	JA1.22	-	-
P73	93	P73	LED0	R223	-	LED0.K	R227	-
P84	62	P84	TFT-B3	R139	R97	TFT.9	-	-
			JA1-IO5	R97	R139	JA1.20	-	-
P85	61	P85	TFT-B2	R138	R100	TFT.8	-	-
			JA1-IO4	R100	R138	JA1.19	-	-
P97	149	P97	OnTFT-DISP	R360	R101, R41	ONTFT1.31	MR7	-
			JA1-IO3	R101	R360, R41	JA1.18	-	-
			JA5-LCDDISP	R41	R360, R101	JA5.20	-	-
LED1	111	PG7	-	-	-	LED1.K	R227	-
LED2	113	PG6	-	-	-	LED2.K	R227	-
LED3	116	PG5	-	-	-	LED3.K	R227	-
PG3	121	PG3	PMOD1-IO3	R229	R57	PMOD1.10	R240	-
			JA5-LCDPWR	R57	R229	JA5.9	-	-
PG2	123	PG2	JA1-IO0	R116	R347	JA1.15	-	-
			SERIAL-RTS	R347	R116	U21.2	-	-
PG1	144	PG1	TFT-YDRIVE	R150	R114	TFT.42	-	-
			JA1-IO1	R114	R150	JA1.16	-	-
PG0	146	PG0	TFT-XDRIVE	R151	R113	TFT.41	-	-
			JA1-IO2	R113	R151	JA1.17	-	-

Table 6-14: General IO & LED Configuration Option Links

6.11 GLCDC Configuration

Table 6-15 and Table 6-16 below details the function of the option links associated with GLCDC Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P42	170	P42	OnTFT-INT	R405	R124, R370	ONTFT2.5	-	-
			JA1-ADC2	R124	R405, R370	JA1.11	-	-
			JA2-RCAP_IRQ	R370	R405, R124	JA2.9	R410	R404
P97	149	P97	OnTFT-DISP	R360	R101, R41	ONTFT1.31	MR7	-
			JA1-IO3	R101	R360, R41	JA1.18	-	-
			JA5-LCDDISP	R41	R360, R101	JA5.20	-	-
P92	160	P92	JA3-A18	R428, R362	R385	JA3.39	-	-
			OnTFT-SCL	R385, R362	R428	OnTFT2.3	-	-
			TFT-SCL			JA1.26	R386	R82
P90	163	P90	JA3-A16	R429, R371	R397	JA3.37	-	-
			OnTFT-SDA	R397, R371	R429	OnTFT2.4	-	-
			TFT-SDA			JA1.25	R396	R88
PB0	104	PB0	JA6-M1WIN	R44, SW4.3:ON	-	JA6.16	-	-
			OnTFT-R3	SW4.4:ON	R44, SW4.3:OFF	ONTFT1.8	MR1	-
			SDRAM-A8	-	R44, SW4.3:OFF	U12.32	-	-
			JA3-A8		SW4.4:OFF	JA3.9	-	-
PA7	106	PA7	OnTFT-R4	SW4.4:ON	SW4.3:OFF	ONTFT1.9	MR2	-
			SDRAM-A7	-	SW4.4:OFF,	U12.31	-	-
			JA3-A7		SW4.3:OFF	JA3.8	-	-
PA6	107	PA6	OnTFT-R5	SW4.4:ON	SW4.3:OFF	ONTFT1.10	MR2	-
						ONTFT1.5	MR1	-
			SDRAM-A6	-	SW4.4:OFF,	U12.30	-	-
			JA3-A6		SW4.3:OFF	JA3.7	-	-
PA5	108	PA5	OnTFT-R6	SW4.4:ON	SW4.3:OFF	ONTFT1.11	MR2	-
						ONTFT1.6	MR1	-
			SDRAM-A5	-	SW4.4:OFF,	U12.29	-	-
			JA3-A5		SW4.3:OFF	JA3.6	-	-
PA4	109	PA4	OnTFT-R7	SW4.4:ON	-	ONTFT1.12	MR2	-
						ONTFT1.7	MR1	-
			SDRAM-A4	-	SW4.4:OFF	U12.26	-	-
			JA3-A4			JA3.5	-	-
PA3	110	PA3	OnTFT-G2	SW4.4:ON	-	ONTFT1.15	MR3	-
			SDRAM-A3	-	SW4.4:OFF	U12.25	-	-
			JA3-A3			JA3.4	-	-
PA2	112	PA2	OnTFT-G3	SW4.4:ON	-	ONTFT1.16	MR3	-
			SDRAM-A2	-	SW4.4:OFF	U12.24	-	-
			JA3-A2			JA3.3	-	-
PA1	114	PA1	OnTFT-G4	SW4.4:ON	-	ONTFT1.17	MR4	-
			SDRAM-A1	-	SW4.4:OFF	U12.23	-	-
			JA3-A1			JA3.2	-	-
PA0	118	PA0	JA3-A0	R437	R343, R395, R96	JA3.1	-	-
			OnTFT-G5	R343	R437, R395, R96	ONTFT1.18	MR4	-
			JA2-M1VP	R395	R343, R437, R96	JA2.15	-	-
			JA2-TIMOUT1	R96	R343, R437, R395	JA2.20	-	-
PB7	94	PB7	JA3-A15	R260	R258, R259, R257	JA3.16	-	-
			OnTFT-BACKLIGHT	R258	R260, R259, R257	U16.5	-	-
			TFT-BACKLIGHT	R259	R258, R260, R257	TFT.35	-	-
			SDSI-D1	R257	R258, R260, R259	SDSI1.15	R256	-

Table 6-15: GLCDC Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PB5	96	PB5	SDSI-CLK	R75, R339, SW4.3:ON	-	SDSI1.11	R252	-
			OnTFT-CLK	SW4.4:ON, R339	R75, SW4.3:OFF	ONTFT1.30	R356	-
			SDRAM-A13	R339	R75, SW4.4:OFF, SW4.3:OFF	U12.20	-	-
			JA3-A13			JA3.14	-	-
PB4	97	PB4	SDSI-CMD	R355, SW4.3:ON	-	SDSI1.5	R251	-
			OnTFT-VSYNC	SW4.4:ON	R355, SW4.3:OFF	ONTFT1.33	MR7	-
			SDRAM-A12	-	R355, SW4.4:OFF, SW4.3:OFF	U12.35	-	-
			JA3-A12			JA3.13	-	-
PB2	99	PB2	SDSI-D2	R61, SW4.3:ON	-	SDSI1.1	R247	-
			OnTFT-HSYNC	SW4.4:ON	R61, SW4.3:OFF	ONTFT1.32	MR7	-
			SDRAM-A10	-	R61, SW4.4:OFF, SW4.3:OFF	U12.34	-	-
			JA3-A10			JA3.11	-	-
PB1	100	PB1	OnTFT-DEN	SW4.4:ON	SW4.3:OFF	ONTFT1.34	MR7	-
			SDRAM-A9	-	SW4.4:OFF, SW4.3:OFF	U12.33	-	-
			JA3-A9			JA3.10	-	-
PE7	125	PE7	OnTFT-G6	SW4.4:ON	-	ONTFT1.19	MR4	-
						ONTFT1.13	MR3	-
			SDRAM-D15	-	SW4.4:OFF	U12.53	-	-
			JA3-D15			JA3.36	-	-
PE6	126	PE6	OnTFT-G7	SW4.4:ON	-	ONTFT1.20	MR4	-
						ONTFT1.14	MR3	-
			SDRAM-D14	-	SW4.4:OFF	U12.51	-	-
			JA3-D14			JA3.35	-	-
PE5	130	PE5	OnTFT-B3	SW4.4:ON	-	ONTFT1.24	MR5	-
			SDRAM-D13	-	SW4.4:OFF	U12.50	-	-
			JA3-D13			JA3.34	-	-
PE4	131	PE4	OnTFT-B4	SW4.4:ON	-	ONTFT1.25	MR6	-
			SDRAM-D12	-	SW4.4:OFF	U12.48	-	-
			JA3-D12			JA3.33	-	-
PE3	132	PE3	OnTFT-B5	SW4.4:ON	-	ONTFT1.26	MR6	-
						ONTFT1.21	MR5	-
			SDRAM-D11	-	SW4.4:OFF	U12.47	-	-
			JA3-D11			JA3.32	-	-
PE2	133	PE2	OnTFT-B6	SW4.4:ON	-	ONTFT1.27	MR6	-
						ONTFT1.22	MR5	-
			SDRAM-D10	-	SW4.4:OFF	U12.45	-	-
			JA3-D10			JA3.31	-	-
PE1	134	PE1	OnTFT-B7	SW4.4:ON	-	ONTFT1.28	MR6	-
						ONTFT1.23	MR5	-
			SDRAM-D9	-	SW4.4:OFF	U12.44	-	-
			JA3-D9			JA3.30	-	-
RESn	21	-	E1-RESn	-	-	E1.13	-	-
			SW-RESn	-	-	RES1(Switch)	-	-
			JA2-RESn	-	-	JA2.1	-	-
			PDC-RESn	-	-	J15.6	R207	-
			TFT-RESn	-	-	TFT.33	R149	-
			ET-RESn	-	-	U14.29	R264	-
			OnTFT-RESn	-	-	ONTFT2.6	R137	-

Table 6-16: GLCDC Configuration Option Links (2)

6.12 I2C & EEPROM Configuration

Table 6-17 and **Table 6-18** below detail the function of the option links associated with I2C & EEPROM Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P13	52	P13	E2P-SDA	R328, R327	R147	U4.5	R118	-
			JA1-SDA			JA1.25	R88	R396
			TFT-VSYNC	R147, R327	R328	TFT.27	-	-
P12	53	P12	E2P-SCL	R312, R311	R46	U4.6	R123	-
			JA1-SCL			JA1.26	R82	R386
			JA6-M1UIN	R46, R311	R312	JA6.14	-	-

Table 6-17: I2C & EEPROM Configuration Option Links (1)

Reference	Explanation	Fit	DNF	Related Ref.
SDA0[FM+], SCL0[FM+]	Connect pull-up resistor to Board_3V3.	R134	R133	U4
	Connect pull-up resistor to Board_5V.	R133	R134	U4
WP	EEPROM Write protect.	R407	-	U4
A0	Device address (0xA6).	R135	-	U4
	Device address (0xA4).	-	R135	U4
SSDA6(PDC-SSDA) , SSCL6(PDC-SSCL)	Connect pull-up resistor to Board_3V3.	R190	-	J15.19, J15.20

Table 6-18: I2C & EEPROM Configuration Option Links (2)

6.13 IRQ & Switch Configuration

Table 6-19 and **Table 6-20** below details the function of the option links associated with IRQ & Switch Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P07	176	P07	SW3	R478	-	SW3	-	-
			JA1-ADTRG	R125	-	JA1.8	-	-
P05	2	P05	SW2	R479	R119	SW2	-	-
			JA1-DAC1	R119	R479	JA1.14	-	-
P03	4	P03	SW1	R480	R120	SW1	-	-
			JA1-DAC0	R120	R480	JA1.13	-	-
P15	50	P15	PDC-PIXD0	R203	R238, R412, R376	J15.18	R218	-
			PMOD1-IO0	R238	R203, R412, R376	PMOD1.7	R237	-
			JA2-IRQa_M1HSIN0	R412	R203, R238, R376	JA2.7	-	-
			JA2-TIMIN0	R376	R203, R238, R412	JA2.21	-	-
P10	68	P10	SERIAL-CTS	R29	R36	U20.2	-	-
			JA3-ALE	R36	R29	JA3.46	R421	R422
P21	44	P21	PDC-PIXD5	R200, R493	R179, R377, R488	J15.13	R215	-
			PMOD2-IO0	R179, R493	R200, R377, R488	PMOD2.7	R180	-
			JA2-TIMOUT0	R377, R493	R200, R179, R488	JA2.19	-	-
			SDHI-CLK	R488, R493	R200, R179, R377	SDHI1.5	R456	-
P20	45	P20	PDC-PIXD4	R199	R174, R374, R489	J15.14	R214	-
			PMOD2-IO1	R174	R199, R374, R489	PMOD2.8	R176	-
			JA2-M1ENC	R374	R199, R174, R489	JA2.23	R373	R469
			SDHI-CMD	R489	R199, R174, R374	SDHI1.2	R455	-

Table 6-19: IRQ & Switch Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P35	26	P35	JP-UPSEL	-	-	J9.2	-	-
			JA2-NMIn	R414	-	JA2.3	-	-
P33	28	P33	PDC-PCKO	R208, R340	R473, R468, R62	J15.5	-	-
			CAN1RX	R473, R340	R208, R468, R62	U3.4	-	-
			JA2-IRQc_M1HSIN2	R468, R340	R473, R208, R62	JA2.23	R469	R373
			JA5-CAN1RX	R62, R340	R473, R208, R468	JA5.6	-	-
P32	29	P32	PDC-VSYNC	R196	R156, R157, R66	J15.9	R211	-
			CAN1TX	R156	R196, R157, R66	U3.1	-	-
			JA2-IRQb_M1HSIN1	R157	R156, R196, R66	JA2.9	R404	R410
			JA5-CAN1TX	R66	R156, R196, R157	JA5.5	-	-
P42	170	P42	OnTFT-INT	R405	R124, R370	ONTFT2.5	-	-
			JA1-ADC2	R124	R405, R370	JA1.11	-	-
			JA2-RCAP_IRQ	R370	R405, R124	JA2.9	R410	R404
PC0	91	PC0	ET-ET0ERXD3	R315	R316	U14.43	R279	-
			JA1-IRQd	R316	R315	JA1.23	-	-
PMOD1-IO1	9	PF5	PMOD1-IO1	-	-	PMOD1.8	R233	-
RESn	21	-	E1-RESn	-	-	E1.13	-	-
			SW-RESn	-	-	RES1(Switch)	-	-
			JA2-RESn	-	-	JA2.1	-	-
			PDC-RESn	-	-	J15.6	R207	-
			TFT-RESn	-	-	TFT.33	R149	-
			ET-RESn	-	-	U14.29	R264	-
			OnTFT-RESn	-	-	ONTFT2.6	R137	-

Table 6-20: IRQ & Switch Configuration Option Links (2)

6.14 MTU & POE Configuration

Table 6-21 and **Table 6-22** below details the function of the option links associated with MTU & POE Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P17	46	P17	PDC-PIXD3	R202	R171, R43, R490	J15.15	R217	-
			PMOD2-IO2	R171	R202, R43, R490	PMOD2.9	R173	-
			JA6-M1TOGGLE	R43	R202, R171, R490	JA6.13	-	-
			SDHI-D3	R490	R202, R171, R43	SDHI1.1	R454	-
P15	50	P15	PDC-PIXD0	R203	R238, R412, R376	J15.18	R218	-
			PMOD1-IO0	R238	R203, R412, R376	PMOD1.7	R237	-
			JA2-IRQa_M1HSIN0	R412	R203, R238, R376	JA2.7	-	-
			JA2-TIMIN0	R376	R203, R238, R412	JA2.21	-	-
P12	53	P12	E2P-SCL	R312, R311	R46	U4.6	R123	-
			JA1-SCL			JA1.26	R82	R386
			JA6-M1UIN	R46, R311	R312	JA6.14	-	-
P11	67	P11	TFT-G2	R144	R42	TFT.14	-	-
			JA6-M1VIN	R42	R144	JA6.15	-	-

Table 6-21: MTU & POE Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P25	38	P25	PDC-HSYNC	R332, R195	R471, R484	J15.10	R210	-
			JA2-M1TRDCLK	R332, R471	R195, R484	JA2.26	-	-
			SDHI-CD	R332, R484	R195, R471	SDHI1.10	R192	-
P24	40	P24	PDC-PIXCLK	R33, R194	R191, R485	J15.8	R209	-
			JA2-M1TRCCLK	R33, R191	R194, R485	JA2.25	-	-
			SDHI-WP	R33, R485	R194, R191	SDHI1.12	R206	-
P23	42	P23	PDC-PIXD7	R198	R115, R486	J15.11	R213	-
			JA2-M1UN	R115	R198, R486	JA2.14	-	-
			SDHI-D1	R486	R198, R115	SDHI1.8	R458	-
P22	43	P22	PDC-PIXD6	R197	R398, R487	J15.12	R212	-
			JA2-M1UP	R398	R197, R487	JA2.13	-	-
			SDHI-D0	R487	R197, R398	SDHI1.7	R457	-
P21	44	P21	PDC-PIXD5	R200	R179, R377, R488	J15.13	R215	-
			PMOD2-IO0	R179	R200, R377, R488	PMOD2.7	R180	-
			JA2-TIMOUT0	R377	R200, R179, R488	JA2.19	-	-
			SDHI-CLK	R488	R200, R179, R377	SDHI1.5	R456	-
P20	45	P20	PDC-PIXD4	R199	R174, R374, R489	J15.14	R214	-
			PMOD2-IO1	R174	R199, R374, R489	PMOD2.8	R176	-
			JA2-M1ENC	R374	R199, R174, R489	JA2.23	R373	R469
			SDHI-CMD	R489	R199, R174, R374	SDHI1.2	R455	-
P33	28	P33	PDC-PCKO	R208, R340	R473, R468, R62	J15.5	-	-
			CAN1RX	R473, R340	R208, R468, R62	U3.4	-	-
			JA2-IRQc_M1HSIN2	R468, R340	R473, R208, R62	JA2.23	R469	R373
			JA5-CAN1RX	R62, R340	R473, R208, R468	JA5.6	-	-
P32	29	P32	PDC-VSYNC	R196	R156, R157, R66	J15.9	R211	-
			CAN1TX	R156	R196, R157, R66	U3.1	-	-
			JA2-IRQb_M1HSIN1	R157	R156, R196, R66	JA2.9	R404	R410
			JA5-CAN1TX	R66	R156, R196, R157	JA5.5	-	-
P54	66	P54	TFT-G1	R143	R73, R384	TFT.13	-	-
			JA6-DACK	R73	R143, R384	JA6.2	-	-
			JA2-M1WP	R384	R143, R73	JA2.17	-	-
P87	47	P87	PDC-PIXD2	R201	R102, R91, R491	J15.16	R216	-
			JA2-M1VN	R102	R201, R91, R491	JA2.16	-	-
			JA2-TIMIN1	R91	R201, R102, R491	JA2.22	-	-
			SDHI-D2	R491	R201, R102, R91	SDHI1.9	R453	-
P93	159	P93	JA3-A19	R427, R363	R89	JA3.40	-	-
			JA2-M1POE	R89, R363	R427	JA2.24	-	-
PA0	118	PA0	JA3-A0	R437	R343, R395, R96	JA3.1	-	-
			OnTFT-G5	R343	R437, R395, R96	ONTFT1.18	MR4	-
			JA2-M1VP	R395	R343, R437, R96	JA2.15	-	-
			JA2-TIMOUT1	R96	R343, R437, R395	JA2.20	-	-
PB0	104	PB0	JA6-M1WIN	R44, SW4.3:ON	-	JA6.16	-	-
			OnTFT-R3	SW4.4:ON	R44, SW4.3:OFF	ONTFT1.8	MR1	-
			SDRAM-A8	-	R44, SW4.3:OFF	U12.32	-	-
			JA3-A8		SW4.4:OFF	JA3.9	-	-
PC3	83	PJ3	JA2-M1WN	R98	R50	JA2.18	-	-
			JA6-TXDc	R50	R98	JA6.9	-	-
PJ3	13	PJ3	PMOD1-CS	R341	R403	PMOD1.1	R235	-
			JA2-M1UD	R403	R341	JA2.11	-	-

Table 6-22: MTU & POE Configuration Option Links (2)

6.15 PDC Configuration

Table 6-23 below details the function of the option links associated with PDC Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P01	7	P01	PMOD1-MISO	R350	R351	PMOD1.3	R230	-
			PDC-SSCL	R351	R350	J15.20	R220, R364	-
P00	8	P00	PMOD1-MOSI	R344	R345	PMOD1.2	R232	-
			PDC-SSDA	R345	R344	J15.19	R221, R357	-
P17	46	P17	PDC-PIXD3	R202	R171, R43, R490	J15.15	R217	-
			PMOD2-IO2	R171	R202, R43, R490	PMOD2.9	R173	-
			JA6-M1TOGGLE	R43	R202, R171, R490	JA6.13	-	-
			SDHI-D3	R490	R202, R171, R43	SDHI1.1	R454	-
P15	50	P15	PDC-PIXD0	R203	R238, R412, R376	J15.18	R218	-
			PMOD1-IO0	R238	R203, R412, R376	PMOD1.7	R237	-
			JA2-IRQa_M1HSIN0	R412	R203, R238, R376	JA2.7	-	-
			JA2-TIMIN0	R376	R203, R238, R412	JA2.21	-	-
P25	38	P25	PDC-HSYNC	R332, R195	R471, R484	J15.10	R210	-
			JA2-M1TRDCLK	R332, R471	R195, R484	JA2.26	-	-
			SDHI-CD	R332, R484	R195, R471	SDHI1.10	R192	-
P24	40	P24	PDC-PIXCLK	R33, R194	R191, R485	J15.8	R209	-
			JA2-M1TRCCLK	R33, R191	R194, R485	JA2.25	-	-
			SDHI-WP	R33, R485	R194, R191	SDHI1.12	R206	-
P23	42	P23	PDC-PIXD7	R198	R115, R486	J15.11	R213	-
			JA2-M1UN	R115	R198, R486	JA2.14	-	-
			SDHI-D1	R486	R198, R115	SDHI1.8	R458	-
P22	43	P22	PDC-PIXD6	R197	R398, R487	J15.12	R212	-
			JA2-M1UP	R398	R197, R487	JA2.13	-	-
			SDHI-D0	R487	R197, R398	SDHI1.7	R457	-
P21	44	P21	PDC-PIXD5	R200	R179, R377, R488	J15.13	R215	-
			PMOD2-IO0	R179	R200, R377, R488	PMOD2.7	R180	-
			JA2-TIMOUT0	R377	R200, R179, R488	JA2.19	-	-
			SDHI-CLK	R488	R200, R179, R377	SDHI1.5	R456	-
P20	45	P20	PDC-PIXD4	R199	R174, R374, R489	J15.14	R214	-
			PMOD2-IO1	R174	R199, R374, R489	PMOD2.8	R176	-
			JA2-M1ENC	R374	R199, R174, R489	JA2.23	R373	R469
			SDHI-CMD	R489	R199, R174, R374	SDHI1.2	R455	-
P33	28	P33	PDC-PCKO	R208, R340	R473, R468, R62	J15.5	-	-
			CAN1RX	R473, R340	R208, R468, R62	U3.4	-	-
			JA2-IRQc_M1HSIN2	R468, R340	R473, R208, R62	JA2.23	R469	R373
			JA5-CAN1RX	R62, R340	R473, R208, R468	JA5.6	-	-
P32	29	P32	PDC-VSYNC	R196	R156, R157, R66	J15.9	R211	-
			CAN1TX	R156	R196, R157, R66	U3.1	-	-
			JA2-IRQb_M1HSIN1	R157	R156, R196, R66	JA2.9	R404	R410
			JA5-CAN1TX	R66	R156, R196, R157	JA5.5	-	-
P87	47	P87	PDC-PIXD2	R201	R102, R91, R491	J15.16	R216	-
			JA2-M1VN	R102	R201, R91, R491	JA2.16	-	-
			JA2-TIMIN1	R91	R201, R102, R491	JA2.22	-	-
			SDHI-D2	R491	R201, R102, R91	SDHI1.9	R453	-
P86	49	P86	PDC-PIXD1	R204	R166, R481	J15.17	R219	-
			PMOD2-IO3	R166	R204, R481	PMOD2.10	R167	-
			SDHI-PE	R481	R204, R166	U13.3	-	-
RESn	21	-	E1-RESn	-	-	E1.13	-	-
			SW-RESn	-	-	RES1(Switch)	-	-
			JA2-RESn	-	-	JA2.1	-	-
			PDC-RESn	-	-	J15.6	R207	-
			TFT-RESn	-	-	TFT.33	R149	-
			ET-RESn	-	-	U14.29	R264	-
			OnTFT-RESn	-	-	ONTFT2.6	R137	-

Table 6-23: PDC Configuration Option Links

6.16 PMOD1 Configuration

Table 6-24 below details the function of the option links associated with PMOD1 Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PMOD1-SCK	6	P02	PMOD1-SCK	R349	-	PMOD1.4	R261	-
P01	7	P01	PMOD1-MISO	R350	R351	PMOD1.3	R230	-
			PDC-SSCL	R351, R364	R350	J15.20	R220	-
P00	8	P00	PMOD1-MOSI	R344	R345	PMOD1.2	R232	-
			PDC-SSDA	R345, R357	R344	J15.19	R221	-
P15	50	P15	PDC-PIXD0	R203	R238, R412, R376	J15.18	R218	-
			PMOD1-IO0	R238	R203, R412, R376	PMOD1.7	R237	-
			JA2-IRQa_M1HSIN0	R412	R203, R238, R376	JA2.7	-	-
			JA2-TIMIN0	R376	R203, R238, R412	JA2.21	-	-
PMOD1-IO1	9	PF5	PMOD1-IO1	-	-	PMOD1.8	R233	-
PMOD1-IO2	119	PG4	PMOD1-IO2	-	-	PMOD1.9	R231	-
PG3	121	PG3	PMOD1-IO3	R229	R57	PMOD1.10	R240	-
			JA5-LCDPWR	R57	R229	JA5.9	-	-
PJ3	13	PJ3	PMOD1-CS	R341	R403	PMOD1.1	R235	-
			JA2-M1UD	R403	R341	JA2.11	-	-

Table 6-24: PMOD1 Configuration Option Links

6.17 PMOD2 Configuration

Table 6-25 below details the function of the option links associated with PMOD2 Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P17	46	P17	PDC-PIXD3	R202	R171, R43, R490	J15.15	R217	-
			PMOD2-IO2	R171	R202, R43, R490	PMOD2.9	R173	-
			JA6-M1TOGGLE	R43	R202, R171, R490	JA6.13	-	-
			SDHI-D3	R490	R202, R171, R43	SDHI1.1	R454	-
P21	44	P21	PDC-PIXD5	R200	R179, R377, R488	J15.13	R215	-
			PMOD2-IO0	R179	R200, R377, R488	PMOD2.7	R180	-
			JA2-TIMOUT0	R377	R200, R179, R488	JA2.19	-	-
			SDHI-CLK	R488	R200, R179, R377	SDHI1.5	R456	-
P20	45	P20	PDC-PIXD4	R199	R174, R374, R489	J15.14	R214	-
			PMOD2-IO1	R174	R199, R374, R489	PMOD2.8	R176	-
			JA2-M1ENC	R374	R199, R174, R489	JA2.23	R373	R469
			SDHI-CMD	R489	R199, R174, R374	SDHI1.2	R455	-
P31	32	P31	RSPI-CS	R275	R15, R14	U6.1	-	-
			TFT-SS	R15	R275, R14	TFT.32	-	-
			PMOD2-CS	R14	R275, R15	PMOD2.1	R187	-
P86	49	P86	PDC-PIXD1	R204	R166, R481	J15.17	R219	-
			PMOD2-IO3	R166	R204, R481	PMOD2.10	R167	-
			SDHI-PE	R481	R204, R166	U13.3	-	-
PF2	31	PF2	E1-TDI_RXD	R447	R448, R170	E1.11	-	-
			SERIAL-RXD	R448	R447, R170	U20.3	-	R60, R121, R483
			PMOD2-MISO	R170	R447, R448	PMOD2.3	R172	-
PF1	34	PF1	E1-TCK	R160, R338	R159	E1.1	-	-
			PMOD2-SCK	R159, R338	R160	PMOD2.4	R161	-
PF0	35	PF0	E1-TDO_TXD	R451	R452, R175	E1.5	-	-
			SERIAL-TXD	R452	R451, R175	U21.3	-	R64, R126, R482
			PMOD2-MOSI	R175	R451, R452	PMOD2.2	R177	-

Table 6-25: PMOD2 Configuration Option Links

6.18 QSPI Configuration

Table 6-26 below details the function of the option links associated with QSPI Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PD7	143	PD7	QSPI-IO1	SW4.4:ON	-	U18.2	-	-
			SDRAM-D7	-	SW4.4:OFF	U12.13	-	-
			JA3-D7			JA3.24	-	-
PD6	145	PD6	QSPI-IO0	SW4.4:ON	-	U18.5	-	-
			SDRAM-D6	-	SW4.4:OFF	U12.11	-	-
			JA3-D6			JA3.23	-	-
PD5	147	PD5	QSPI-CLK	SW4.4:ON, R365	-	U18.6	-	-
			SDRAM-D5	R365	SW4.4:OFF	U12.10	-	-
			JA3-D5			JA3.22	-	-
PD4	148	PD4	QSPI-CS	SW4.4:ON	-	U18.1	-	-
			SDRAM-D4	-	SW4.4:OFF	U12.8	-	-
			JA3-D4			JA3.21	-	-
PD3	150	PD3	QSPI-IO3	SW4.4:ON	-	U18.7	-	-
			SDRAM-D3	-	SW4.4:OFF	U12.7	-	-
			JA3-D3			JA3.20	-	-
PD2	154	PD2	QSPI-IO2	SW4.4:ON	-	U18.3	-	-
			SDRAM-D2	-	SW4.4:OFF	U12.5	-	-
			JA3-D2			JA3.19	-	-

Table 6-26: QSPI Configuration Option Links

6.19 RSPI Configuration

Table 6-27 below details the function of the option links associated with RSPI Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P27	36	P27	RSPI-CLK	R281, R336	R295	U6.6	-	-
			TFT-SCK	R295, R336	R281	TFT.29	-	-
P26	37	P26	RSPI-MOSI	R301	R302, R317	U6.5	-	-
			JA3-CSc	R302	R301, R317	JA3.45	R148	R424
			TFT-MOSI	R317	R301, R302	TFT.31	-	-
P31	32	P31	RSPI-CS	R275	R15, R14	U6.1	-	-
			TFT-SS	R15	R275, R14	TFT.32	-	-
			PMOD2-CS	R14	R275, R15	PMOD2.1	R187	-
P30	33	P30	RSPI-MISO	R285	R286	U6.2	-	-
			TFT-MISO	R286	R285	TFT.30	-	-

Table 6-27: RSPI Configuration Option Links

6.20 Serial & USB to Serial Configuration

Table 6-28 below details the function of the option links associated with Serial & USB to Serial Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P10	68	P10	SERIAL-CTS	R29	R36	U20.2	-	-
			JA3-ALE	R36	R29	JA3.46	R421	R422
P52	70	P52	SERIAL-RXD	R121	R436, R122	U20.3	-	R60, R448, R483
			JA2-RXDa	R122	R121, R436	JA2.8	-	-
			JA3-RDn	R436	R121, R122	JA3.25	-	-
P51	71	P51	JA3-WRHn	R334, R330	R331, R333	JA3.47	R419	R420
			JA3-WAIT	R333, R330	R331, R334	JA3.45	R424	R148
			JA2-SCKa	R331, R330	R334, R333	JA2.10	-	-
P50	72	P50	SERIAL-TXD	R126	R127, R313, R314	U21.3	-	R64, R452, R482
			JA2-TXDa	R127	R126, R313, R314	JA2.6	-	-
			JA3-WRn	R313	R314, R126, R127	JA3.26	R433	R434
			JA3-WRLn	R314	R313, R126, R127	JA3.48	R417	R416
PC3	83	PJ3	JA2-M1WN	R98	R50	JA2.18	-	-
			JA6-TXDc	R50	R98	JA6.9	-	-
PC2	86	PC2	ET-ET0RXDV	R267	R265	U14.39	-	-
			JA6-RXDc	R265	R267	JA6.12	-	-
PC1	89	PC1	ET-ET0ERXD2	R288, R38	R287	U14.44	R290	-
			JA6-SCKc	R287, R38	R288	JA6.11	-	-
PF2	31	PF2	E1-TDI_RXD	R447	R448, R170	E1.11	-	-
			SERIAL-RXD	R448	R447, R170	U20.3	-	R60, R121, R483
			PMOD2-MISO	R170	R447, R448	PMOD2.3	R172	-
PF0	35	PF0	E1-TDO_TXD	R451	R452, R175	E1.5	-	-
			SERIAL-TXD	R452	R451, R175	U21.3	-	R64, R126, R482
			PMOD2-MOSI	R175	R451, R452	PMOD2.2	R177	-
JA2-CTSaRTSa	11	PJ5	JA2-CTSaRTSa	-	-	JA2.12	-	-
PG2	123	PG2	JA1-IO0	R116	R347	JA1.15	-	-
			SERIAL-RTS	R347	R116	U21.2	-	-
PJ2	58	PJ2	TFT-HSYNC	R145	R59, R482	TFT.24	-	-
			JA6-TXDb	R59	R145, R482	JA6.8	-	-
			SERIAL-TXD	R482	R145, R59	U21.3	-	R64, R126, R452
PJ1	59	PJ1	TFT-LCDDEN	R146	R54, R483	TFT.26	-	-
			JA6-RXDb	R54	R146, R483	JA6.7	-	-
			SERIAL-RXD	R483	R146, R54	U20.3	-	R121, R448, R60
PJ0	60	PJ0	TFT-B1	R342	R51	TFT.7	-	-
			JA6-SCKb	R51	R342	JA6.10	-	-

Table 6-28: Serial & USB to Serial Configuration Option Links

6.21 SDHI Configuration

Table 6-29 below details the function of the option links associated with SDHI Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P17	46	P17	PDC-PIXD3	R202	R171, R43, R490	J15.15	R217	-
			PMOD2-IO2	R171	R202, R43, R490	PMOD2.9	R173	-
			JA6-M1TOGGLE	R43	R202, R171, R490	JA6.13	-	-
			SDHI-D3	R490	R202, R171, R43	SDHI1.1	R454	-
P25	38	P25	PDC-HSYNC	R332, R195	R471, R484	J15.10	R210	-
			JA2-M1TRDCLK	R332, R471	R195, R484	JA2.26	-	-
			SDHI-CD	R332, R484	R195, R471	SDHI1.10	R192	-
P24	40	P24	PDC-PIXCLK	R33, R194	R191, R485	J15.8	R209	-
			JA2-M1TRCCLK	R33, R191	R194, R485	JA2.25	-	-
			SDHI-WP	R33, R485	R194, R191	SDHI1.12	R206	-
P23	42	P23	PDC-PIXD7	R198	R115, R486	J15.11	R213	-
			JA2-M1UN	R115	R198, R486	JA2.14	-	-
			SDHI-D1	R486	R198, R115	SDHI1.8	R458	-
P22	43	P22	PDC-PIXD6	R197	R398, R487	J15.12	R212	-
			JA2-M1UP	R398	R197, R487	JA2.13	-	-
			SDHI-D0	R487	R197, R398	SDHI1.7	R457	-
P21	44	P21	PDC-PIXD5	R200	R179, R377, R488	J15.13	R215	-
			PMOD2-IO0	R179	R200, R377, R488	PMOD2.7	R180	-
			JA2-TIMOUT0	R377	R200, R179, R488	JA2.19	-	-
			SDHI-CLK	R488	R200, R179, R377	SDHI1.5	R456	-
P20	45	P20	PDC-PIXD4	R199	R174, R374, R489	J15.14	R214	-
			PMOD2-IO1	R174	R199, R374, R489	PMOD2.8	R176	-
			JA2-M1ENC	R374	R199, R174, R489	JA2.23	R373	R469
			SDHI-CMD	R489	R199, R174, R374	SDHI1.2	R455	-
P87	47	P87	PDC-PIXD2	R201	R102, R91, R491	J15.16	R216	-
			JA2-M1VN	R102	R201, R91, R491	JA2.16	-	-
			JA2-TIMIN1	R91	R201, R102, R491	JA2.22	-	-
			SDHI-D2	R491	R201, R102, R91	SDHI1.9	R453	-
P86	49	P86	PDC-PIXD1	R204	R166, R481	J15.17	R219	-
			PMOD2-IO3	R166	R204, R481	PMOD2.10	R167	-
			SDHI-PE	R481	R204, R166	U13.3	-	-

Table 6-29: SDHI Configuration Option Links

6.22 SDSI Configuration

Table 6-30 below details the function of the option links associated with SDSI Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PB7	94	PB7	JA3-A15	R260	R258, R259, R257	JA3.16	-	-
			OnTFT-BACKLIGHT	R258	R260, R259, R257	U16.5	-	-
			TFT-BACKLIGHT	R259	R258, R260, R257	TFT.35	-	-
			SDSI-D1	R257	R258, R260, R259	SDSI1.15	R256	-
PB6	95	PB6	SDRAM-A14	R253	R254	U12.21	-	-
			JA3-A14			JA3.15	-	-
			SDSI-D0	R254	R253	SDSI1.13	R255	
PB5	96	PB5	SDSI-CLK	R75, R339, SW4.3:ON	-	SDSI1.11	R252	-
			OnTFT-CLK	SW4.4:ON, R339	R75, SW4.3:OFF	ONTFT1.30	R356	-
			SDRAM-A13	R339	R75, SW4.4:OFF, SW4.3:OFF	U12.20	-	-
			JA3-A13			JA3.14	-	-
PB4	97	PB4	SDSI-CMD	R355, SW4.3:ON	-	SDSI1.5	R251	-
			OnTFT-VSYNC	SW4.4:ON	R355, SW4.3:OFF	ONTFT1.33	MR7	-
			SDRAM-A12	-	R355, SW4.4:OFF, SW4.3:OFF	U12.35	-	-
			JA3-A12			JA3.13	-	-
PB2	99	PB2	SDSI-D2	R61, SW4.3:ON	-	SDSI1.1	R247	-
			OnTFT-HSYNC	SW4.4:ON	R61, SW4.3:OFF	ONTFT1.32	MR7	-
			SDRAM-A10	-	R61, SW4.4:OFF, SW4.3:OFF	U12.34	-	-
			JA3-A10			JA3.11	-	-
PB3	98	PB3	SDRAM-A11	R248	R249	U12.22	-	-
			JA3-A11			JA3.12	-	-
			SDSI-D3	R249	R248	SDSI1.3	R250	-

Table 6-30: SDSI Configuration Option Links

6.23 TFT Header Configuration

Table 6-31 to Table 6-32 below details the function of the option links associated with TFT Header Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P14	51	P14	USB0-OVRCURA	R24, R32	R292	U5.2	-	-
			TFT-DOTCLK	R292, R32	R24	TFT.25	-	-
P13	52	P13	E2P-SDA	R328, R327	R147	U4.5	R118	-
			JA1-SDA			JA1.25	R88	R396
			TFT-VSYNC	R147, R327	R328	TFT.27	-	-
P11	67	P11	TFT-G2	R144	R42	TFT.14	-	-
			JA6-M1VIN	R42	R144	JA6.15	-	-
P27	36	P27	RSPI-CLK	R281, R336	R295	U6.6	-	-
			TFT-SCK	R295, R336	R281	TFT.29	-	-
P26	37	P26	RSPI-MOSI	R301	R302, R317	U6.5	-	-
			JA3-CSc	R302	R301, R317	JA3.45	R148	R424
			TFT-MOSI	R317	R301, R302	TFT.31	-	-
P31	32	P31	RSPI-CS	R275	R15, R14	U6.1	-	-
			TFT-SS	R15	R275, R14	TFT.32	-	-
			PMOD2-CS	R14	R275, R15	PMOD2.1	R187	-
P30	33	P30	RSPI-MISO	R285	R286	U6.2	-	-
			TFT-MISO	R286	R285	TFT.30	-	-
P47	165	P47	TFT-YINPUT2	R154	R70	TFT.46	-	-
			JA5-ADC7	R70	R154	JA5.4	-	-
P46	166	P46	TFT-XINPUT2	R155	R71	TFT.45	-	-
			JA5-ADC6	R71	R155	JA5.3	-	-
P45	167	P45	TFT-YINPUT1	R152	R78	TFT.44	-	-
			JA5-ADC5	R78	R152	JA5.2	-	-
P44	168	P44	TFT-XINPUT1	R153	R79	TFT.43	-	-
			JA5-ADC4	R79	R153	JA5.1	-	-
P57	63	P57	TFT-B4	R140	R95	TFT.10	-	-
			JA1-IO6	R95	R140	JA1.21	-	-
P56	64	P56	TFT-B5	R141	R94	TFT.11	-	-
			JA1-IO7	R94	R141	JA1.22	-	-
P55	65	P55	TFT-G0	R142	R67	TFT.12	-	-
			JA6-DREQ	R67	R142	JA6.1	-	-
P54	66	P54	TFT-G1	R143	R73, R384	TFT.13	-	-
			JA6-DACK	R73	R143, R384	JA6.2	-	-
			JA2-M1WP	R384	R143, R73	JA2.17	-	-

Table 6-31: TFT Header Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P85	61	P85	TFT-B2	R138	R100	TFT.8	-	-
			JA1-IO4	R100	R138	JA1.19	-	-
P84	62	P84	TFT-B3	R139	R97	TFT.9	-	-
			JA1-IO5	R97	R139	JA1.20	-	-
P83	74	P83	ET-ET0CRS_RMII0CRSDV	R269	R268	U14.40	-	-
			TFT-G3	R268	R269	TFT.15	-	-
P82	79	P82	ET-ET0ETXD1_RMII0TXD1	R321	R320	U14.4	R307	-
			TFT-R2	R320	R321	TFT.19	-	-
P81	80	P81	ET-ET0ETXD0_RMII0TXD0	R305	R319	U14.3	R306	-
			TFT-R3	R319	R305	TFT.20	-	-
P80	81	P80	ET-ET0TXEN_RMII0TXDEN	R304	R318	U14.2	-	-
			TFT-R4	R318	R304	TFT.21	-	-
P92	160	P92	JA3-A18	R428, R362	R385	JA3.39	-	-
			OnTFT-SCL	R385, R362	R428	OnTFT2.3	-	-
			TFT-SCL			JA1.26	R386	R82
P90	163	P90	JA3-A16	R429, R371	R397	JA3.37	-	-
			OnTFT-SDA	R397, R371	R429	OnTFT2.4	-	-
			TFT-SDA			JA1.25	R396	R88
PB7	94	PB7	JA3-A15	R260	R258, R259, R257	JA3.16	-	-
			OnTFT-BACKLIGHT	R258	R260, R259, R257	U16.5	-	-
			TFT-BACKLIGHT	R259	R258, R260, R257	TFT.35	-	-
			SDSI-D1	R257	R258, R260, R259	SDSI1.15	R256	-
PC7	76	PC7	ET-ET0COL	R409 or J12 (1-2pin short)	R402	U14.42	-	-
			E1-UB	J12 (2-3pin short)	R409, R402	E1.10	-	-
			DSW-UB			SW4.2	-	-
			TFT-G4	R402	R409, J12 open	TFT.16	-	-
PC6	77	PC6	ET-ET0ETXD3	R324	R325	U14.6	R308	-
			TFT-G5	R325	R324	TFT.17	-	-
PC5	78	PC5	ET-ET0ETXD2	R17	R27	U14.5	R322	-
			TFT-R1	R27	R17	TFT.18	-	-
PC4	82	PC4	ET-ET0TXCLK	R16, R26	R294	U14.1	R303	-
			TFT-R5	R294, R26	R16	TFT.22	-	-
PG1	144	PG1	TFT-YDRIVE	R150	R114	TFT.42	-	-
			JA1-IO1	R114	R150	JA1.16	-	-
PG0	146	PG0	TFT-XDRIVE	R151	R113	TFT.41	-	-
			JA1-IO2	R113	R151	JA1.17	-	-
PJ2	58	PJ2	TFT-HSYNC	R145	R59, R482	TFT.24	-	-
			JA6-TXDb	R59	R145, R482	JA6.8	-	-
			SERIAL-TXD	R482	R145, R59	U21.3	-	R64, R126, R452
PJ1	59	PJ1	TFT-LCDDEN	R146	R54, R483	TFT.26	-	-
			JA6-RXDb	R54	R146, R483	JA6.7	-	-
			SERIAL-RXD	R483	R146, R54	U20.3	-	R121, R448, R60
PJ0	60	PJ0	TFT-B1	R342	R51	TFT.7	-	-
			JA6-SCKb	R51	R342	JA6.10	-	-
RESn	21	-	E1-RESn	-	-	E1.13	-	-
			SW-RESn	-	-	RES1(Switch)	-	-
			JA2-RESn	-	-	JA2.1	-	-
			PDC-RESn	-	-	J15.6	R207	-
			TFT-RESn	-	-	TFT.33	R149	-
			ET-RESn	-	-	U14.29	R264	-
			OnTFT-RESn	-	-	ONTFT2.6	R137	-

Table 6-32: TFT Header Configuration Option Links (2)

6.24 USB Configuration

Table 6-33 below details the function of the option links associated with the USB Configuration.

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P16	48	P16	USB0-VBUS	J16(1-2 short), J6(2-3 short) or R9, R22, R11	-	USB0_1.1, USB0_2.1	J7(2-3 short), R6 or L1	-
			USB0-VBUSEN	J16(2-3 short)		U5.1	-	-
P14	51	P14	USB0-OVRCURA	R24, R32	R292	U5.2	-	-
			TFT-DOTCLK	R292, R32	R24	TFT.25	-	-
P35	26	P35	JP-UPSEL	-	-	J9.2	-	-
			JA2-NMIn	R414	-	JA2.3	-	-
USB0-DP	56	-	USB0-DP	R10 or L2	-	USB0_1.3	R7	-
						USB0_2.3	R4	-
USB0-DN	55	-	USB0-DN	R12 or L2	-	USB0_1.2	R8	-
						USB0_2.2	R5	-

Table 6-33: USB Configuration Option Links

Table 6-34 below details the function of the jumpers associated with the USB Configuration.

Reference	Jumper Position	Explanation	Related Ref.
J6(DNF) *1	Shorted Pin1-2	Bus-powered	J7, R9
	Shorted Pin2-3	Self-powered	J7, R9
	All open	Self-powered by R9	R9
J7	Shorted Pin1-2	USB0 Host mode	-
	Shorted Pin2-3	USB0 Function mode	J6
	All open	DO NOT SET.	-

Table 6-34: USB Configuration Jumper Option Links

*1: In case of fit J6, remove R9.

7. Headers

7.1 Application Headers

This RSK+ board is fitted with application headers, which can be used to connect compatible Renesas application devices or as easy access to MCU pins.

Table 7-1 below lists the connections of the application header, JA1.

Application Header JA1					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	5V JA1-5V	-	2	0V GROUND	-
3	3V3 JA1-3V3	-	4	0V GROUND	-
5	AVCC JA1-AVCC	175, 3	6	AVSS JA1-AVSS	1, 5, 172
7	AVREF JA1-VREFH	174	8	ADTRG JA1-ADTRG	176
9	ADC0 JA1-ADC0	173	10	ADC1 JA1-ADC1	171
11	ADC2 JA1-ADC2	170	12	ADC3 JA1-ADC3	169
13	DAC0 JA1-DAC0	4	14	DAC1 JA1-DAC1	2
15	IO_0 JA1-IO0	123	16	IO_1 JA1-IO1	144
17	IO_2 JA1-IO2	146	18	IO_3 JA1-IO3	149
19	IO_4 JA1-IO4	61	20	IO_5 JA1-IO5	62
21	IO_6 JA1-IO6	63	22	IO_7 JA1-IO7	64
23	IRQd / IRQAEC / M2_HSIN0 JA1-IRQd	91 / NC / NC	24	IIC_EX NC	NC
25	IIC_SDA / SDA(For TFT Header touch) *1 JA1-25PIN	52 / 163	26	IIC_SCL / SCL(For TFT Header touch) *1 JA1-26PIN	53 / 160

Table 7-1: Application Header JA1 Connections

*1: Nonstandard features

Table 7-2 below lists the connections of the application header, JA2.

Application Header JA2					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	RESET JA2-RESn	21	2	EXTAL JA2-EXTAL	24
3	NMI JA2-NMIn	26	4	Vss1 GROUND	-
5	WDT_OVF NC	NC	6	SCIaTX JA2-TXDa	72
7	IRQa / WKUP / M1_HSIN0 JA2-7PIN	50	8	SCIaRX JA2-RXDa	70
9	IRQb / M1_HSIN1 / RCAP_IRQ *1 JA2-9PIN	29 / 29 / 170	10	SCIaCK JA2-SCKa	71
11	M1_UD JA2-M1UD	13	12	CTSaRTSa JA2-CTSaRTSa	11
13	M1_UP JA2-M1UP	43	14	M1_UN JA2-M1UN	42
15	M1_VP JA2-M1VP	118	16	M1_VN JA2-M1VN	47
17	M1_WP JA2-M1WP	66	18	M1_WN JA2-M1WN	83
19	TimerOut0 JA2-TIMOUT0	44	20	TimerOut1 JA2-TIMOUT1	118
21	TimerIn0 JA2-TIMIN0	50	22	TimerIn1 JA2-TIMIN1	47
23	IRQc / M1_EncZ / M1_HSIN2 JA2-23PIN	28 / 45 / 28	24	M1_POE JA2-M1POE	159
25	M1_TRCCLK JA2-M1TRCCLK	40	26	M1_TRDCLK JA2-M1TRDCLK	38

Table 7-2: Application Header JA2 Connections

*1: Nonstandard features

Table 7-3 below lists the connections of the BUS application header, JA3.

Application Header JA3 (Bus)					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	A0 JA3-A0	118	2	A1 JA3-A1	114
3	A2 JA3-A2	112	4	A3 JA3-A3	110
5	A4 JA3-A4	109	6	A5 JA3-A5	108
7	A6 JA3-A6	107	8	A7 JA3-A7	106
9	A8 JA3-A8	104	10	A9 JA3-A9	100
11	A10 JA3-A10	99	12	A11 JA3-A11	98
13	A12 JA3-A12	97	14	A13 JA3-A13	96
15	A14 JA3-A14	95	16	A15 JA3-A15	94
17	D0 JA3-D0	158	18	D1 JA3-D1	156
19	D2 JA3-D2	154	20	D3 JA3-D3	150
21	D4 JA3-D4	148	22	D5 JA3-D5	147
23	D6 JA3-D6	145	24	D7 JA3-D7	143
25	RDn JA3-RDn	70	26	WR / SDWE JA3-26PIN	72 / 136
27	CSa JA3-CSa	141	28	CSb JA3-CSb	139
29	D8 JA3-D8	135	30	D9 JA3-D9	134
31	D10 JA3-D10	133	32	D11 JA3-D11	132
33	D12 JA3-D12	131	34	D13 JA3-D13	130
35	D14 JA3-D14	126	36	D15 JA3-D15	125
37	A16 JA3-A16	163	38	A17 JA3-A17	161
39	A18 JA3-A18	160	40	A19 JA3-A19	159
41	A20 JA3-A20	157	42	A21 JA3-A21	155
43	A22 JA3-A22	152	44	SDCLK JA3-44PIN	128 / 69
45	CSc / Wait JA3-45PIN	37 / 71	46	ALE / SDCKE JA3-46PIN	68 / 124
47	HWRn / DQMH JA3-47PIN	71 / 120	48	LWRn / DQML JA3-48PIN	72 / 122
49	CAS JA3-CAS	137	50	RAS JA3-RAS	138

Table 7-3: Application Header JA3 Connections

Table 7-4 below lists the connections of the application header, JA5.

Application Header JA5					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	ADC4 JA5-ADC4	168	2	ADC5 JA5-ADC5	167
3	ADC6 JA5-ADC6	166	4	ADC7 JA5-ADC7	165
5	CAN1TX JA5-CAN1TX	29	6	CAN1RX JA5-CAN1RX	28
7	CAN2TX NC	NC	8	CAN2RX NC	NC
9	IRQe / M2_EncZ / M2HSIN1 / TFT Header LCD power *1 JA5-LCDPWR	NC / NC / NC / 121	10	IRQf / M2_HSIN2 NC	NC
11	M2_UD NC	NC	12	M2_Uin NC	NC
13	M2_Vin NC	NC	14	M2_Win NC	NC
15	M2_Toggle NC	NC	16	M2_POE NC	NC
17	M2_TRCCLK NC	NC	18	M2_TRDCLK NC	NC
19	M2_UP NC	NC	20	M2_Un / TFT Header LCD ON-OFF *1 JA5-LCDDISP	NC / 149
21	M2_VP NC	NC	22	M2_Vn NC	NC
23	M2_WP NC	NC	24	M2_Wn NC	NC

Table 7-4: Application Header JA5 Connections

*1: Non standard features

Table 7-5 below lists the connections of the application header, JA6.

Application Header JA6					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	DREQ JA6-DREQ	65	2	DACK JA6-DACK	66
3	TEND NC	NC	4	STBYn NC	NC
5	RS232TX JA6-RS232TX	NC	6	RS232RX JA6-RS232RX	NC
7	SCIbRX JA6-RXDb	59	8	SCIbTX JA6-TXDb	58
9	SCIcTX JA6-TXDc	83	10	SCIbCK JA6-SCKb	60
11	SCIcCK JA6-SCKc	89	12	SCIcRX JA6-RXDc	86
13	M1_Toggle JA6-M1TOGGLE	46	14	M1_Uin JA6-M1UIN	53
15	M1_Vin JA6-M1VIN	67	16	M1_Win JA6-M1WIN	104
17	EXT_USB_VBUS NC	NC	18	Reserved NC	NC
19	EXT_USB_BATT NC	NC	20	Reserved NC	NC
21	EXT_USB_CHG NC	NC	22	Reserved NC	NC
23	Unregulated_VCC Unregulated_VCC	-	24	Vss GROUND	-

Table 7-5: Application Header JA6 Connections

7.2 Generic Headers

Generic headers, used to provide easy connections to various pins from devices fitted to the RSK+.
Table 7-6 below lists the connections of the LCD Direct Drive (TFT) Header.

LCD Direct Drive Header (TFT)					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	5V Board_5V	-	2	5V Board_5V	-
3	3V3 Board_3V3	-	4	3V3 Board_3V3	-
5	Reserved NC	NC	6	Reserved NC	NC
7	B1 TFT-B1	60	8	B2 TFT-B2	61
9	B3 TFT-B3	62	10	B4 TFT-B4	63
11	B5 TFT-B5	64	12	G0 TFT-G0	65
13	G1 TFT-G1	66	14	G2 TFT-G2	67
15	G3 TFT-G3	74	16	G4 TFT-G4	76
17	G5 TFT-G5	77	18	R1 TFT-R1	78
19	R2 TFT-R2	79	20	R3 TFT-R3	80
21	R4 TFT-R4	81	22	R5 TFT-R5	82
23	EDACK NC	NC	24	HSYNC TFT-HSYNC	58
25	DOTCLK TFT-DOTCLK	51	26	LCDDEN TFT-LCDDEN	59
27	VSYNC TFT-VSYNC	52	28	EDREQ NC	NC
29	SCK TFT-SCK	36	30	MISO TFT-MISO	33
31	MOSI TFT-MOSI	37	32	SS TFT-SS	32
33	RESET TFT-RESn	21	34	GND GROUND	-
35	BACKLIGHT TFT-BACKLIGHT	94	36	SD_DOTCLK NC	NC
37	GND GROUND	-	38	GND GROUND	-
39	GND GROUND	-	40	GND GROUND	-
41	X_DRIVE TFT-XDRIVE	146	42	Y_DRIVE TFT-YDRIVE	144
43	X_INPUT1 TFT-XINPUT1	168	44	Y_INPUT1 TFT-YINPUT1	167
45	X_INPUT2 TFT-XINPUT2	166	46	Y_INPUT2 TFT-YINPUT2	165
47	Reserved NC	NC	48	Reserved NC	NC
49	Reserved NC	NC	50	Reserved NC	NC

Table 7-6: TFT Connector Connections

8. Code Development

8.1 Overview

For all code debugging using Renesas software tools, the RSK+ board must be connected to a PC via an E1/E20/E2 Lite debugger. An E1/E2 Lite debugger is supplied with this RSK+ product.

For further information regarding the debugging capabilities of the E1/E20/E2 Lite debuggers, refer to E1/E20 Emulator, E2 Emulator Lite Additional Document for User's Manual (R20UT0399EJ).

8.2 Compiler Restrictions

The compiler supplied with this RSK is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the compiler will default to a maximum of 128k code and data. To use the compiler with programs greater than this size you need to purchase the full tools from your distributor.

The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

8.3 Mode Support

The MCU supports Single Chip and Boot Modes (SCI and USB), which are configured on the RSK+ board. Details of the modifications required can be found in §6.2. All other MCU operating modes are configured within the MCU's registers, which are listed in the RX65N Group, RX651 Group User's Manual: Hardware.

Only ever change the MCU operating mode whilst the RSK+ is in reset, or turned off; otherwise the MCU may become damaged as a result.

8.4 Debugging Support

The E1 Emulator or E2 Emulator Lite (as supplied with this RSK+) supports break points, event points (including mid-execution insertion) and basic trace functionality. It is limited to a maximum of 8 on-chip event points, 256 software breaks and 256 branch/cycle trace. For further details, refer E1/E20 Emulator User's Manual (R20UT0398EJ) or E2 Emulator Lite User's Manual (R20UT3240EJ).

8.5 Address Space

For the MCU address space details, refer to the 'Address Space' section of RX65N Group, RX651 Group User's Manual: Hardware.

8.6 Note of Flash Access Window Setting Register

This register is used to set the write protection flag and start-up area select flag for setting the flash access window start address, flash access window end address, and access window.

Once 0 is written to this bit, the bit can never be restored to 1.
Therefore, the access window and the BTFLG bit will never be set again. If set the TM function will never be disabled, once enabled. Exercise extra caution when handling the FSPR bit.

9. Additional Information

Technical Support

For information about the RX65N Group, RX651 Group microcontrollers refer to the RX65N Group, RX651 Group Hardware Manual.

For information about the RX assembly language, refer to the RX Family Software Manual.

Technical Contact Details

Please refer to the contact details listed in section 8 of the "Quick Start Guide"

General information on Renesas microcontrollers can be found on the Renesas website at:
https://www.renesas.com/

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